

IS31LT3916

Isolated or Non-isolated configuration LED driver with active PFC

January 2013

General Description

The IS31LT3916 is a primary side, peak current mode, isolated or non-isolated type HBLED driver. The device works at a constant frequency in discontinuous conduction mode to provide a constant power to the output. It eliminates the need for an opto-coupler, TL431, or any other type of secondary side feedback. It operates from a wide input voltage range of 85VAC to 265VAC.

The IS31LT3916 integrates over current protection, over voltage protection, as well as includes a thermal shutdown to halt the switching action in the case of abnormally high operating temperatures.

Features

- Power factor correction to > 0.95
- 5% typical current accuracy
- High efficiency
- No loop compensation required
- Wide input voltage range: 85V to 265VAC
- Isolation and Non-isolation application
- Internal over-temperature protection
- Over voltage protection
- Primary side over current protection

Applications

- LED bulb lamp
- LED tube lamp
- General LED Lighting

Typical Operating Circuit

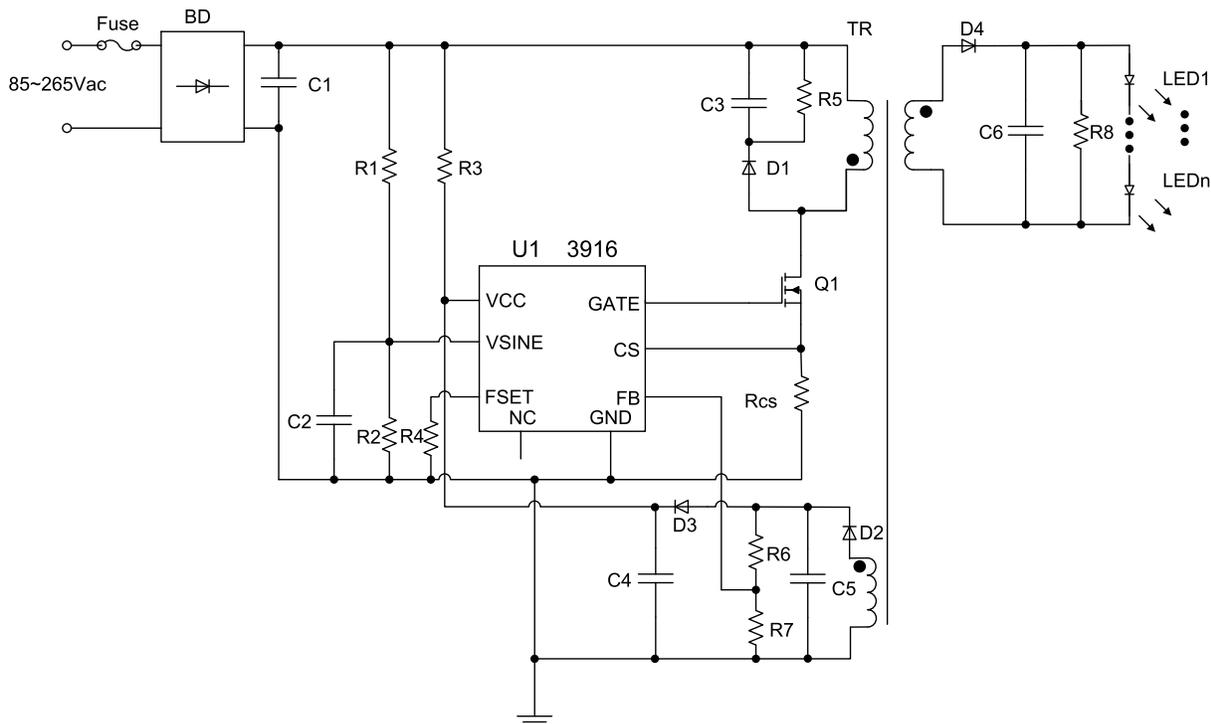


Figure 1 Typical Operating Isolated Circuit

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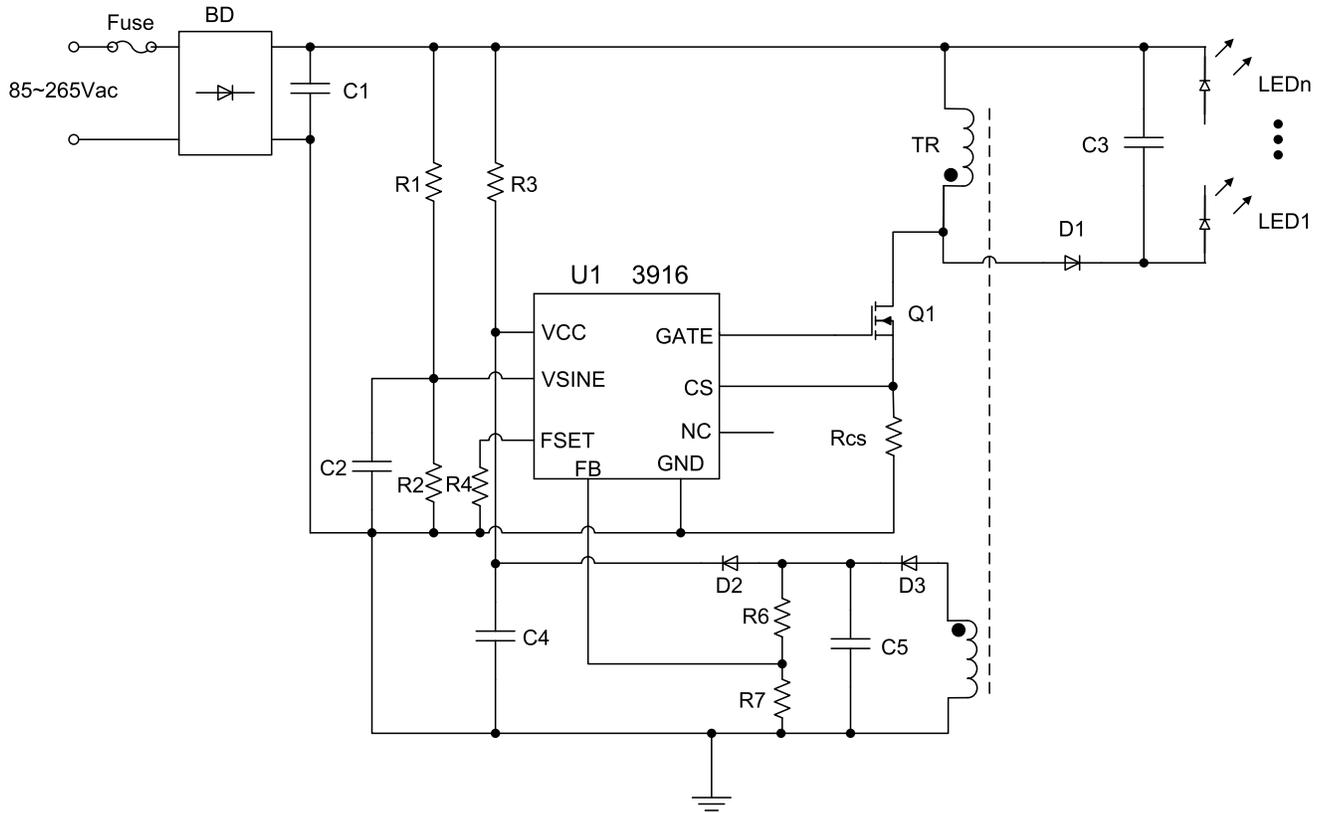


Figure 2 Typical Operating non-Isolated Circuit

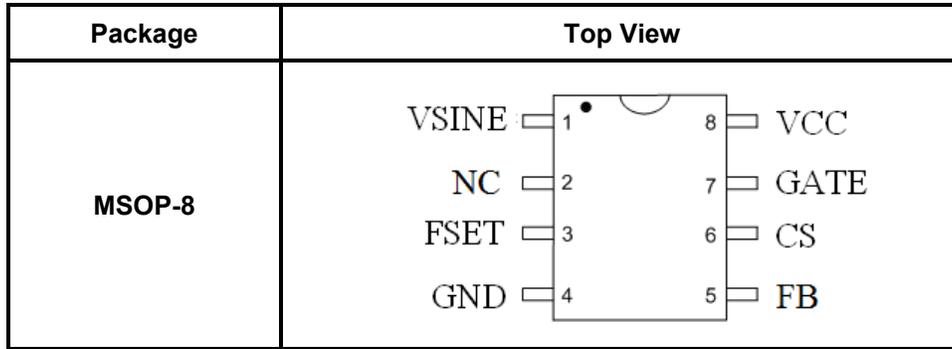
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- a.) the risk of injury or damage has been minimized;
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Pin Configurations



Pin Descriptions

Pin	Name	Function
1	VSINE	Line voltage sense input required for PFC.
2	NC	No connect. Must leave floating in the application.
3	FSET	Connect a resistor from this pin to GND to set the operating frequency
4	GND	Ground. Common to all internal circuitry.
5	FB	Auxiliary winding voltage sensing pin for OVP.
6	CS	Primary winding peak current detection input.
7	GATE	Power NMOS gate driving output.
8	VCC	Internal circuit power supply input.

Ordering Information

Order Part No.	Package	QTY/Reel
IS31LT3916-GRLS2-TR	MSOP-8, Lead-free	2500

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Absolute Maximum Ratings

Parameter	Value
VCC to GND	-0.3V to 24V
VSINE, NC, FSET, CS, FB	-0.3V to 5.5V
VCC Max. Input Current(<i>note</i>)	10mA
Operating Temperature Ranges:	-45°C to +105°C
Junction Temperature Range	150°C
Storage Temperature Range	-65°C to +150°C
Package Thermal Resistance junction to ambient (θ_{JA})	210 °C/W
ESD Human Model	2000V

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(Unless otherwise specified, VCC=16V, FB=0V, VSINE=2.5V, RSET=300K Ω , and T_{amb}=25 °C)

Symbol	Parameter	Conditions	spec			Unit
			Min	Typ	Max	
VCC	VCC operation range		9		22	V
Vth_s	VCC start voltage threshold	VCC rising	14.5	16	17.5	V
Vth_d	VCC under voltage threshold	VCC falling	7	8	9	V
V _{GATEclp}	GATE output voltage clamp value	VCC =22V	15	17.5	19	V
I _{cc}	Quiescent Supply Current	Not switching		800		uA
I _{st}	Startup current	VCC < Vth_s		60	80	uA
V _{cs}	Primary peak current control threshold voltage		0.493	0.5	0.507	V
T _{blank}	Blanking time			500	800	ns
Tr	Rise time	VCC=16V, CL=1nF, V _{GA} TE from 0V to 7V		100	120	ns
Tf	Fall time	VCC=16V, CL=1nF		50	80	ns
V _{ovp_H}	OVP rising voltage threshold of FB		1.2	1.25	1.3	V
V _{ovp_L}	OVP falling voltage threshold of FB		0.95	1.0	1.05	V
f	Operating frequency	RSET = 300k	49	50	51	kHz
T _{OCP}	CS over current protection delay	F = 50kHz	500	600	750	us
V _{ocp-th}	CS over current protection threshold	F = 50kHz	0.65	0.7	0.75	V

Typical Performance Characteristics

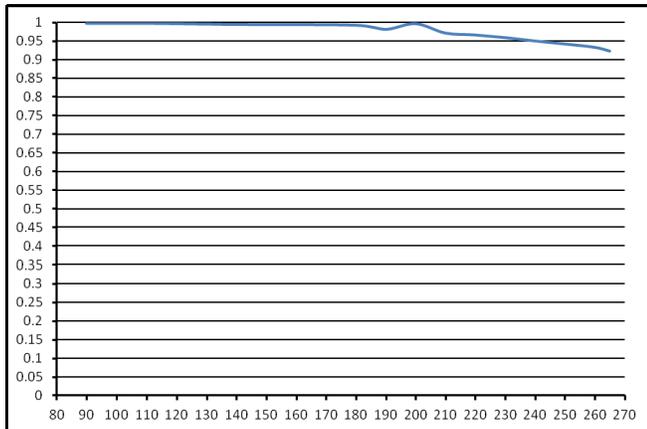


Figure 3 Vin VS PF (Output: Vout=40V Iout=0.45A)

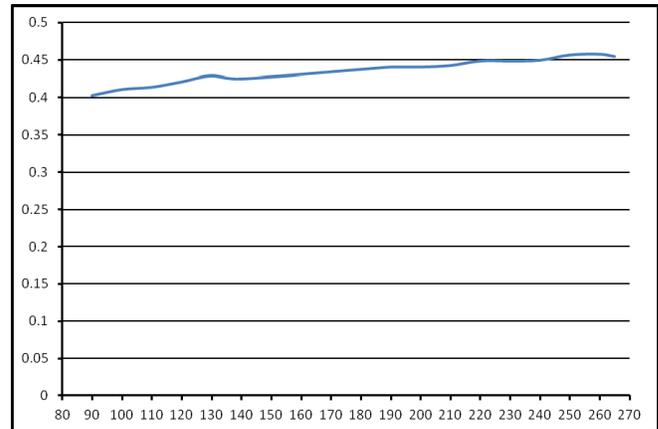


Figure 6 Vin VS Iout (Output: Vout=40V Iout=0.45A without line compensation circuit)

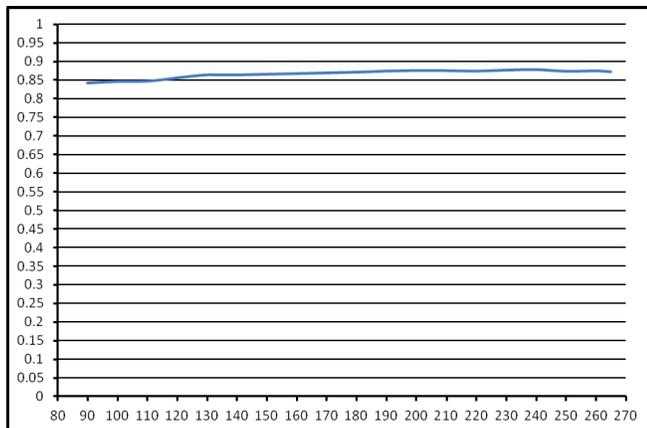


Figure 4 Vin VS Efficiency (Output:Vout=40V Iout=0.45A)

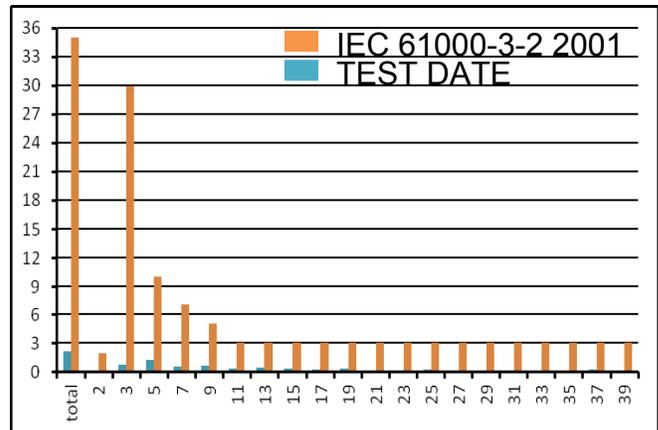


Figure 7 THD of Vin=110V (Output: Vout=40V Iout=0.45A)

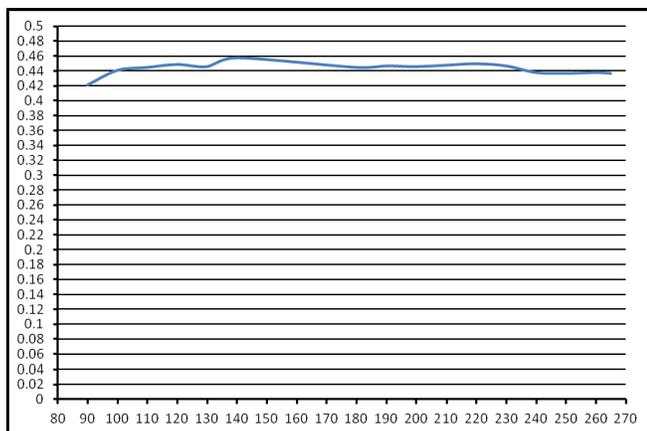


Figure 5 Vin VS Iout (Output: Vout=40V Iout=0.45A with line compensation circuit)

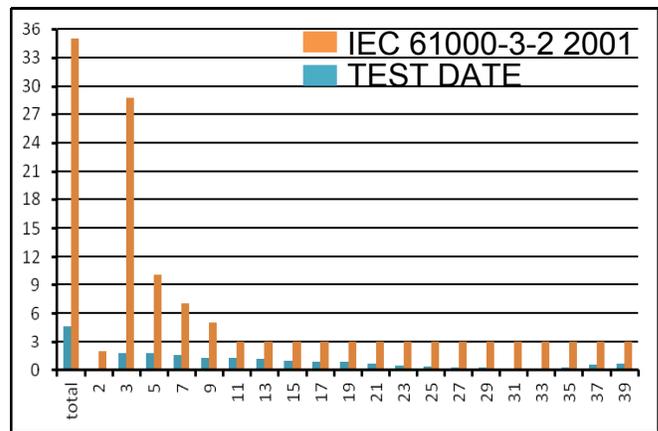


Figure 8 THD of Vin=220V (Output: Vout=40V Iout=0.45A)

Block Diagram

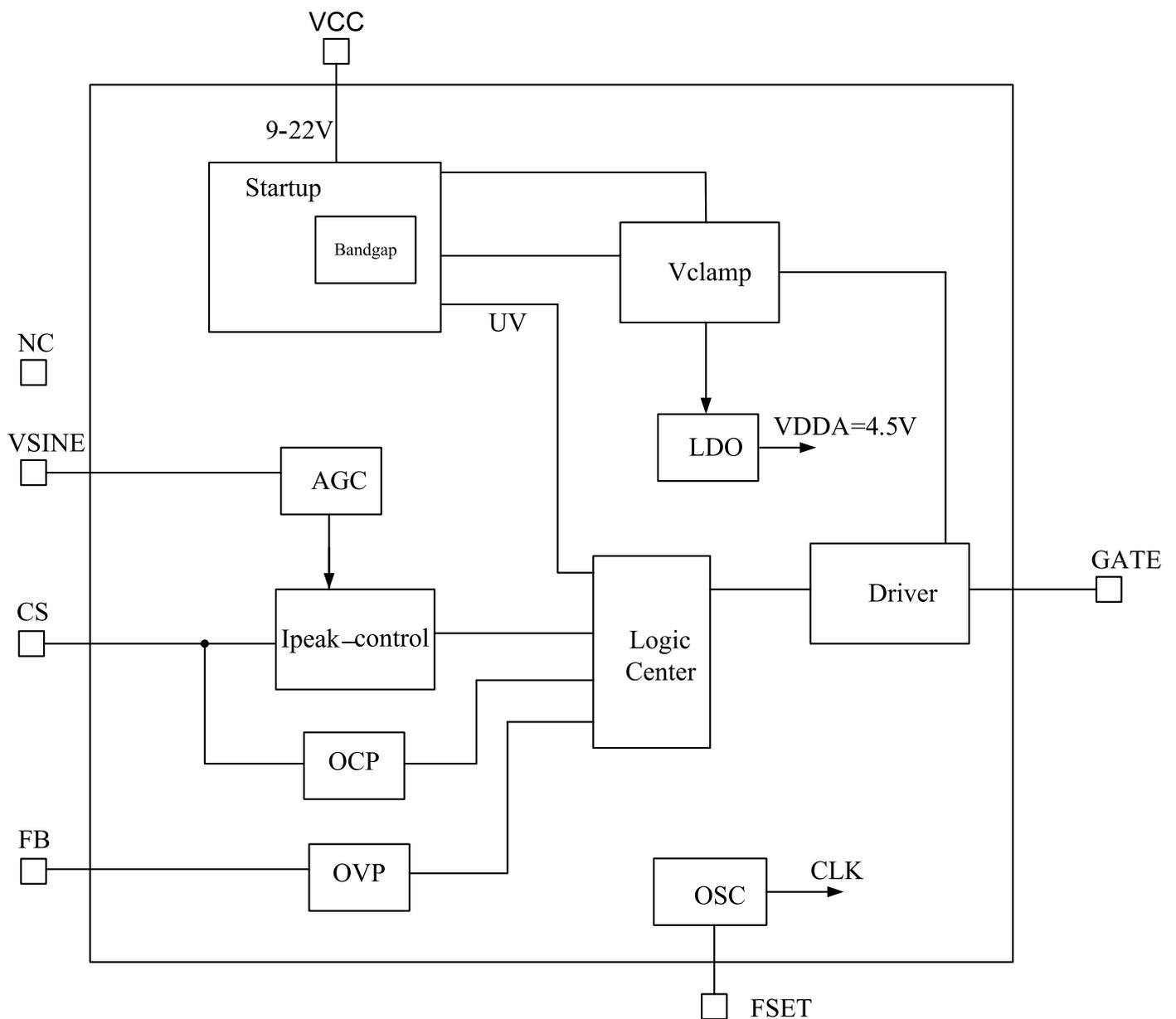


Figure 9 Block Diagram

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Application Information

Startup voltage

After power is applied to the circuit, R3 provides a trickle current to allow C4 to begin charging. The IC starts working when the voltage of C4 reaches the start threshold for the IC of 16.5V. The value of R3 & C4 can be determined by the input voltage. Choosing a larger value of R3 increases the startup time, but reduces the power losses after the circuit is running. A low ESR capacitor of 10 μ F, 25V is recommended for C4.

Soft start control

When the IC is initially powered up, the internal AGC output is at the minimum value, so the peak CS threshold is initially much less than 0.5V. The AGC steps up cycle by cycle until the CS threshold at the peak of the input sine wave is equal to 0.5V. In this manner, it will take several cycles of the AC waveform for the final value of current to be attained, as shown in Figure 9.

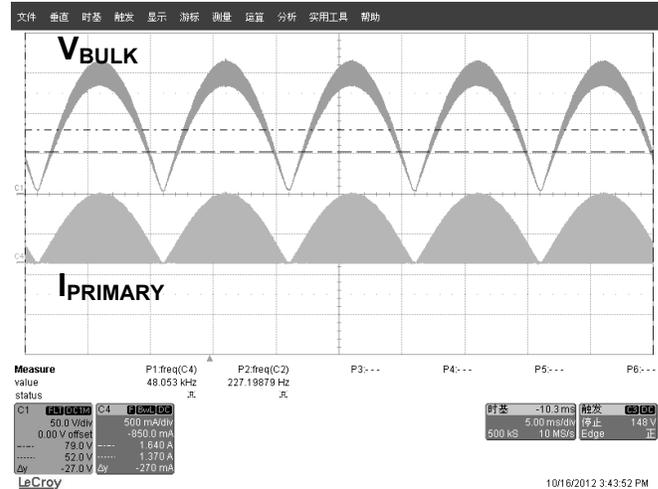


Figure 11 Active PFC

VSINE is used to detect the input voltage which controls the peak current waveform in the primary inductor. An integrated AGC ensures that the peak current of the inductor remains constant with changing input voltage. This allows the IS31LT3916 to actively correct the power factor while maintaining a constant power output during operation. The internal AGC is designed for an input range of 0.8V to 2.5V at the VSINE pin, meaning that the AGC gain achieves a minimum value when the voltage at VSINE is 2.5V, however, there is no internal voltage clamp preventing the VSINE voltage from exceeding 2.5V. If the peak input voltage at VSINE exceeds 2.5V, the CS threshold can no longer be maintained at 0.5V, causing the line regulation to suffer. Thus, the resistor network connected to VSINE should be computed such that the worst case peak input voltage condition corresponds to ~2.4V. Thus, for 265VAC, the peak voltage is 374.7V. At 374.7V input, the output of the network should be 2.4V, thus values of R1=1.86M and R2 = 12k are appropriate. High tolerance Resistance value of 1% should be used. A small capacitor, C2, is used to filter high frequency noise that may couple to the VSINE pin.

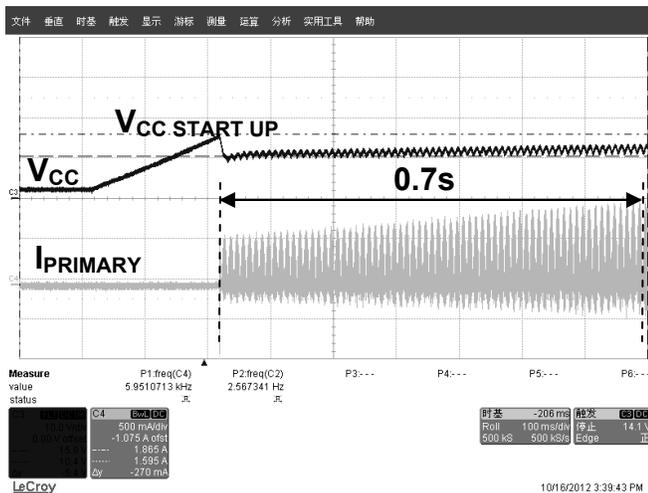


Figure 10 soft start

GATE output voltage clamp

IS31LT3916 has the voltage clamp for GATE output. When the voltage of VCC is smaller than the $V_{GATEclp}$ threshold, the output high voltage of GATE output is about VCC. When the voltage of VCC is greater than $V_{GATEclp}$ threshold, the output high voltage of GATE is limited to the $V_{GATEclp}$ threshold.

VSINE detection network and active PFC

The voltage of VSINE pin is used to control the waveform of input current make it follow the input voltage waveform, V_{BULK} , to achieve high PF and low THD performance, as shown in figure 11.

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Working Frequency

The working frequency is set by connecting a resistor between the FSET pin and ground. The relationship between the frequency and resistance is:

$$f = \frac{15 \times 10^9}{R_{EXT}}$$

Output open circuit protection

Open circuit protection is realized by connecting a resistor network from the auxiliary winding to the FB pin. By sensing the voltage of the auxiliary winding, which is proportional to the output voltage, the IS31LT3916 detects when there is an open circuit condition on the secondary and consequently stop the switching action. The threshold voltage for the FB pin is 1.25V.

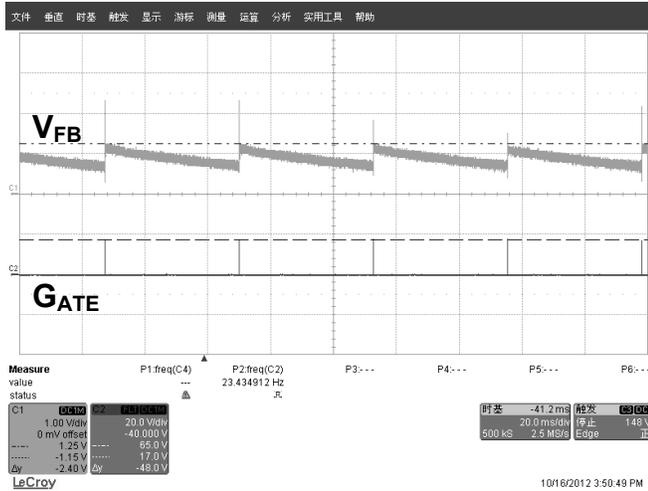


Figure 12 Output open circuit protect

Output short circuit protection

If the output of the circuit is suddenly shorted, the voltage of the secondary winding is quickly reduced. This in-turn reduces the reflected voltage in the auxiliary winding, so VCC of the device drops rapidly. If the VCC voltage drops below the UVLO, the device will stop switching, thus indirectly achieving output short circuit protection.

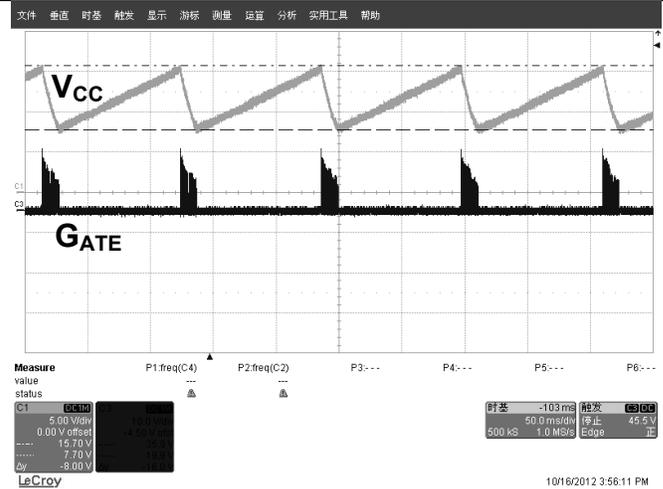


Figure 13 Output short circuit protect

UVLO protection

After triggering the device UVLO, the device will stop operating until the VCC voltage raises above the startup threshold, at which point the device will start again.

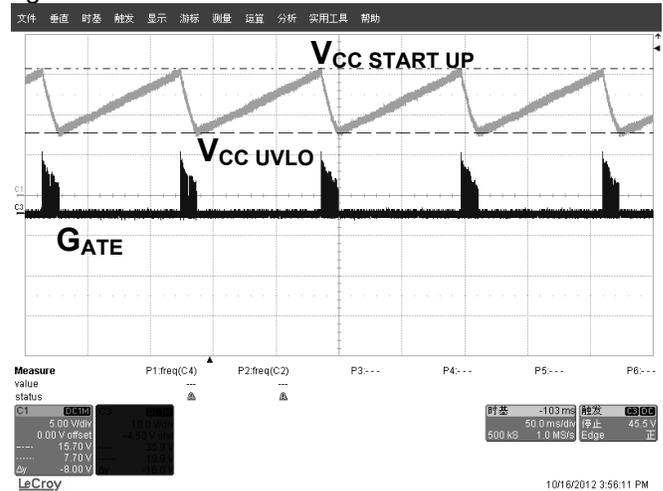


Figure 14 UVLO

Line regulation compensation design

The output power of IS31LT3916 varies slightly with input voltage due to the small delay associated with the current sense control loop. At high input voltages, the slope of the input current is quite steep, and, thus, will overshoot the target value by more than at low input voltage conditions. Therefore, under wide input voltage conditions, and without additional voltage compensation, the output power varies over the full input voltage range, 85VAC to 265VAC, by about +/- 5%. To further improve the line regulation, a simple compensation circuit may be added, as in Figures 16 & 17, components R7, R11, R15, R19, R16 and C8.

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Transformer design

The transformer design is beyond the scope of the datasheet. Refer to the document entitled “3916 calculator” to design the transformer.

PCB design considerations

- (1) As Figure 15 shows, Components such as R17,R13,R20,R21,R22, R23, R18, C7, C9etc. Which are connected to the IC should be mounted as close to the IC as possible.
- (2) Bypass capacitors should always be mounted as close to the IC as possible.
- (3) Switching signal traces should be kept as short as possible and not be routed parallel to one another so as to prevent coupling.
- (4) It is best to keep Power Ground and Signal Ground separate, and make the traces of Power Ground as short as possible.

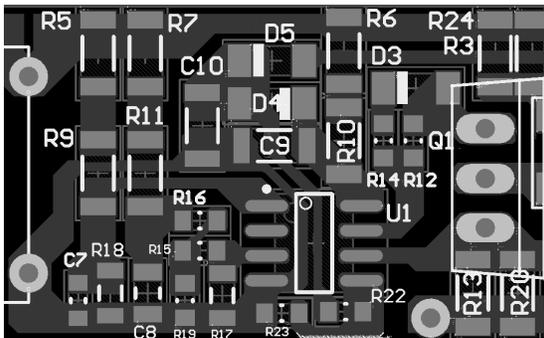


Figure 15 typical PCB layer out

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Typical Application Circuit (Full input voltage range, output: 40V, 0.45A)

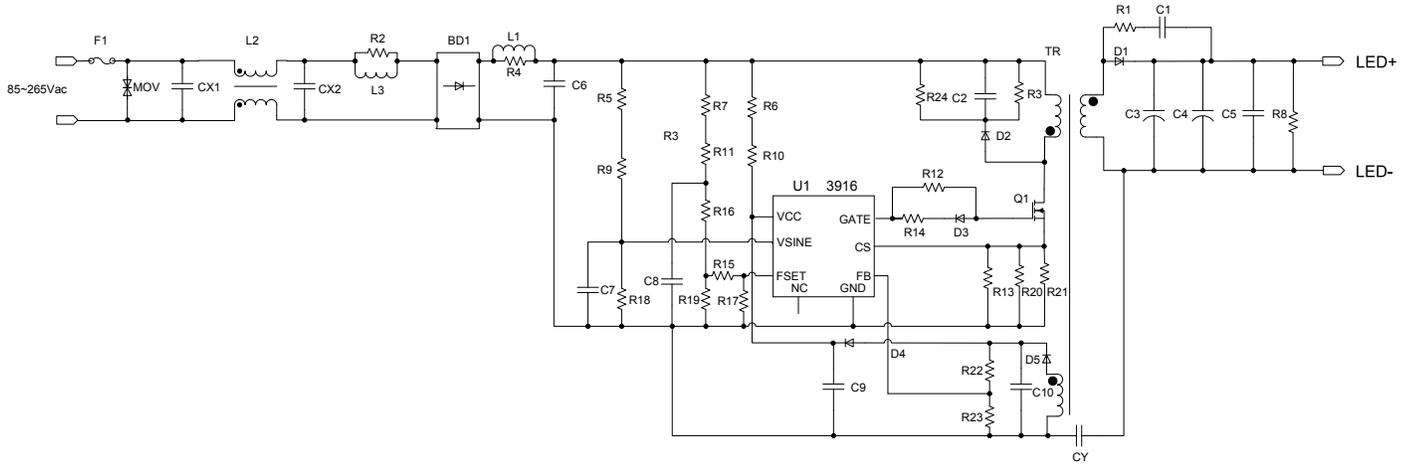


Figure 16 Typical Isolation Application Circuit

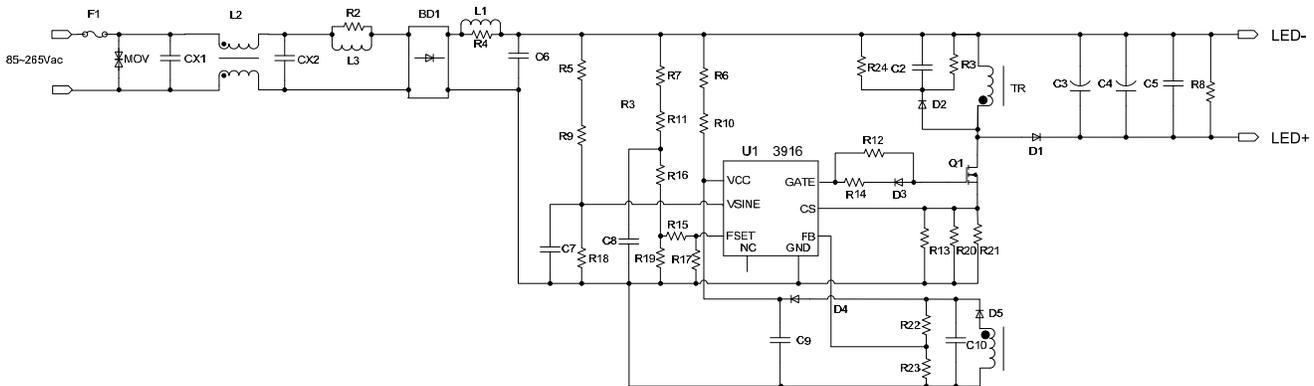
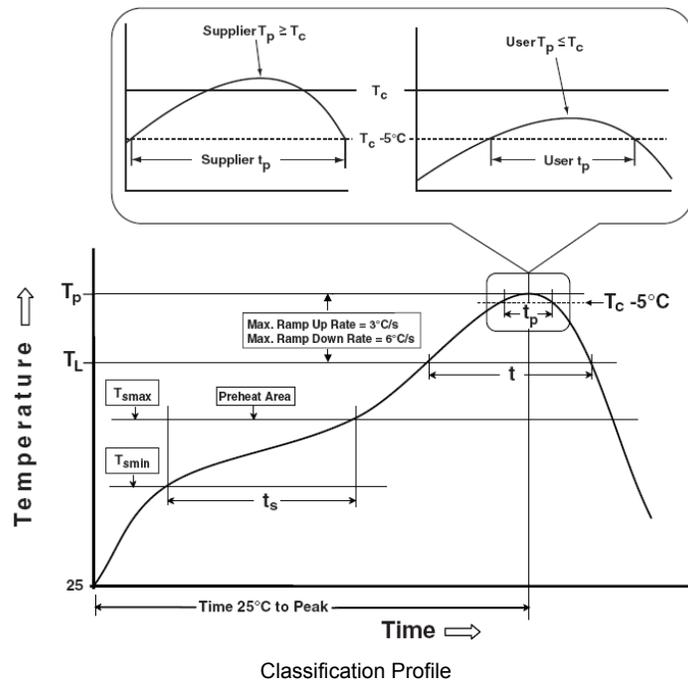


Figure 17 Typical Non-isolation Application Circuit

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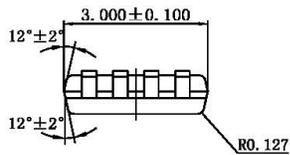
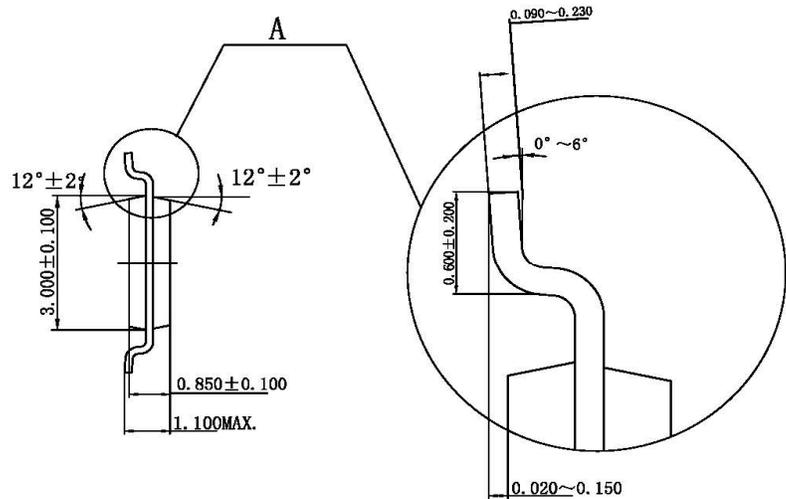
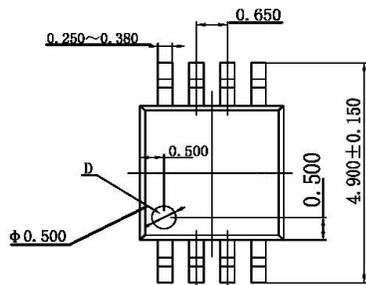
Classification Reflow Profiles

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (T _{sm}) Temperature max (T _{sm}) Time (T _{sm} to T _{sm}) (t _s)	150°C 200°C 60-120 seconds
Average ramp-up rate (T _{sm} to T _p)	3°C/second max.
Liquidous temperature (T _L) Time at liquidous (t _L)	217°C 60-150 seconds
Peak package body temperature (T _p)*	Max 260°C
Time (t _p)** within 5°C of the specified classification temperature (T _c)	Max 30 seconds
Average ramp-down rate (T _p to T _{sm})	6°C/second max.
Time 25°C to peak temperature	8 minutes max.



IS31LT3916

Package Information



THE REQUEST OF TECHNOLOGY

1. DETAIL "D" ROUND SURFACE SHOULD BE POLISHED FINISH;

2. COPLANARITY: 0.05;

3. ALL UNITS ARE IN MILLIMETER;

4. THE DIRECTION OF VIEW: 