

32-bit MCU family built on the Power Architecture® for automotive body electronics applications

Datasheet - production data

Features

- e200z4d, 32-bit Power Architecture®
 - Up to 120 MHz and 200 MIPs operation
- e200z0h, 32-bit Power Architecture
 - Up to 80 MHz and 75 MIPs operation
- Memory
 - Up to 3 MByte on-chip Flash with ECC
 - Up to 256 KByte on-chip SRAM with ECC
 - 64KByte on-chip Data Flash with ECC
 - 16-entry memory protection unit (MPU)
 - User selectable Memory BIST
- Interrupts
 - 255 interrupt sources with 16 priority levels
 - Up to 54 ext. IRQ including 30 wake-up
- GPIOs: from 147 (QFP176) to 199 (BGA256)
- System timer units
 - 8-ch. 32-bit periodic interrupt timer (PIT)
 - 4-channel 32-bit system timer (STM)
 - Safety System Watchdog Timer (SWT)
 - Real-time clock timer (RTC/API)
- eMIOS, 16-bit counter timed I/O units
 - Up to 64 channels with PWM/MC/IC/OC
- Two ADC (10-bit and 12-bit)
 - Up to 62 channels extendable to 90 ch.
 - Multiple Analog Watchdog
- Dedicated diagnostic features for lighting
 - Advanced shifted PWM generation
 - ADC conversion synchronized on PWM
- Communication interfaces
 - Up to 6 FlexCAN with 64 buffers each
 - Up to 10 LINFlex/UART channels
 - Up to 8 buffered DSPI channels
 - I²C interface
 - One FleyRay (dual-ch.) with 128 buffers
 - Fast Ethernet Controller
- Cryptographic Services Engine (CSE)
 - AES-128 en/decryption, CMAC auth.
 - Secured device boot mode
- 32-ch. eDMA with multiple request sources
- Clock generation
 - 4 to 40 MHz main oscillator
 - 16 MHz internal RC oscillator
 - Software-controlled FMPLL
 - 128 kHz internal RC oscillator
 - 32 kHz auxiliary oscillator
 - Clock Monitoring Unit (CMU)
- Low power capabilities
 - Ultra low power STANDBY
 - CAN Sampler to store CAN ID in STBY
 - Fast wake-up and execute from RAM
- Exhaustive debugging capability
 - Nexus 3+ interface on LBGA256 only
 - Nexus 1 on all devices
- Voltage supply
 - Single 5 V or 3.3 V supply
 - On-chip Vreg with external ballast transistor
- Operating temperature range -40 to 125 °C

Table 1. Device summary

Package	Part number		
	1.5 MByte	2 MByte	3 MByte
LQFP176	SPC564B64L7	SPC564B70L7	SPC564B74L7
	SPC56EC64L7	SPC56EC70L7	SPC56EC74L7
LQFP208	SPC564B64L8	SPC564B70L8	SPC564B74L8
	SPC56EC64L8	SPC56EC70L8	SPC56EC74L8
BGA256	SPC56EC64B3	SPC56EC70B3	SPC56EC74B3

Contents

1	Introduction	8
1.1	Document Overview	8
1.2	Description	8
1.3	Block diagram	11
2	Package pinouts and signal descriptions	14
2.1	Pad types	18
2.2	System pins	18
2.3	Functional ports	18
3	Electrical Characteristics	48
3.1	Parameter classification	48
3.2	NVUSRO register	48
3.2.1	NVUSRO [PAD3V5V(0)] field description	49
3.2.2	NVUSRO [PAD3V5V(1)] field description	49
3.3	Absolute maximum ratings	49
3.4	Recommended operating conditions	51
3.5	Thermal characteristics	54
3.5.1	Package thermal characteristics	54
3.5.2	Power considerations	54
3.6	I/O pad electrical characteristics	55
3.6.1	I/O pad types	55
3.6.2	I/O input DC characteristics	56
3.6.3	I/O output DC characteristics	57
3.6.4	Output pin transition times	59
3.6.5	I/O pad current specification	60
3.7	RESET electrical characteristics	61
3.8	Power management electrical characteristics	64
3.8.1	Voltage regulator electrical characteristics	64
3.8.2	VDD_BV options	65
3.8.3	Voltage monitor electrical characteristics	66
3.9	Low voltage domain power consumption	68
3.10	Flash memory electrical characteristics	69

3.10.1	Program/Erase characteristics	69
3.10.2	Flash memory power supply DC characteristics	71
3.10.3	Flash memory start-up/switch-off timings	72
3.11	Electromagnetic compatibility (EMC) characteristics	72
3.11.1	Designing hardened software to avoid noise problems	72
3.11.2	Electromagnetic interference (EMI)	73
3.11.3	Absolute maximum ratings (electrical sensitivity)	73
3.12	Fast external crystal oscillator (4–40 MHz) electrical characteristics	74
3.13	Slow external crystal oscillator (32 kHz) electrical characteristics	77
3.14	FMPLL electrical characteristics	80
3.15	Fast internal RC oscillator (16 MHz) electrical characteristics	80
3.16	Slow internal RC oscillator (128 kHz) electrical characteristics	82
3.17	ADC electrical characteristics	82
3.17.1	Introduction	82
3.18	Fast Ethernet Controller	93
3.18.1	MII Receive Signal Timing (RXD[3:0], RX_DV, RX_ER, and RX_CLK)	93
3.18.2	MII Transmit Signal Timing (TXD[3:0], TX_EN, TX_ER, TX_CLK)	94
3.18.3	MII Async Inputs Signal Timing (CRS and COL)	95
3.18.4	MII Serial Management Channel Timing (MDIO and MDC)	95
3.19	On-chip peripherals	97
3.19.1	Current consumption	97
3.19.2	DSPI characteristics	98
3.19.3	Nexus characteristics	104
3.19.4	JTAG characteristics	106
4	Package characteristics	108
4.1	ECOPACK®	108
4.2	Package mechanical data	109
4.2.1	LQFP176 package mechanical drawing	109
4.2.2	LQFP208 package mechanical drawing	111
4.2.3	LBGA208 package mechanical drawing	113
4.2.4	LBGA256 package mechanical drawing	115
5	Ordering information	117
Appendix A	Abbreviations	118

Revision history 119



List of tables

Table 1.	Device summary	1
Table 2.	SPC564Bxx and SPC56ECxx family comparison.	9
Table 3.	SPC564Bxx and SPC56ECxx series block summary.	12
Table 4.	System pin descriptions	18
Table 5.	Functional port pin descriptions	19
Table 6.	Parameter classifications	48
Table 7.	PAD3V5V(0) field description	49
Table 8.	PAD3V5V(1) field description	49
Table 9.	Absolute maximum ratings	49
Table 10.	Recommended operating conditions (3.3 V)	51
Table 11.	Recommended operating conditions (5.0 V)	52
Table 12.	LQFP thermal characteristics	54
Table 13.	LBGA208 thermal characteristics	54
Table 14.	LBGA256 thermal characteristics	54
Table 15.	I/O input DC electrical characteristics.	56
Table 16.	I/O pull-up/pull-down DC electrical characteristics	57
Table 17.	SLOW configuration output buffer electrical characteristics	57
Table 18.	MEDIUM configuration output buffer electrical characteristics	58
Table 19.	FAST configuration output buffer electrical characteristics.	58
Table 20.	Output pin transition times	59
Table 21.	I/O supplies.	60
Table 22.	I/O consumption	60
Table 23.	Reset electrical characteristics	62
Table 24.	Voltage regulator electrical characteristics	65
Table 25.	Low voltage monitor electrical characteristics.	67
Table 26.	Low voltage power domain electrical characteristics	68
Table 27.	Code flash memory—Program and erase specifications	69
Table 28.	Data flash memory—Program and erase specifications.	70
Table 29.	Flash memory module life.	70
Table 30.	Flash memory read access timing	71
Table 31.	Flash memory power supply DC electrical characteristics	71
Table 32.	Start-up time/Switch-off time.	72
Table 33.	EMI radiated emission measurement	73
Table 34.	ESD absolute maximum ratings	73
Table 35.	Latch-up results	74
Table 36.	Crystal description	75
Table 37.	Fast external crystal oscillator (4 to 40 MHz) electrical characteristics.	76
Table 38.	Crystal motional characteristics	78
Table 39.	Slow external crystal oscillator (32 kHz) electrical characteristics	79
Table 40.	FMPLL electrical characteristics	80
Table 41.	Fast internal RC oscillator (16 MHz) electrical characteristics	80
Table 42.	Slow internal RC oscillator (128 kHz) electrical characteristics	82
Table 43.	ADC input leakage current	88
Table 44.	ADC conversion characteristics (10-bit ADC_0).	88
Table 45.	Conversion characteristics (12-bit ADC_1).	91
Table 46.	MII Receive Signal Timing	93
Table 47.	MII transmit signal timing	94
Table 48.	MII Async Inputs Signal Timing	95

Table 49.	MII serial management channel timing	95
Table 50.	On-chip peripherals current consumption	97
Table 51.	DSPI timing	98
Table 52.	Nexus debug port timing	104
Table 53.	JTAG characteristics	106
Table 54.	LQFP176 mechanical data	110
Table 55.	LQFP208 mechanical data	112
Table 56.	LBGA208 mechanical data	114
Table 57.	LBGA256 mechanical data	116
Table 58.	Abbreviations	118
Table 59.	Revision history	119

List of figures

Figure 1.	SPC564Bxx and SPC56ECxx block diagram	11
Figure 2.	176-pin LQFP configuration	14
Figure 3.	208-pin LQFP configuration	15
Figure 4.	LBGA208 configuration	16
Figure 5.	256-pin BGA configuration	17
Figure 6.	I/O input DC electrical characteristics definition	56
Figure 7.	Start-up reset requirements	62
Figure 8.	Noise filtering on reset signal	62
Figure 9.	Voltage regulator capacitance connection	64
Figure 10.	Low voltage monitor vs. Reset	67
Figure 11.	Crystal oscillator and resonator connection scheme	75
Figure 12.	Fast external crystal oscillator (4 to 40 MHz) electrical characteristics.	76
Figure 13.	Crystal oscillator and resonator connection scheme	77
Figure 14.	Equivalent circuit of a quartz crystal	78
Figure 15.	Slow external crystal oscillator (32 kHz) electrical characteristics	79
Figure 16.	ADC_0 characteristic and error definitions	83
Figure 17.	Input equivalent circuit (precise channels)	84
Figure 18.	Input equivalent circuit (extended channels)	85
Figure 19.	Transient behavior during sampling phase	85
Figure 20.	Spectral representation of input signal	87
Figure 21.	ADC_1 characteristic and error definitions	90
Figure 22.	MII receive signal timing diagram	94
Figure 23.	MII transmit signal timing diagram	95
Figure 24.	MII async inputs timing diagram	95
Figure 25.	MII serial management channel timing diagram	96
Figure 26.	DSPI classic SPI timing—master, CPHA = 0	100
Figure 27.	DSPI classic SPI timing—master, CPHA = 1	100
Figure 28.	DSPI classic SPI timing—slave, CPHA = 0	101
Figure 29.	DSPI classic SPI timing—slave, CPHA = 1	101
Figure 30.	DSPI modified transfer format timing—master, CPHA = 0	102
Figure 31.	DSPI modified transfer format timing—master, CPHA = 1	102
Figure 32.	DSPI modified transfer format timing—slave, CPHA = 0	103
Figure 33.	DSPI modified transfer format timing—slave, CPHA = 1	103
Figure 34.	DSPI PCS strobe (PCSS) timing	104
Figure 35.	Nexus output timing	105
Figure 36.	Nexus TDI, TMS, TDO timing	106
Figure 37.	Timing diagram - JTAG boundary scan	107
Figure 38.	LQFP176 package mechanical drawing	109
Figure 39.	LQFP208 mechanical drawing	111
Figure 40.	LBGA208 package mechanical drawing	113
Figure 41.	LBGA256 mechanical drawing	115
Figure 42.	Ordering information scheme	117

1 Introduction

1.1 Document Overview

This document describes the features of the family and options available within the family members, and highlights important electrical and physical characteristics of the SPC564Bxx and SPC56ECxx device. To ensure a complete understanding of the device functionality, refer also to the SPC564Bxx and SPC56ECxx Reference Manual.

1.2 Description

The SPC564Bxx and SPC56ECxx is a new family of next generation microcontrollers built on the Power Architecture embedded category. This document describes the features of the family and options available within the family members, and highlights important electrical and physical characteristics of the device.

The SPC564Bxx and SPC56ECxx family expands the range of the C560B microcontroller family. It provides the scalability needed to implement platform approaches and delivers the performance required by increasingly sophisticated software architectures. The advanced and cost-efficient host processor core of the SPC564Bxx and SPC56ECxx automotive controller family complies with the Power Architecture embedded category, which is 100 percent user-mode compatible with the original Power Architecture user instruction set architecture (UIA). It operates at speeds of up to 120 MHz and offers high performance processing optimized for low power consumption. It also capitalizes on the available development infrastructure of current Power Architecture devices and is supported with software drivers, operating systems and configuration code to assist with users implementations.

Table 2. SPC564Bxx and SPC56ECxx family comparison⁽¹⁾

Feature	SPC564B64		SPC56EC64			SPC564B70		SPC56EC70			SPC564B74		SPC56EC74		
Package	LQFP 176	LQFP 208	LQFP 176	LQFP 208	BGA 256	LQFP 176	LQFP 208	LQFP 176	LQFP 208	BGA2 56	LQFP 176	LQFP 208	LQFP 176	LQFP 208	BGA 256
CPU	e200z4d		e200z4d + e200z0h			e200z4d		e200z4d + e200z0h			e200z4d		e200z4d + e200z0h		
Execution speed ⁽²⁾	Up to 120 MHz (e200z4d)		Up to 120 MHz (e200z4d) Up to 80 MHz (e200z0h) ⁽³⁾			Up to 120 MHz (e200z4d)		Up to 120 MHz (e200z4d) Up to 80 MHz (e200z0h) ⁽³⁾			Up to 120 MHz (e200z4d)		Up to 120 MHz (e200z4d) Up to 80 MHz (e200z0h) ⁽³⁾		
Code flash memory	1.5 MB					2 MB					3 MB				
Data flash memory	4 x16 KB														
SRAM	128 KB		192 KB			160 KB		256 KB			192 KB		256 KB		
MPU	16-entry														
eDMA ⁽⁴⁾	32 ch														
10-bit ADC		27 ch	33 ch	27 ch	33 ch	27 ch	33 ch	27 ch	33 ch	27 ch	33 ch	27 ch	33 ch	27 ch	33 ch
	dedicated ^{(5), (6)}														
	shared with 12-bit ADC ⁽⁷⁾	19 ch													
12-bit ADC		5 ch	10 ch	5 ch	10 ch	5 ch	10 ch	5 ch	10 ch	5 ch	10 ch	5 ch	10 ch	5 ch	10 ch
	dedicated ⁽⁸⁾														
	shared with 10-bit ADC ⁷	19 ch													
CTU		64 ch													
Total timer I/O ⁽⁹⁾ eMIOS		64 ch, 16-bit													
SCI (LINFlexD)		10													
SPI (DSPI)		8													
CAN (FlexCAN) ⁽¹⁰⁾		6													

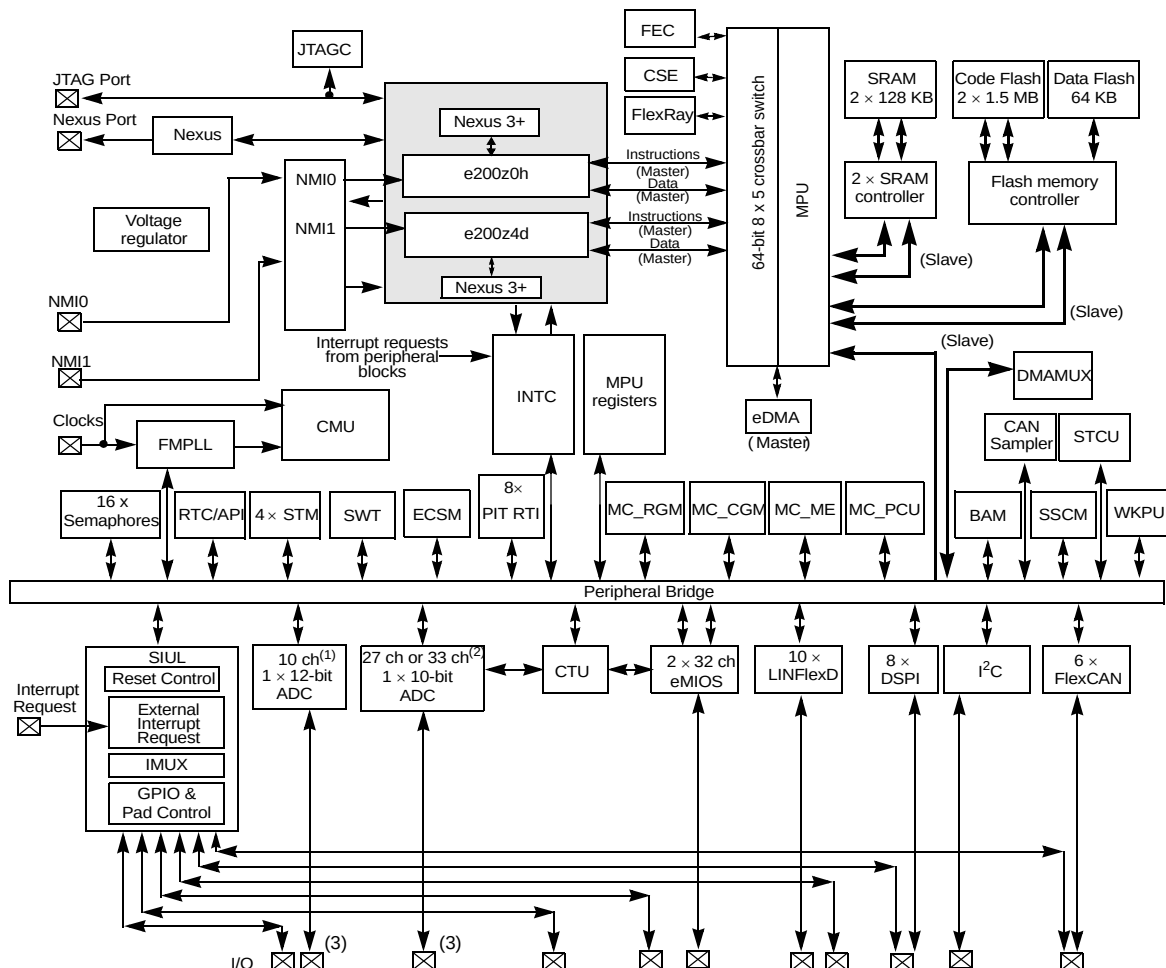
Table 2. SPC564Bxx and SPC56ECxx family comparison⁽¹⁾ (continued)

Feature	SPC564B64		SPC56EC64			SPC564B70		SPC56EC70			SPC564B74		SPC56EC74		
Package	LQFP 176	LQFP 208	LQFP 176	LQFP 208	BGA 256	LQFP 176	LQFP 208	LQFP 176	LQFP 208	BGA2 56	LQFP 176	LQFP 208	LQFP 176	LQFP 208	BGA 256
FlexRay	Yes														
STCU ⁽¹¹⁾	Yes														
Ethernet	No		Yes			No		Yes			No		Yes		
I ² C	1														
32 kHz oscillator (SXOSC)	Yes														
GPIO ⁽¹²⁾	147	177	147	177	199	147	177	147	177	199	147	177	147	177	199
Debug	JTAG				Nexus 3+	JTAG				Nexus 3+	JTAG				Nexus 3+
Cryptographic Services Engine (CSE)	Optional														

1. Feature set dependent on selected peripheral multiplexing; table shows example.
2. Based on 125 °C ambient operating temperature and subject to full device characterisation.
3. The e200z0h can run at speeds up to 80 MHz. However, if system frequency is >80 MHz (e.g., e200z4d running at 120 MHz) the e200z0h needs to run at 1/2 system frequency. There is a configurable e200z0 system clock divider for this purpose.
4. DMAMUX also included that allows for software selection of 32 out of a possible 57 sources.
5. Not shared with 12-bit ADC, but possibly shared with other alternate functions.
6. There are 23 dedicated ANS plus 4 dedicated ANX channels on LQPF176. For higher pin count packages, there are 29 dedicated ANS plus 4 dedicated ANX channels.
7. 16x precision channels (ANP) and 3x standard (ANS).
8. Not shared with 10-bit ADC, but possibly shared with other alternate functions.
9. As a minimum, all timer channels can function as PWM or Input Capture and Output Control. Refer to the eMIOS section of the device reference manual for information on the channel configuration and functions.
10. CAN Sampler also included that allows ID of CAN message to be captured when in low power mode.
11. STCU controls MBIST activation and reporting.
12. Estimated I/O count for proposed packages based on multiplexing with peripherals.

1.3 Block diagram

Figure 1 shows the detailed block diagram of the SPC564Bxx and SPC56ECxx.



Legend:	ADC	Analog-to-Digital Converter	JTAGC	JTAG controller
	BAM	Boot Assist Module	LINFlexD	Local Interconnect Network Flexible with DMA support
	CSE	Cryptographic Services Engine	MC_ME	Mode Entry Module
	CAN	Controller Area Network (FlexCAN)	MC_CGM	Clock Generation Module
	CMU	Clock Monitor Unit	MC_PCU	Power Control Unit
	CTU	Cross Triggering Unit	MC_RGM	Reset Generation Module
	DMAMUX	DMA Channel Multiplexer	MPU	Memory Protection Unit
	DSPI	Deserial Serial Peripheral Interface	Nexus	Nexus Development Interface
	eDMA	enhanced Direct Memory Access	NMI	Non-Maskable Interrupt
	FlexCAN	Controller Area Network controller modules	PIT_RT1	Periodic Interrupt Timer with Real-Time Interrupt
	FEC	Fast Ethernet Controller	RTC/API	Real-Time Clock/ Autonomous Periodic Interrupt
	eMIOS	Enhanced Modular Input Output System	SIUL	System Integration Unit Lite
	ECSM	Error Correction Status Module	SRAM	Static Random-Access Memory
	FMPLL	Frequency-Modulated Phase-Locked Loop	SSCM	System Status Configuration Module
	FlexRay	FlexRay Communication Controller	STM	System Timer Module
	I2C	Inter-integrated Circuit Bus	SWT	Software Watchdog Timer
	IMUX	Internal Multiplexer	STCU	Self Test Control Unit
	INTC	Interrupt Controller	WKPU	WakeUp Unit

Notes:

- 1) 10 dedicated channels plus up to 19 shared channels. See the device-comparison table.
- 2) Package dependent. 27 or 33 dedicated channels plus up to 19 shared channels. See the device-comparison table.
- 3) 16 x precision channels (ANP) are mapped on input only I/O cells.

Figure 1. SPC564Bxx and SPC56ECxx block diagram

[Table 3](#) summarizes the functions of the blocks present on the SPC564Bxx and SPC56ECxx.

Table 3. SPC564Bxx and SPC56ECxx series block summary

Block	Function
Analog-to-digital converter (ADC)	Converts analog voltages to digital values
Boot assist module (BAM)	A block of read-only memory containing VLE code which is executed according to the boot mode of the device
Clock monitor unit (CMU)	Monitors clock source (internal and external) integrity
Cross triggering unit (CTU)	Enables synchronization of ADC conversions with a timer event from the eMIOS or from the PIT
Cryptographic Security Engine (CSE)	Supports the encoding and decoding of any kind of data
Crossbar (XBAR) switch	Supports simultaneous connections between two master ports and three slave ports. The crossbar supports a 32-bit address bus width and a 64-bit data bus width
DMA Channel Multiplexer (DMAMUX)	Allows to route DMA sources (called slots) to DMA channels
Deserial serial peripheral interface (DSPI)	Provides a synchronous serial interface for communication with external devices
Error Correction Status Module (ECSM)	Provides a myriad of miscellaneous control functions for the device including program-visible information about configuration and revision levels, a reset status register, wakeup control for exiting sleep modes, and optional features such as information on memory errors reported by error-correcting codes
Enhanced Direct Memory Access (eDMA)	Performs complex data transfers with minimal intervention from a host processor via "n" programmable channels.
Enhanced modular input output system (eMIOS)	Provides the functionality to generate or measure events
Flash memory	Provides non-volatile storage for program code, constants and variables
FlexCAN (controller area network)	Supports the standard CAN communications protocol
FMPLL (frequency-modulated phase-locked loop)	Generates high-speed system clocks and supports programmable frequency modulation
FlexRay (FlexRay communication controller)	Provides high-speed distributed control for advanced automotive applications
Fast Ethernet Controller (FEC)	Ethernet Media Access Controller (MAC) designed to support both 10 and 100 Mbps Ethernet/IEEE 802.3 networks
Internal multiplexer (IMUX) SIUL subblock	Allows flexible mapping of peripheral interface on the different pins of the device
Inter-integrated circuit (I ² C™) bus	A two wire bidirectional serial bus that provides a simple and efficient method of data exchange between devices
Interrupt controller (INTC)	Provides priority-based preemptive scheduling of interrupt requests for both e200z0h and e200z4d cores
JTAG controller	Provides the means to test chip functionality and connectivity while remaining transparent to system logic when not in test mode

Table 3. SPC564Bxx and SPC56ECxx series block summary (continued)

Block	Function
LinFlexD (Local Interconnect Network Flexible with DMA support)	Manages a high number of LIN (Local Interconnect Network protocol) messages efficiently with a minimum of CPU load
Memory protection unit (MPU)	Provides hardware access control for all memory references generated in a device
Clock generation module (MC_CGM)	Provides logic and control required for the generation of system and peripheral clocks
Power control unit (MC_PCU)	Reduces the overall power consumption by disconnecting parts of the device from the power supply via a power switching device; device components are grouped into sections called "power domains" which are controlled by the PCU
Reset generation module (MC_RGM)	Centralizes reset sources and manages the device reset sequence of the device
Mode entry module (MC_ME)	Provides a mechanism for controlling the device operational mode and modetransition sequences in all functional states; also manages the power control unit, reset generation module and clock generation module, and holds the configuration, control and status registers accessible for applications
Non-Maskable Interrupt (NMI)	Handles external events that must produce an immediate response, such as power down detection
Nexus Development Interface (NDI)	Provides real-time development capabilities for e200z0h and e200z4d core processor
Periodic interrupt timer/ Real Time Interrupt Timer (PIT_RTI)	Produces periodic interrupts and triggers
Real-time counter (RTC/API)	A free running counter used for time keeping applications, the RTC can be configured to generate an interrupt at a predefined interval independent of the mode of operation (run mode or low-power mode). Supports autonomous periodic interrupt (API) function to generate a periodic wakeup request to exit a low power mode or an interrupt request
Static random-access memory (SRAM)	Provides storage for program code, constants, and variables
System integration unit lite (SIUL)	Provides control over all the electrical pad controls and up 32 ports with 16 bits of bidirectional, general-purpose input and output signals and supports up to 32 external interrupts with trigger event configuration
System status and configuration module (SSCM)	Provides system configuration and status data (such as memory size and status, device mode and security status), device identification data, debug status port enable and selection, and bus and peripheral abort enable/disable
System timer module (STM)	Provides a set of output compare events to support AutoSAR and operating system tasks
Semaphores	Provides the hardware support needed in multi-core systems for sharing resources and provides a simple mechanism to achieve lock/unlock operations via a single write access.
Wake Unit (WKPU)	Supports external sources that can generate interrupts or wakeup events, of which can cause non-maskable interrupt requests or wakeup events.

2 Package pinouts and signal descriptions

The available LQFP pinouts and the LBGA ballmaps are provided in the following figures.
For functional port pin description, see [Table 6](#).

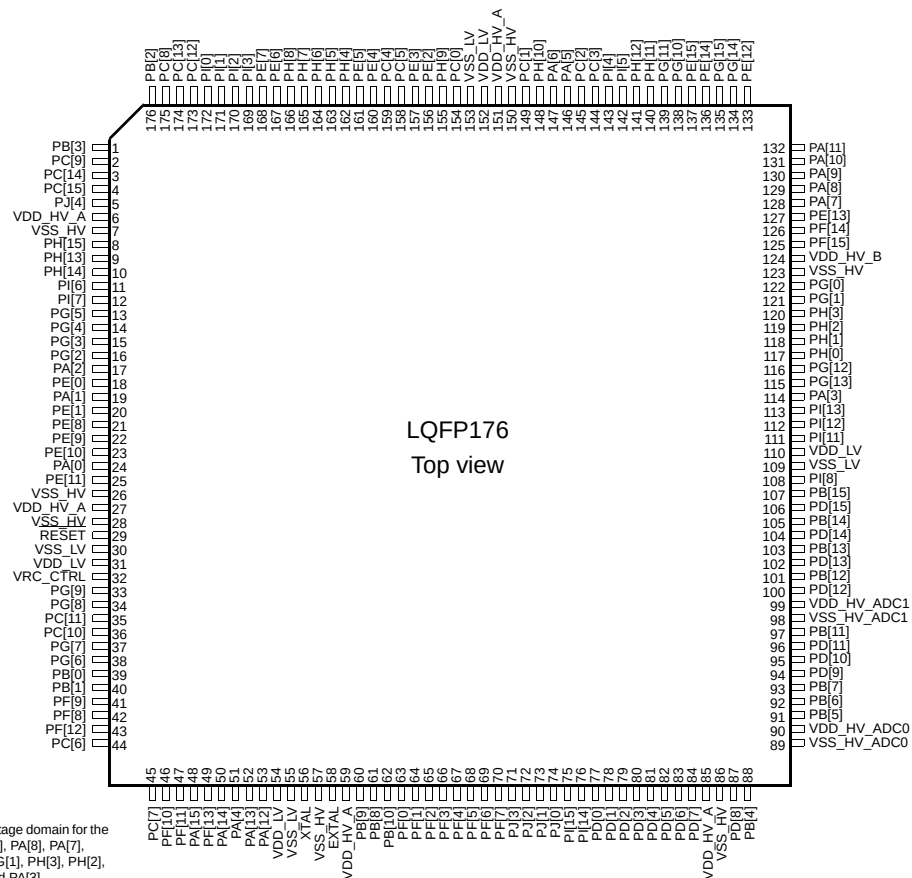
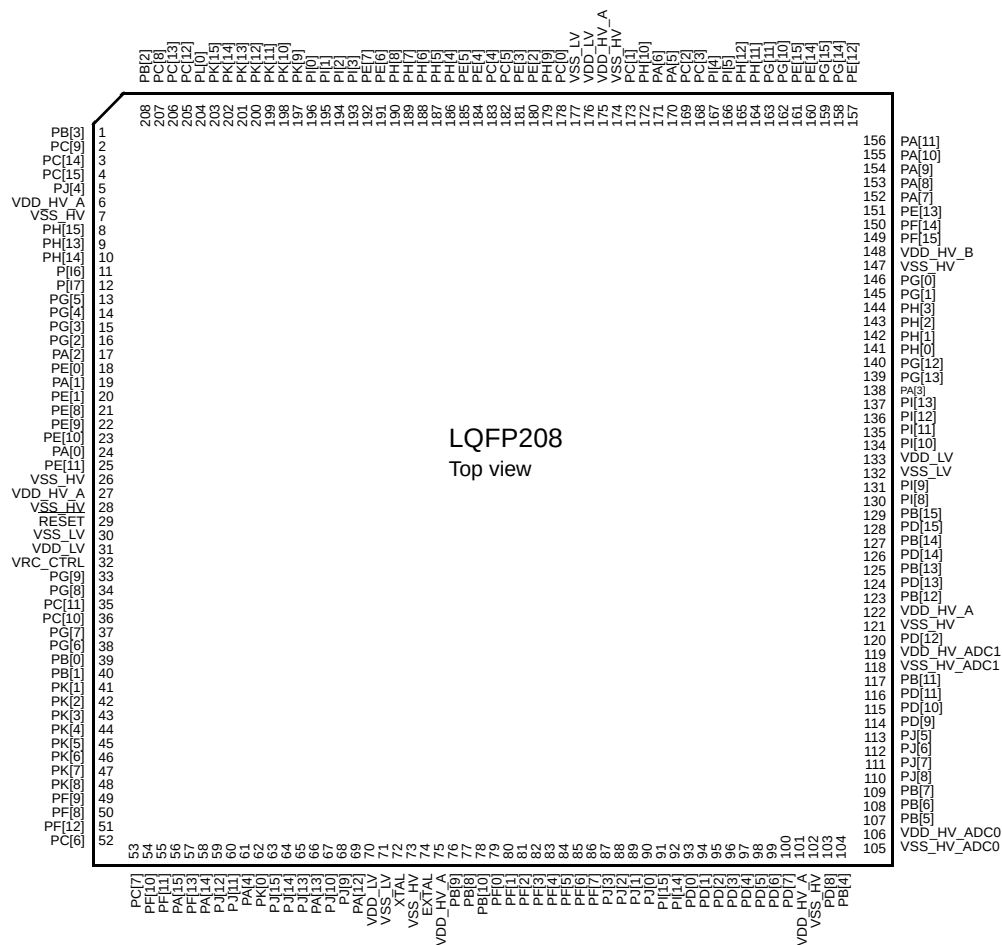


Figure 2. 176-pin LQFP configuration

**NOTE**

- 1) VDD_HV_B supplies the IO voltage domain for the pins PE[12], PA[11], PA[10], PA[9], PA[8], PA[7], PE[13], PF[14], PF[15], PG[0], PG[1], PH[3], PH[2], PH[1], PH[0], PG[12], PG[13], and PA[3].
- 2) Availability of port pin alternate functions depends on product selection.

Figure 3. 208-pin LQFP configuration

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	PC[15]	PB[2]	PC[13]	PI[1]	PE[7]	PH[8]	PE[2]	PE[4]	PC[4]	PE[3]	PH[9]	PI[4]	PH[11]	PE[14]	PA[10]	PG[11]	A
B	PH[13]	PC[14]	PC[8]	PC[12]	PI[3]	PE[6]	PH[5]	PE[5]	PC[5]	PC[0]	PC[2]	PH[12]	PG[10]	PA[11]	PA[9]	PA[8]	B
C	PH[14]	VDD_HV_A	PC[9]	PL[0]	PI[0]	PH[7]	PH[6]	VSS_LV	VDD_HV_A	PA[5]	PC[3]	PE[15]	PG[14]	PE[12]	PA[7]	PE[13]	C
D	PG[5]	PI[6]	PJ[4]	PB[3]	PK[15]	PI[2]	PH[4]	VDD_LV	PC[1]	PH[10]	PA[6]	PI[5]	PG[15]	PF[14]	PF[15]	PH[2]	D
E	PG[3]	PI[7]	PH[15]	PG[2]									PG[0]	PG[1]	PH[0]	VDD_HV_A	E
F	PA[2]	PG[4]	PA[1]	PE[1]									PH[1]	PH[3]	PG[12]	PG[13]	F
G	PE[8]	PE[0]	PE[10]	PA[0]									VDD_HV_B	PI[13]	PI[12]	PA[3]	G
H	PE[9]	VDD_HV_A	PE[11]	PK[1]									VDD_HV_A	VDD_LV	VSS_LV	PI[11]	H
J	VSS_HV	VRC_CTL	VDD_LV	PG[9]									PD[15]	PI[8]	PI[9]	PI[10]	J
K	RESET	VSS_LV	PG[8]	PC[11]									PD[14]	PD[13]	PB[14]	PB[15]	K
L	PC[10]	PG[7]	PB[0]	PK[2]									PD[12]	PB[12]	PB[13]	VDD_HV_ADC1	L
M	PG[6]	PB[1]	PK[4]	PF[9]									PB[11]	PD[10]	PD[11]	VSS_HV_ADC1	M
N	PK[3]	PF[8]	PC[6]	PC[7]	PJ[13]	VDD_HV_A	PB[10]	PF[6]	VDD_HV_A	PJ[1]	PD[2]	PJ[5]	PB[5]	PB[6]	PJ[6]	PD[9]	N
P	PF[12]	PF[10]	PF[13]	PA[14]	PJ[9]	PA[12]	PF[0]	PF[5]	PF[7]	PJ[3]	PI[15]	PD[4]	PD[7]	PD[8]	PJ[8]	PJ[7]	P
R	PF[11]	PA[15]	PJ[11]	PJ[15]	PA[13]	PF[2]	PF[3]	PF[4]	VDD_LV	PJ[2]	PJ[0]	PD[0]	PD[3]	PD[6]	VDD_HV_ADC0	PB[7]	R
T	PJ[12]	PA[4]	PK[0]	PJ[14]	PJ[10]	PF[1]	XTAL	EXTAL	VSS_LV	PB[9]	PB[8]	PI[14]	PD[1]	PD[5]	VSS_HV_ADC0	PB[4]	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

Notes:

1. VDD_HV_B supplies the IO voltage domain for the pins PE[12], PA[11], PA[10], PA[9], PA[8], PA[7], PE[13], PF[14], PF[15], PG[0], PG[1], PH[3], PH[2], PH[1], PH[0], PG[12], PG[13], and PA[3].
2. Availability of port pin alternate functions depends on product selection.

Figure 4. LPGA208 configuration

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	PC[15]	PB[2]	PC[13]	PI[1]	PE[7]	PH[8]	PE[2]	PE[4]	PC[4]	PE[3]	PH[9]	PI[4]	PH[11]	PE[14]	PA[10]	PG[11]	A
B	PH[13]	PC[14]	PC[8]	PC[12]	PI[3]	PE[6]	PH[5]	PE[5]	PC[5]	PC[0]	PC[2]	PH[12]	PG[10]	PA[11]	PA[9]	PA[8]	B
C	PH[14]	VDD_HV_A	PC[9]	PL[0]	PI[0]	PH[7]	PH[6]	VSS_LV	VDD_HV_A	PA[5]	PC[3]	PE[15]	PG[14]	PE[12]	PA[7]	PE[13]	C
D	PG[5]	PI[6]	PJ[4]	PB[3]	PK[15]	PI[2]	PH[4]	VDD_LV	PC[1]	PH[10]	PA[6]	PI[5]	PG[15]	PF[14]	PF[15]	PH[2]	D
E	PG[3]	PI[7]	PH[15]	PG[2]	VDD_LV	VSS_LV	PK[10]	PK[9]	PM[1]	PM[0]	PL[15]	PL[14]	PG[0]	PG[1]	PH[0]	VDD_HV_A	E
F	PA[2]	PG[4]	PA[1]	PE[1]	PL[2]	PM[6]	PL[1]	PK[11]	PM[5]	PL[13]	PL[12]	PM[2]	PH[1]	PH[3]	PG[12]	PG[13]	F
G	PE[8]	PE[0]	PE[10]	PA[0]	PL[3]	VSS_HV	VSS_HV	VSS_HV	VSS_HV	VSS_HV	VSS_HV	PK[12]	VDD_HV_B	PI[13]	PI[12]	PA[3]	G
H	PE[9]	VDD_HV_A	PE[11]	PK[1]	PL[4]	VSS_LV	VSS_LV	VSS_HV	VSS_HV	VSS_HV	VSS_HV	PK[13]	VDD_HV_A	VDD_LV	VSS_LV	PI[11]	H
J	VSS_HV	VRC_CTL	VDD_LV	PG[9]	PL[5]	VSS_LV	VSS_LV	VSS_LV	VSS_HV	VSS_HV	VSS_HV	PK[14]	PD[15]	PI[8]	PI[9]	PI[10]	J
K	RESET	VSS_LV	PG[8]	PC[11]	PL[6]	VSS_LV	VSS_LV	VSS_LV	VSS_LV	VDD_LV	VDD_LV	PM[3]	PD[14]	PD[13]	PB[14]	PB[15]	K
L	PC[10]	PG[7]	PB[0]	PK[2]	PL[7]	VSS_LV	VSS_LV	VSS_LV	VSS_LV	VDD_LV	VDD_LV	PM[4]	PD[12]	PB[12]	PB[13]	VDD_HV_ADC1	L
M	PG[6]	PB[1]	PK[4]	PF[9]	PK[5]	PK[6]	PK[7]	PK[8]	PL[8]	PL[9]	PL[10]	PL[11]	PB[11]	PD[10]	PD[11]	VSS_HV_ADC1	M
N	PK[3]	PF[8]	PC[6]	PC[7]	PJ[13]	VDD_HV_A	PB[10]	PF[6]	VDD_HV_A	PJ[1]	PD[2]	PJ[5]	PB[5]	PB[6]	PJ[6]	PD[9]	N
P	PF[12]	PF[10]	PF[13]	PA[14]	PJ[9]	PA[12]	PF[0]	PF[5]	PF[7]	PJ[3]	PI[15]	PD[4]	PD[7]	PD[8]	PJ[8]	PJ[7]	P
R	PF[11]	PA[15]	PJ[11]	PJ[15]	PA[13]	PF[2]	PF[3]	PF[4]	VDD_LV	PJ[2]	PJ[0]	PD[0]	PD[3]	PD[6]	VDD_HV_ADC0	PB[7]	R
T	PJ[12]	PA[4]	PK[0]	PJ[14]	PJ[10]	PF[1]	XTAL	EXTAL	VSS_LV	PB[9]	PB[8]	PI[14]	PD[1]	PD[5]	VSS_HV_ADC0	PB[4]	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

Notes:

- 1) VDD_HV_B supplies the IO voltage domain for the pins PE[12], PA[11], PA[10], PA[9], PA[8], PA[7], PE[13], PF[14], PF[15], PG[0], PG[1], PH[3], PH[2], PH[1], PH[0], PG[12], PG[13], PA[3], PM[3], and PM[4].
- 2) Availability of port pin alternate functions depends on product selection.

Figure 5. 256-pin BGA configuration

2.1 Pad types

In the device the following types of pads are available for system pins and functional port pins:

S = Slow^(a)

M = Medium^{(a), (b)}

F = Fast^{(a), (b)}

I = Input only with analog feature^(a)

A = Analog

2.2 System pins

The system pins are listed in [Table 4](#).

Table 4. System pin descriptions

Port pin	Function	I/O direction	Pad type	RESET config.	Pin number			
					LQFP 176	LQFP 208	LBGA208	LBGA 256
RESET	Bidirectional reset with Schmitt-Trigger characteristics and noise filter.	I/O	M	Input, weak pull-up only after PHASE2	29	29	K1	K1
EXTAL	Analog input of the oscillator amplifier circuit. Needs to be grounded if oscillator bypass mode is used.	I	A ⁽¹⁾	—	58	74	T8	T8
XTAL	Analog output of the oscillator amplifier circuit, when the oscillator is not in bypass mode. Analog input for the clock generator when the oscillator is in bypass mode.	I/O	A ⁽¹⁾	—	56	72	T7	T7

1. For analog pads, it is not recommended to enable IBE if APC is enabled to avoid extra current in middle range voltage.

2.3 Functional ports

The functional port pins are listed in [Table 5](#).

-
- a. See the I/O pad electrical characteristics in the device datasheet for details.
 - b. All medium and fast pads are in slow configuration by default at reset and can be configured as fast or medium. For example, Fast/Medium pad will be Medium by default at reset. Similarly, Slow/Medium pad will be Slow by default. Only exception is PC[1] which is in medium configuration by default (refer to PCR.SRC in the reference manual, Pad Configuration Registers (PCR0—PCR198)).

Table 5. Functional port pin descriptions

Port pin	PCR	Alternate function ⁽¹⁾	Function	Peripheral	I/O direction ⁽²⁾	Pad type	RESET config.	Pin number			
								LQFP 176	LQFP 208	LBGA208	LBGA256
PA[0]	PCR[0]	AF0 AF1 AF2 AF3 — —	GPIO[0] E0UC[0] CLKOUT E0UC[13] WKPU[19] CAN1RX	SIUL eMIOS_0 MC_CGM eMIOS_0 WKPU FlexCAN_1	I/O I/O O I/O I I	M/ S	Tristate	24	24	G4	G4
PA[1]	PCR[1]	AF0 AF1 AF2 AF3 — — —	GPIO[1] E0UC[1] — — — WKPU[2] CAN3RX NMI[0] ⁽³⁾	SIUL eMIOS_0 — — — WKPU FlexCAN_3 WKPU	I/O I/O — — — I I I	S	Tristate	19	19	F3	F3
PA[2]	PCR[2]	AF0 AF1 AF2 AF3 — —	GPIO[2] E0UC[2] — MA[2] WKPU[3] NMI[1] ⁽³⁾	SIUL eMIOS_0 — ADC_0 WKPU WKPU	I/O I/O — O I I	S	Tristate	17	17	F1	F1
PA[3]	PCR[3]	AF0 AF1 AF2 AF3 — — —	GPIO[3] E0UC[3] LIN5TX CS4_1 RX_ER_CLK EIRQ[0] ADC1_S[0]	SIUL eMIOS_0 LINFlexD_5 DSPI_1 FEC SIUL ADC_1	I/O I/O O O I I I	M/ S	Tristate	114	138	G16	G16
PA[4]	PCR[4]	AF0 AF1 AF2 AF3 — —	GPIO[4] E0UC[4] — CS0_1 LIN5RX WKPU[9]	SIUL eMIOS_0 — DSPI_1 LINFlexD_5 WKPU	I/O I/O — I/O I I	S	Tristate	51	61	T2	T2
PA[5]	PCR[5]	AF0 AF1 AF2	GPIO[5] E0UC[5] LIN4TX	SIUL eMIOS_0 LINFlexD_4	I/O I/O O	M/ S	Tristate	146	170	C10	C10

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function ⁽¹⁾	Function	Peripheral	I/O direction ⁽²⁾	Pad type	RESET config.	Pin number			
								LQFP 176	LQFP 208	LBGA208	LBGA256
PA[6]	PCR[6]	AF0	GPIO[6]	SIUL	I/O	S	Tristate	147	171	D11	D11
		AF1	E0UC[6]	eMIOS_0	I/O						
		AF2	—	—	—						
		AF3	CS1_1	DSPI_1	O						
		—	LIN4RX	LINFlexD_4	I						
		—	EIRQ[1]	SIUL	I						
PA[7]	PCR[7]	AF0	GPIO[7]	SIUL	I/O	M/ S	Tristate	128	152	C15	C15
		AF1	E0UC[7]	eMIOS_0	I/O						
		AF2	LIN3TX	LINFlexD_3	O						
		AF3	—	—	—						
		—	RXD[2]	FEC	I						
		—	EIRQ[2]	SIUL	I						
PA[8]	PCR[8]	—	ADC1_S[1]	ADC_1	I						
		AF0	GPIO[8]	SIUL	I/O	M/ S	Input, weak pull-up	129	153	B16	B16
		AF1	E0UC[8]	eMIOS_0	I/O						
		AF2	E0UC[14]	eMIOS_0	I/O						
		AF3	—	—	—						
		—	RXD[1]	FEC	I						
		—	EIRQ[3]	SIUL	I						
PA[9]	PCR[9]	—	ABS[0]	MC_RGM	I						
		—	LIN3RX	LINFlexD_3	I						
		AF0	GPIO[9]	SIUL	I/O	M/ S	Pull- down	130	154	B15	B15
		AF1	E0UC[9]	eMIOS_0	I/O						
		AF2	—	—	—						
		AF3	CS2_1	DSPI1	O						
		—	RXD[0]	FEC	I						
		—	FAB	MC_RGM	I						
PA[10]	PCR[10]	AF0	GPIO[10]	SIUL	I/O	M/ S	Tristate	131	155	A15	A15
		AF1	E0UC[10]	eMIOS_0	I/O						
		AF2	SDA	I ² C	I/O						
		AF3	LIN2TX	LINFlexD_2	O						
		—	COL	FEC	I						
		—	ADC1_S[2]	ADC_1	I						
PA[10]	PCR[10]	—	SIN_1	DSPI_1	I						

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function ⁽¹⁾	Function	Peripheral	I/O direction ⁽²⁾	Pad type	RESET config.	Pin number			
								LQFP 176	LQFP 208	LBGA208	LBGA256
PA[11]	PCR[11]	AF0	GPIO[11]	SIUL	I/O	M/S	Tristate	132	156	B14	B14
		AF1	E0UC[11]	eMIOS_0	I/O						
		AF2	SCL	I ² C	I/O						
		AF3	—	—	—						
		—	RX_ER	FEC	I						
		—	EIRQ[16]	SIUL	I						
		—	LIN2RX	LINFlexD_2	I						
PA[12]	PCR[12]	—	ADC1_S[3]	ADC_1	I						
		AF0	GPIO[12]	SIUL	I/O	S	Tristate	53	69	P6	P6
		AF1	—	—	—						
		AF2	E0UC[28]	eMIOS_0	I/O						
		AF3	CS3_1	DSPI1	O						
		—	EIRQ[17]	SIUL	I						
		—	SIN_0	DSPI_0	I						
PA[13]	PCR[13]	AF0	GPIO[13]	SIUL	I/O	M/S	Tristate	52	66	R5	R5
		AF1	SOUT_0	DSPI_0	O						
		AF2	E0UC[29]	eMIOS_0	I/O						
		AF3	—	—	—						
PA[14]	PCR[14]	AF0	GPIO[14]	SIUL	I/O	M/S	Tristate	50	58	P4	P4
		AF1	SCK_0	DSPI_0	I/O						
		AF2	CS0_0	DSPI_0	I/O						
		AF3	E0UC[0]	eMIOS_0	I/O						
PA[15]	PCR[15]	—	EIRQ[4]	SIUL	I						
		AF0	GPIO[15]	SIUL	I/O	M/S	Tristate	48	56	R2	R2
		AF1	CS0_0	DSPI_0	I/O						
		AF2	SCK_0	DSPI_0	I/O						
		AF3	E0UC[1]	eMIOS_0	I/O						
		—	WKPU[10]	WKPU	I						
PB[0]	PCR[16]	AF0	GPIO[16]	SIUL	I/O	M/S	Tristate	39	39	L3	L3
		AF1	CAN0TX	FlexCAN_0	O						
		AF2	E0UC[30]	eMIOS_0	I/O						
		AF3	LIN0TX	LINFlexD_0	I						
PB[1]	PCR[17]	AF0	GPIO[17]	SIUL	I/O	S	Tristate	40	40	M2	M2
		AF1	—	—	—						
		AF2	E0UC[31]	eMIOS_0	I/O						
		—	LIN0RX	LINFlexD_0	I						
		—	WKPU[4]	WKPU	I						
		—	CAN0RX	FlexCAN_0	I						

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function ⁽¹⁾	Function	Peripheral	I/O direction ⁽²⁾	Pad type	RESET config.	Pin number			
								LQFP 176	LQFP 208	LBGA208	LBGA256
PB[2]	PCR[18]	AF0 AF1 AF2 AF3	GPIO[18] LIN0TX SDA E0UC[30]	SIUL LINFlexD_0 I ² C eMIOS_0	I/O O I/O I/O	M/ S	Tristate	176	208	A2	A2
PB[3]	PCR[19]	AF0 AF1 AF2 AF3 — —	GPIO[19] E0UC[31] SCL — WKPU[11] LIN0RX	SIUL eMIOS_0 I ² C — WKPU LINFlexD_0	I/O I/O I/O — I I	S	Tristate	1	1	D4	D4
PB[4]	PCR[20]	AF0 AF1 AF2 AF3 — —	GPI[20] — — — ADC0_P[0] ADC1_P[0]	SIUL — — — ADC_0 ADC_1	I — — — I I	I	Tristate	88	104	T16	T16
PB[5]	PCR[21]	AF0 AF1 AF2 AF3 — —	GPI[21] — — — ADC0_P[1] ADC1_P[1]	SIUL — — — ADC_0 ADC_1	I — — — I I	I	Tristate	91	107	N13	N13
PB[6]	PCR[22]	AF0 AF1 AF2 AF3 — —	GPI[22] — — — ADC0_P[2] ADC1_P[2]	SIUL — — — ADC_0 ADC_1	I — — — I I	I	Tristate	92	108	N14	N14
PB[7]	PCR[23]	AF0 AF1 AF2 AF3 — —	GPI[23] — — — ADC0_P[3] ADC1_P[3]	SIUL — — — ADC_0 ADC_1	I — — — I I	I	Tristate	93	109	R16	R16

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function ⁽¹⁾	Function	Peripheral	I/O direction ⁽²⁾	Pad type	RESET config.	Pin number			
								LQFP 176	LQFP 208	LBGA208	LBGA256
PB[8]	PCR[24]	AF0	GPI[24]	SIUL	I	I	—	61	77	T11	T11
		AF1	—	—	I						
		AF2	—	—	I						
		AF3	—	—	I						
		—	ADC0_S[0]	ADC_0	I						
		—	ADC1_S[4]	ADC_1	I						
		—	WKPU[25]	WKPU	I						
		—	OSC32k_XTAL ⁽⁴⁾	SXOSC	I						
PB[9] ⁽⁵⁾	PCR[25]	AF0	GPI[25]	SIUL	I	I	—	60	76	T10	T10
		AF1	—	—	I						
		AF2	—	—	I						
		AF3	—	—	I						
		—	ADC0_S[1]	ADC_0	I						
		—	ADC1_S[5]	ADC_1	I						
		—	WKPU[26]	WKPU	I						
		—	OSC32k_EXTAL ⁽⁴⁾	SXOSC	I						
PB[10]	PCR[26]	AF0	GPIO[26]	SIUL	I/O	S	Tristate	62	78	N7	N7
		AF1	SOUT_1	DSPI_1	O						
		AF2	CAN3TX	FlexCAN_3	—						
		AF3	—	—	—						
		—	ADC0_S[2]	ADC_0	I						
		—	ADC1_S[6]	ADC_1	I						
		—	WKPU[8]	WKPU	I						
		—	—	—	—						
PB[11]	PCR[27]	AF0	GPIO[27]	SIUL	I/O	S	Tristate	97	117	M13	M13
		AF1	E0UC[3]	eMIOS_0	I/O						
		AF2	—	—	—						
		AF3	CS0_0	DSPI_0	I/O						
		—	ADC0_S[3]	ADC_0	I						
		—	—	—	—						
PB[12]	PCR[28]	AF0	GPIO[28]	SIUL	I/O	S	Tristate	101	123	L14	L14
		AF1	E0UC[4]	eMIOS_0	I/O						
		AF2	—	—	—						
		AF3	CS1_0	DSPI_0	O						
		—	ADC0_X[0]	ADC_0	I						
		—	—	—	—						
PB[13]	PCR[29]	AF0	GPIO[29]	SIUL	I/O	S	Tristate	103	125	L15	L15
		AF1	E0UC[5]	eMIOS_0	I/O						
		AF2	—	—	—						
		AF3	CS2_0	DSPI_0	O						
		—	ADC0_X[1]	ADC_0	I						
		—	—	—	—						

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function ⁽¹⁾	Function	Peripheral	I/O direction ⁽²⁾	Pad type	RESET config.	Pin number			
								LQFP 176	LQFP 208	LBGA208	LBGA256
PB[14]	PCR[30]	AF0 AF1 AF2 AF3 —	GPIO[30] E0UC[6] — CS3_0 ADC0_X[2]	SIUL eMIOS_0 — DSPI_0 ADC_0	I/O I/O — O I	S	Tristate	105	127	K15	K15
PB[15]	PCR[31]	AF0 AF1 AF2 AF3 —	GPIO[31] E0UC[7] — CS4_0 ADC0_X[3]	SIUL eMIOS_0 — DSPI_0 ADC_0	I/O I/O — O I	S	Tristate	107	129	K16	K16
PC[0] ⁽⁶⁾	PCR[32]	AF0 AF1 AF2 AF3	GPIO[32] — TDI —	SIUL — JTAGC —	I/O — I —	M/ S	Input, weak pull-up	154	178	B10	B10
PC[1] ⁽⁶⁾	PCR[33]	AF0 AF1 AF2 AF3	GPIO[33] — TDO —	SIUL — JTAGC —	I/O — O —	F/ M	Tristate	149	173	D9	D9
PC[2]	PCR[34]	AF0 AF1 AF2 AF3 —	GPIO[34] SCK_1 CAN4TX — EIRQ[5]	SIUL DSPI_1 FlexCAN_4 — SIUL	I/O I/O O — I	M/ S	Tristate	145	169	B11	B11
PC[3]	PCR[35]	AF0 AF1 AF2 AF3 — — —	GPIO[35] CS0_1 MA[0] — CAN1RX CAN4RX EIRQ[6]	SIUL DSPI_1 ADC_0 — FlexCAN_1 FlexCAN_4 SIUL	I/O I/O O — I I I	S	Tristate	144	168	C11	C11
PC[4]	PCR[36]	AF0 AF1 AF2 AF3 ALT4 — — —	GPIO[36] E1UC[31] — FR_B_TX_EN SIN_1 CAN3RX EIRQ[18]	SIUL eMIOS_1 — Flexray DSPI_1 FlexCAN_3 SIUL	I/O I/O — O I I I	M/ S	Tristate	159	183	A9	A9

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function ⁽¹⁾	Function	Peripheral	I/O direction ⁽²⁾	Pad type	RESET config.	Pin number			
								LQFP 176	LQFP 208	LBGA208	LBGA256
PC[5]	PCR[37]	AF0 AF1 AF2 AF3 ALT4 —	GPIO[37] SOUT_1 CAN3TX — FR_A_TX EIRQ[7]	SIUL DSPI_1 FlexCAN_3 — Flexray SIUL	I/O O O — O I	M/ S	Tristate	158	182	B9	B9
PC[6]	PCR[38]	AF0 AF1 AF2 AF3	GPIO[38] LIN1TX E1UC[28] —	SIUL LINFlexD_1 eMIOS_1 —	I/O O I/O —	S	Tristate	44	52	N3	N3
PC[7]	PCR[39]	AF0 AF1 AF2 AF3 — —	GPIO[39] — E1UC[29] — LIN1RX WKPU[12]	SIUL — eMIOS_1 — LINFlexD_1 WKPU	I/O — I/O — I I	S	Tristate	45	53	N4	N4
PC[8]	PCR[40]	AF0 AF1 AF2 AF3	GPIO[40] LIN2TX E0UC[3] —	SIUL LINFlexD_2 eMIOS_0 —	I/O O I/O —	S	Tristate	175	207	B3	B3
PC[9]	PCR[41]	AF0 AF1 AF2 AF3 — —	GPIO[41] — E0UC[7] — LIN2RX WKPU[13]	SIUL — eMIOS_0 — LINFlexD_2 WKPU	I/O — I/O — I I	S	Tristate	2	2	C3	C3
PC[10]	PCR[42]	AF0 AF1 AF2 AF3	GPIO[42] CAN1TX CAN4TX MA[1]	SIUL FlexCAN_1 FlexCAN_4 ADC_0	I/O O O O	M/ S	Tristate	36	36	L1	L1
PC[11]	PCR[43]	AF0 AF1 AF2 AF3 — — —	GPIO[43] — — MA[2] CAN1RX CAN4RX WKPU[5]	SIUL — — ADC_0 FlexCAN_1 FlexCAN_4 WKPU	I/O — — O I I I	S	Tristate	35	35	K4	K4

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function ⁽¹⁾	Function	Peripheral	I/O direction ⁽²⁾	Pad type	RESET config.	Pin number			
								LQFP 176	LQFP 208	LBGA208	LBGA256
PC[12]	PCR[44]	AF0	GPIO[44]	SIUL	I/O	M/S	Tristate	173	205	B4	B4
		AF1	E0UC[12]	eMIOS_0	I/O						
		AF2	—	—	—						
		AF3	—	—	—						
		ALT4	FR_DBG[0]	Flexray	O						
		—	SIN_2	DSPI_2	I						
		—	EIRQ[19]	SIUL	I						
PC[13]	PCR[45]	AF0	GPIO[45]	SIUL	I/O	M/S	Tristate	174	206	A3	A3
		AF1	E0UC[13]	eMIOS_0	I/O						
		AF2	SOUT_2	DSPI_2	O						
		AF3	—	—	—						
		ALT4	FR_DBG[1]	Flexray	O						
PC[14]	PCR[46]	AF0	GPIO[46]	SIUL	I/O	M/S	Tristate	3	3	B2	B2
		AF1	E0UC[14]	eMIOS_0	I/O						
		AF2	SCK_2	DSPI_2	I/O						
		AF3	—	—	—						
		ALT4	FR_DBG[2]	Flexray	O						
		—	EIRQ[8]	SIUL	I						
PC[15]	PCR[47]	AF0	GPIO[47]	SIUL	I/O	M/S	Tristate	4	4	A1	A1
		AF1	E0UC[15]	eMIOS_0	I/O						
		AF2	CS0_2	DSPI_2	I/O						
		AF3	—	—	—						
		ALT4	FR_DBG[3]	Flexray	O						
PD[0]	PCR[48]	—	EIRQ[20]	SIUL	I	I	Tristate	77	93	R12	R12
		AF0	GPI[48]	SIUL	I						
		AF1	—	—	—						
		AF2	—	—	—						
		AF3	—	—	—						
		—	ADC0_P[4]	ADC_0	I						
		—	ADC1_P[4]	ADC_1	I						
PD[1]	PCR[49]	—	WKPU[27]	WKPU	I	I	Tristate	78	94	T13	T13
		AF0	GPI[49]	SIUL	I						
		AF1	—	—	—						
		AF2	—	—	—						
		AF3	—	—	—						
		—	ADC0_P[5]	ADC_0	I						
		—	ADC1_P[5]	ADC_1	I						
		—	WKPU[28]	WKPU	I						

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function ⁽¹⁾	Function	Peripheral	I/O direction ⁽²⁾	Pad type	RESET config.	Pin number			
								LQFP 176	LQFP 208	LBGA208	LBGA256
PD[2]	PCR[50]	AF0	GPI[50]	SIUL	I	I	Tristate	79	95	N11	N11
		AF1	—	—	—						
		AF2	—	—	—						
		AF3	—	—	—						
		—	ADC0_P[6]	ADC_0	I						
		—	ADC1_P[6]	ADC_1	I						
PD[3]	PCR[51]	AF0	GPI[51]	SIUL	I	I	Tristate	80	96	R13	R13
		AF1	—	—	—						
		AF2	—	—	—						
		AF3	—	—	—						
		—	ADC0_P[7]	ADC_0	I						
		—	ADC1_P[7]	ADC_1	I						
PD[4]	PCR[52]	AF0	GPI[52]	SIUL	I	I	Tristate	81	97	P12	P12
		AF1	—	—	—						
		AF2	—	—	—						
		AF3	—	—	—						
		—	ADC0_P[8]	ADC_0	I						
		—	ADC1_P[8]	ADC_1	I						
PD[5]	PCR[53]	AF0	GPI[53]	SIUL	I	I	Tristate	82	98	T14	T14
		AF1	—	—	—						
		AF2	—	—	—						
		AF3	—	—	—						
		—	ADC0_P[9]	ADC_0	I						
		—	ADC1_P[9]	ADC_1	I						
PD[6]	PCR[54]	AF0	GPI[54]	SIUL	I	I	Tristate	83	99	R14	R14
		AF1	—	—	—						
		AF2	—	—	—						
		AF3	—	—	—						
		—	ADC0_P[10]	ADC_0	I						
		—	ADC1_P[10]	ADC_1	I						
PD[7]	PCR[55]	AF0	GPI[55]	SIUL	I	I	Tristate	84	100	P13	P13
		AF1	—	—	—						
		AF2	—	—	—						
		AF3	—	—	—						
		—	ADC0_P[11]	ADC_0	I						
		—	ADC1_P[11]	ADC_1	I						

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function ⁽¹⁾	Function	Peripheral	I/O direction ⁽²⁾	Pad type	RESET config.	Pin number			
								LQFP 176	LQFP 208	LBGA208	LBGA256
PD[8]	PCR[56]	AF0	GPI[56]	SIUL	I	I	Tristate	87	103	P14	P14
		AF1	—	—	—						
		AF2	—	—	—						
		AF3	—	—	—						
		—	ADC0_P[12]	ADC_0	I						
		—	ADC1_P[12]	ADC_1	I						
PD[9]	PCR[57]	AF0	GPI[57]	SIUL	I	I	Tristate	94	114	N16	N16
		AF1	—	—	—						
		AF2	—	—	—						
		AF3	—	—	—						
		—	ADC0_P[13]	ADC_0	I						
		—	ADC1_P[13]	ADC_1	I						
PD[10]	PCR[58]	AF0	GPI[58]	SIUL	I	I	Tristate	95	115	M14	M14
		AF1	—	—	—						
		AF2	—	—	—						
		AF3	—	—	—						
		—	ADC0_P[14]	ADC_0	I						
		—	ADC1_P[14]	ADC_1	I						
PD[11]	PCR[59]	AF0	GPI[59]	SIUL	I	I	Tristate	96	116	M15	M15
		AF1	—	—	—						
		AF2	—	—	—						
		AF3	—	—	—						
		—	ADC0_P[15]	ADC_0	I						
		—	ADC1_P[15]	ADC_1	I						
PD[12]	PCR[60]	AF0	GPIO[60]	SIUL	I/O	S	Tristate	100	120	L13	L13
		AF1	CS5_0	DSPI_0	O						
		AF2	E0UC[24]	eMIOS_0	I/O						
		AF3	—	—	—						
		—	ADC0_S[4]	ADC_0	I						
PD[13]	PCR[61]	AF0	GPIO[61]	SIUL	I/O	S	Tristate	102	124	K14	K14
		AF1	CS0_1	DSPI_1	I/O						
		AF2	E0UC[25]	eMIOS_0	I/O						
		AF3	—	—	—						
		—	ADC0_S[5]	ADC_0	I						
PD[14]	PCR[62]	AF0	GPIO[62]	SIUL	I/O	S	Tristate	104	126	K13	K13
		AF1	CS1_1	DSPI_1	O						
		AF2	E0UC[26]	eMIOS_0	I/O						
		AF3	—	—	—						
		ALT4	FR_DBG[0]	Flexray	O						
		—	ADC0_S[6]	ADC_0	I						

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function ⁽¹⁾	Function	Peripheral	I/O direction ⁽²⁾	Pad type	RESET config.	Pin number			
								LQFP 176	LQFP 208	LBGA208	LBGA256
PD[15]	PCR[63]	AF0	GPIO[63]	SIUL	I/O	S	Tristate	106	128	J13	J13
		AF1	CS2_1	DSPI_1	O						
		AF2	E0UC[27]	eMIOS_0	I/O						
		AF3	—	—	—						
		ALT4	FR_DBG[1]	Flexray	O						
		—	ADC0_S[7]	ADC_0	I						
PE[0]	PCR[64]	AF0	GPIO[64]	SIUL	I/O	S	Tristate	18	18	G2	G2
		AF1	E0UC[16]	eMIOS_0	I/O						
		AF2	—	—	—						
		AF3	—	—	—						
		—	CAN5RX	FlexCAN_5	I						
		—	WKPU[6]	WKPU	I						
PE[1]	PCR[65]	AF0	GPIO[65]	SIUL	I/O	M/ S	Tristate	20	20	F4	F4
		AF1	E0UC[17]	eMIOS_0	I/O						
		AF2	CAN5TX	FlexCAN_5	O						
		AF3	—	—	—						
		—	—	—	—						
PE[2]	PCR[66]	AF0	GPIO[66]	SIUL	I/O	M/ S	Tristate	156	180	A7	A7
		AF1	E0UC[18]	eMIOS_0	I/O						
		AF2	—	—	—						
		AF3	—	—	—						
		ALT4	FR_A_TX_EN	Flexray	O						
		—	SIN_1	DSPI_1	I						
PE[3]	PCR[67]	—	EIRQ[21]	SIUL	I						
		AF0	GPIO[67]	SIUL	I/O	M/ S	Tristate	157	181	A10	A10
		AF1	E0UC[19]	eMIOS_0	I/O						
		AF2	SOUT_1	DSPI_1	O						
		AF3	—	—	—						
		—	FR_A_RX	Flexray	I						
PE[4]	PCR[68]	—	WKPU[29]	WKPU	I						
		AF0	GPIO[68]	SIUL	I/O	M/ S	Tristate	160	184	A8	A8
		AF1	E0UC[20]	eMIOS_0	I/O						
		AF2	SCK_1	DSPI_1	I/O						
		AF3	—	—	—						
		ALT4	FR_B_TX	Flexray	O						
		—	EIRQ[9]	SIUL	I						

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function ⁽¹⁾	Function	Peripheral	I/O direction ⁽²⁾	Pad type	RESET config.	Pin number			
								LQFP 176	LQFP 208	LBGA208	LBGA256
PE[5]	PCR[69]	AF0	GPIO[69]	SIUL	I/O	M/S	Tristate	161	185	B8	B8
		AF1	E0UC[21]	eMIOS_0	I/O						
		AF2	CS0_1	DSPI_1	I/O						
		AF3	MA[2]	ADC_0	O						
		—	FR_B_RX	Flexray	I						
		—	WKPU[30]	WKPU	I						
PE[6]	PCR[70]	AF0	GPIO[70]	SIUL	I/O	M/S	Tristate	167	191	B6	B6
		AF1	E0UC[22]	eMIOS_0	I/O						
		AF2	CS3_0	DSPI_0	O						
		AF3	MA[1]	ADC_0	O						
		—	EIRQ[22]	SIUL	I						
		—	—	—	—						
PE[7]	PCR[71]	AF0	GPIO[71]	SIUL	I/O	M/S	Tristate	168	192	A5	A5
		AF1	E0UC[23]	eMIOS_0	I/O						
		AF2	CS2_0	DSPI_0	O						
		AF3	MA[0]	ADC_0	O						
		—	EIRQ[23]	SIUL	I						
		—	—	—	—						
PE[8]	PCR[72]	AF0	GPIO[72]	SIUL	I/O	M/S	Tristate	21	21	G1	G1
		AF1	CAN2TX	FlexCAN_2	O						
		AF2	E0UC[22]	eMIOS_0	I/O						
		AF3	CAN3TX	FlexCAN_3	O						
		—	—	—	—						
PE[9]	PCR[73]	AF0	GPIO[73]	SIUL	I/O	S	Tristate	22	22	H1	H1
		AF1	—	—	—						
		AF2	E0UC[23]	eMIOS_0	I/O						
		AF3	—	—	—						
		—	WKPU[7]	WKPU	I						
		—	CAN2RX	FlexCAN_2	I						
		—	CAN3RX	FlexCAN_3	I						
PE[10]	PCR[74]	AF0	GPIO[74]	SIUL	I/O	S	Tristate	23	23	G3	G3
		AF1	LIN3TX	LINFlexD_3	O						
		AF2	CS3_1	DSPI_1	O						
		AF3	E1UC[30]	eMIOS_1	I/O						
		—	EIRQ[10]	SIUL	I						
		—	—	—	—						
PE[11]	PCR[75]	AF0	GPIO[75]	SIUL	I/O	S	Tristate	25	25	H3	H3
		AF1	E0UC[24]	eMIOS_0	I/O						
		AF2	CS4_1	DSPI_1	O						
		AF3	—	—	—						
		—	LIN3RX	LINFlexD_3	I						
		—	WKPU[14]	WKPU	I						

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function ⁽¹⁾	Function	Peripheral	I/O direction ⁽²⁾	Pad type	RESET config.	Pin number			
								LQFP 176	LQFP 208	LBGA208	LBGA256
PE[12]	PCR[76]	AF0	GPIO[76]	SIUL	I/O	M/S	Tristate	133	157	C14	C14
		AF1	—	—	—						
		AF2	E1UC[19]	eMIOS_1	I/O						
		AF3	—	—	—						
		—	CRS	FEC	I						
		—	SIN_2	DSPI_2	I						
		—	EIRQ[11]	SIUL	I						
		—	ADC1_S[7]	ADC_1	I						
PE[13]	PCR[77]	AF0	GPIO[77]	SIUL	I/O	M/S	Tristate	127	151	C16	C16
		AF1	SOUT_2	DSPI_2	O						
		AF2	E1UC[20]	eMIOS_1	I/O						
		AF3	—	—	—						
		—	RXD[3]	FEC	I						
PE[14]	PCR[78]	AF0	GPIO[78]	SIUL	I/O	M/S	Tristate	136	160	A14	A14
		AF1	SCK_2	DSPI_2	I/O						
		AF2	E1UC[21]	eMIOS_1	I/O						
		AF3	—	—	—						
		—	EIRQ[12]	SIUL	I						
PE[15]	PCR[79]	AF0	GPIO[79]	SIUL	I/O	M/S	Tristate	137	161	C12	C12
		AF1	CS0_2	DSPI_2	I/O						
		AF2	E1UC[22]	eMIOS_1	I/O						
		AF3	SCK_6	DSPI_6	I/O						
PF[0]	PCR[80]	AF0	GPIO[80]	SIUL	I/O	S	Tristate	63	79	P7	P7
		AF1	E0UC[10]	eMIOS_0	I/O						
		AF2	CS3_1	DSPI_1	O						
		AF3	—	—	—						
		—	ADC0_S[8]	ADC_0	I						
PF[1]	PCR[81]	AF0	GPIO[81]	SIUL	I/O	S	Tristate	64	80	T6	T6
		AF1	E0UC[11]	eMIOS_0	I/O						
		AF2	CS4_1	DSPI_1	O						
		AF3	—	—	—						
		—	ADC0_S[9]	ADC_0	I						
PF[2]	PCR[82]	AF0	GPIO[82]	SIUL	I/O	S	Tristate	65	81	R6	R6
		AF1	E0UC[12]	eMIOS_0	I/O						
		AF2	CS0_2	DSPI_2	I/O						
		AF3	—	—	—						
		—	ADC0_S[10]	ADC_0	I						

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function ⁽¹⁾	Function	Peripheral	I/O direction ⁽²⁾	Pad type	RESET config.	Pin number			
								LQFP 176	LQFP 208	LBGA208	LBGA256
PF[3]	PCR[83]	AF0	GPIO[83]	SIUL	I/O	S	Tristate	66	82	R7	R7
		AF1	E0UC[13]	eMIOS_0	I/O						
		AF2	CS1_2	DSPI_2	O						
		AF3	—	—	—						
		—	ADC0_S[11]	ADC_0	I						
PF[4]	PCR[84]	AF0	GPIO[84]	SIUL	I/O	S	Tristate	67	83	R8	R8
		AF1	E0UC[14]	eMIOS_0	I/O						
		AF2	CS2_2	DSPI_2	O						
		AF3	—	—	—						
		—	ADC0_S[12]	ADC_0	I						
PF[5]	PCR[85]	AF0	GPIO[85]	SIUL	I/O	S	Tristate	68	84	P8	P8
		AF1	E0UC[22]	eMIOS_0	I/O						
		AF2	CS3_2	DSPI_2	O						
		AF3	—	—	—						
		—	ADC0_S[13]	ADC_0	I						
PF[6]	PCR[86]	AF0	GPIO[86]	SIUL	I/O	S	Tristate	69	85	N8	N8
		AF1	E0UC[23]	eMIOS_0	I/O						
		AF2	CS1_1	DSPI_1	O						
		AF3	—	—	—						
		—	ADC0_S[14]	ADC_0	I						
PF[7]	PCR[87]	AF0	GPIO[87]	SIUL	I/O	S	Tristate	70	86	P9	P9
		AF1	—	—	—						
		AF2	CS2_1	DSPI_1	O						
		AF3	—	—	—						
		—	ADC0_S[15]	ADC_0	I						
PF[8]	PCR[88]	AF0	GPIO[88]	SIUL	I/O	M/ S	Tristate	42	50	N2	N2
		AF1	CAN3TX	FlexCAN_3	O						
		AF2	CS4_0	DSPI_0	O						
		AF3	CAN2TX	FlexCAN_2	O						
PF[9]	PCR[89]	AF0	GPIO[89]	SIUL	I/O	S	Tristate	41	49	M4	M4
		AF1	E1UC[1]	eMIOS_1	I/O						
		AF2	CS5_0	DSPI_0	O						
		AF3	—	—	—						
		—	CAN2RX	FlexCAN_2	I						
		—	CAN3RX	FlexCAN_3	I						
		—	WKPU[22]	WKPU	I						

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function ⁽¹⁾	Function	Peripheral	I/O direction ⁽²⁾	Pad type	RESET config.	Pin number			
								LQFP 176	LQFP 208	LBGA208	LBGA256
PF[10]	PCR[90]	AF0 AF1 AF2 AF3	GPIO[90] CS1_0 LIN4TX E1UC[2]	SIUL DSPI_0 LINFlexD_4 eMIOS_1	I/O O O I/O	M/ S	Tristate	46	54	P2	P2
PF[11]	PCR[91]	AF0 AF1 AF2 AF3 — —	GPIO[91] CS2_0 E1UC[3] — LIN4RX WKPU[15]	SIUL DSPI_0 eMIOS_1 — LINFlexD_4 WKPU	I/O O I/O — I I	S	Tristate	47	55	R1	R1
PF[12]	PCR[92]	AF0 AF1 AF2 AF3	GPIO[92] E1UC[25] LIN5TX —	SIUL eMIOS_1 LINFlexD_5 —	I/O I/O O —	M/ S	Tristate	43	51	P1	P1
PF[13]	PCR[93]	AF0 AF1 AF2 AF3 — —	GPIO[93] E1UC[26] — — LIN5RX WKPU[16]	SIUL eMIOS_1 — — LINFlexD_5 WKPU	I/O I/O — — I I	S	Tristate	49	57	P3	P3
PF[14]	PCR[94]	AF0 AF1 AF2 AF3 ALT4	GPIO[94] CAN4TX E1UC[27] CAN1TX MDIO	SIUL FlexCAN_4 eMIOS_1 FlexCAN_1 FEC	I/O O I/O O I/O	M/ S	Tristate	126	150	D14	D14
PF[15]	PCR[95]	AF0 AF1 AF2 AF3 — — — —	GPIO[95] E1UC[4] — — RX_DV CAN1RX CAN4RX EIRQ[13]	SIUL eMIOS_1 — — FEC FlexCAN_1 FlexCAN_4 SIUL	I/O I/O — — I I I I	M/ S	Tristate	125	149	D15	D15
PG[0]	PCR[96]	AF0 AF1 AF2 AF3 ALT4	GPIO[96] CAN5TX E1UC[23] — MDC	SIUL FlexCAN_5 eMIOS_1 — FEC	I/O O I/O — O	F	Tristate	122	146	E13	E13

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function ⁽¹⁾	Function	Peripheral	I/O direction ⁽²⁾	Pad type	RESET config.	Pin number			
								LQFP 176	LQFP 208	LBGA208	LBGA256
PG[1]	PCR[97]	AF0	GPIO[97]	SIUL	I/O	M	Tristate	121	145	E14	E14
		AF1	—	—	—						
		AF2	E1UC[24]	eMIOS_1	I/O						
		AF3	—	—	—						
		—	TX_CLK	FEC	I						
		—	CAN5RX	FlexCAN_5	I						
		—	EIRQ[14]	SIUL	I						
PG[2]	PCR[98]	AF0	GPIO[98]	SIUL	I/O	M/S	Tristate	16	16	E4	E4
		AF1	E1UC[11]	eMIOS_1	I/O						
		AF2	SOUT_3	DSPI_3	O						
		AF3	—	—	—						
PG[3]	PCR[99]	AF0	GPIO[99]	SIUL	I/O	S	Tristate	15	15	E1	E1
		AF1	E1UC[12]	eMIOS_1	I/O						
		AF2	CS0_3	DSPI_3	I/O						
		AF3	—	—	—						
		—	WKPU[17]	WKPU	I						
PG[4]	PCR[100]	AF0	GPIO[100]	SIUL	I/O	M/S	Tristate	14	14	F2	F2
		AF1	E1UC[13]	eMIOS_1	I/O						
		AF2	SCK_3	DSPI_3	I/O						
		AF3	—	—	—						
PG[5]	PCR[101]	AF0	GPIO[101]	SIUL	I/O	S	Tristate	13	13	D1	D1
		AF1	E1UC[14]	eMIOS_1	I/O						
		AF2	—	—	—						
		AF3	—	—	—						
		—	WKPU[18]	WKPU	I						
		—	SIN_3	DSPI_3	I						
PG[6]	PCR[102]	AF0	GPIO[102]	SIUL	I/O	M/S	Tristate	38	38	M1	M1
		AF1	E1UC[15]	eMIOS_1	I/O						
		AF2	LIN6TX	LINFlexD_6	O						
		AF3	—	—	—						
PG[7]	PCR[103]	AF0	GPIO[103]	SIUL	I/O	S	Tristate	37	37	L2	L2
		AF1	E1UC[16]	eMIOS_1	I/O						
		AF2	E1UC[30]	eMIOS_1	I/O						
		AF3	—	—	—						
		—	LIN6RX	LINFlexD_6	I						
		—	WKPU[20]	WKPU	I						

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function ⁽¹⁾	Function	Peripheral	I/O direction ⁽²⁾	Pad type	RESET config.	Pin number			
								LQFP 176	LQFP 208	LBGA208	LBGA256
PG[8]	PCR[104]	AF0	GPIO[104]	SIUL	I/O	S	Tristate	34	34	K3	K3
		AF1	E1UC[17]	eMIOS_1	I/O						
		AF2	LIN7TX	LINFlexD_7	O						
		AF3	CS0_2	DSPI_2	I/O						
		—	EIRQ[15]	SIUL	I						
PG[9]	PCR[105]	AF0	GPIO[105]	SIUL	I/O	S	Tristate	33	33	J4	J4
		AF1	E1UC[18]	eMIOS_1	I/O						
		AF2	—	—	—						
		AF3	SCK_2	DSPI_2	I/O						
		—	LIN7RX	LINFlexD_7	I						
PG[10]	PCR[106]	—	WKPU[21]	WKPU	I						
		AF0	GPIO[106]	SIUL	I/O	S	Tristate	138	162	B13	B13
		AF1	E0UC[24]	eMIOS_0	I/O						
		AF2	E1UC[31]	eMIOS_1	I/O						
		AF3	—	—	—						
		—	SIN_4	DSPI_4	I						
PG[11]	PCR[107]	AF0	GPIO[107]	SIUL	I/O	M/ S	Tristate	139	163	A16	A16
		AF1	E0UC[25]	eMIOS_0	I/O						
		AF2	CS0_4	DSPI_4	I/O						
		AF3	CS0_6	DSPI_6	I/O						
PG[12]	PCR[108]	AF0	GPIO[108]	SIUL	I/O	M/ S	Tristate	116	140	F15	F15
		AF1	E0UC[26]	eMIOS_0	I/O						
		AF2	SOUT_4	DSPI_4	O						
		AF3	—	—	—						
		ALT4	TXD[2]	FEC	O						
PG[13]	PCR[109]	AF0	GPIO[109]	SIUL	I/O	M/ S	Tristate	115	139	F16	F16
		AF1	E0UC[27]	eMIOS_0	I/O						
		AF2	SCK_4	DSPI_4	I/O						
		AF3	—	—	—						
		ALT4	TXD[3]	FEC	O						
PG[14]	PCR[110]	AF0	GPIO[110]	SIUL	I/O	S	Tristate	134	158	C13	C13
		AF1	E1UC[0]	eMIOS_1	I/O						
		AF2	LIN8TX	LINFlexD_8	O						
		AF3	—	—	—						
		—	SIN_6	DSPI_6	I						

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function ⁽¹⁾	Function	Peripheral	I/O direction ⁽²⁾	Pad type	RESET config.	Pin number			
								LQFP 176	LQFP 208	LBGA208	LBGA256
PG[15]	PCR[111]	AF0	GPIO[111]	SIUL	I/O	M/S	Tristate	135	159	D13	D13
		AF1	E1UC[1]	eMIOS_1	I/O						
		AF2	SOUT_6	DSPI_6	O						
		AF3	—	—	—						
		—	LIN8RX	LINFlexD_8	I						
PH[0]	PCR[112]	AF0	GPIO[112]	SIUL	I/O	M/S	Tristate	117	141	E15	E15
		AF1	E1UC[2]	eMIOS_1	I/O						
		AF2	—	—	—						
		AF3	—	—	—						
		ALT4	TXD[1]	FEC	O						
PH[1]	PCR[113]	—	SIN_1	DSPI_1	I						
		AF0	GPIO[113]	SIUL	I/O	M/S	Tristate	118	142	F13	F13
		AF1	E1UC[3]	eMIOS_1	I/O						
		AF2	SOUT_1	DSPI_1	O						
		AF3	—	—	—						
		ALT4	TXD[0]	FEC	O						
PH[2]	PCR[114]	AF0	GPIO[114]	SIUL	I/O	M/S	Tristate	119	143	D16	D16
		AF1	E1UC[4]	eMIOS_1	I/O						
		AF2	SCK_1	DSPI_1	I/O						
		AF3	—	—	—						
		ALT4	TX_EN	FEC	O						
PH[3]	PCR[115]	AF0	GPIO[115]	SIUL	I/O	M/S	Tristate	120	144	F14	F14
		AF1	E1UC[5]	eMIOS_1	I/O						
		AF2	CS0_1	DSPI_1	I/O						
		AF3	—	—	—						
		ALT4	TX_ER	FEC	O						
PH[4]	PCR[116]	AF0	GPIO[116]	SIUL	I/O	M/S	Tristate	162	186	D7	D7
		AF1	E1UC[6]	eMIOS_1	I/O						
		AF2	SOUT_7	DSPI_7	O						
		AF3	—	—	—						
PH[5]	PCR[117]	AF0	GPIO[117]	SIUL	I/O	S	Tristate	163	187	B7	B7
		AF1	E1UC[7]	eMIOS_1	I/O						
		AF2	—	—	—						
		AF3	—	—	—						
		—	SIN_7	DSPI_7	I						
PH[6]	PCR[118]	AF0	GPIO[118]	SIUL	I/O	M/S	Tristate	164	188	C7	C7
		AF1	E1UC[8]	eMIOS_1	I/O						
		AF2	SCK_7	DSPI_7	I/O						
		AF3	MA[2]	ADC_0	O						

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function ⁽¹⁾	Function	Peripheral	I/O direction ⁽²⁾	Pad type	RESET config.	Pin number			
								LQFP 176	LQFP 208	LBGA208	LBGA256
PH[7]	PCR[119]	AF0	GPIO[119]	SIUL	I/O	M/S	Tristate	165	189	C6	C6
		AF1	E1UC[9]	eMIOS_1	I/O						
		AF2	CS3_2	DSPI_2	O						
		AF3	MA[1]	ADC_0	O						
		ALT4	CS0_7	DSPI_7	I/O						
PH[8]	PCR[120]	AF0	GPIO[120]	SIUL	I/O	M/S	Tristate	166	190	A6	A6
		AF1	E1UC[10]	eMIOS_1	I/O						
		AF2	CS2_2	DSPI_2	O						
		AF3	MA[0]	ADC_0	O						
PH[9] ⁽⁶⁾	PCR[121]	AF0	GPIO[121]	SIUL	I/O	S	Input, weak pull-up	155	179	A11	A11
		AF1	—	—	—						
		AF2	—	—	—						
		AF3	—	—	—						
		—	TCK	JTAGC	I						
PH[10] ⁽⁶⁾	PCR[122]	AF0	GPIO[122]	SIUL	I/O	M/S	Input, weak pull-up	148	172	D10	D10
		AF1	—	—	—						
		AF2	—	—	—						
		AF3	—	—	—						
		—	TMS	JTAGC	I						
PH[11]	PCR[123]	AF0	GPIO[123]	SIUL	I/O	M/S	Tristate	140	164	A13	A13
		AF1	SOUT_3	DSPI_3	O						
		AF2	CS0_4	DSPI_4	I/O						
		AF3	E1UC[5]	eMIOS_1	I/O						
PH[12]	PCR[124]	AF0	GPIO[124]	SIUL	I/O	M/S	Tristate	141	165	B12	B12
		AF1	SCK_3	DSPI_3	I/O						
		AF2	CS1_4	DSPI_4	O						
		AF3	E1UC[25]	eMIOS_1	I/O						
PH[13]	PCR[125]	AF0	GPIO[125]	SIUL	I/O	M/S	Tristate	9	9	B1	B1
		AF1	SOUT_4	DSPI_4	O						
		AF2	CS0_3	DSPI_3	I/O						
		AF3	E1UC[26]	eMIOS_1	I/O						
PH[14]	PCR[126]	AF0	GPIO[126]	SIUL	I/O	M/S	Tristate	10	10	C1	C1
		AF1	SCK_4	DSPI_4	I/O						
		AF2	CS1_3	DSPI_3	O						
		AF3	E1UC[27]	eMIOS_1	I/O						
PH[15]	PCR[127]	AF0	GPIO[127]	SIUL	I/O	M/S	Tristate	8	8	E3	E3
		AF1	SOUT_5	DSPI_5	O						
		AF2	—	—	—						
		AF3	E1UC[17]	eMIOS_1	I/O						

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function ⁽¹⁾	Function	Peripheral	I/O direction ⁽²⁾	Pad type	RESET config.	Pin number			
								LQFP 176	LQFP 208	LBGA208	LBGA256
PI[0]	PCR[128]	AF0 AF1 AF2 AF3	GPIO[128] E0UC[28] LIN8TX —	SIUL eMIOS_0 LINFlexD_8 —	I/O I/O O —	S	Tristate	172	196	C5	C5
PI[1]	PCR[129]	AF0 AF1 AF2 AF3 — —	GPIO[129] E0UC[29] — — WKPU[24] LIN8RX	SIUL eMIOS_0 — — WKPU LINFlexD_8	I/O I/O — — I I	S	Tristate	171	195	A4	A4
PI[2]	PCR[130]	AF0 AF1 AF2 AF3	GPIO[130] E0UC[30] LIN9TX —	SIUL eMIOS_0 LINFlexD_9 —	I/O I/O O —	S	Tristate	170	194	D6	D6
PI[3]	PCR[131]	AF0 AF1 AF2 AF3 — —	GPIO[131] E0UC[31] — — WKPU[23] LIN9RX	SIUL eMIOS_0 — — WKPU LINFlexD_9	I/O I/O — — I I	S	Tristate	169	193	B5	B5
PI[4]	PCR[132]	AF0 AF1 AF2 AF3	GPIO[132] E1UC[28] SOUT_4 —	SIUL eMIOS_1 DSPI_4 —	I/O I/O O —	M/ S	Tristate	143	167	A12	A12
PI[5]	PCR[133]	AF0 AF1 AF2 AF3 ALT4	GPIO[133] E1UC[29] SCK_4 CS2_5 CS2_6	SIUL eMIOS_1 DSPI_4 DSPI_5 DSPI_6	I/O I/O I/O O O	M/ S	Tristate	142	166	D12	D12
PI[6]	PCR[134]	AF0 AF1 AF2 AF3 ALT4	GPIO[134] E1UC[30] CS0_4 CS0_5 CS0_6	SIUL eMIOS_1 DSPI_4 DSPI_5 DSPI_6	I/O I/O I/O I/O I/O	S	Tristate	11	11	D2	D2
PI[7]	PCR[135]	AF0 AF1 AF2 AF3 ALT4	GPIO[135] E1UC[31] CS1_4 CS1_5 CS1_6	SIUL eMIOS_1 DSPI_4 DSPI_5 DSPI_6	I/O I/O O O O	S	Tristate	12	12	E2	E2

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function ⁽¹⁾	Function	Peripheral	I/O direction ⁽²⁾	Pad type	RESET config.	Pin number			
								LQFP 176	LQFP 208	LBGA208	LBGA256
PI[8]	PCR[136]	AF0	GPIO[136]	SIUL	I/O	S	Tristate	108	130	J14	J14
		AF1	—	—	—						
		AF2	—	—	—						
		AF3	—	—	—						
		—	ADC0_S[16]	ADC_0	I						
PI[9]	PCR[137]	AF0	GPIO[137]	SIUL	I/O	S	Tristate	—	131	J15	J15
		AF1	—	—	—						
		AF2	—	—	—						
		AF3	—	—	—						
		—	ADC0_S[17]	ADC_0	I						
PI[10]	PCR[138]	AF0	GPIO[138]	SIUL	I/O	S	Tristate	—	134	J16	J16
		AF1	—	—	—						
		AF2	—	—	—						
		AF3	—	—	—						
		—	ADC0_S[18]	ADC_0	I						
PI[11]	PCR[139]	AF0	GPIO[139]	SIUL	I/O	S	Tristate	111	135	H16	H16
		AF1	—	—	—						
		AF2	—	—	—						
		AF3	—	—	—						
		—	ADC0_S[19]	ADC_0	I						
PI[12]	PCR[140]	—	SIN_3	DSPI_3	I						
		AF0	GPIO[140]	SIUL	I/O	S	Tristate	112	136	G15	G15
		AF1	CS0_3	DSPI_3	I/O						
		AF2	CS0_2	DSPI_2	I/O						
		AF3	—	—	—						
		—	ADC0_S[20]	ADC_0	I						
PI[13]	PCR[141]	AF0	GPIO[141]	SIUL	I/O	S	Tristate	113	137	G14	G14
		AF1	CS1_3	DSPI_3	O						
		AF2	CS1_2	DSPI_2	O						
		AF3	—	—	—						
		—	ADC0_S[21]	ADC_0	I						
PI[14]	PCR[142]	AF0	GPIO[142]	SIUL	I/O	S	Tristate	76	92	T12	T12
		AF1	—	—	—						
		AF2	—	—	—						
		AF3	—	—	—						
		—	ADC0_S[22]	ADC_0	I						
		—	SIN_4	DSPI_4	I						

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function ⁽¹⁾	Function	Peripheral	I/O direction ⁽²⁾	Pad type	RESET config.	Pin number			
								LQFP 176	LQFP 208	LBGA208	LBGA256
PI[15]	PCR[143]	AF0	GPIO[143]	SIUL	I/O	S	Tristate	75	91	P11	P11
		AF1	CS0_4	DSPI_4	I/O						
		AF2	CS2_2	DSPI_2	O						
		AF3	—	—	—						
		—	ADC0_S[23]	ADC_0	I						
PJ[0]	PCR[144]	AF0	GPIO[144]	SIUL	I/O	S	Tristate	74	90	R11	R11
		AF1	CS1_4	DSPI_4	O						
		AF2	CS3_2	DSPI_2	O						
		AF3	—	—	—						
		—	ADC0_S[24]	ADC_0	I						
PJ[1]	PCR[145]	AF0	GPIO[145]	SIUL	I/O	S	Tristate	73	89	N10	N10
		AF1	—	—	—						
		AF2	—	—	—						
		AF3	—	—	—						
		—	ADC0_S[25]	ADC_0	I						
		—	SIN_5	DSPI_5	I						
PJ[2]	PCR[146]	AF0	GPIO[146]	SIUL	I/O	S	Tristate	72	88	R10	R10
		AF1	CS0_5	DSPI_5	I/O						
		AF2	CS0_6	DSPI_6	I/O						
		AF3	CS0_7	DSPI_7	I/O						
		—	ADC0_S[26]	ADC_0	I						
PJ[3]	PCR[147]	AF0	GPIO[147]	SIUL	I/O	S	Tristate	71	87	P10	P10
		AF1	CS1_5	DSPI_5	O						
		AF2	CS1_6	DSPI_6	O						
		AF3	CS1_7	DSPI_7	O						
		—	ADC0_S[27]	ADC_0	I						
PJ[4]	PCR[148]	AF0	GPIO[148]	SIUL	I/O	M/ S	Tristate	5	5	D3	D3
		AF1	SCK_5	DSPI_5	I/O						
		AF2	E1UC[18]	eMIOS_1	I/O						
		AF3	—	—	—						
PJ[5]	PCR[149]	AF0	GPIO[149]	SIUL	I/O	S	Tristate	—	113	N12	N12
		AF1	—	—	—						
		AF2	—	—	—						
		AF3	—	—	—						
		—	ADC0_S[28]	ADC_0	I						

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function ⁽¹⁾	Function	Peripheral	I/O direction ⁽²⁾	Pad type	RESET config.	Pin number			
								LQFP 176	LQFP 208	LBGA208	LBGA256
PJ[6]	PCR[150]	AF0	GPIO[150]	SIUL	I/O	S	Tristate	—	112	N15	N15
		AF1	—	—	—						
		AF2	—	—	—						
		AF3	—	—	—						
		—	ADC0_S[29]	ADC_0	I						
PJ[7]	PCR[151]	AF0	GPIO[151]	SIUL	I/O	S	Tristate	—	111	P16	P16
		AF1	—	—	—						
		AF2	—	—	—						
		AF3	—	—	—						
		—	ADC0_S[30]	ADC_0	I						
PJ[8]	PCR[152]	AF0	GPIO[152]	SIUL	I/O	S	Tristate	—	110	P15	P15
		AF1	—	—	—						
		AF2	—	—	—						
		AF3	—	—	—						
		—	ADC0_S[31]	ADC_0	I						
PJ[9]	PCR[153]	AF0	GPIO[153]	SIUL	I/O	S	Tristate	—	68	P5	P5
		AF1	—	—	—						
		AF2	—	—	—						
		AF3	—	—	—						
		—	ADC1_S[8]	ADC_1	I						
PJ[10]	PCR[154]	AF0	GPIO[154]	SIUL	I/O	S	Tristate	—	67	T5	T5
		AF1	—	—	—						
		AF2	—	—	—						
		AF3	—	—	—						
		—	ADC1_S[9]	ADC_1	I						
PJ[11]	PCR[155]	AF0	GPIO[155]	SIUL	I/O	S	Tristate	—	60	R3	R3
		AF1	—	—	—						
		AF2	—	—	—						
		AF3	—	—	—						
		—	ADC1_S[10]	ADC_1	I						
PJ[12]	PCR[156]	AF0	GPIO[156]	SIUL	I/O	S	Tristate	—	59	T1	T1
		AF1	—	—	—						
		AF2	—	—	—						
		AF3	—	—	—						
		—	ADC1_S[11]	ADC_1	I						

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function ⁽¹⁾	Function	Peripheral	I/O direction ⁽²⁾	Pad type	RESET config.	Pin number			
								LQFP 176	LQFP 208	LBGA208	LBGA256
PJ[13]	PCR[157]	AF0	GPIO[157]	SIUL	I/O	S	Tristate	—	65	N5	N5
		AF1	—	—	—						
		AF2	CS1_7	DSPI_7	O						
		AF3	—	—	—						
		—	CAN4RX	FlexCAN_4	I						
		—	ADC1_S[12]	ADC_1	I						
		—	CAN1RX	FlexCAN_1	I						
PJ[14]	PCR[158]	—	WKPU[31]	WKPU	I	M/S	Tristate	—	64	T4	T4
		AF0	GPIO[158]	SIUL	I/O						
		AF1	CAN1TX	FlexCAN_1	O						
		AF2	CAN4TX	FlexCAN_4	O						
PJ[15]	PCR[159]	AF3	CS2_7	DSPI_7	O	M/S	Tristate	—	63	R4	R4
		AF0	GPIO[159]	SIUL	I/O						
		AF1	—	—	—						
		AF2	CS1_6	DSPI_6	O						
		—	—	—	—						
PK[0]	PCR[160]	—	CAN1RX	FlexCAN_1	I	M/S	Tristate	—	62	T3	T3
		AF0	GPIO[160]	SIUL	I/O						
		AF1	CAN1TX	FlexCAN_1	O						
		AF2	CS2_6	DSPI_6	O						
PK[1]	PCR[161]	AF3	—	—	—	M/S	Tristate	—	41	H4	H4
		AF0	GPIO[161]	SIUL	I/O						
		AF1	CS3_6	DSPI_6	O						
		AF2	—	—	—						
		—	—	—	—						
PK[2]	PCR[162]	—	CAN4RX	FlexCAN_4	I	M/S	Tristate	—	42	L4	L4
		AF0	GPIO[162]	SIUL	I/O						
		AF1	CAN4TX	FlexCAN_4	O						
		AF2	—	—	—						
PK[3]	PCR[163]	AF3	—	—	—	M/S	Tristate	—	43	N1	N1
		AF0	GPIO[163]	SIUL	I/O						
		AF1	E1UC[0]	eMIOS_1	I/O						
		AF2	—	—	—						
		—	—	—	—						
		—	CAN5RX	FlexCAN_5	I						
		—	LIN8RX	LINFlexD_8	I						

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function ⁽¹⁾	Function	Peripheral	I/O direction ⁽²⁾	Pad type	RESET config.	Pin number			
								LQFP 176	LQFP 208	LPGA208	LPGA256
PK[4]	PCR[164]	AF0	GPIO[164]	SIUL	I/O	M/ S	Tristate	—	44	M3	M3
		AF1	LIN8TX	LINFlexD_8	O						
		AF2	CAN5TX	FlexCAN_5	O						
		AF3	E1UC[1]	eMIOS_1	I/O						
PK[5]	PCR[165]	AF0	GPIO[165]	SIUL	I/O	M/ S	Tristate	—	45	—	M5
		AF1	—	—	—						
		AF2	—	—	—						
		AF3	—	—	—						
		—	CAN2RX	FlexCAN_2	I						
		—	LIN2RX	LINFlexD_2	I						
PK[6]	PCR[166]	AF0	GPIO[166]	SIUL	I/O	M/ S	Tristate	—	46	—	M6
		AF1	CAN2TX	FlexCAN_2	O						
		AF2	LIN2TX	LINFlexD_2	O						
		AF3	—	—	—						
PK[7]	PCR[167]	AF0	GPIO[167]	SIUL	I/O	M/ S	Tristate	—	47	—	M7
		AF1	—	—	—						
		AF2	—	—	—						
		AF3	—	—	—						
		—	CAN3RX	FlexCAN_3	I						
		—	LIN3RX	LINFlexD_3	I						
PK[8]	PCR[168]	AF0	GPIO[168]	SIUL	I/O	M/ S	Tristate	—	48	—	M8
		AF1	CAN3TX	FlexCAN_3	O						
		AF2	LIN3TX	LINFlexD_3	O						
		AF3	—	—	—						
PK[9]	PCR[169]	AF0	GPIO[169]	SIUL	I/O	M/ S	Tristate	—	197	—	E8
		AF1	—	—	—						
		AF2	—	—	—						
		AF3	—	—	—						
		—	SIN_4	DSPI_4	I						
PK[10]	PCR[170]	AF0	GPIO[170]	SIUL	I/O	M/ S	Tristate	—	198	—	E7
		AF1	SOUT_4	DSPI_4	O						
		AF2	—	—	—						
		AF3	—	—	—						
PK[11]	PCR[171]	AF0	GPIO[171]	SIUL	I/O	M/ S	Tristate	—	199	—	F8
		AF1	SCK_4	DSPI_4	I/O						
		AF2	—	—	—						
		AF3	—	—	—						

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function ⁽¹⁾	Function	Peripheral	I/O direction ⁽²⁾	Pad type	RESET config.	Pin number			
								LQFP 176	LQFP 208	LBGA208	LBGA256
PK[12]	PCR[172]	AF0 AF1 AF2 AF3	GPIO[172] CS0_4 — —	SIUL DSPI_4 — —	I/O I/O — —	M/ S	Tristate	—	200	—	G12
PK[13]	PCR[173]	AF0 AF1 AF2 AF3 —	GPIO[173] CS3_6 CS2_7 SCK_1 CAN3RX	SIUL DSPI_6 DSPI_7 DSPI_1 FlexCAN_3	I/O O O I/O I	M/ S	Tristate	—	201	—	H12
PK[14]	PCR[174]	AF0 AF1 AF2 AF3	GPIO[174] CAN3TX CS3_7 CS0_1	SIUL FlexCAN_3 DSPI_7 DSPI_1	I/O O O I/O	M/ S	Tristate	—	202	—	J12
PK[15]	PCR[175]	AF0 AF1 AF2 AF3 — —	GPIO[175] — — — SIN_1 SIN_7	SIUL — — — DSPI_1 DSPI_7	I/O — — — I I	M/ S	Tristate	—	203	D5	D5
PL[0]	PCR[176]	AF0 AF1 AF2 AF3	GPIO[176] SOUT_1 SOUT_7 —	SIUL DSPI_1 DSPI_7 —	I/O O O —	M/ S	Tristate	—	204	C4	C4
PL[1]	PCR[177]	AF0 AF1 AF2 AF3	GPIO[177] — — —	SIUL — — —	I/O — — —	M/ S	Tristate	—	—	—	F7
PL[2]	PCR[178] (7)	AF0 AF1 AF2 AF3	GPIO[178] — MDO0 ⁽⁸⁾ —	SIUL — Nexus —	I/O — O —	M/ S	Tristate	—	—	—	F5
PL[3]	PCR[179]	AF0 AF1 AF2 AF3	GPIO[179] — MDO1 —	SIUL — Nexus —	I/O — O —	M/ S	Tristate	—	—	—	G5
PL[4]	PCR[180]	AF0 AF1 AF2 AF3	GPIO[180] — MDO2 —	SIUL — Nexus —	I/O — O —	M/ S	Tristate	—	—	—	H5

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function ⁽¹⁾	Function	Peripheral	I/O direction ⁽²⁾	Pad type	RESET config.	Pin number			
								LQFP 176	LQFP 208	LBGA208	LBGA256
PL[5]	PCR[181]	AF0 AF1 AF2 AF3	GPIO[181] — MDO3 —	SIUL — Nexus —	I/O — O —	M/ S	Tristate	—	—	—	J5
PL[6]	PCR[182]	AF0 AF1 AF2 AF3	GPIO[182] — MDO4 —	SIUL — Nexus —	I/O — O —	M/ S	Tristate	—	—	—	K5
PL[7]	PCR[183]	AF0 AF1 AF2 AF3	GPIO[183] — MDO5 —	SIUL — Nexus —	I/O — O —	M/ S	Tristate	—	—	—	L5
PL[8]	PCR[184]	AF0 AF1 AF2 AF3 —	GPIO[184] — — — EVTI	SIUL — — — Nexus	I/O — — — I	S	Pull-up	—	—	—	M9
PL[9]	PCR[185]	AF0 AF1 AF2 AF3	GPIO[185] — MSEO —	SIUL — Nexus —	I/O — O —	M/ S	Tristate	—	—	—	M10
PL[10]	PCR[186]	AF0 AF1 AF2 AF3	GPIO[186] — MCKO —	SIUL — Nexus —	I/O — O —	F/S	Tristate	—	—	—	M11
PL[11]	PCR[187]	AF0 AF1 AF2 AF3	GPIO[187] — — —	SIUL — — —	I/O — — —	M/ S	Tristate	—	—	—	M12
PL[12]	PCR[188]	AF0 AF1 AF2 AF3	GPIO[188] — EVTO —	SIUL — Nexus —	I/O — O —	M/ S	Tristate	—	—	—	F11
PL[13]	PCR[189]	AF0 AF1 AF2 AF3	GPIO[189] — MDO6 —	SIUL — Nexus —	I/O — O —	M/ S	Tristate	—	—	—	F10

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function ⁽¹⁾	Function	Peripheral	I/O direction ⁽²⁾	Pad type	RESET config.	Pin number			
								LQFP 176	LQFP 208	LBGA208	LBGA256
PL[14]	PCR[190]	AF0	GPIO[190]	SIUL	I/O	M/S	Tristate	—	—	—	E12
		AF1	—	—	—						
		AF2	MDO7	Nexus	O						
		AF3	—	—	—						
PL[15]	PCR[191]	AF0	GPIO[191]	SIUL	I/O	M/S	Tristate	—	—	—	E11
		AF1	—	—	—						
		AF2	MDO8	Nexus	O						
		AF3	—	—	—						
PM[0]	PCR[192]	AF0	GPIO[192]	SIUL	I/O	M/S	Tristate	—	—	—	E10
		AF1	—	—	—						
		AF2	MDO9	Nexus	O						
		AF3	—	—	—						
PM[1]	PCR[193]	AF0	GPIO[193]	SIUL	I/O	M/S	Tristate	—	—	—	E9
		AF1	—	—	—						
		AF2	MDO10	Nexus	O						
		AF3	—	—	—						
PM[2]	PCR[194]	AF0	GPIO[194]	SIUL	I/O	M/S	Tristate	—	—	—	F12
		AF1	—	—	—						
		AF2	MDO11	Nexus	O						
		AF3	—	—	—						
PM[3]	PCR[195]	AF0	GPIO[195]	SIUL	I/O	M/S	Tristate	—	—	—	K12
		AF1	—	—	—						
		AF2	—	—	—						
		AF3	—	—	—						
PM[4]	PCR[196]	AF0	GPIO[196]	SIUL	I/O	M/S	Tristate	—	—	—	L12
		AF1	—	—	—						
		AF2	—	—	—						
		AF3	—	—	—						
PM[5]	PCR[197]	AF0	GPIO[197]	SIUL	I/O	M/S	Tristate	—	—	—	F9
		AF1	—	—	—						
		AF2	—	—	—						
		AF3	—	—	—						
PM[6]	PCR[198]	AF0	GPIO[198]	SIUL	I/O	M/S	Tristate	—	—	—	F6
		AF1	—	—	—						
		AF2	—	—	—						
		AF3	—	—	—						

1. Alternate functions are chosen by setting the values of the PCR.PA bitfields inside the SIUL module. PCR.PA = 000 → AF0; PCR.PA = 001 → AF1; PCR.PA = 010 → AF2; PCR.PA = 011 → AF3; PCR.PA = 100 → ALT4. This is intended to select the output functions; to use one of the input functions, the PCR.IBE bit must be written to '1', regardless of the values selected in the PCR.PA bitfields. For this reason, the value corresponding to an input only function is reported as "—".

2. Multiple inputs are routed to all respective modules internally. The input of some modules must be configured by setting the values of the PSMIO.PADSELx bitfields inside the SIUL module.
3. NMI[0] and NMI[1] have a higher priority than alternate functions. When NMI is selected, the PCR.PA field is ignored.
4. SXOSC's OSC32k_XTAL and OSC32k_EXTAL pins are shared with GPIO functionality. When used as crystal pins, other functionality of the pin cannot be used and it should be ensured that application never programs OBE and PUE bit of the corresponding PCR to "1".
5. If you want to use OSC32K functionality through PB[8] and PB[9], you must ensure that PB[10] is static in nature as PB[10] can induce coupling on PB[9] and disturb oscillator frequency.
6. Out of reset all the functional pins except PC[0:1] and PH[9:10] are available to the user as GPIO.
PC[0:1] are available as JTAG pins (TDI and TDO respectively).
PH[9:10] are available as JTAG pins (TCK and TMS respectively).
It is up to the user to configure these pins as GPIO when needed.
7. When MBIST is enabled to run (STCU Enable = 1), the application must not drive or tie PAD[178] (MDO[0]) to 0 V before the device exits reset (external reset is removed) as the pad is internally driven to 1 to indicate MBIST operation. When MBIST is not enabled (STCU Enable = 0), there are no restriction as the device does not internally drive the pad.
8. These pins can be configured as Nexus pins during reset by the debugger writing to the Nexus Development Interface "Port Control Register" rather than the SIUL. Specifically, the debugger can enable the MDO[7:0], MSEO, and MCKO ports by programming NDI (PCR[MCKO_EN] or PCR[PSTAT_EN]). MDO[8:11] ports can be enabled by programming NDI ((PCR[MCKO_EN] and PCR[FPM]) or PCR[PSTAT_EN]).

3 Electrical Characteristics

This section contains electrical characteristics of the device as well as temperature and power considerations.

This product contains devices to protect the inputs against damage due to high static voltages. However, it is advisable to take precautions to avoid application of any voltage higher than the specified maximum rated voltages.

To enhance reliability, unused inputs can be driven to an appropriate logic voltage level (V_{DD} or V_{SS_HV}). This could be done by the internal pull-up and pull-down, which is provided by the product for most general purpose pins.

The parameters listed in the following tables represent the characteristics of the device and its demands on the system.

In the tables where the device logic provides signals with their respective timing characteristics, the symbol "CC" for Controller Characteristics is included in the Symbol column.

In the tables where the external system must provide signals with their respective timing characteristics to the device, the symbol "SR" for System Requirement is included in the Symbol column.

3.1 Parameter classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the classifications listed in [Table 6](#) are used and the parameters are tagged accordingly in the tables where appropriate.

Table 6. Parameter classifications

Classification tag	Tag description
P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

Note: The classification is shown in the column labeled "C" in the parameter tables where appropriate.

3.2 NVUSRO register

Portions of the device configuration, such as high voltage supply is controlled via bit values in the Non-Volatile User Options Register (NVUSRO). For a detailed description of the NVUSRO register, see SPC564Bxx and SPC56ECxx Reference Manual.

3.2.1 NVUSRO [PAD3V5V(0)] field description

[Table 7](#) shows how NVUSRO [PAD3V5V(0)] controls the device configuration for $V_{DD_HV_A}$ domain.

Table 7. PAD3V5V(0) field description

Value ⁽¹⁾	Description
0	High voltage supply is 5.0 V
1	High voltage supply is 3.3 V

1. '1' is delivery value. It is part of shadow flash memory, thus programmable by customer.

The DC electrical characteristics are dependent on the PAD3V5V(0,1) bit value.

3.2.2 NVUSRO [PAD3V5V(1)] field description

[Table 8](#) shows how NVUSRO [PAD3V5V(1)] controls the device configuration the device configuration for $V_{DD_HV_B}$ domain.

Table 8. PAD3V5V(1) field description

Value ⁽¹⁾	Description
0	High voltage supply is 5.0 V
1	High voltage supply is 3.3 V

1. '1' is delivery value. It is part of shadow flash memory, thus programmable by customer.

The DC electrical characteristics are dependent on the PAD3V5V(0,1) bit value.

3.3 Absolute maximum ratings

Table 9. Absolute maximum ratings

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
V_{SS_HV}	S R	Digital ground on VSS_HV pins	—	0	0	V
$V_{DD_HV_A}$	S R	Voltage on VDD_HV_A pins with respect to ground (V_{SS_HV})	—	-0.3	6.0	V
$V_{DD_HV_B}^{(1)}$	S R	Voltage on VDD_HV_B pins with respect to common ground (V_{SS_HV})	—	-0.3	6.0	V
V_{SS_LV}	S R	Voltage on VSS_LV (low voltage digital supply) pins with respect to ground (V_{SS_HV})	—	$V_{SS_HV} - 0.1$	$V_{SS_HV} + 0.1$	V

Table 9. Absolute maximum ratings (continued)

Symbol	Parameter	Conditions	Value		Unit
			Min	Max	
$V_{RC_CTRL}^{(2)}$		Base control voltage for external BCP68 NPN device Relative to V_{DD_LV}	0	$V_{DD_LV} + 1$	V
V_{SS_ADC}	S R	Voltage on $V_{SS_HV_ADC0}$, $V_{SS_HV_ADC1}$ (ADC reference) pin with respect to ground (V_{SS_HV})	—	$V_{SS_HV} - 0.1$ $V_{SS_HV} + 0.1$	V
$V_{DD_HV_ADC0}$	S R	Voltage on $V_{DD_HV_ADC0}$ with respect to ground (V_{SS_HV})	—	-0.3 6.0	V
		Relative to $V_{DD_HV_A}^{(3)}$	$V_{DD_HV_A} - 0.3$	$V_{DD_HV_A} + 0.3$	
$V_{DD_HV_ADC1}^{(4)}$	S R	Voltage on $V_{DD_HV_ADC1}$ with respect to ground (V_{SS_HV})	—	-0.3 6.0	V
		Relative to $V_{DD_HV_A}^{(2)}$	$V_{DD_HV_A} - 0.3$	$V_{DD_HV_A} + 0.3$	
V_{IN}	S R	Voltage on any GPIO pin with respect to ground (V_{SS_HV})	Relative to $V_{DD_HV_A/HV_B}$	$V_{DD_HV_A/HV_B} - 0.3$ $V_{DD_HV_A/HV_B} + 0.3$	V
I_{INJPAD}	S R	Injected input current on any pin during overload condition	—	-10 10	mA
I_{INJSUM}	S R	Absolute sum of all injected input currents during overload condition	—	-50 50	
$I_{AVGSEG}^{(5)}$	S R	Sum of all the static I/O current within a supply segment ($V_{DD_HV_A}$ or $V_{DD_HV_B}$)	$V_{DD} = 5.0\text{ V} \pm 10\%$, PAD3V5V = 0	70	mA
			$V_{DD} = 3.3\text{ V} \pm 10\%$, PAD3V5V = 1	64	
$T_{STORAGE}$	S R	Storage temperature	—	-55 ⁽⁶⁾ 150	°C

1. $V_{DD_HV_B}$ can be independently controlled from $V_{DD_HV_A}$. These can ramp up or ramp down in any order. Design is robust against any supply order.
2. This voltage is internally generated by the device and no external voltage should be supplied.
3. Both the relative and the fixed conditions must be met. For instance: If $V_{DD_HV_A}$ is 5.9 V, $V_{DD_HV_ADC0}$ maximum value is 6.0 V then, despite the relative condition, the max value is $V_{DD_HV_A} + 0.3 = 6.2$ V.
4. PA3, PA7, PA10, PA11 and PE12 ADC_1 channels are coming from $V_{DD_HV_B}$ domain hence $V_{DD_HV_ADC1}$ should be within ± 300 mV of $V_{DD_HV_B}$ when these channels are used for ADC_1.
5. Any temperature beyond 125 °C should limit the current to 50 mA (max).
6. This is the storage temperature for the flash memory.

Note: Stresses exceeding the recommended absolute maximum ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. During overload conditions ($V_{IN} > V_{DD_HV_A/HV_B}$ or $V_{IN} < V_{SS_HV}$), the voltage on pins with respect to ground (V_{SS_HV}) must not exceed the recommended values.

3.4 Recommended operating conditions

Table 10. Recommended operating conditions (3.3 V)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
V_{SS_HV}	SR	Digital ground on VSS_HV pins	—	0	0	V
$V_{DD_HV_A}^{(1)}$	SR	Voltage on VDD_HV_A pins with respect to ground (V_{SS_HV})	—	3.0	3.6	V
$V_{DD_HV_B}^{(1)}$	SR	Voltage on VDD_HV_B pins with respect to ground (V_{SS_HV})	—	3.0	3.6	V
$V_{SS_LV}^{(2)}$	SR	Voltage on VSS_LV (low voltage digital supply) pins with respect to ground (V_{SS_HV})	—	$V_{SS_HV} - 0.1$	$V_{SS_HV} + 0.1$	V
$V_{RC_CTRL}^{(3)}$		Base control voltage for external BCP68 NPN device	Relative to V_{DD_LV}	0	$V_{DD_LV} + 1$	V
V_{SS_ADC}	SR	Voltage on VSS_HV_ADC0, VSS_HV_ADC1 (ADC reference) pin with respect to ground (V_{SS_HV})	—	$V_{SS_HV} - 0.1$	$V_{SS_HV} + 0.1$	V
$V_{DD_HV_ADC0}^{(4)}$	SR	Voltage on VDD_HV_ADC0 with respect to ground (V_{SS_HV})	—	3.0 ⁽⁵⁾	3.6	V
			Relative to $V_{DD_HV_A}^{(6)}$	$V_{DD_HV_A} - 0.1$	$V_{DD_HV_A} + 0.1$	
$V_{DD_HV_ADC1}^{(7)}$	SR	Voltage on VDD_HV_ADC1 with respect to ground (V_{SS_HV})	—	3.0	3.6	V
			Relative to $V_{DD_HV_A}^{(6)}$	$V_{DD_HV_A} - 0.1$	$V_{DD_HV_A} + 0.1$	
V_{IN}	SR	Voltage on any GPIO pin with respect to ground (V_{SS_HV})	—	$V_{SS_HV} - 0.1$	—	V
			Relative to $V_{DD_HV_A/HV_B}$	—	$V_{DD_HV_A/HV_B} + 0.1$	
I_{INJPAD}	SR	Injected input current on any pin during overload condition	—	-5	5	mA
I_{INJSUM}	SR	Absolute sum of all injected input currents during overload condition	—	-50	50	
TV_{DD}	SR	$V_{DD_HV_A}$ slope to ensure correct power up ⁽⁸⁾	—	—	0.5	V/ μ s
			—	0.5	—	V/min

Table 10. Recommended operating conditions (3.3 V) (continued)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
T_A	SR	Ambient temperature under bias	f_{CPU} up to 120 MHz + 2%	-40	125	°C
T_J	SR	Junction temperature under bias	—	-40	150	

- 100 nF EMI capacitance need to be provided between each VDD/VSS_HV pair.
- 100 nF EMI capacitance needs to be provided between each VDD_LV/VSS_LV supply pair. 10 μ F bulk capacitance needs to be provided as CREG on each VDD_LV pin. For details refer to the Power Management chapter of the MPC5646C Reference Manual.
- This voltage is internally generated by the device and no external voltage should be supplied.
- 100 nF capacitance needs to be provided between V_{DD_ADC}/V_{SS_ADC} pair.
- Full electrical specification cannot be guaranteed when voltage drops below 3.0 V. In particular, ADC electrical characteristics and I/Os DC electrical specification may not be guaranteed. When voltage drops below V_{LVDHVL}, device is reset.
- Both the relative and the fixed conditions must be met. For instance: If V_{DD_HV_A} is 5.9 V, V_{DD_HV_ADC0} maximum value is 6.0 V then, despite the relative condition, the max value is V_{DD_HV_A} + 0.3 = 6.2 V.
- PA3, PA7, PA10, PA11 and PE12 ADC_1 channels are coming from V_{DD_HV_B} domain hence V_{DD_HV_ADC1} should be within ± 100 mV of V_{DD_HV_B} when these channels are used for ADC_1.
- Guaranteed by the device validation.

Table 11. Recommended operating conditions (5.0 V)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
V _{SS_HV}	S R	Digital ground on VSS_HV pins	—	0	0	V
V _{DD_HV_A} ⁽¹⁾	S R	Voltage on VDD_HV_A pins with respect to ground (V _{SS_HV})	—	4.5	5.5	V
			Voltage drop ⁽²⁾	3.0	5.5	
V _{DD_HV_B}	S R	Generic GPIO functionality	—	3.0	5.5	V
		Ethernet/3.3 V functionality (See the notes in all figures in Section 2: Package pinouts and signal descriptions for the list of channels operating in V _{DD_HV_B} domain)	—	3.0	3.6	V
V _{SS_LV} ⁽³⁾	S R	Voltage on VSS_LV (Low voltage digital supply) pins with respect to ground (V _{SS_HV})	—	V _{SS_HV} - 0.1	V _{SS_HV} + 0.1	V
V _{RC_CTRL} ⁽⁴⁾		Base control voltage for external BCP68 NPN device	Relative to V _{DD_LV}	0	V _{DD_LV} + 1	V
V _{SS_ADC}	S R	Voltage on VSS_HV_ADC0, VSS_HV_ADC1 (ADC reference) pin with respect to ground (V _{SS_HV})	—	V _{SS_HV} - 0.1	V _{SS_HV} + 0.1	V

Table 11. Recommended operating conditions (5.0 V) (continued)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
$V_{DD_HV_ADC0(5)}$	S R	Voltage on VDD_HV_ADC0 with respect to ground (V_{SS_HV})	—	4.5	5.5	V
			Voltage drop ⁽²⁾	3.0	5.5	
			Relative to $V_{DD_HV_A}$ ⁽⁶⁾	$V_{DD_HV_A} - 0.1$	$V_{DD_HV_A} + 0.1$	
$V_{DD_HV_ADC1(7)}$	S R	Voltage on VDD_HV_ADC1 with respect to ground (V_{SS_HV})	—	4.5	5.5	V
			Voltage drop ⁽²⁾	3.0	5.5	
			Relative to $V_{DD_HV_A}$ ⁽⁶⁾	$V_{DD_HV_A} - 0.1$	$V_{DD_HV_A} + 0.1$	
V_{IN}	S R	Voltage on any GPIO pin with respect to ground (V_{SS_HV})	—	$V_{SS_HV} - 0.1$	—	V
			Relative to $V_{DD_HV_A/HV_B}$	—	$V_{DD_HV_A/HV_B} + 0.1$	
I_{INJPAD}	S R	Injected input current on any pin during overload condition	—	−5	5	mA
I_{INJSUM}	S R	Absolute sum of all injected input currents during overload condition	—	−50	50	
TV_{DD}	S R	$V_{DD_HV_A}$ slope to ensure correct power up ⁽⁸⁾	—	—	0.5	V/μs
			—	0.5	—	V/min
T_A C-Grade Part	S R	Ambient temperature under bias	—	−40	85	°C
T_J C-Grade Part	S R	Junction temperature under bias	—	−40	110	
T_A V-Grade Part	S R	Ambient temperature under bias	—	−40	105	
T_J V-Grade Part	S R	Junction temperature under bias	—	−40	130	
T_A M-Grade Part	S R	Ambient temperature under bias	—	−40	125	
T_J M-Grade Part	S R	Junction temperature under bias	—	−40	150	

- 100 nF EMI capacitance need to be provided between each VDD/VSS_HV pair.
- Full device operation is guaranteed by design from 3.0 V–5.5 V. OSC functionality is guaranteed from the entire range 3.0V–5.5 V, the parametrics measured are at 3.0V and 5.5V (extreme voltage ranges to cover the range of operation). The parametrics might have some variation in the intermediate voltage range, but there is no impact to functionality.
- 100 nF EMI capacitance needs to be provided between each VDD_LV/VSS_LV supply pair. 10 μF bulk capacitance needs to be provided as CREG on each VDD_LV pin.
- This voltage is internally generated by the device and no external voltage should be supplied.
- 100 nF capacitance needs to be provided between $V_{DD_HV_A(ADC0/ADC1)}/V_{SS_HV_A(ADC0/ADC1)}$ pair.
- Both the relative and the fixed conditions must be met. For instance: If $V_{DD_HV_A}$ is 5.9 V, $V_{DD_HV_ADC0}$ maximum value is 6.0 V then, despite the relative condition, the max value is $V_{DD_HV_A} + 0.3 = 6.2$ V.
- PA3, PA7, PA10, PA11 and PE12 ADC_1 channels are coming from $V_{DD_HV_B}$ domain hence VDD_HV_ADC1 should be within ±100 mV of $V_{DD_HV_B}$ when these channels are used for ADC_1.

8. Guaranteed by device validation.

Note: SRAM retention guaranteed to LVD levels.

3.5 Thermal characteristics

3.5.1 Package thermal characteristics

Table 12. LQFP thermal characteristics⁽¹⁾

Symbol		C	Parameter	Conditions ⁽²⁾	Pin count	Value ⁽³⁾			Unit
						Min	Typ	Max	
R _{θJA}	CC	D	Thermal resistance, junction-to-ambient natural convection	Single-layer board—1s	176	—	—	44.4 ⁽⁴⁾	°C/W
					208	—	—	TBD	°C/W
R _{θJA}	CC	D	Thermal resistance, junction-to-ambient natural convection	Four-layer board—2s2p ⁽⁵⁾	176	—	—	36.1	°C/W
					208	—	—	TBD	°C/W

1. Thermal characteristics are targets based on simulation that are subject to change per device characterization.
2. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = -40 to 125 °C.
3. All values need to be confirmed during device validation.
4. 1s board as per standard Jedec (JESD51-7) in natural convection
5. 2s2p board as per standard JEDEC (JESD51-7) in natural convection.

Table 13. LPGA208 thermal characteristics⁽¹⁾

Symbol		C	Parameter	Conditions	Value	Unit
R _{θJA}	CC	—	Thermal resistance, junction-to-ambient natural convection	Single-layer board—1s	TBD	°C/W
				Four-layer board—2s2p	TBD	

1. Thermal characteristics are targets based on simulation that are subject to change per device characterization.

Table 14. LPGA256 thermal characteristics⁽¹⁾

Symbol		C	Parameter	Conditions	Value	Unit
R _{θJA}	CC	—	Thermal resistance, junction-to-ambient natural convection	Single-layer board—1s	TBD	°C/W
				Four-layer board—2s2p	TBD	

1. Thermal characteristics are targets based on simulation that are subject to change per device characterization.

3.5.2 Power considerations

The average chip-junction temperature, T_J, in degrees Celsius, may be calculated using [Equation 1](#):

$$\text{Equation 1 } T_J = T_A + (P_D \times R_{\theta JA})$$

Where:

T_A is the ambient temperature in °C.

$R_{\theta JA}$ is the package junction-to-ambient thermal resistance, in °C/W.

P_D is the sum of P_{INT} and $P_{I/O}$ ($P_D = P_{INT} + P_{I/O}$).

P_{INT} is the product of I_{DD} and V_{DD} , expressed in watts. This is the chip internal power.

$P_{I/O}$ represents the power dissipation on input and output pins; user determined.

Most of the time for the applications, $P_{I/O} < P_{INT}$ and may be neglected. On the other hand, $P_{I/O}$ may be significant, if the device is configured to continuously drive external modules and/or memories.

An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is given by:

$$\text{Equation 2 } P_D = K / (T_J + 273 \text{ }^{\circ}\text{C})$$

Therefore, solving equations [Equation 1](#) and [Equation 2](#):

$$\text{Equation 3 } K = P_D \times (T_A + 273 \text{ }^{\circ}\text{C}) + R_{\theta JA} \times P_D^2$$

Where:

K is a constant for the particular part, which may be determined from [Equation 3](#) by measuring P_D (at equilibrium) for a known T_A . Using this value of K , the values of P_D and T_J may be obtained by solving equations [Equation 1](#) and [Equation 2](#) iteratively for any value of T_A .

3.6 I/O pad electrical characteristics

3.6.1 I/O pad types

The device provides four main I/O pad types depending on the associated alternate functions:

- Slow pads—These pads are the most common pads, providing a good compromise between transition time and low electromagnetic emission.
- Medium pads—These pads provide transition fast enough for the serial communication channels with controlled current to reduce electromagnetic emission.
- Fast pads—These pads provide maximum speed. These are used for improved Nexus debugging capability.
- Input only pads—These pads are associated to ADC channels and 32 kHz low power external crystal oscillator providing low input leakage.
- Low power pads—These pads are active in standby mode for wakeup source.

Also, medium/slow and fast/medium pads are available in design which can be configured to behave like a slow/medium and medium/fast pads depending upon the slew-rate control.

Medium and fast pads can use slow configuration to reduce electromagnetic emission, at the cost of reducing AC performance.

3.6.2 I/O input DC characteristics

Table 15 provides input DC electrical characteristics as described in Figure 6.

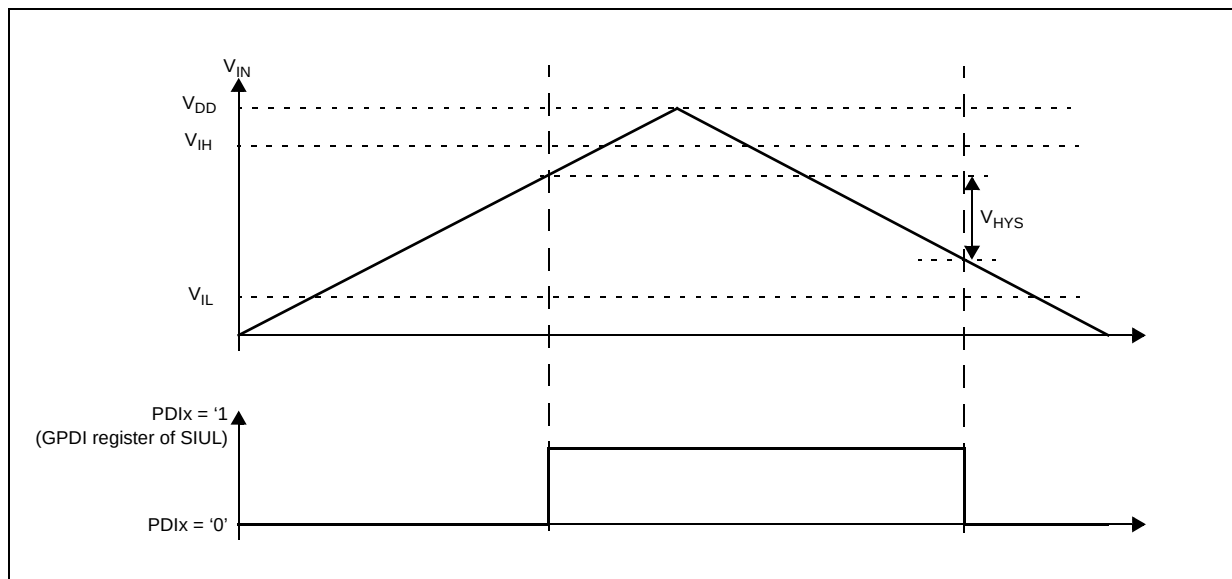


Figure 6. I/O input DC electrical characteristics definition

Table 15. I/O input DC electrical characteristics

Symbol		C	Parameter	Conditions ⁽¹⁾		Value ⁽²⁾			Unit
						Min	Typ	Max	
V _{IH}	S R	P	Input high level CMOS (Schmitt Trigger)	—		0.65V _{DD}	—	V _{DD} + 0.4	V
V _{IL}	S R	P	Input low level CMOS (Schmitt Trigger)	—		−0.3	—	0.35V _{DD}	
V _{HYS}	C C	C	Input hysteresis CMOS (Schmitt Trigger)	—		0.1V _{DD}	—	—	
I _{LKG}	C C D P	P	Digital input leakage	No injection on adjacent pin	T _A = −40 °C	—	2	—	nA
		T _A = 25 °C			—	2	—		
		T _A = 105 °C			—	12	500		
		T _A = 125 °C			—	70	1000		
W _{FI}	S R	P	Width of input pulse rejected by analog filter ⁽³⁾	—		—	—	40 ⁽⁴⁾	ns
W _{NFI}	S R	P	Width of input pulse accepted by analog filter ⁽³⁾	—		1000 ⁽⁴⁾	—	—	ns

1. $V_{DD} = 3.3\text{ V} \pm 10\% / 5.0\text{ V} \pm 10\%$, $T_A = -40\text{ to }125\text{ °C}$, unless otherwise specified.

2. V_{DD} as mentioned in the table is $V_{DD_HV_A}/V_{DD_HV_B}$. All values need to be confirmed during device validation.

3. Analog filters are available on all wakeup lines.

4. The width of input pulse in between 40 ns to 1000 ns is indeterminate. It may pass the noise or may not depending on silicon sample to sample variation.

3.6.3 I/O output DC characteristics

The following tables provide DC characteristics for bidirectional pads:

- [Table 16](#) provides weak pull figures. Both pull-up and pull-down resistances are supported.
- [Table 17](#) provides output driver characteristics for I/O pads when in SLOW configuration.
- [Table 18](#) provides output driver characteristics for I/O pads when in MEDIUM configuration.
- [Table 19](#) provides output driver characteristics for I/O pads when in FAST configuration.

Table 16. I/O pull-up/pull-down DC electrical characteristics

Symbol		C	Parameter	Conditions ^{(1),(2)}		Value			Unit
						Min	Typ	Max	
I _{WPU}	CC	P	Weak pull-up current absolute value	V _{IN} = V _{IL} , V _{DD} = 5.0 V ± 10%	PAD3V5V = 0	10	—	150	μA
		C			PAD3V5V = 1 ⁽³⁾	10	—	250	
		P		V _{IN} = V _{IL} , V _{DD} = 3.3 V ± 10%	PAD3V5V = 1	10	—	150	
I _{WPD}	CC	P	Weak pull-down current absolute value	V _{IN} = V _{IH} , V _{DD} = 5.0 V ± 10%	PAD3V5V = 0	10	—	150	μA
		C			PAD3V5V = 1	10	—	250	
		P		V _{IN} = V _{IH} , V _{DD} = 3.3 V ± 10%	PAD3V5V = 1	10	—	150	

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = -40 to 125 °C, unless otherwise specified.

2. V_{DD} as mentioned in the table is V_{DD_HV_A}/V_{DD_HV_B}.

3. The configuration PAD3V5 = 1 when V_{DD} = 5 V is only a transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

Table 17. SLOW configuration output buffer electrical characteristics

Symbol		C	Parameter		Conditions ^{(1),(2)}		Value			Unit
							Min	Typ	Max	
V _{O_H}	CC	P	Output high level SLOW configuration	Push Pull		I _{OH} = -3 mA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 0	0.8V _{DD}	—	—	V
		C				I _{OH} = -3 mA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 1 ⁽³⁾	0.8V _{DD}	—	—	
		P				I _{OH} = -1.5 mA, V _{DD} = 3.3 V ± 10%, PAD3V5V = 1	V _{DD} - 0.8	—	—	
V _{O_L}	CC	P	Output low level SLOW configuration	Push Pull		I _{OL} = 3 mA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	0.1V _{DD}	V
		C				I _{OL} = 3 mA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 1 ⁽³⁾	—	—	0.1V _{DD}	
		P				I _{OL} = 1.5 mA, V _{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	0.5	

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = -40 to 125 °C, unless otherwise specified.

- V_{DD} as mentioned in the table is $V_{DD_HV_A}/V_{DD_HV_B}$.
- The configuration PAD3V5 = 1 when $V_{DD} = 5$ V is only a transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

Table 18. MEDIUM configuration output buffer electrical characteristics

Symbol		C	Parameter	Conditions ^{(1),(2)}		Value			Unit
						Min	Typ	Max	
V _{OH}	CC	C	Output high level MEDIUM configuration	Push Pull	I _{OH} = −3 mA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 0	0.8V _{DD}	—	—	V
		C			I _{OH} = −1.5 mA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 1 ⁽³⁾	0.8V _{DD}	—	—	
		C			I _{OH} = −2 mA, V _{DD} = 3.3 V ± 10%, PAD3V5V = 1	V _{DD} − 0.8	—	—	
V _{OL}	CC	C	Output low level MEDIUM configuration	Push Pull	I _{OL} = 3 mA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	0.2V _{DD}	V
		C			I _{OL} = 1.5 mA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 1 ⁽³⁾	—	—	0.1V _{DD}	
		C			I _{OL} = 2 mA, V _{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	0.5	

- $V_{DD} = 3.3$ V $\pm$ 10% / 5.0 V $\pm$ 10%, $T_A = -40$ to 125 °C, unless otherwise specified.
- V_{DD} as mentioned in the table is $V_{DD_HV_A}/V_{DD_HV_B}$.
- The configuration PAD3V5 = 1 when $V_{DD} = 5$ V is only a transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

Table 19. FAST configuration output buffer electrical characteristics

Symbol		C	Parameter	Conditions ^{(1),(2)}		Value			Unit
						Min	Typ	Max	
V _{OH}	CC	P	Output high level FAST configuration	Push Pull	I _{OH} = −14 mA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 0	0.8V _{DD}	—	—	V
		C			I _{OH} = −7 mA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 1 ⁽³⁾	0.8V _{DD}	—	—	
		C			I _{OH} = −11 mA, V _{DD} = 3.3 V ± 10%, PAD3V5V = 1	V _{DD} − 0.8	—	—	

Table 19. FAST configuration output buffer electrical characteristics (continued)

Symbol		C	Parameter	Conditions ^{(1),(2)}		Value			Unit
						Min	Typ	Max	
V _{OL}	CC	P	Output low level FAST configuration	Push Pull	I _{OL} = 14 mA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	0.1V _{DD}	V
		C			I _{OL} = 7 mA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 1 ⁽³⁾	—	—	0.1V _{DD}	
		C			I _{OL} = 11 mA, V _{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	0.5	

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = -40 to 125 °C, unless otherwise specified.

2. V_{DD} as mentioned in the table is V_{DD_HV_A}/V_{DD_HV_B}.

3. The configuration PAD3V5 = 1 when V_{DD} = 5 V is only a transient configuration during power-up. All pads but RESET and Nexus outputs (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

3.6.4 Output pin transition times

Table 20. Output pin transition times

Symbol		C	Parameter	Conditions ^{(1),(2)}		Value ⁽³⁾			Unit
						Min	Typ	Max	
T _{tr}	CC	D	Output transition time output pin ⁽⁴⁾ SLOW configuration	C _L = 25 pF	V _{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	50	ns
		T		C _L = 50 pF		—	—	100	
		D		C _L = 100 pF		—	—	125	
		D		C _L = 25 pF	V _{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	40	
		T		C _L = 50 pF		—	—	50	
		D		C _L = 100 pF		—	—	75	
T _{tr}	CC	D	Output transition time output pin ⁽⁴⁾ MEDIUM configuration	C _L = 25 pF	V _{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	10	ns
		T		C _L = 50 pF		—	—	20	
		D		C _L = 100 pF		—	—	40	
		D		C _L = 25 pF	V _{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	12	
		T		C _L = 50 pF		—	—	25	
		D		C _L = 100 pF		—	—	40	
T _{tr}	CC	D	Output transition time output pin ⁽⁴⁾ FAST configuration	C _L = 25 pF	V _{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	4	ns
				C _L = 50 pF		—	—	6	
				C _L = 100 pF		—	—	12	
				C _L = 25 pF	V _{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	4	
				C _L = 50 pF		—	—	7	
				C _L = 100 pF		—	—	12	

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = -40 to 125 °C, unless otherwise specified.

2. V_{DD} as mentioned in the table is $V_{DD_HV_A}/V_{DD_HV_B}$.
3. All values need to be confirmed during device validation.
4. C_L includes device and package capacitances ($C_{PKG} < 5$ pF).

3.6.5 I/O pad current specification

The I/O pads are distributed across the I/O supply segment. Each I/O supply is associated to a V_{DD}/V_{SS_HV} supply pair as described in [Table 21](#).

[Table 22](#) provides I/O consumption figures.

In order to ensure device reliability, the average current of the I/O on a single segment should remain below the I_{AVGSEG} maximum value.

In order to ensure device functionality, the sum of the dynamic and static current of the I/O on a single segment should remain below the I_{DYNSEG} maximum value.

Table 21. I/O supplies

Package	I/O Supplies							
LBGA208	Equivalent to 208-pin LQFP segment pad distribution							
LBGA256 ⁽¹⁾	Equivalent to 208-pin LQFP segment pad distribution + G6, G11, H11, J11							
LQFP208	pin6 ($V_{DD_HV_A}$) pin7 (V_{SS_HV})	pin27 ($V_{DD_HV_A}$) pin28 (V_{SS_HV})	pin73 (V_{SS_HV}) pin75 ($V_{DD_HV_A}$)	pin101 ($V_{DD_HV_A}$) pin102 (V_{SS_HV})	pin132 (V_{SS_HV}) pin133 ($V_{DD_HV_A}$)	pin147 (V_{SS_HV}) pin148 ($V_{DD_HV_B}$)	pin174 (V_{SS_HV}) pin175 ($V_{DD_HV_A}$)	—
LQFP176	pin6 ($V_{DD_HV_A}$) pin7 (V_{SS_HV})	pin27 ($V_{DD_HV_A}$) pin28 (V_{SS_HV})	pin57 (V_{SS_HV}) pin59 ($V_{DD_HV_A}$)	pin85 ($V_{DD_HV_A}$) pin86 (V_{SS_HV})	pin123 (V_{SS_HV}) pin124 ($V_{DD_HV_B}$)	pin150 (V_{SS_HV}) pin151 ($V_{DD_HV_A}$)	—	—

1. $V_{DD_HV_B}$ supplies the IO voltage domain for the pins PE[12], PA[11], PA[10], PA[9], PA[8], PA[7], PE[13], PF[14], PF[15], PG[0], PG[1], PH[3], PH[2], PH[1], PH[0], PG[12], PG[13], and PA[3].

Table 22. I/O consumption

Symbol		C	Parameter	Conditions ^{(1),(2)}		Value ⁽³⁾			Unit
						Min	Typ	Max	
I _{SWTSLW} ⁽⁴⁾	C C	D	Peak I/O current for SLOW configuration	C _L = 25 pF	V _{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	19.9	mA
					V _{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	15.5	
I _{SWTMED} ⁽⁴⁾	C C	D	Peak I/O current for MEDIUM configuration	C _L = 25 pF	V _{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	28.8	mA
					V _{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	16.3	

Table 22. I/O consumption (continued)

Symbol		C	D	Parameter	Conditions ^{(1),(2)}		Value ⁽³⁾			Unit
							Min	Typ	Max	
I _{SWTFST} ⁽⁴⁾	C	C	D	Peak I/O current for FAST configuration	C _L = 25 pF	V _{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	113.5	mA
						V _{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	52.1	
I _{RMSSLW}	C	C	D	Root mean square I/O current for SLOW configuration	C _L = 25 pF, 2 MHz	V _{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	2.22	mA
					C _L = 25 pF, 4 MHz		—	—	3.13	
					C _L = 100 pF, 2 MHz		—	—	6.54	
					C _L = 25 pF, 2 MHz	V _{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	1.51	
					C _L = 25 pF, 4 MHz		—	—	2.14	
					C _L = 100 pF, 2 MHz		—	—	4.33	
I _{RMSMED}	C	C	D	Root mean square I/O current for MEDIUM configuration	C _L = 25 pF, 13 MHz	V _{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	6.5	mA
					C _L = 25 pF, 40 MHz		—	—	13.32	
					C _L = 100 pF, 13 MHz		—	—	18.26	
					C _L = 25 pF, 13 MHz	V _{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	4.91	
					C _L = 25 pF, 40 MHz		—	—	8.47	
					C _L = 100 pF, 13 MHz		—	—	10.94	
I _{RMSFST}	C	C	D	Root mean square I/O current for FAST configuration	C _L = 25 pF, 40 MHz	V _{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	21.05	mA
					C _L = 25 pF, 64 MHz		—	—	33	
					C _L = 100 pF, 40 MHz		—	—	55.77	
					C _L = 25 pF, 40 MHz	V _{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	14	
					C _L = 25 pF, 64 MHz		—	—	20	
					C _L = 100 pF, 40 MHz		—	—	34.89	
I _{AVGSEG}	S	R	D	Sum of all the static I/O current within a supply segment	V _{DD} = 5.0 V ± 10%, PAD3V5V = 0		—	—	70	mA
					V _{DD} = 3.3 V ± 10%, PAD3V5V = 1		—	—	65 ⁽⁴⁾	

1. $V_{\text{DD}} = 3.3 \text{ V} \pm 10\%$ / $5.0 \text{ V} \pm 10\%$, $T_A = -40$ to $125 \text{ }^\circ\text{C}$, unless otherwise specified.

2. V_{DD} as mentioned in the table is $V_{\text{DD_HV_A}}/V_{\text{DD_HV_B}}$.

3. All values need to be confirmed during device validation.

4. Stated maximum values represent peak consumption that lasts only a few ns during I/O transition.

3.7 RESET electrical characteristics

The device implements a dedicated bidirectional $\overline{\text{RESET}}$ pin.

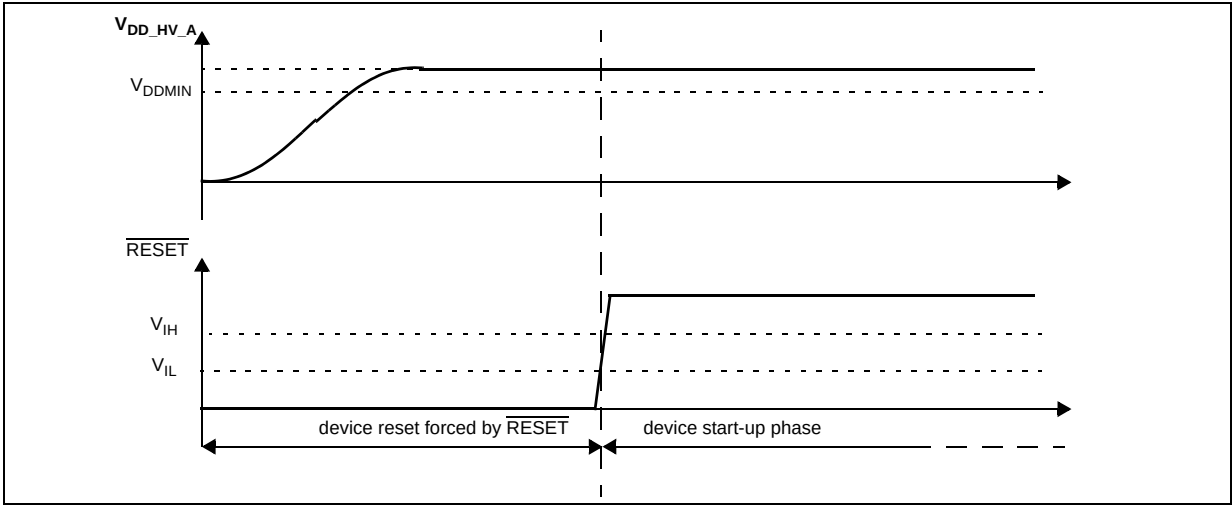


Figure 7. Start-up reset requirements

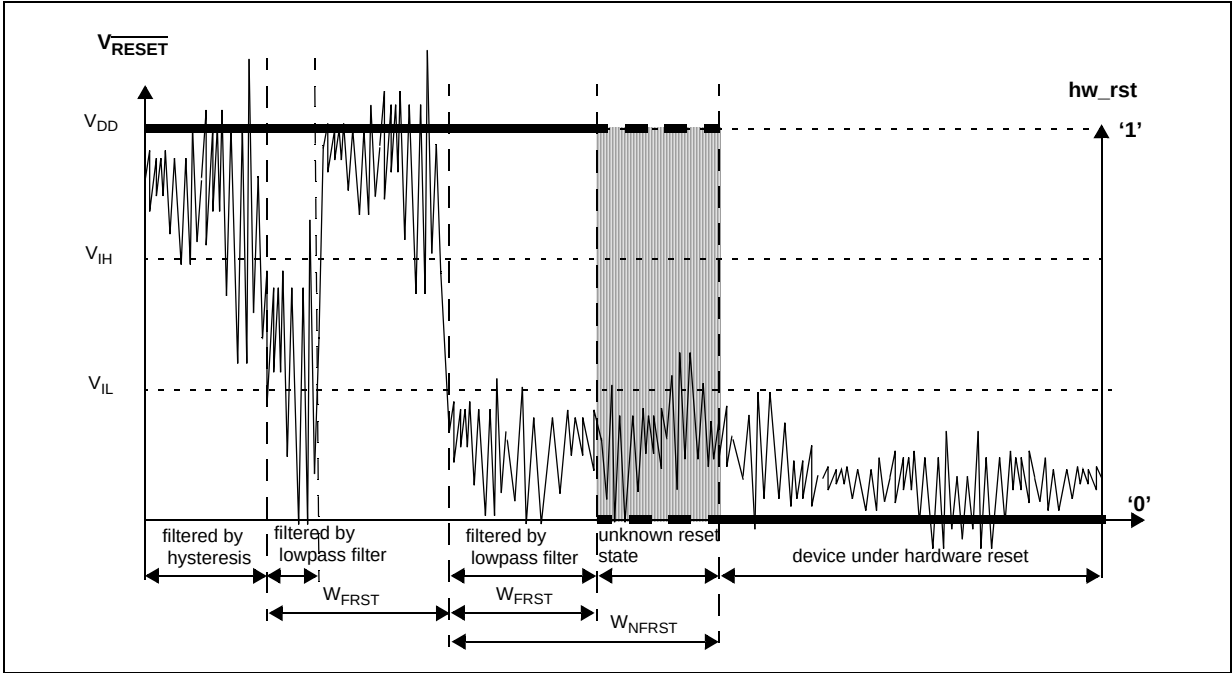


Figure 8. Noise filtering on reset signal

Table 23. Reset electrical characteristics

Symbol		C	Parameter	Conditions ⁽¹⁾	Value ⁽²⁾			Unit
					Min	Typ	Max	
V _{IH}	S R	P	Input High Level CMOS (Schmitt Trigger)	—	0.65V _{DD}	—	V _{DD} + 0.4	V
V _{IL}	S R	P	Input low Level CMOS (Schmitt Trigger)	—	−0.3	—	0.35V _{DD}	V

Table 23. Reset electrical characteristics (continued)

Symbol	C	C	Parameter	Conditions ⁽¹⁾	Value ⁽²⁾			Unit
					Min	Typ	Max	
V _{HYS}	C	C	Input hysteresis CMOS (Schmitt Trigger)	—	0.1V _{DD}	—	—	V
V _{OL}	C	P	Output low level	Push Pull, I _{OL} = 2 mA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	—	—	0.1V _{DD}	V
				Push Pull, I _{OL} = 1 mA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 1 ⁽³⁾	—	—	0.1V _{DD}	
				Push Pull, I _{OL} = 1 mA, V _{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	—	—	0.5	
T _{tr}	C	D	Output transition time output pin ⁽⁴⁾ MEDIUM configuration	C _L = 25 pF, V _{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	10	ns
				C _L = 50 pF, V _{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	20	
				C _L = 100 pF, V _{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	40	
				C _L = 25 pF, V _{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	12	
				C _L = 50 pF, V _{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	25	
				C _L = 100 pF, V _{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	40	
W _{FRST}	S	P	Reset input filtered pulse	—	—	—	40	ns
W _{NFRS} T	S	P	Reset input not filtered pulse	—	1000	—	—	ns
I _{WPUL}	C	P	Weak pull-up current absolute value	V _{DD} = 3.3 V ± 10%, PAD3V5V = 1	10	—	150	μA
				V _{DD} = 5.0 V ± 10%, PAD3V5V = 0	10	—	150	
				V _{DD} = 5.0 V ± 10%, PAD3V5V = 1 ⁽⁵⁾	10	—	250	

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = -40 to 125 °C, unless otherwise specified.
2. V_{DD} as mentioned in the table is V_{DD_HV_A}/V_{DD_HV_B}. All values need to be confirmed during device validation.
3. This is a transient configuration during power-up, up to the end of reset PHASE2 (refer to the RGM module section of the device Reference Manual).
4. C_L includes device and package capacitance (C_{PKG} < 5 pF).
5. The configuration PAD3V5 = 1 when V_{DD} = 5 V is only transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

3.8 Power management electrical characteristics

3.8.1 Voltage regulator electrical characteristics

The device implements an internal voltage regulator to generate the low voltage core supply V_{DD_LV} from the high voltage supply $V_{DD_HV_A}$. The following supplies are involved:

- HV: High voltage external power supply for voltage regulator module. This must be provided externally through $V_{DD_HV_A}$ power pin.
- LV: Low voltage internal power supply for core, FMPLL and Flash digital logic. This is generated by the on-chip VREG with an external ballast (BCP68 NPN device). It is further split into four main domains to ensure noise isolation between critical LV modules within the device:
 - LV_COR: Low voltage supply for the core. It is also used to provide supply for FMPLL through double bonding.
 - LV_CFLA0/CFLA1: Low voltage supply for the two code Flash modules. It is shorted with LV_COR through double bonding.
 - LV_DFLA: Low voltage supply for data Flash module. It is shorted with LV_COR through double bonding.
 - LV_PLL: Low voltage supply for FMPLL. It is shorted to LV_COR through double bonding.

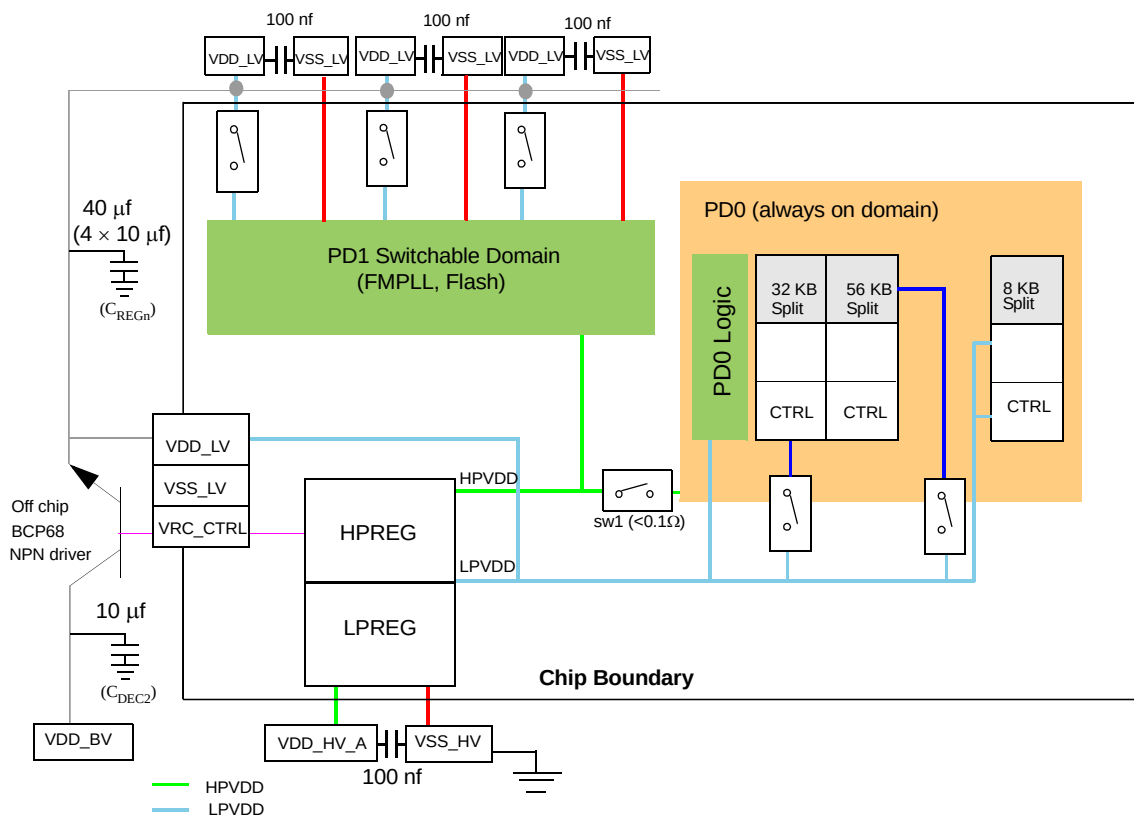


Figure 9. Voltage regulator capacitance connection

The internal voltage regulator requires external bulk capacitance (C_{REGn}) to be connected to the device to provide a stable low voltage digital supply to the device. Also required for stability is the C_{DEC2} capacitor at ballast collector. This is needed to minimize sharp injection current when ballast is turning ON. Apart from the bulk capacitance, user should connect EMI/decoupling cap (C_{REGP}) at each V_{DD_LV}/V_{SS_LV} pin pair.

Recommendations

- The external NPN driver must be BCP68 type.
- V_{DD_LV} should be implemented as a power plane from the emitter of the ballast transistor.
- 10 μ F capacitors should be connected to the 4 pins closest to the outside of the package and should be evenly distributed around the package. For BGA packages, the balls should be used are D8, H14, R9, J3—one cap on each side of package.
 - There should be a track direct from the capacitor to this pin (pin also connects to V_{DD_LV} plane). The tracks ESR should be less than 100 m Ω .
 - The remaining V_{DD_LV} pins (exact number will vary with package) should be decoupled with 0.1 μ F caps, connected to the pin as per 10 μ F.

(see [Section 3.4: Recommended operating conditions](#)).

3.8.2 V_{DD_BV} options

- Option 1: V_{DD_BV} shared with $V_{DD_HV_A}$
 V_{DD_BV} must be star routed from $V_{DD_HV_A}$ from the common source. This is to eliminate ballast noise injection on the MCU.
- Option 2: V_{DD_BV} independent of the MCU supply
 $V_{DD_BV} > 2.6$ V for correct functionality. The device is not monitoring this supply hence the external component must meet the 2.6 V criteria through external monitoring if required.

Table 24. Voltage regulator electrical characteristics

Symbol	C	Parameter	Conditions ⁽¹⁾	Value ⁽²⁾			Unit
				Min	Typ	Max	
C_{REGn}	S R	External ballast stability capacitance	—	40	—	60	μ F
R_{REG}	S R	Stability capacitor equivalent serial resistance	—	—	—	0.2	W
C_{REGP}	S R	Decoupling capacitance (Close to the pin)	$V_{DD_HV_A}/V_{SS_HV}$ pair		100	—	nF
			V_{DD_LV}/V_{SS_LV} pair		100	—	nF
C_{DEC2}	S R	Stability capacitance regulator supply (Close to the ballast collector)	V_{DD_BV}/V_{SS_HV}	10	—	40	μ F
V_{MREG}	C C	P Main regulator output voltage	After trimming $T_A = 25^\circ\text{C}$	1.20	1.28	1.32	V

Table 24. Voltage regulator electrical characteristics (continued)

Symbol		C	Parameter	Conditions ⁽¹⁾	Value ⁽²⁾			Unit
					Min	Typ	Max	
I _{MREG}	S R	—	Main regulator current provided to V _{DD_LV} domain	—	—	350	mA	
I _{MREGINT}	C C	D	Main regulator module current consumption	I _{MREG} = 200 mA	—	—	2	mA
				I _{MREG} = 0 mA	—	—	1	
V _{LPREG}	C C	P	Low power regulator output voltage	After trimming T _A = 25 °C	1.17	1.27	1.32	V
I _{LPREG}	S R	—	Low power regulator current provided to V _{DD_LV} domain	—	—	—	50	mA
I _{LPREGINT}	C C	D	Low power regulator module current consumption	I _{LPREG} = 15 mA; T _A = 55 °C	—	—	600	μA
		—		I _{LPREG} = 0 mA; T _A = 55 °C	—	20	—	
I _{VREGREF}	C C	D	Main LVDs and reference current consumption (low power and main regulator switched off)	T _A = 55 °C	—	2	—	μA
I _{VREDLVD12}	C C	D	Main LVD current consumption (switch-off during standby)	T _A = 55 °C	—	1	—	μA
I _{DD_HV_A}	C C	D	In-rush current on V _{DD_BV} during power-up	—	—	—	600 (3)	mA

1. $V_{DD_HV_A} = 3.3$ V $\pm$ 10% / 5.0 V $\pm$ 10%, $T_A = -40$ to 125 °C, unless otherwise specified.

2. All values need to be confirmed during device validation.

3. Inrush current is seen more like steps of 600 mA peak. The startup of the regulator happens in steps of 50 mV in ~25 steps to reach ~1.2 V V_{DD_LV} . Each step peak current is within 600 mA

3.8.3 Voltage monitor electrical characteristics

The device implements a Power-on Reset module to ensure correct power-up initialization, as well as four low voltage detectors to monitor the $V_{DD_HV_A}$ and the V_{DD_LV} voltage while device is supplied:

- POR monitors $V_{DD_HV_A}$ during the power-up phase to ensure device is maintained in a safe reset state
- LVDHV3 monitors $V_{DD_HV_A}$ to ensure device is reset below minimum functional supply
- LVDHV5 monitors $V_{DD_HV_A}$ when application uses device in the 5.0 V $\pm$ 10% range
- LVDLVCOR monitors power domain No. 1 (PD1)
- LVDLVBKP monitors power domain No. 0 (PD0). V_{DD_LV} is same as PD0 supply.

Note: When enabled, PD2 (RAM retention) is monitored through LVD_DIGBKP.

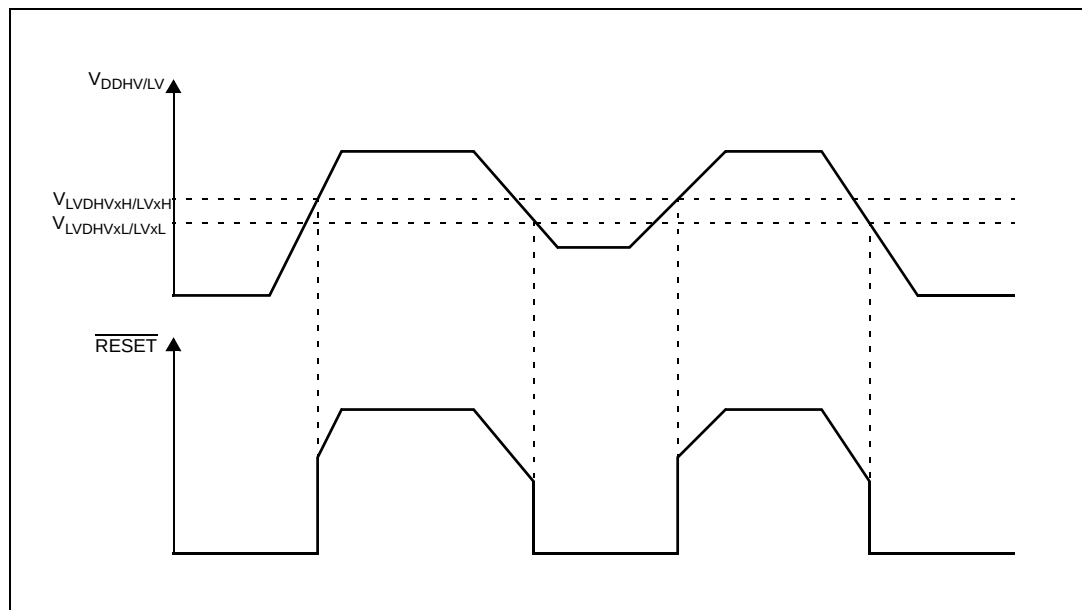


Figure 10. Low voltage monitor vs. Reset

Table 25. Low voltage monitor electrical characteristics

Symbol		C	Parameter	Conditions ⁽¹⁾	Value ⁽²⁾			Unit
					Min	Typ	Max	
V _{PORUP}	S R	P	Supply for functional POR module	—	1.0	—	5.5	V
V _{PORH}	C C	P	Power-on reset threshold	—	1.5	—	2.6	
V _{LVDHV3H}	C C	T	LVDHV3 low voltage detector high threshold	—	2.7	—	2.85	
V _{LVDHV3L}	C C	T	LVDHV3 low voltage detector low threshold	—	2.6	—	2.74	
V _{LVDHV5H}	C C	T	LVDHV5 low voltage detector high threshold	—	4.3	—	4.5	
V _{LVDHV5L}	C C	T	LVDHV5 low voltage detector low threshold	—	4.2	—	4.4	
V _{LVDLVCORL}	C C	P	LVDLVCOR low voltage detector low threshold	T _A = 25 °C, after trimming	1.08	—	1.17	
V _{LVDLVBKPL}	C C	P	LVDLVBKP low voltage detector low threshold		1.08	—	1.17	

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = -40 to 125 °C, unless otherwise specified.

2. All values need to be confirmed during device validation.

3.9 Low voltage domain power consumption

[Table 26](#) provides DC electrical characteristics for significant application modes. These values are indicative values; actual consumption depends on the application.

Table 26. Low voltage power domain electrical characteristics⁽¹⁾

Symbol		C	Parameter	Conditions ⁽²⁾		Value			Unit
						Min	Typ ⁽³⁾	Max ⁽⁴⁾	
I _{DDMAX} ⁽⁵⁾	C C	D	RUN mode maximum average current	—		—	210	300 ⁽⁶⁾ , (7)	mA
I _{DDRUN}	C C C	P	RUN mode typical average current ⁽⁸⁾	at 120 MHz	T _A = 25 °C	—	150	208 ⁽⁹⁾	mA
		at 80 MHz		T _A = 25 °C	—	110 ⁽⁸⁾	150 ⁽¹⁰⁾	mA	
		at 120 MHz		T _A = 125 °C	—	180	280	mA	
I _{DDHALT}	C C	P	HALT mode current ⁽¹¹⁾	at 120 MHz	T _A = 25 °C	—	20	27	mA
		C		at 120 MHz	T _A = 125 °C	—	35	100	mA
I _{DDSTOP}	C C	P	STOP mode current ⁽¹²⁾	No clocks active	T _A = 25 °C	—	0.4	5	mA
		C			T _A = 125 °C	—	16	72	mA
I _{DDSTDBY3} (96 KB RAM retained)	C C	P	STANDBY3 mode current ⁽¹³⁾	No clocks active	T _A = 25 °C	—	50	96	μA
		C			T _A = 125 °C	—	630	2400	μA
I _{DDSTDBY2} (64 KB RAM retained)	C C	C	STANDBY2 mode current ⁽¹⁴⁾	No clocks active	T _A = 25 °C	—	40	92	μA
		C			T _A = 125 °C	—	500	2000	μA
I _{DDSTDBY1} (8 KB RAM retained)	C C	C	STANDBY1 mode current ⁽¹⁵⁾	No clocks active	T _A = 25 °C	—	25	85	μA
		C			T _A = 125 °C	—	230	1100	μA
Adders in LP mode	C C	T	32 KHz OSC	—	T _A = 25 °C	—	—	5	μA
			4–40 MHz OSC	—	T _A = 25 °C	—	—	3	mA
			16 MHz IRC	—	T _A = 25 °C	—	—	500	μA
			128 KHz IRC	—	T _A = 25 °C	—	—	5	μA

1. Except for I_{DDMAX} , all the current values are total current drawn from $V_{DD_HV_A}$.
2. $V_{DD} = 3.3\text{ V} \pm 10\% / 5.0\text{ V} \pm 10\%$, $T_A = -40\text{ to }125\text{ °C}$, unless otherwise specified. All temperatures are based on an ambient temperature.
3. Target typical current consumption for the following typical operating conditions and configuration. Process = typical, Voltage = 1.2 V.
4. Target maximum current consumption for mode observed under typical operating conditions. Process = Fast, Voltage = 1.32 V.
5. Running consumption is given on voltage regulator supply (V_{DDREG}). It does not include consumption linked to I/Os toggling. This value is highly dependent on the application. The given value is thought to be a worst case value with all cores and peripherals running, and code fetched from code flash while modify operation on-going on data flash. It is to be noticed that this value can be significantly reduced by application: switch-off not used peripherals (default), reduce peripheral frequency through internal prescaler, fetch from RAM most used functions, use low power mode when possible.
6. Higher current may be sunk by device during power-up and standby exit. Please refer to inrush current in [Table 24](#).
7. Maximum “allowed” current is package dependent.

8. Only for the "P" classification: Code fetched from RAM: Serial IPs CAN and LIN in loop back mode, DSPI as Master, PLL as system Clock (4 x Multiplier) peripherals on (eMIOS/CTU/ADC) and running at max frequency, periodic SW/WDG timer reset enabled. RUN current measured with typical application with accesses on both code flash and RAM.
9. Subject to change, Configuration: 1 x e200z4d + 4 kbit/s Cache, 1 x e200z0h (1/2 system frequency), CSE, 1 x eDMA (10 ch.), 6 x FlexCAN (4 x 500 kbit/s, 2 x 125 kbit/s), 4 x LINFlexD (20 kbit/s), 6 x DSPI (2 x 2 Mbit/s, 3 x 4 Mbit/s, 1 x 10 Mbit/s), 16 x Timed I/O, 16 x ADC Input, 1 x FlexRay (2 ch., 10 Mbit/s), 1 x FEC (100 Mbit/s), 1 x RTC, 4 PIT channels, 1 x SWT, 1 x STM. For lower pin count packages reduce the amount of timed I/O's and ADC channels. RUN current measured with typical application with accesses on both code flash and RAM.
10. This value is obtained from limited sample set.
11. Data Flash Power Down. Code Flash in Low Power. SIRC 128 kHz and FIRC 16 MHz ON. 16 MHz XTAL clock. FlexCAN: instances: 0, 1, 2 ON (clocked but no reception or transmission), instances: 4, 5, 6 clocks gated. LINFlex: instances: 0, 1, 2 ON (clocked but no reception or transmission), instance: 3-9 clocks gated. eMIOS: instance: 0 ON (16 channels on PA[0]-PA[11] and PC[12]-PC[15]) with PWM 20 kHz, instance: 1 clock gated. DSPI: instance: 0 (clocked but no communication, instance: 1-7 clocks gated). RTC/API ON. PIT ON. STM ON. ADC ON but no conversion except 2 analog watchdogs.
12. Only for the "P" classification: No clock, FIRC 16 MHz OFF, SIRC128 kHz ON, PLL OFF, HPVreg OFF, LPVreg ON. All possible peripherals off and clock gated. Flash in power down mode.
13. Only for the "P" classification: LPreg ON, HPVreg OFF, 96 KB RAM ON, device configured for minimum consumption, all possible modules switched-off.
14. Only for the "P" classification: LPreg ON, HPVreg OFF, 64 KB RAM ON, device configured for minimum consumption, all possible modules switched-off.
15. LPreg ON, HPVreg OFF, 8 KB RAM ON, device configured for minimum consumption, all possible modules switched OFF.

3.10 Flash memory electrical characteristics

3.10.1 Program/Erase characteristics

[Table 27](#) shows the code flash memory program and erase characteristics.

Table 27. Code flash memory—Program and erase specifications

Symbol	C	Parameter	Value				Unit
			Min	Typ ⁽¹⁾	Initial max ⁽²⁾	Max ⁽³⁾	
T _{dwprogram}	C	Double word (64 bits) program time ⁽⁴⁾	—	18	50	500	μs
T _{16Kpperase}		16 KB block pre-program and erase time	—	200	500	5000	ms
T _{32Kpperase}		32 KB block pre-program and erase time	—	300	600	5000	ms
T _{128Kpperase}		128 KB block pre-program and erase time	—	600	1300	5000	ms
T _{eslat}	C	D Erase Suspend Latency	—	—	30	30	μs
t _{ESRT} ⁽⁵⁾	C	Erase Suspend Request Rate	20	—	—	—	ms
t _{PABT}	D	Program Abort Latency	—	—	10	10	μs
t _{EAPT}	D	Erase Abort Latency	—	—	30	30	μs

1. Typical program and erase times assume nominal supply values and operation at 25 °C. All times are subject to change pending device characterization.
2. Initial factory condition: < 100 program/erase cycles, 25 °C, typical supply voltage.
3. The maximum program and erase times occur after the specified number of program/erase cycles. These maximum values are characterized but not guaranteed.
4. Actual hardware programming times. This does not include software overhead.
5. It is Time between erase suspend resume and the next erase suspend request.

Table 28 shows the data flash memory program and erase characteristics.

Table 28. Data flash memory—Program and erase specifications

Symbol	C	Parameter	Value				Unit
			Min	Typ ⁽¹⁾	Initial max ⁽²⁾	Max ⁽³⁾	
$T_{wprogram}$	C	Word (32 bits) program time ⁽⁴⁾	—	30	70	500	μs
$T_{16Kpperase}$		16 KB block pre-program and erase time	—	700	800	5000	ms
T_{eslat}		Erase Suspend Latency	—	—	30	30	μs
$t_{ESRT}^{(5)}$		Erase Suspend Request Rate	10	—	—	—	ms
t_{PABT}		Program Abort Latency	—	—	12	12	μs
t_{EAPT}		Erase Abort Latency	—	—	30	30	μs

1. Typical program and erase times assume nominal supply values and operation at 25 °C. All times are subject to change pending device characterization.
2. Initial factory condition: < 100 program/erase cycles, 25 °C, typical supply voltage.
3. The maximum program and erase times occur after the specified number of program/erase cycles. These maximum values are characterized but not guaranteed.
4. Actual hardware programming times. This does not include software overhead.
5. It is time between erase suspend resume and next erase suspend.

Table 29. Flash memory module life

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Typ	
P/E	CC	C	Number of program/erase cycles per block for 16 Kbyte blocks over the operating temperature range (T _J)	—	100000	100000	cycles
			Number of program/erase cycles per block for 32 Kbyte blocks over the operating temperature range (T _J)	—	10000	100000	cycles
			Number of program/erase cycles per block for 128 Kbyte blocks over the operating temperature range (T _J)	—	1000	100000	cycles
Retention	CC	C	Minimum data retention at 85 °C average ambient temperature ⁽¹⁾	Blocks with 0–1000 P/E cycles	20	—	years
				Blocks with 10000 P/E cycles	10	—	years
				Blocks with 100000 P/E cycles	5	—	years

1. Ambient temperature averaged over duration of application, not to exceed recommended product operating temperature range.

ECC circuitry provides correction of single bit faults and is used to improve further automotive reliability results. Some units will experience single bit corrections throughout the life of the product with no impact to product reliability.

Table 30. Flash memory read access timing⁽¹⁾

Symbol	C	Parameter	Conditions ⁽²⁾		Frequency range	Unit
			Code flash memory	Data flash memory		
f _{READ}	CC	P	5 wait states	13 wait states	120—100	MHz
		C	4 wait states	11 wait states	100—80	
		D	3 wait states	9 wait states	80—64	
		C	2 wait states	7 wait states	64—40	
		C	1 wait states	4 wait states	40—20	
		C	0 wait states	2 wait states	20—0	

1. Max speed is the maximum speed allowed including PLL frequency modulation (FM).

2. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = -40 to 125 °C, unless otherwise specified.

3.10.2 Flash memory power supply DC characteristics

[Table 31](#) shows the flash memory power supply DC characteristics on external supply.

Table 31. Flash memory power supply DC electrical characteristics

Symbol	C	Parameter	Conditions ⁽¹⁾	Value ⁽²⁾			Unit
				Min	Typ	Max	
I _{CFREAD} ⁽³⁾	C	Sum of the current consumption on V _{DD_HV_A} on read access	Flash memory module read f _{CPU} = 120 MHz + 2% ⁽⁴⁾			33	mA
I _{DFREAD} ⁽³⁾	C					13	
I _{CFMOD} ⁽³⁾	C	Sum of the current consumption on V _{DD_HV_A} (program/erase)	Program/Erase on-going while reading flash memory registers f _{CPU} = 120 MHz + 2% ⁽⁴⁾			52	mA
I _{DFMOD} ⁽³⁾	C					13	
I _{CFLPW} ⁽³⁾	C	Sum of the current consumption on V _{DD_HV_A} during flash memory low power mode				1.1	mA
I _{CFPWD} ⁽³⁾	C	Sum of the current consumption on V _{DD_HV_A} during flash memory power down mode				150	μA
I _{DFPWD} ⁽³⁾	C					150	

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = -40 to 125 °C, unless otherwise specified.

2. All values need to be confirmed during device validation.

3. Data based on characterization results, not tested in production.

4. f_{CPU} 120 MHz + 2% can be achieved over full temperature 125 °C ambient, 150 °C junction temperature.

3.10.3 Flash memory start-up/switch-off timings

Table 32. Start-up time/Switch-off time

Symbol	C	Parameter	Conditions (1)	Value			Unit
				Min	Typ	Max	
T _{FLARSTEXIT}	C C	D Delay for flash memory module to exit reset mode	—	—	—	125	μs
				—	—		
T _{FLALPEXIT}	C C	T Delay for flash memory module to exit low-power mode	—	—	—	0.5	
T _{FLAPDEXIT}	C C	T Delay for flash memory module to exit power-down mode	—	—	—	30	
				—	—		
T _{FLALPENTRY}	C C	T Delay for flash memory module to enter low-power mode	—	—	—	0.5	

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = -40 to 125 °C, unless otherwise specified.

3.11 Electromagnetic compatibility (EMC) characteristics

Susceptibility tests are performed on a sample basis during product characterization.

3.11.1 Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user apply EMC software optimization and pre-qualification tests in relation with the EMC level requested for the application.

- Software recommendations – The software flowchart must include the management of runaway conditions such as:
 - Corrupted program counter
 - Unexpected reset
 - Critical data corruption (control registers)
- Pre-qualification trials – Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the reset pin or the oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note *Software Techniques For Improving Microcontroller EMC Performance* (AN1015)).

3.11.2 Electromagnetic interference (EMI)

The product is monitored in terms of emission based on a typical application. This emission test conforms to the IEC61967-1 standard, which specifies the general conditions for EMI measurements.

Table 33. EMI radiated emission measurement⁽¹⁾⁽²⁾

Symbol		C	Parameter	Conditions		Value			Unit
						Min	Typ	Max	
—	S R	—	Scan range	—		0.150		1000	MHz
f _{CPU}	S R	—	Operating frequency	—		—	120	—	MHz
V _{DD_LV}	S R	—	LV operating voltages	—		—	1.28	—	V
S _{EMI}	C C	T	Peak level	V _{DD} = 5 V, T _A = 25 °C, LQFP176 package Test conforming to IEC 61967-2, f _{OSC} = 40 MHz/f _{CPU} = 120 MHz	No PLL frequency modulation	—	—	18	dBμV
					± 2% PLL frequency modulation	—	—	14 ⁽³⁾	dBμV

1. EMI testing and I/O port waveforms per IEC 61967-1, -2, -4.
2. For information on conducted emission and susceptibility measurement (norm IEC 61967-4), please contact your local marketing representative.
3. All values need to be confirmed during device validation.

3.11.3 Absolute maximum ratings (electrical sensitivity)

Based on two different tests (ESD and LU) using specific measurement methods, the product is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pin). This test conforms to the AEC-Q100-002/-003/-011 standard. For more details, refer to the application note *Electrostatic Discharge Sensitivity Measurement* (AN1181).

Table 34. ESD absolute maximum ratings⁽¹⁾⁽²⁾

Symbol	Ratings	Conditions	Class	Max value ⁽³⁾	Unit
V _{ESD(HBM)}	Electrostatic discharge voltage (Human Body Model)	T _A = 25 °C conforming to AEC-Q100-002	H1C	2000	V
V _{ESD(MM)}	Electrostatic discharge voltage (Machine Model)	T _A = 25 °C conforming to AEC-Q100-003	M2	200	
V _{ESD(CDM)}	Electrostatic discharge voltage (Charged Device Model)	T _A = 25 °C conforming to AEC-Q100-011	C3A	500 750 (corners)	

1. All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

2. A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.
3. Data based on characterization results, not tested in production.

Static latch-up (LU)

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply over-voltage is applied to each power supply pin.
- A current injection is applied to each input, output and configurable I/O pin.

These tests are compliant with the EIA/JESD 78 IC latch-up standard.

Table 35. Latch-up results

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	$T_A = 125\text{ }^{\circ}\text{C}$ conforming to JESD 78	II level A

3.12 Fast external crystal oscillator (4–40 MHz) electrical characteristics

The device provides an oscillator/resonator driver. [Figure 11](#) describes a simple model of the internal oscillator driver and provides an example of a connection for an oscillator or a resonator.

[Table 36](#) provides the parameter description of 4 MHz to 40 MHz crystals used for the design simulations.

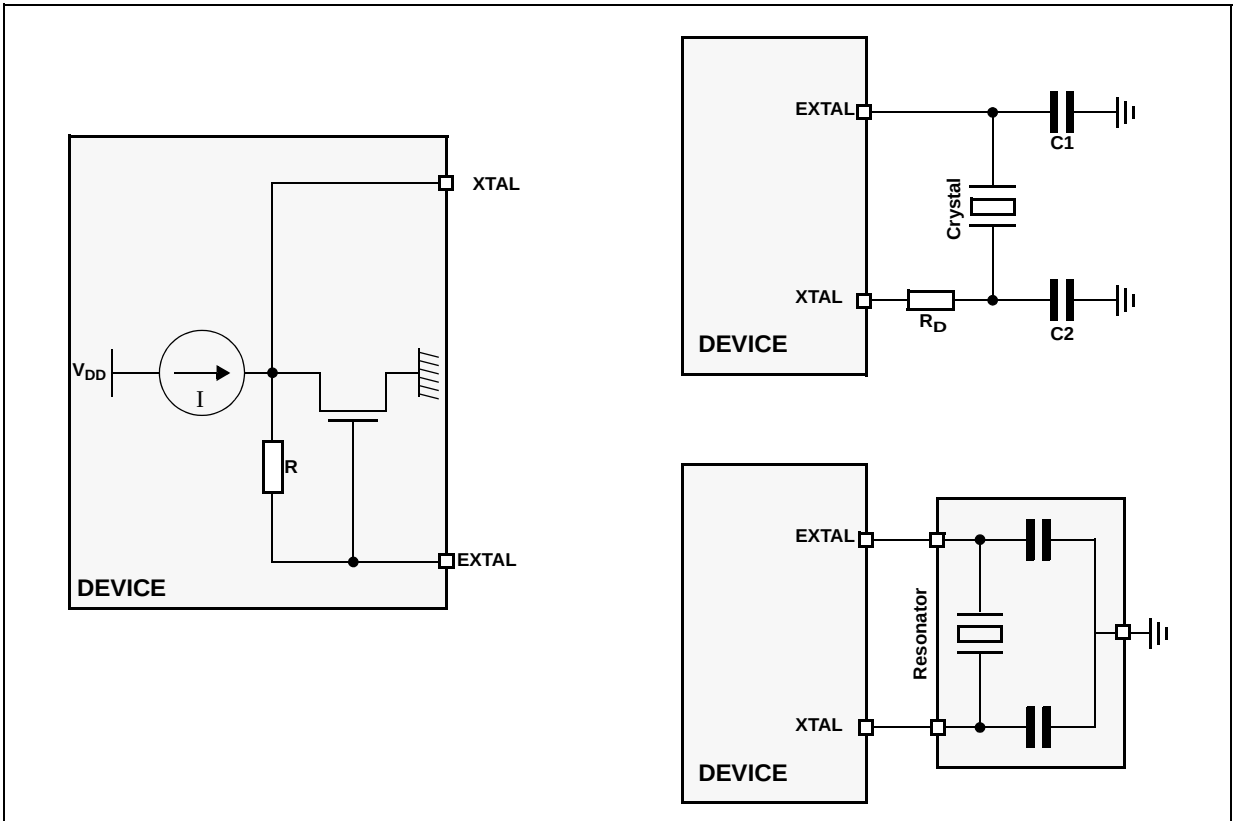


Figure 11. Crystal oscillator and resonator connection scheme

Note: XTAL/EXTAL must not be directly used to drive external circuits.

Table 36. Crystal description

Nominal frequency (MHz)	NDK crystal reference	Crystal equivalent series resistance ESR Ω	Crystal motional capacitance (C_m) fF	Crystal motional inductance (L_m) mH	Load on xtal/xtalout $C1 = C2$ (pF) ⁽¹⁾	Shunt capacitance between xtalout and xtal in $C0$ ⁽²⁾ (pF)
4	NX8045GB	300	2.68	591.0	21	2.93
8	NX5032GA	300	2.46	160.7	17	3.01
10		150	2.93	86.6	15	2.91
12		120	3.11	56.5	15	2.93
16		120	3.90	25.3	10	3.00
40	NX5032GA	50	6.18	2.56	8	3.49

1. The values specified for C1 and C2 are the same as used in simulations. It should be ensured that the testing includes all the parasitics (from the board, probe, crystal, etc.) as the AC / transient behavior depends upon them.
2. The value of C0 specified here includes 2 pF additional capacitance for parasitics (to be seen with bond-pads, package, etc.).

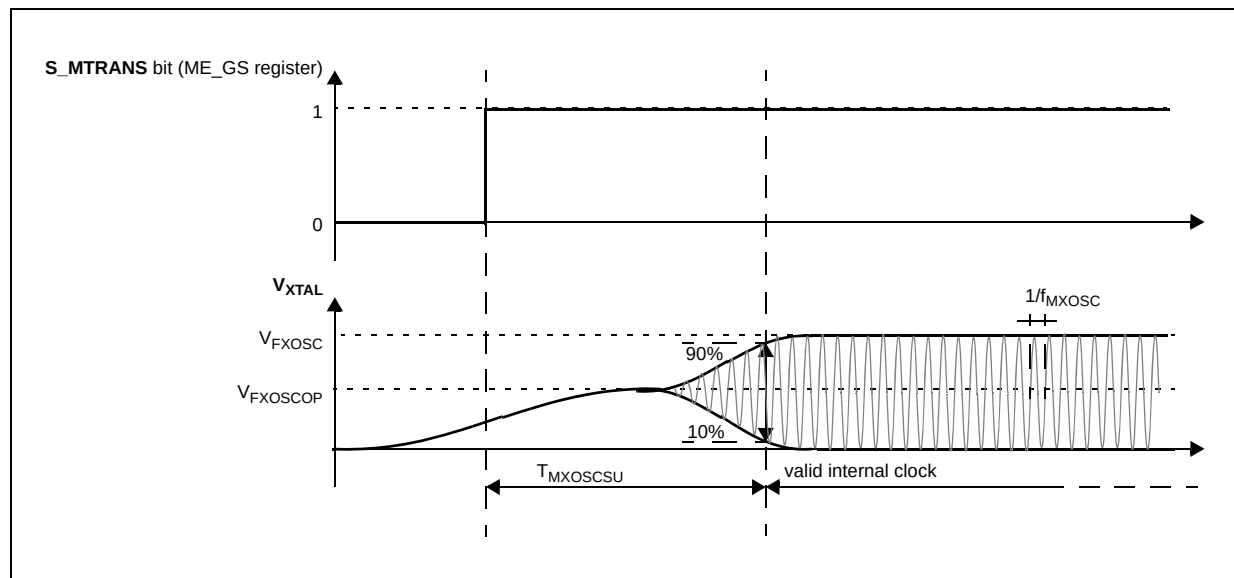


Figure 12. Fast external crystal oscillator (4 to 40 MHz) electrical characteristics

Table 37. Fast external crystal oscillator (4 to 40 MHz) electrical characteristics

Symbol	C	Parameter	Conditions ⁽¹⁾	Value ⁽²⁾			Unit
				Min	Typ	Max	
f _{FXOSC}	SR	Fast external crystal oscillator frequency	—	4.0	—	40.0	MHz
g _{mFXOSC}	CC	Fast external crystal oscillator transconductance	V _{DD} = 3.3 V ± 10%	4 ⁽³⁾	—	20 ⁽³⁾	mA/V
			V _{DD} = 5.0 V ± 10%	6.5 ⁽³⁾	—	25 ⁽³⁾	
V _{FXOSC}	CC	Oscillation amplitude at EXTAL	f _{OSC} = 40 MHz For both V _{DD} = 3.3 V ± 10%, V _{DD} = 5.0 V ± 10%	—	0.95	—	V
V _{FXOSCOP}	CC	Oscillation operating point	—	—	1.8	—	V
I _{FXOSC} ⁽⁴⁾	CC	Fast external crystal oscillator consumption	V _{DD} = 3.3 V ± 10%, f _{OSC} = 40 MHz	—	2	2.2	mA
			V _{DD} = 5.0 V ± 10%, f _{OSC} = 40 MHz	—	2.3	2.5	
			V _{DD} = 3.3 V ± 10%, f _{OSC} = 16 MHz	—	1.3	1.5	
			V _{DD} = 5.0 V ± 10%, f _{OSC} = 16 MHz	—	1.6	1.8	
T _{FXOSCSU}	CC	Fast external crystal oscillator start-up time	f _{OSC} = 40 MHz For both V _{DD} = 3.3 V ± 10%, V _{DD} = 5.0 V ± 10%	—	—	5	ms

Table 37. Fast external crystal oscillator (4 to 40 MHz) electrical characteristics (continued)

Symbol		C	Parameter	Conditions ⁽¹⁾	Value ⁽²⁾			Unit
					Min	Typ	Max	
V _{IH}	SR	P	Input high level CMOS (Schmitt Trigger)	Oscillator bypass mode	0.65V _{DD_} HV_A	—	V _{DD_HV_A} + 0.4	V
V _{IL}	SR	P	Input low level CMOS (Schmitt Trigger)	Oscillator bypass mode	−0.3	—	0.35V _{DD_HV_A}	V

1. $V_{DD} = 3.3\text{ V} \pm 10\% / 5.0\text{ V} \pm 10\%$, $T_A = -40$ to $125\text{ }^{\circ}\text{C}$, unless otherwise specified.
2. All values need to be confirmed during device validation.
3. Based on ATE Cz
4. Stated values take into account only analog module consumption but not the digital contributor (clock tree and enabled peripherals).

3.13 Slow external crystal oscillator (32 kHz) electrical characteristics

The device provides a low power oscillator/resonator driver.

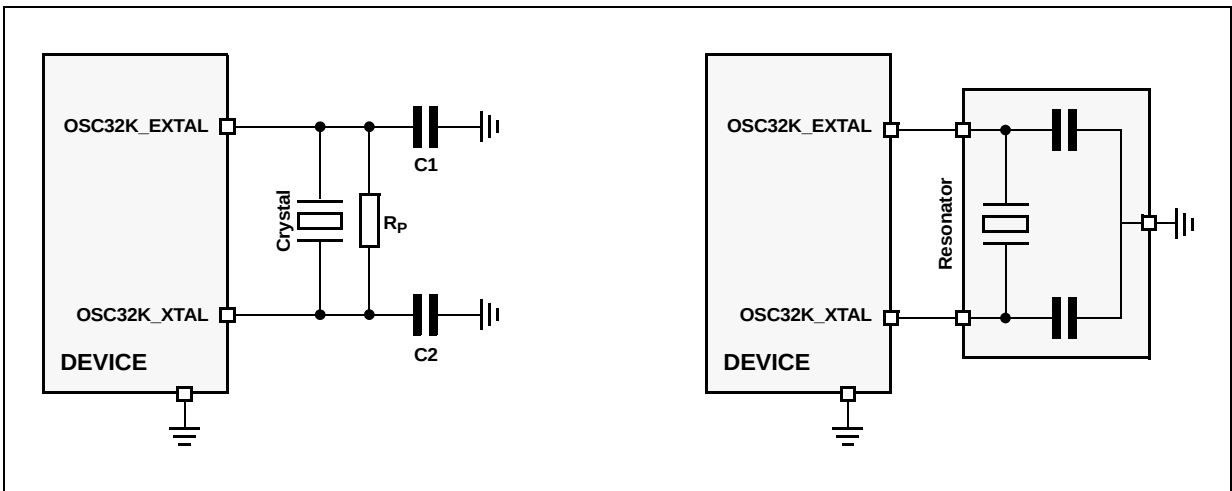


Figure 13. Crystal oscillator and resonator connection scheme

Note: OSC32K_XTAL/OSC32K_EXTAL must not be directly used to drive external circuits.

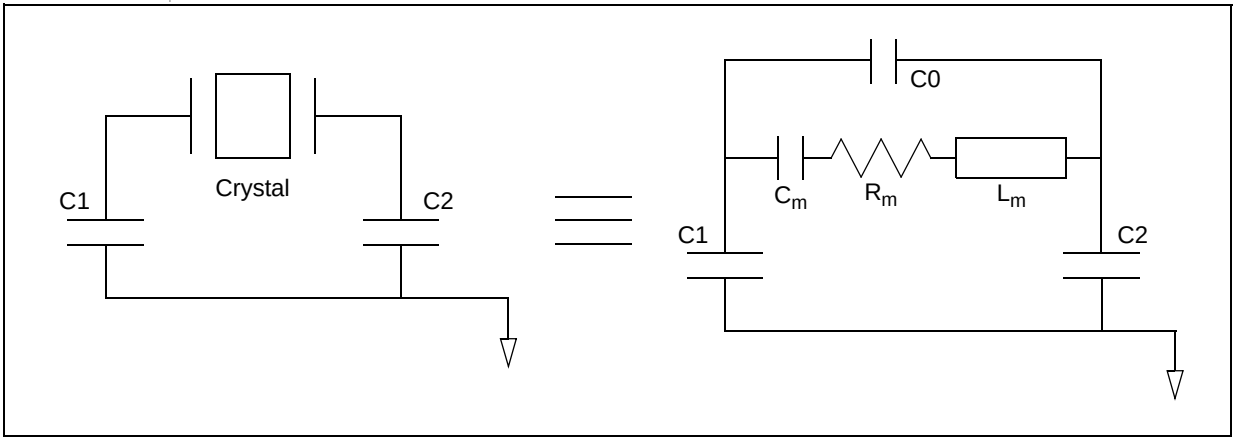


Figure 14. Equivalent circuit of a quartz crystal

Table 38. Crystal motional characteristics⁽¹⁾

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
L_m	Motional inductance	—	—	11.796	—	KH
C_m	Motional capacitance	—	—	2	—	fF
C1/C2	Load capacitance at OSC32K_XTAL and OSC32K_EXTAL with respect to ground ⁽²⁾	—	18	—	28	pF
$R_m^{(3)}$	Motional resistance	AC coupled @ $C_0 = 2.85 \text{ pF}^{(4)}$	—	—	65	kW
		AC coupled @ $C_0 = 4.9 \text{ pF}^{(4)}$	—	—	50	
		AC coupled @ $C_0 = 7.0 \text{ pF}^{(4)}$	—	—	35	
		AC coupled @ $C_0 = 9.0 \text{ pF}^{(4)}$	—	—	30	

1. The crystal used is Epson Toyocom MC306.
2. This is the recommended range of load capacitance at OSC32K_XTAL and OSC32K_EXTAL with respect to ground. It includes all the parasitics due to board traces, crystal and package.
3. Maximum ESR (R_m) of the crystal is 50 kΩ.
4. C_0 Includes a parasitic capacitance of 2.0 pF between OSC32K_XTAL and OSC32K_EXTAL pins.

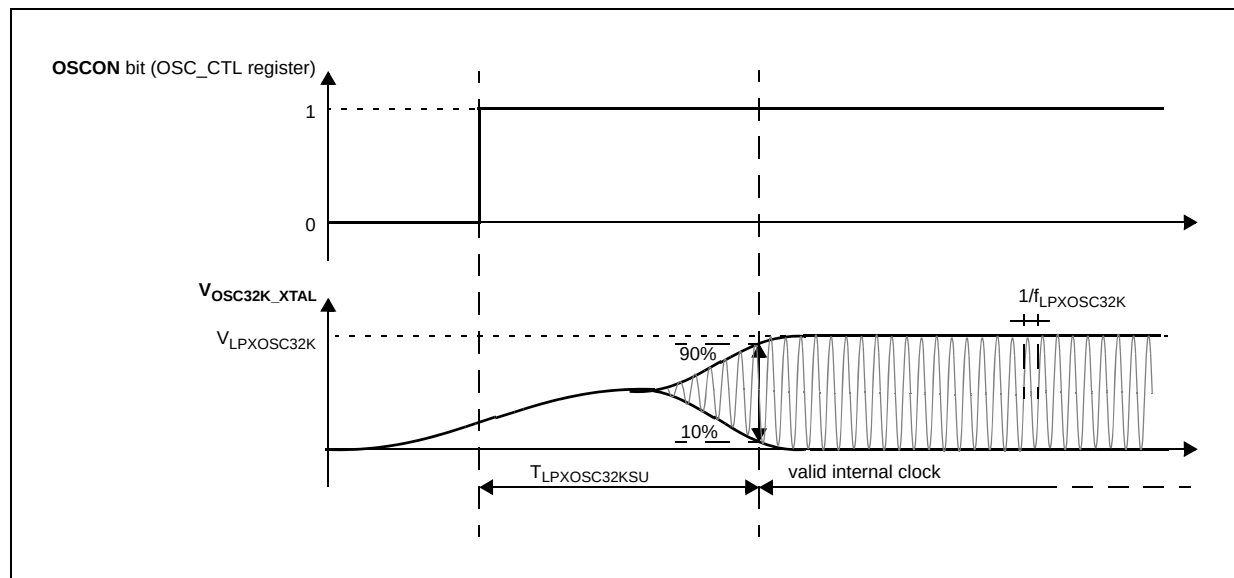


Figure 15. Slow external crystal oscillator (32 kHz) electrical characteristics

Table 39. Slow external crystal oscillator (32 kHz) electrical characteristics

Symbol	C	Parameter	Conditions ⁽¹⁾	Value ⁽²⁾			Unit
				Min	Typ	Max	
f_{SXOSC}	S R	Slow external crystal oscillator frequency	—	32	32.76 8	40	kHz
g_{mSXOSC}	C C	Slow external crystal oscillator transconductance	$V_{DD} = 3.3 \text{ V} \pm 10\%$, $V_{DD} = 5.0 \text{ V} \pm 10\%$	13 ⁽³⁾ 15 ⁽³⁾	—	33 ⁽³⁾ 35 ⁽³⁾	$\mu\text{A/V}$
V_{SXOSC}	C C	Oscillation amplitude	—	1.2	1.4	1.7	V
$I_{SXOSCBIAS}$	C C	Oscillation bias current	—	1.2	—	4.4	μA
I_{SXOSC}	C C	Slow external crystal oscillator consumption	—	—	—	7	μA
$T_{SXOSCSU}$	C C	Slow external crystal oscillator start-up time	—	—	—	2 ⁽⁴⁾	s

1. $V_{DD} = 3.3 \text{ V} \pm 10\% / 5.0 \text{ V} \pm 10\%$, $T_A = -40$ to 125°C , unless otherwise specified.

2. All values need to be confirmed during device validation.

3. Based on ATE CZ

4. Start-up time has been measured with EPSON TOYOCOM MC306 crystal. Variation may be seen with other crystal.

3.14 FMPLL electrical characteristics

The device provides a frequency-modulated phase-locked loop (FMPLL) module to generate a fast system clock from the main oscillator driver.

Table 40. FMPLL electrical characteristics

Symbol	C	Parameter	Conditions ⁽¹⁾	Value ⁽²⁾			Unit
				Min	Typ	Max	
f_{PLLIN}	S R	—	FMPLL reference clock ⁽³⁾	—	—	—	—
Δ_{PLLIN}	S R	—	FMPLL reference clock duty cycle ⁽³⁾	—	—	—	—
f_{PLLOUT}	C C	P	FMPLL output clock frequency	—	—	—	—
f_{CPU}	S R	—	System clock frequency	—	—	—	—
f_{FREE}	C C	P	Free-running frequency	—	—	—	—
t_{LOCK}	C C	P	FMPLL lock time	Stable oscillator ($f_{PLLIN} = 16$ MHz)			—
Δt_{LTJIT}	C C	—	FMPLL long term jitter	$f_{PLLIN} = 40$ MHz (resonator), f_{PLLCLK} @ 120 MHz, 4000 cycles			—
I_{PLL}	C C	C	FMPLL consumption	$T_A = 25$ °C			—

- $V_{DD} = 3.3\text{ V} \pm 10\% / 5.0\text{ V} \pm 10\%$, $T_A = -40$ to 125 °C, unless otherwise specified.
- All values need to be confirmed during device validation.
- PLLIN clock retrieved directly from 4-40 MHz XOSC or 16 MIRC. Input characteristics are granted when oscillator is used in functional mode. When bypass mode is used, oscillator input clock should verify f_{PLLIN} and Δ_{PLLIN} .
- f_{CPU} 120 + 2% MHz can be achieved at 125 °C.

3.15 Fast internal RC oscillator (16 MHz) electrical characteristics

The device provides a 16 MHz main internal RC oscillator. This is used as the default clock at the power-up of the device and can also be used as input to PLL.

Table 41. Fast internal RC oscillator (16 MHz) electrical characteristics

Symbol	C	Parameter	Conditions ⁽¹⁾	Value ⁽²⁾			Unit
				Min	Typ	Max	
f_{FIRC}	C C	Fast internal RC oscillator high frequency	$T_A = 25$ °C, trimmed	—	16	—	MHz
	S R		—	12	—	20	

Table 41. Fast internal RC oscillator (16 MHz) electrical characteristics (continued)

Symbol		C	Parameter	Conditions ⁽¹⁾		Value ⁽²⁾			Unit
						Min	Typ	Max	
$I_{\text{FIRCRUN}}^{(3)}$	C C	T	Fast internal RC oscillator high frequency current in running mode	$T_A = 25\text{ }^{\circ}\text{C}$, trimmed		—	—	200	μA
I_{FIRCPWD}	C C C	D	Fast internal RC oscillator high frequency current in power down mode	$T_A = 25\text{ }^{\circ}\text{C}$		—	—	100	nA
		$T_A = 55\text{ }^{\circ}\text{C}$		—	—	200	nA		
		$T_A = 125\text{ }^{\circ}\text{C}$		—	—	1	μA		
I_{FIRCSTOP}	C C C	T	Fast internal RC oscillator high frequency and system clock current in stop mode	$T_A = 25\text{ }^{\circ}\text{C}$	sysclk = off	—	500	—	μA
					sysclk = 2 MHz	—	600	—	
					sysclk = 4 MHz	—	700	—	
					sysclk = 8 MHz	—	900	—	
					sysclk = 16 MHz	—	1250	—	
T_{FIRCSU}	C C C C	C — — —	Fast internal RC oscillator start-up time	$T_A = 55\text{ }^{\circ}\text{C}$	$V_{\text{DD}} = 5.0\text{ V} \pm 10\%$	—	—	2.0	μs
					$V_{\text{DD}} = 3.3\text{ V} \pm 10\%$	—	—	5	
				$T_A = 125\text{ }^{\circ}\text{C}$	$V_{\text{DD}} = 5.0\text{ V} \pm 10\%$	—	—	2.0	
					$V_{\text{DD}} = 3.3\text{ V} \pm 10\%$	—	—	5	
Δ_{FIRCPRE}	C C	C	Fast internal RC oscillator precision after software trimming of f_{FIRC}	$T_A = 25\text{ }^{\circ}\text{C}$		−1	—	+1	%
Δ_{FIRCTRIM}	C C	C	Fast internal RC oscillator trimming step	$T_A = 25\text{ }^{\circ}\text{C}$		—	1.6		%
Δ_{FIRCVAR}	C C	C	Fast internal RC oscillator variation over temperature and supply with respect to f_{FIRC} at $T_A = 25\text{ }^{\circ}\text{C}$ in high-frequency configuration	—		−5	—	+5	%

1. $V_{DD} = 3.3\text{ V} \pm 10\% / 5.0\text{ V} \pm 10\%$, $T_A = -40\text{ to }125\text{ }^{\circ}\text{C}$, unless otherwise specified.

2. All values need to be confirmed during device validation.

3. This does not include consumption linked to clock tree toggling and peripherals consumption when RC oscillator is ON.

3.16 Slow internal RC oscillator (128 kHz) electrical characteristics

The device provides a 128 kHz low power internal RC oscillator. This can be used as the reference clock for the RTC module.

Table 42. Slow internal RC oscillator (128 kHz) electrical characteristics

Symbol	C	Parameter	Conditions ⁽¹⁾	Value ⁽²⁾			Unit
				Min	Typ	Max	
f _{SIRC}	C	Slow internal RC oscillator low frequency	T _A = 25 °C, trimmed	—	128	—	kHz
	S		untrimmed, across temperatures	84	—	205	
I _{SIRC} ⁽³⁾	C	Slow internal RC oscillator low frequency current	T _A = 25 °C, trimmed	—	—	5	μA
T _{SIRCSU}	C	Slow internal RC oscillator start-up time	T _A = 25 °C, V _{DD} = 5.0 V ± 10%	—	8	12	μs
Δ _{SIRCPRE}	C	Slow internal RC oscillator precision after software trimming of f _{SIRC}	T _A = 25 °C	−2	—	+2	%
Δ _{SIRCTRIM}	C	Slow internal RC oscillator trimming step	—	—	2.7	—	
Δ _{SIRCVAR}	C	Variation in f _{SIRC} across temperature and fluctuation in supply voltage, post trimming	—	−10	—	+10	%

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = −40 to 125 °C, unless otherwise specified.

2. All values need to be confirmed during device validation.

3. This does not include consumption linked to clock tree toggling and peripherals consumption when RC oscillator is ON.

3.17 ADC electrical characteristics

3.17.1 Introduction

The device provides two Successive Approximation Register (SAR) analog-to-digital converters (10-bit and 12-bit).

Note: *Due to ADC limitations, the two ADCs cannot sample a shared channel at the same time i.e., their sampling windows cannot overlap if a shared channel is selected. If this is done, neither of the ADCs can guarantee their conversion accuracies.*

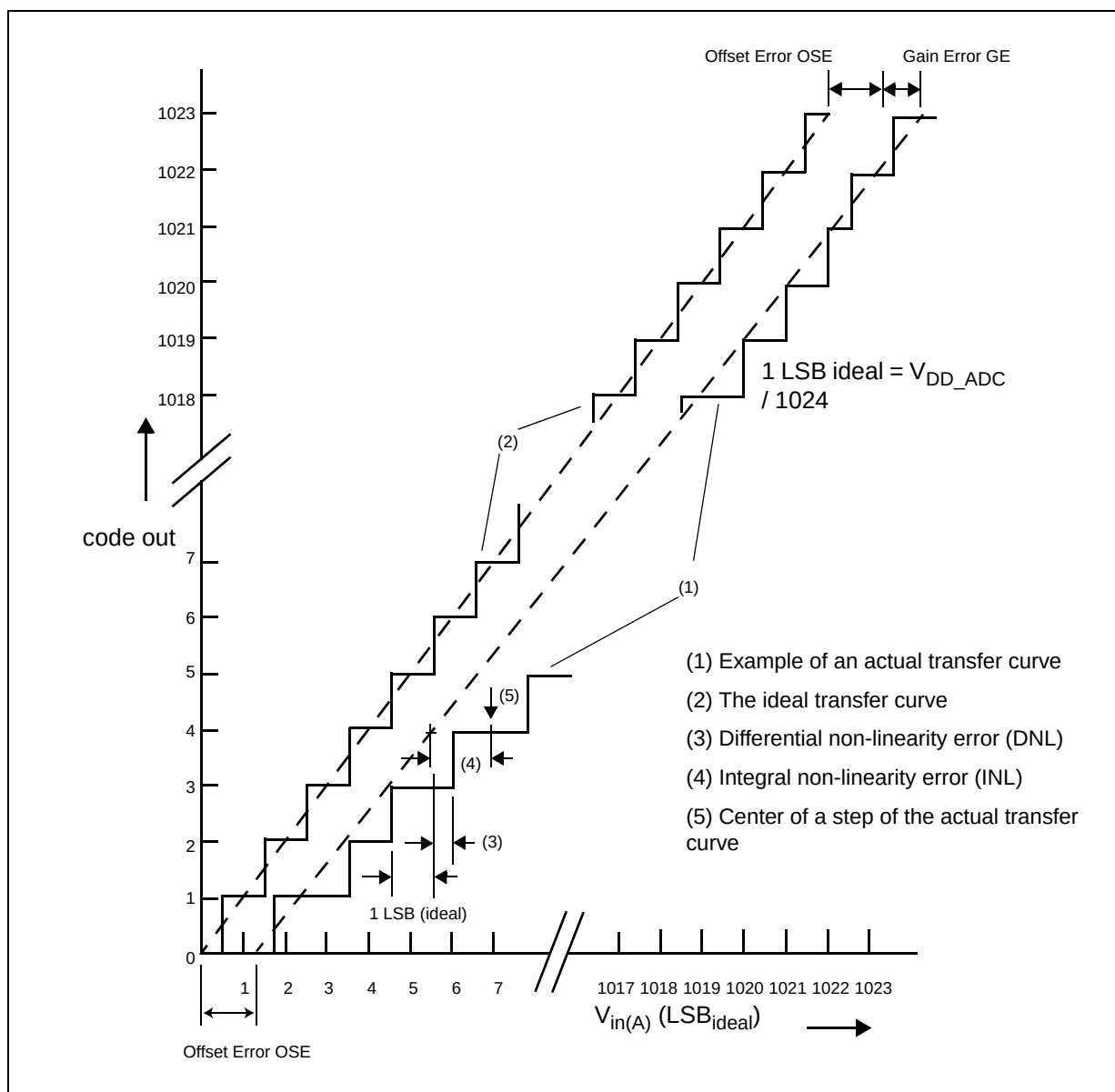


Figure 16. ADC_0 characteristic and error definitions

Input impedance and ADC accuracy

To preserve the accuracy of the A/D converter, it is necessary that analog input pins have low AC impedance. Placing a capacitor with good high frequency characteristics at the input pin of the device, can be effective: the capacitor should be as large as possible, ideally infinite. This capacitor contributes to attenuating the noise present on the input pin; furthermore, it sources charge during the sampling phase, when the analog signal source is a high-impedance source. A real filter, can typically be obtained by using a series resistance with a capacitor on the input pin (simple RC Filter). The RC filtering may be limited according to the value of source impedance of the transducer or circuit supplying the analog signal to be measured. The filter at the input pins must be designed taking into account the

dynamic characteristics of the input signal (bandwidth) and the equivalent input impedance of the ADC itself.

In fact a current sink contributor is represented by the charge sharing effects with the sampling capacitance: being C_S and C_{P2} substantially two switched capacitances, with a frequency equal to the conversion rate of the ADC, it can be seen as a resistive path to ground. For instance, assuming a conversion rate of 1MHz, with $C_S + C_{P2}$ equal to 3pF, a resistance of 330K Ω is obtained ($R_{eq} = 1 / (f_c * (C_S + C_{P2}))$), where f_c represents the conversion rate at the considered channel). To minimize the error induced by the voltage partitioning between this resistance (sampled voltage on $C_S + C_{P2}$) and the sum of $R_S + R_F$, the external circuit must be designed to respect the following relation

Equation 4

$$V_A \cdot \frac{R_S + R_F}{R_{EQ}} < \frac{1}{2} \text{LSB}$$

The formula above provides a constraint for external network design, in particular on resistive path.

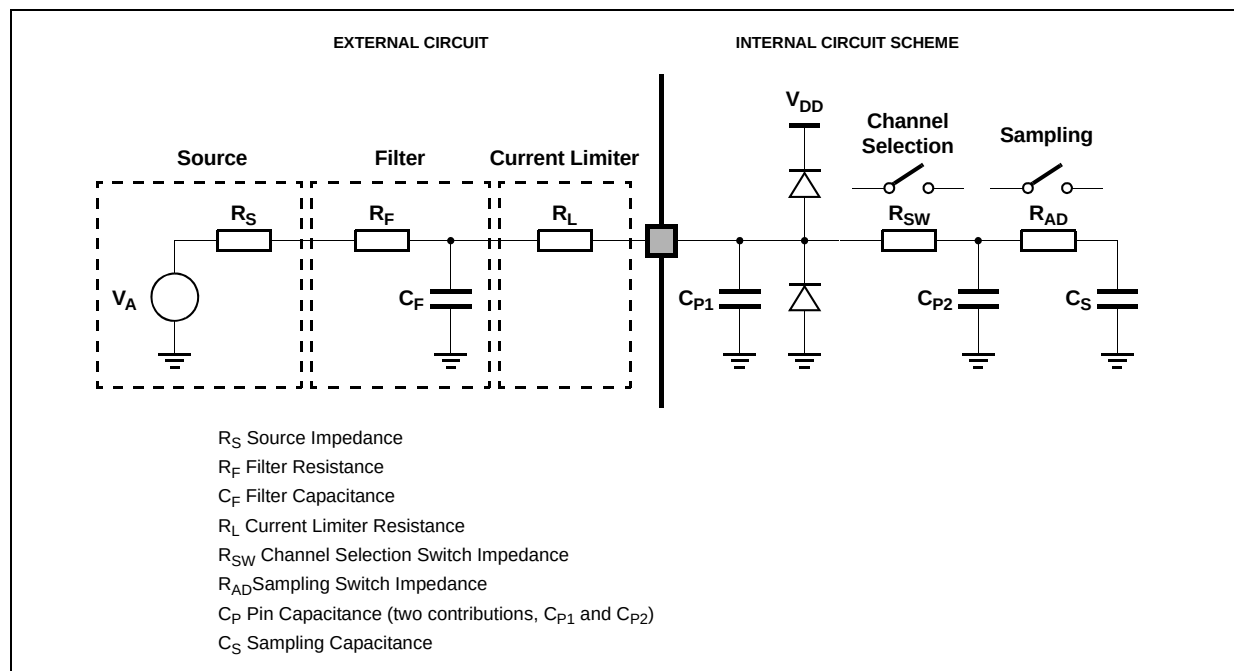


Figure 17. Input equivalent circuit (precise channels)

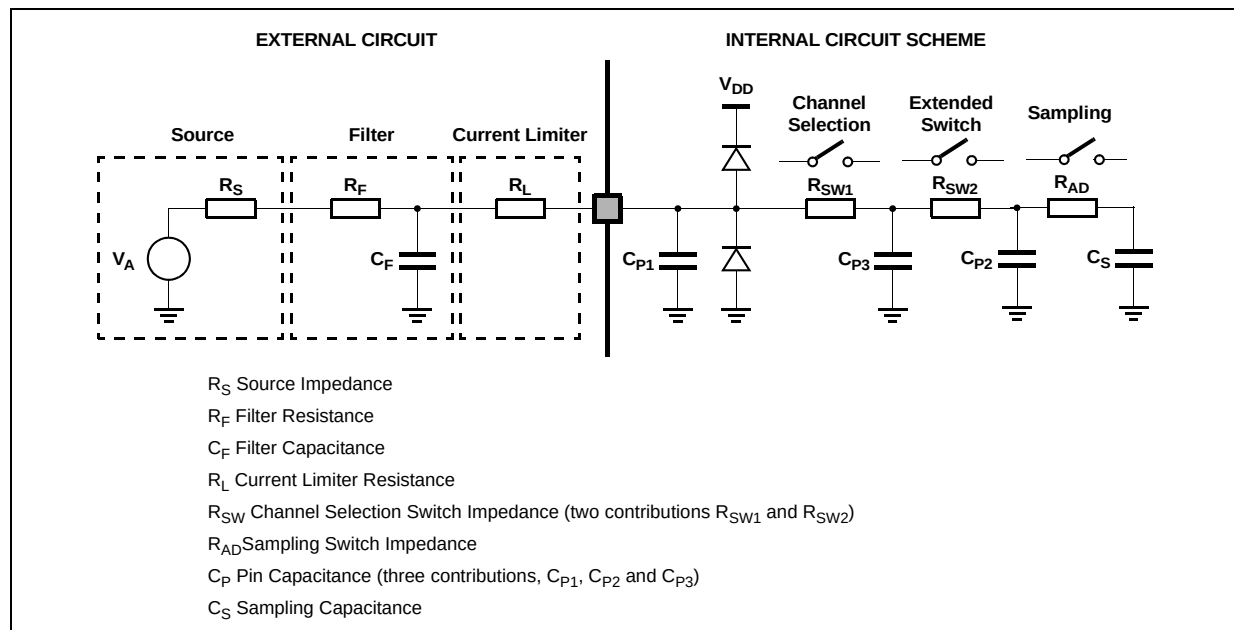


Figure 18. Input equivalent circuit (extended channels)

A second aspect involving the capacitance network shall be considered. Assuming the three capacitances C_F , C_{P1} and C_{P2} initially charged at the source voltage V_A (refer to the equivalent circuit reported in [Figure 17](#)): when the sampling phase is started (A/D switch close), a charge sharing phenomena is installed.

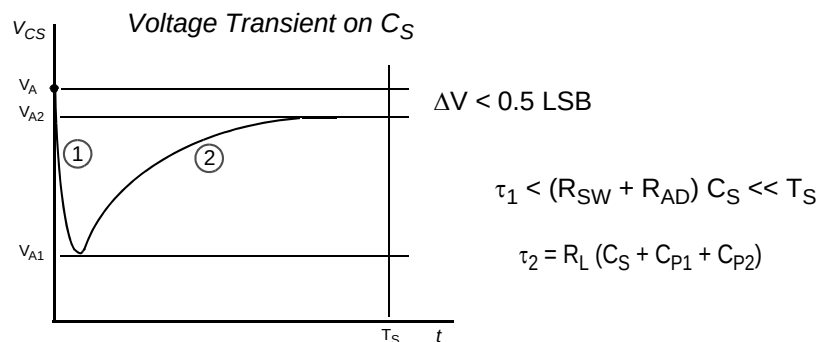


Figure 19. Transient behavior during sampling phase

In particular two different transient periods can be distinguished:

- A first and quick charge transfer from the internal capacitance C_{P1} and C_{P2} to the sampling capacitance C_S occurs (C_S is supposed initially completely discharged): considering a worst case (since the time constant in reality would be faster) in which C_{P2} is reported in parallel to C_{P1} (call $C_P = C_{P1} + C_{P2}$), the two capacitances C_P and C_S are in series, and the time constant is

Equation 5

$$\tau_1 = (R_{SW} + R_{AD}) \cdot \frac{C_P \cdot C_S}{C_P + C_S}$$

This relation can again be simplified considering C_S as an additional worst condition. In reality, transient is faster, but the A/D converter circuitry has been designed to be robust also in very worst case: the sampling time T_S is always much longer than the internal time constant.

Equation 6

$$\tau_1 < (R_{SW} + R_{AD}) \cdot C_S \ll T_S$$

The charge of C_{P1} and C_{P2} is redistributed on C_S , determining a new value of the voltage V_{A1} on the capacitance according to the following equation

Equation 7

$$V_{A1} \cdot (C_S + C_{P1} + C_{P2}) = V_A \cdot (C_{P1} + C_{P2})$$

A second charge transfer involves also C_F (that is typically bigger than the on-chip capacitance) through the resistance R_L : again considering the worst case in which C_{P2} and C_S were in parallel to C_{P1} (since the time constant in reality would be faster), the time constant is:

Equation 8

$$\tau_2 < R_L \cdot (C_S + C_{P1} + C_{P2})$$

In this case, the time constant depends on the external circuit: in particular imposing that the transient is completed well before the end of sampling time T_S , a constraints on R_L sizing is obtained:

Equation 9

$$8.5 \cdot \tau_2 = 8.5 \cdot R_L \cdot (C_S + C_{P1} + C_{P2}) < T_S$$

Of course, R_L shall be sized also according to the current limitation constraints, in combination with R_S (source impedance) and R_F (filter resistance). Being C_F definitively bigger than C_{P1} , C_{P2} and C_S , then the final voltage V_{A2} (at the end of the charge transfer transient) will be much higher than V_{A1} . The following equation must be respected (charge balance assuming now C_S already charged at V_{A1}):

Equation 10

$$V_{A2} \cdot (C_S + C_{P1} + C_{P2} + C_F) = V_A \cdot C_F + V_{A1} \cdot (C_{P1} + C_{P2} + C_S)$$

The two transients above are not influenced by the voltage source that, due to the presence of the $R_F C_F$ filter, is not able to provide the extra charge to compensate the voltage drop on C_S with respect to the ideal source V_A ; the time constant $R_F C_F$ of the filter is very high with respect to the sampling time (T_S). The filter is typically designed to act as anti-aliasing

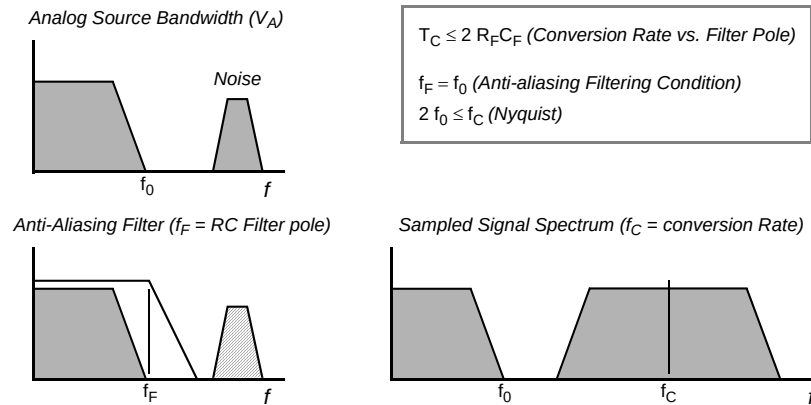


Figure 20. Spectral representation of input signal

Calling f_0 the bandwidth of the source signal (and as a consequence the cut-off frequency of the anti-aliasing filter, f_F), according to the Nyquist theorem the conversion rate f_C must be at least $2f_0$; it means that the constant time of the filter is greater than or at least equal to twice the conversion period (T_C). Again the conversion period T_C is longer than the sampling time T_S , which is just a portion of it, even when fixed channel continuous conversion mode is selected (fastest conversion rate at a specific channel): in conclusion it is evident that the time constant of the filter $R_F C_F$ is definitively much higher than the sampling time T_S , so the charge level on C_S cannot be modified by the analog signal source during the time in which the sampling switch is closed.

The considerations above lead to impose new constraints on the external circuit, to reduce the accuracy error due to the voltage drop on C_S ; from the two charge balance equations above, it is simple to derive [Equation 11](#) between the ideal and real sampled voltage on C_S :

Equation 11

$$\frac{V_{A2}}{V_A} = \frac{C_{P1} + C_{P2} + C_F}{C_{P1} + C_{P2} + C_F + C_S}$$

From this formula, in the worst case (when V_A is maximum, that is for instance 5 V), assuming to accept a maximum error of half a count, a constraint is evident on C_F value:

Equation 12 ADC_0 (10-bit)

$$C_F > 2048 \cdot C_S$$

Equation 13 ADC_1 (12-bit)

$$C_F > 8192 \cdot C_S$$

ADC electrical characteristics

Table 43. ADC input leakage current

Symbol	C	Parameter	Conditions	Value			Unit
				Min	Typ	Max	
I_{LK_G}	C C C P	Input leakage current	$T_A = -40\text{ }^{\circ}\text{C}$	—	1	—	nA
			$T_A = 25\text{ }^{\circ}\text{C}$	—	1	—	
			$T_A = 105\text{ }^{\circ}\text{C}$	—	8	200	
			$T_A = 125\text{ }^{\circ}\text{C}$	—	45	400	

Table 44. ADC conversion characteristics (10-bit ADC_0)

Symbol	C	Parameter	Conditions ⁽¹⁾	Value			Unit
				Min	Typ	Max	
V_{SS_ADC0}	S R	—	Voltage on VSS_HV_ADC0 (ADC_0 reference) pin with respect to ground (V_{SS_HV}) ⁽²⁾	—	—	0.1	V
V_{DD_ADC0}	S R	—	Voltage on VDD_HV_ADC0 pin (ADC_0 reference) with respect to ground (V_{SS_HV})	—	$V_{DD_HV_A} - 0.1$	$V_{DD_HV_A} + 0.1$	V
V_{AINx}	S R	—	Analog input voltage ⁽³⁾	—	$V_{SS_ADC0} - 0.1$	$V_{DD_ADC0} + 0.1$	V
f_{ADC0}	S R	—	ADC_0 analog frequency	—	6	$32 \pm 2\%$	MHz
t_{ADC0_PU}	S R	—	ADC_0 power up delay	—	—	1.5	μs
t_{ADC0_S}	C C	T	Sample time ⁽⁴⁾	$f_{ADC} = 32\text{ MHz}$	500	—	ns
t_{ADC0_C}	C C	P	Conversion time ^{(5),(6)}	$f_{ADC} = 32\text{ MHz}$	0.625	—	μs
				$f_{ADC} = 30\text{ MHz}$	0.700	—	
C_S	C C	D	ADC_0 input sampling capacitance	—	—	3	pF
C_{P1}	C C	D	ADC_0 input pin capacitance 1	—	—	3	pF
C_{P2}	C C	D	ADC_0 input pin capacitance 2	—	—	1	pF

Table 44. ADC conversion characteristics (10-bit ADC_0) (continued)

Symbol		C	Parameter	Conditions ⁽¹⁾		Value			Unit
						Min	Typ	Max	
C _{P3}	C C	D	ADC_0 input pin capacitance 3	—		—	—	1	pF
R _{SW1}	C C	D	Internal resistance of analog source	—		—	—	3	kΩ
R _{SW2}	C C	D	Internal resistance of analog source	—		—	—	2	kΩ
R _{AD}	C C	D	Internal resistance of analog source	—		—	—	2	kΩ
I _{INJ} ⁽⁷⁾	S R	—	Input current Injection	Current injection on one ADC_0 input, different from the converted one	V _{DD} = 3.3 V ± 10%	−5	—	5	mA
					V _{DD} = 5.0 V ± 10%	−5	—	5	
INL	C C	T	Absolute value for integral non-linearity	No overload		—	0.5	1.5	LSB
DNL	C C	T	Absolute differential non-linearity	No overload		—	0.5	1.0	LSB
OFS	C C	T	Absolute offset error	—		—	0.5	—	LSB
GNE	C C	T	Absolute gain error	—		—	0.6	—	LSB
TUEP	C C	P	Total unadjusted error ⁽⁸⁾ for precise channels, input only pins	Without current injection		−2	0.6	2	LSB
		With current injection		−3		3			
TUEX	C C	T	Total unadjusted error ⁽⁸⁾ for extended channel	Without current injection		−3	1	3	LSB
		With current injection		−4		4			

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = -40 to 125 °C, unless otherwise specified.
2. Analog and digital V_{SS_HV} must be common (to be tied together externally).
3. V_{AINx} may exceed V_{SS_ADC0} and V_{DD_ADC0} limits, remaining on absolute maximum ratings, but the results of the conversion will be clamped respectively to 0x000 or 0x3FF.
4. During the sample time the input capacitance C_S can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_{ADC0_S}. After the end of the sample time t_{ADC0_S}, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_{ADC0_S} depend on programming.
5. This parameter does not include the sample time t_{ADC0_S}, but only the time for determining the digital result and the time to load the result's register with the conversion result.
6. Refer to ADC conversion table for detailed calculations.

7. PB10 should not have any current injected. It can disturb accuracy on other ADC_0 pins.
8. Total Unadjusted Error: The maximum error that occurs without adjusting Offset and Gain errors. This error is a combination of Offset, Gain and Integral Linearity errors.

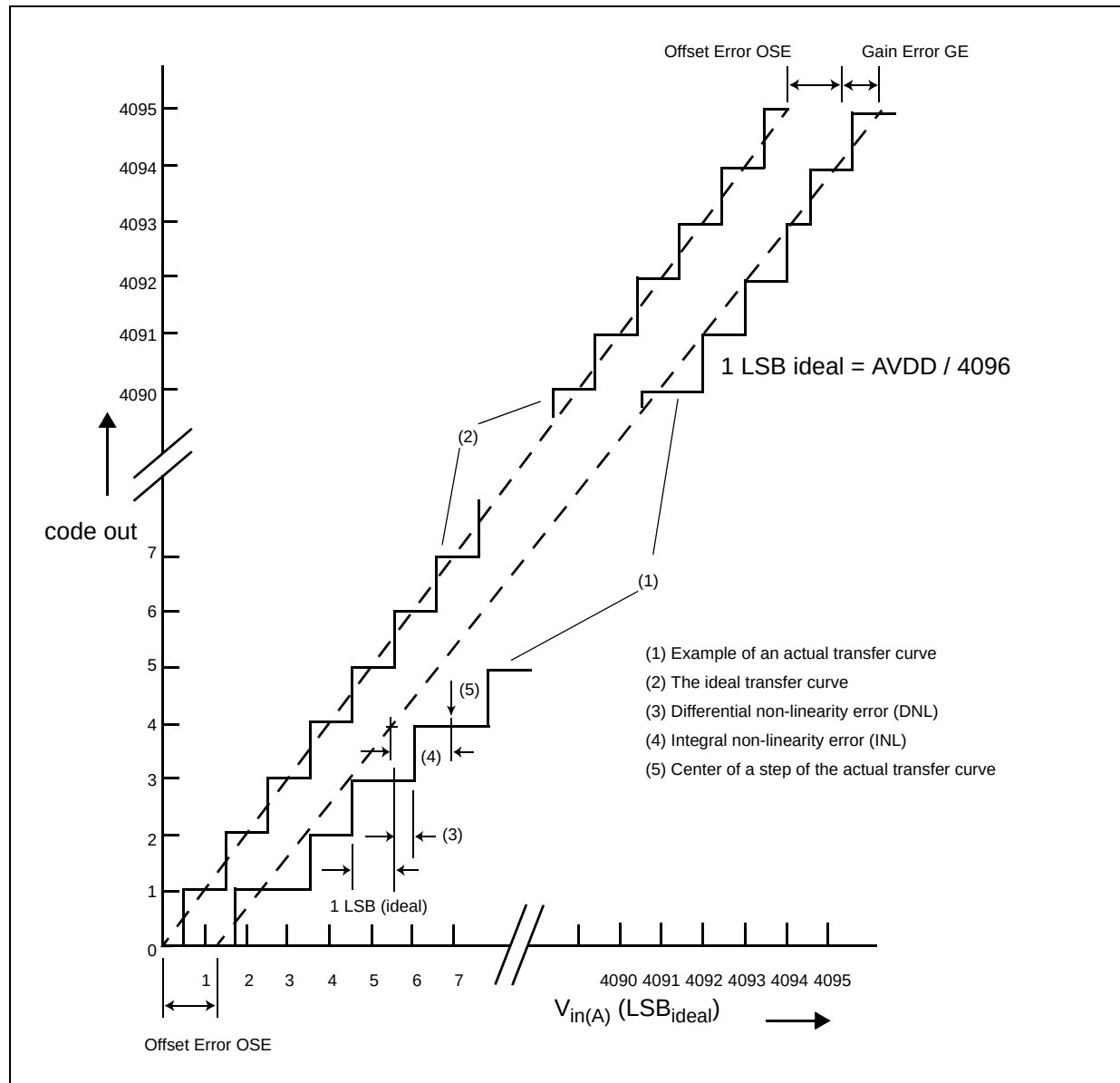


Figure 21. ADC_1 characteristic and error definitions

Table 45. Conversion characteristics (12-bit ADC_1)

Symbol		C	Parameter	Conditions ⁽¹⁾	Value			Unit
					Min	Typ	Max	
V_{SS_ADC1}	SR	—	Voltage on VSS_HV_ADC1 (ADC_1 reference) pin with respect to ground (V_{SS_HV}) ⁽²⁾	—	−0.1		0.1	V
$V_{DD_3_ADC1}$	SR	—	Voltage on VDD_HV_ADC1 pin (ADC_1 reference) with respect to ground (V_{SS_HV})	—	$V_{DD_HV_A} - 0.1$		$V_{DD_HV_A} + 0.1$	V
V_{AINx} ^{(3), (4)}	SR	—	Analog input voltage ⁽⁵⁾	—	$V_{SS_ADC1} - 0.1$		$V_{DD_ADC1} + 0.1$	V
f_{ADC1}	SR	—	ADC_1 analog frequency	—	8 + 2%		32 + 2%	MHz
t_{ADC1_PU}	SR	—	ADC_1 power up delay	—	1.5			μs
t_{ADC1_S}	CC	T	Sample time ⁽⁶⁾ VDD=5.0 V	—	440			ns
			Sample time ⁽⁶⁾ VDD=3.3 V	—	530			
t_{ADC1_C}	CC	P	Conversion time ^{(7), (8)} VDD=5.0 V	$f_{ADC1} = 32$ MHz	2			μs
			Conversion time ^{(7), (6)} VDD =5.0 V	$f_{ADC1} = 30$ MHz	2.1			
			Conversion time ^{(7), (6)} VDD=3.3 V	$f_{ADC1} = 20$ MHz	3			
			Conversion time ^{(7), (6)} VDD =3.3 V	$f_{ADC1} = 15$ MHz	3.01			
C_S	CC	D	ADC_1 input sampling capacitance	—	5			pF
C_{P1}	CC	D	ADC_1 input pin capacitance 1	—	3			pF
C_{P2}	CC	D	ADC_1 input pin capacitance 2	—	1			pF

Table 45. Conversion characteristics (12-bit ADC_1) (continued)

Symbol		C	Parameter	Conditions ⁽¹⁾		Value			Unit
						Min	Typ	Max	
C _{P3}	CC	D	ADC_1 input pin capacitance 3	—		1.5			pF
R _{SW1}	CC	D	Internal resistance of analog source	—				1	kΩ
R _{SW2}	CC	D	Internal resistance of analog source	—				2	kΩ
R _{AD}	CC	D	Internal resistance of analog source	—				0.3	kΩ
I _{INJ}	SR	—	Input current Injection	Current injection on one ADC_1 input, different from the converted one	V _{DD} = 3.3 V ± 10%	−5	—	5	mA
					V _{DD} = 5.0 V ± 10%	−5	—	5	
INLP	CC	T	Absolute Integral non-linearity- Precise channels	No overload			1	3	LSB
INLS	CC	T	Absolute Integral non-linearity- Standard channels	No overload			1.5	5	LSB
DNL	CC	T	Absolute Differential non-linearity	No overload			0.5	1	LSB
OFS	CC	T	Absolute Offset error	—			2		LSB
GNE	CC	T	Absolute Gain error	—			2		LSB
TUEP ⁽⁹⁾	CC	P	Total Unadjusted Error for precise channels, input only pins	Without current injection		−6		6	LSB
		T		With current injection		−8		8	LSB
TUES ⁽⁹⁾	CC	T	Total Unadjusted Error for standard channel	Without current injection		−10		10	LSB
		T		With current injection		−12		12	LSB

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = −40 to 125 °C, unless otherwise specified.

2. Analog and digital V_{SS_HV} must be common (to be tied together externally).

3. PA3, PA7, PA10, PA11 and PE12 ADC_1 channels are coming from $V_{DD_HV_B}$ domain hence $V_{DD_HV_ADC1}$ should be within ± 100 mV of $V_{DD_HV_B}$ when these channels are used for ADC_1.
4. $V_{DD_HV_ADC1}$ can operate at 5V condition while $V_{DD_HV_B}$ can operate at 3.3V provided that ADC_1 channels coming from $V_{DD_HV_B}$ domain are limited in max swing as $V_{DD_HV_B}$.
5. V_{AINx} may exceed V_{SS_ADC1} and V_{DD_ADC1} limits, remaining on absolute maximum ratings, but the results of the conversion will be clamped respectively to 0x000 or 0xFFFF.
6. During the sample time the input capacitance C_S can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_{ADC1_S} . After the end of the sample time t_{ADC1_S} , changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_{ADC1_S} depend on programming.
7. Conversion time = Bit evaluation time + Sampling time + 1 Clock cycle delay.
8. Refer to ADC conversion table for detailed calculations.
9. Total Unadjusted Error: The maximum error that occurs without adjusting Offset and Gain errors. This error is a combination of Offset, Gain and Integral Linearity errors.

3.18 Fast Ethernet Controller

MII signals use CMOS signal levels compatible with devices operating at 3.3 V. Signals are not TTL compatible. They follow the CMOS electrical characteristics.

3.18.1 MII Receive Signal Timing (RXD[3:0], RX_DV, RX_ER, and RX_CLK)

The receiver functions correctly up to a RX_CLK maximum frequency of 25 MHz +1%. There is no minimum frequency requirement. In addition, the system clock frequency must exceed four times the RX_CLK frequency in 2:1 mode and two times the RX_CLK frequency in 1:1 mode.

Table 46. MII Receive Signal Timing

Spec	Characteristic	Min	Max	Unit
M1	RXD[3:0], RX_DV, RX_ER to RX_CLK setup	5	—	ns
M2	RX_CLK to RXD[3:0], RX_DV, RX_ER hold	5	—	ns
M3	RX_CLK pulse width high	35%	65%	RX_CLK period
M4	RX_CLK pulse width low	35%	65%	RX_CLK period

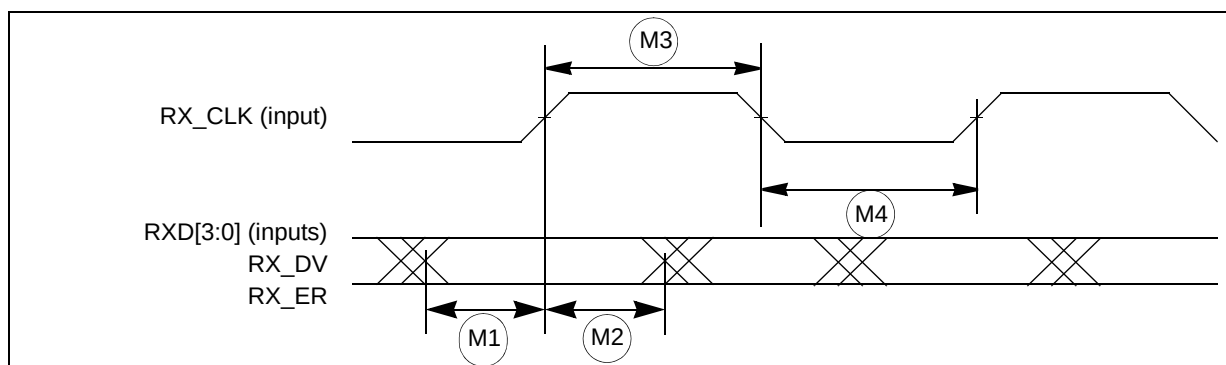


Figure 22. MII receive signal timing diagram

3.18.2 MII Transmit Signal Timing (TXD[3:0], TX_EN, TX_ER, TX_CLK)

The transmitter functions correctly up to a TX_CLK maximum frequency of 25 MHz +1%. There is no minimum frequency requirement. In addition, the system clock frequency must exceed four times the TX_CLK frequency in 2:1 mode and two times the TX_CLK frequency in 1:1 mode.

The transmit outputs (TXD[3:0], TX_EN, TX_ER) can be programmed to transition from either the rising or falling edge of TX_CLK, and the timing is the same in either case. This options allows the use of non-compliant MII PHYs.

Refer to the Fast Ethernet Controller (FEC) chapter of the SPC564B74 and SPC56EC74 Reference Manual for details of this option and how to enable it.

Table 47. MII transmit signal timing⁽¹⁾

Spec	Characteristic	Min	Max	Unit
M5	TX_CLK to TXD[3:0], TX_EN, TX_ER invalid	5	—	ns
M6	TX_CLK to TXD[3:0], TX_EN, TX_ER valid	—	25	ns
M7	TX_CLK pulse width high	35%	65%	TX_CLK period
M8	TX_CLK pulse width low	35%	65%	TX_CLK period

1. Output pads configured with SRE = 0b11.

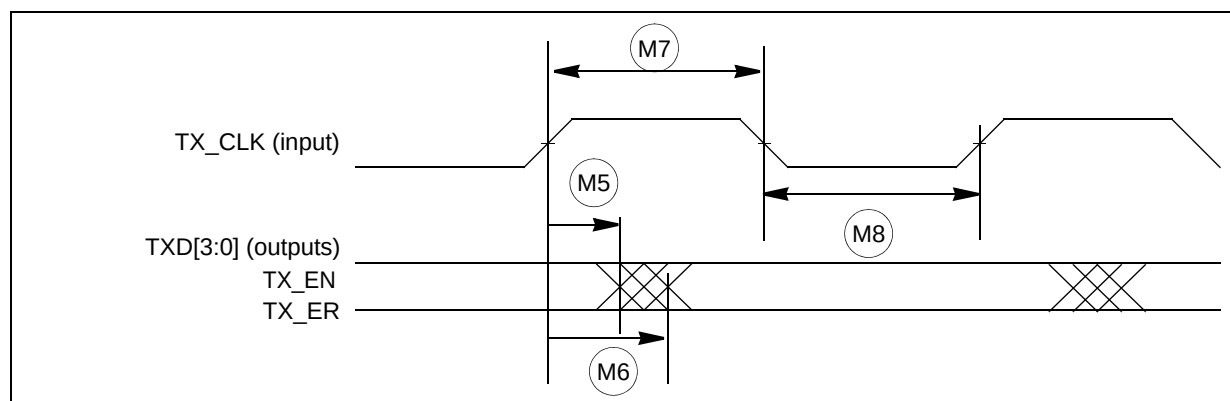


Figure 23. MII transmit signal timing diagram

3.18.3 MII Async Inputs Signal Timing (CRS and COL)

Table 48. MII Async Inputs Signal Timing⁽¹⁾

Spec	Characteristic	Min	Max	Unit
M9	CRS, COL minimum pulse width	1.5	—	TX_CLK period

1. Output pads configured with SRE = 0b11.

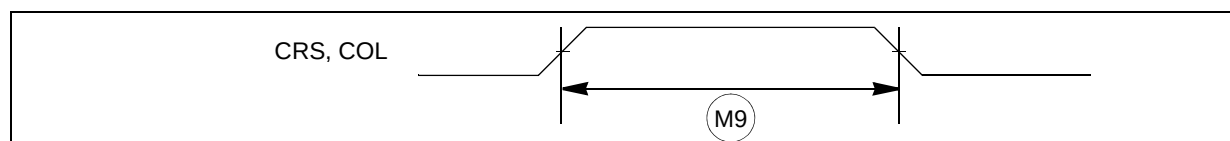


Figure 24. MII async inputs timing diagram

3.18.4 MII Serial Management Channel Timing (MDIO and MDC)

The FEC functions correctly with a maximum MDC frequency of 2.5 MHz.

Table 49. MII serial management channel timing⁽¹⁾

Spec	Characteristic	Min	Max	Unit
M10	MDC falling edge to MDIO output invalid (minimum propagation delay)	0	—	ns
M11	MDC falling edge to MDIO output valid (max prop delay)	—	25	ns
M12	MDIO (input) to MDC rising edge setup	28	—	ns
M13	MDIO (input) to MDC rising edge hold	0	—	ns
M14	MDC pulse width high	40%	60%	MDC period
M15	MDC pulse width low	40%	60%	MDC period

1. Output pads configured with SRE = 0b11.

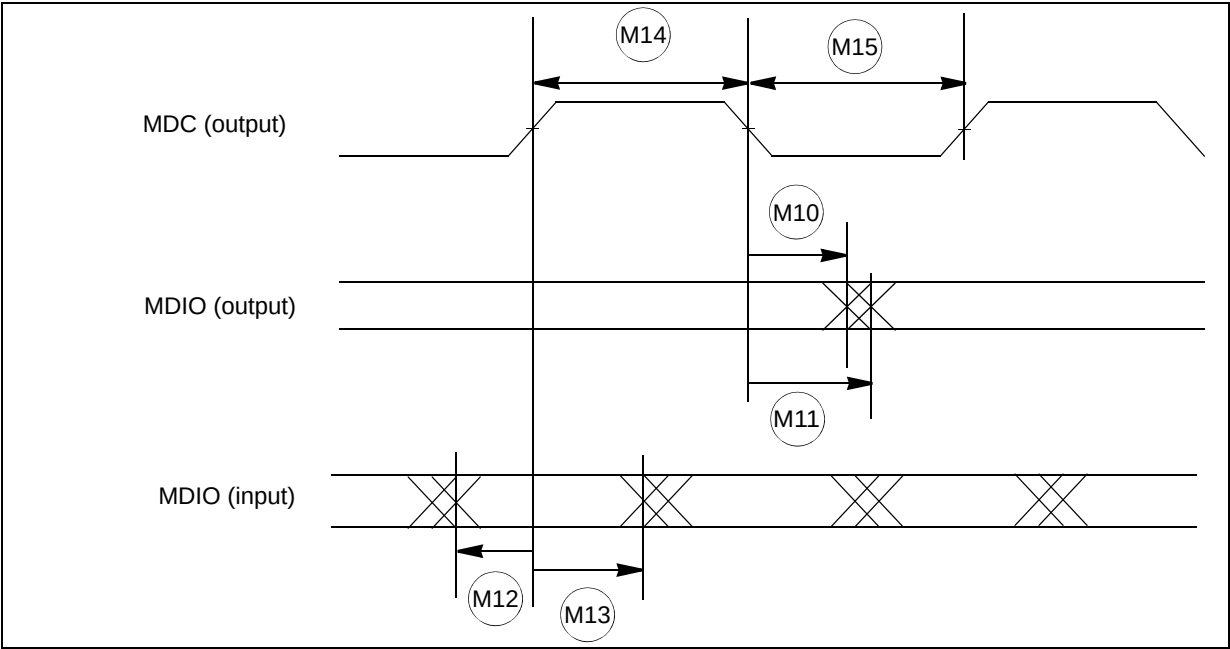


Figure 25. MII serial management channel timing diagram

3.19 On-chip peripherals

3.19.1 Current consumption

Table 50. On-chip peripherals current consumption⁽¹⁾

Symbol	C	Parameter	Conditions	Value ⁽²⁾	Unit
				Typ	
$I_{DD_HV_A(CAN)}$	CC	D	CAN (FlexCAN) supply current on $V_{DD_HV_A}$ 500 Kbps 125 Kbps	Total (static + dynamic) consumption: FlexCAN in loop-back mode XTAL@8 MHz used as CAN engine clock source Message sending period is 580 μ s	$7.652 \times f_{periph} + 84.73$ $8.0743 \times f_{periph} + 26.757$
$I_{DD_HV_A(eMIOS)}$	CC	D	eMIOS supply current on $V_{DD_HV_A}$	Static consumption: eMIOS channel OFF Global prescaler enabled	$28.7 \times f_{periph}$
				Dynamic consumption: It does not change varying the frequency (0.003 mA)	3
$I_{DD_HV_A(SCI)}$	CC	D	SCI (LINFlex) supply current on $V_{DD_HV_A}$	Total (static + dynamic) consumption: LIN mode Baudrate: 20 Kbps	$4.7804 \times f_{periph} + 30.946$
$I_{DD_HV_A(SPI)}$	CC	D	SPI (DSPI) supply current on $V_{DD_HV_A}$	Ballast static consumption (only clocked)	1
				Ballast dynamic consumption (continuous communication): Baudrate: 2 Mbit Transmission every 8 μ s Frame: 16 bits	$16.3 \times f_{periph}$
$I_{DD_HV_A(ADC)}$	CC	D	ADC supply current on $V_{DD_HV_A}$	$V_{DD} = 5.5$ V Ballast static consumption (no conversion)	$0.0409 \times f_{periph}$
				$V_{DD} = 5.5$ V Ballast dynamic consumption (continuous conversion)	$0.0049 \times f_{periph}$

Table 50. On-chip peripherals current consumption⁽¹⁾

Symbol		C	Parameter	Conditions		Value ⁽²⁾	Unit
						Typ	
IDD_HV_ADC0	CC	D	ADC_0 supply current on V _{DD_HV_ADC0}	V _{DD} = 5.5 V	Analog static consumption (no conversion)	200	μA
					Analog dynamic consumption (continuous conversion)	4	mA
IDD_HV_ADC1	CC	D	ADC_1 supply current on V _{DD_HV_ADC1}	V _{DD} = 5.5 V	Analog static consumption (no conversion)	300 × f _{periph}	μA
				V _{DD} = 5.5 V	Analog dynamic consumption (continuous conversion)	6	mA
I _{DD_HV(FLASH)}	CC	D	CFlash + DFlash supply current on V _{DD_HV_ADC}	V _{DD} = 5.5 V	—	13.25	mA
I _{DD_HV(PLL)}	CC	D	PLL supply current on V _{DD_HV}	V _{DD} = 5.5 V	—	0.0031 × f _{periph}	

1. Operating conditions: T_A = 25 °C, f_{periph} = 8 MHz to 120 MHz.

2. f_{periph} is in absolute value.

3.19.2 DSPI characteristics

Table 51. DSPI timing

Spec	Characteristic	Symbol			Unit
			Min	Max	
1	DSPI Cycle Time	t _{SCK}	Refer note ⁽¹⁾	—	ns
—	Internal delay between pad associated to SCK and pad associated to CSn in master mode for CSn1->0	Δt _{CSC}	—	115	ns
—	Internal delay between pad associated to SCK and pad associated to CSn in master mode for CSn1->1	Δt _{ASC}	15	—	ns
2	CS to SCK Delay ⁽²⁾	t _{CSC}	7	—	ns
3	After SCK Delay ⁽³⁾	t _{ASC}	15	—	ns
4	SCK Duty Cycle	t _{SDC}	0.4 × t _{SCK}	0.6 × t _{SCK}	ns

Table 51. DSPI timing (continued)

Spec	Characteristic	Symbol			Unit
			Min	Max	
—	Slave Setup Time ($\overline{SS}$ active to SCK setup time)	t_{SUSS}	5	—	ns
—	Slave Hold Time ($\overline{SS}$ active to SCK hold time)	t_{HSS}	10	—	ns
5	Slave Access Time ($\overline{SS}$ active to SOUT valid) ⁽⁴⁾	t_A	—	42	ns
6	Slave SOUT Disable Time ($\overline{SS}$ inactive to SOUT High-Z or invalid)	t_{DIS}	—	25	ns
7	CSx to $\overline{PCSS}$ time	t_{PCSC}	0	—	ns
8	$\overline{PCSS}$ to PCSx time	t_{PASC}	0	—	ns
9	Data Setup Time for Inputs Master (MTFE = 0)	t_{SUI}	36	—	ns
	Slave		5	—	ns
	Master (MTFE = 1, CPHA = 0) ⁽⁵⁾		36	—	ns
	Master (MTFE = 1, CPHA = 1)		36	—	ns
10	Data Hold Time for Inputs Master (MTFE = 0)	t_{HI}	0	—	ns
	Slave		4	—	ns
	Master (MTFE = 1, CPHA = 0) ⁽⁵⁾		0	—	ns
	Master (MTFE = 1, CPHA = 1)		0	—	ns
11	Data Valid (after SCK edge) Master (MTFE = 0)	t_{SUO}	—	12	ns
	Slave		—	37	ns
	Master (MTFE = 1, CPHA = 0)		—	12	ns
	Master (MTFE = 1, CPHA = 1)		—	12	ns
12	Data Hold Time for Outputs Master (MTFE = 0)	t_{HO}	0 ⁽⁶⁾	—	ns
	Slave		9.5	—	ns
	Master (MTFE = 1, CPHA = 0)		0 ⁽⁷⁾	—	ns
	Master (MTFE = 1, CPHA = 1)		0 ⁽⁸⁾	—	ns

1. This value of this parameter is dependent upon the external device delays and the other parameters mentioned in this table.
2. The maximum value is programmable in DSPI_CTARn [PSSCK] and DSPI_CTARn [CSSCK]. For SPC564B74 and SPC56EC74, the spec value of t_{CSC} will be attained only if $T_{DSPI} \times PSSCK \times CSSCK > \Delta t_{CSC}$.
3. The maximum value is programmable in DSPI_CTARn [PASC] and DSPI_CTARn [ASC]. For SPC564B74 and SPC56EC74, the spec value of t_{ASC} will be attained only if $T_{DSPI} \times PASC \times ASC > \Delta t_{ASC}$.
4. The parameter value is obtained from t_{SUSS} and t_{SUO} for slave.
5. This number is calculated assuming the SMPL_PT bitfield in DSPI_MCR is set to 0b00.
6. For DSPI1, the Data Hold Time for Outputs in Master (MTFE = 0) is –2 ns.
7. For DSPI1, the Data Hold Time for Outputs in Master (MTFE = 1, CPHA = 0) is –2 n.
8. For DSPI1, the Data Hold Time for Outputs in Master (MTFE = 1, CPHA = 1) is –2 ns.

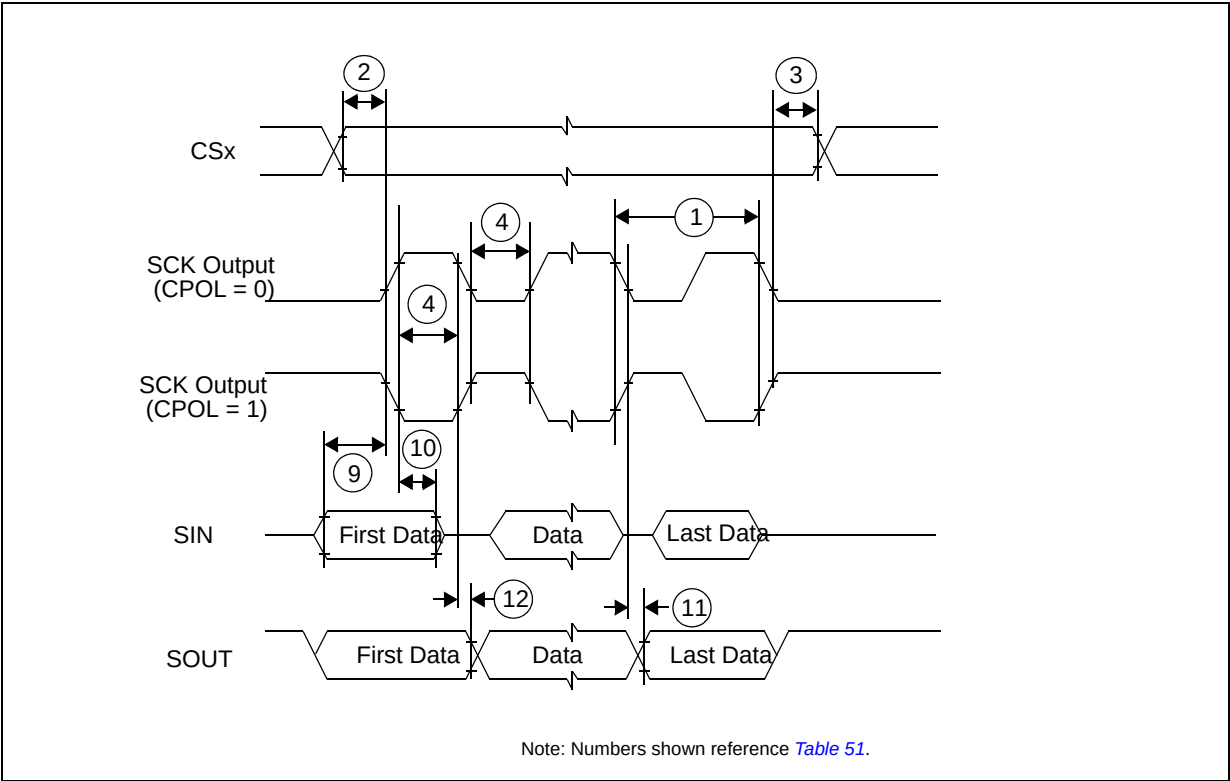


Figure 26. DSPI classic SPI timing-master, CPHA = 0

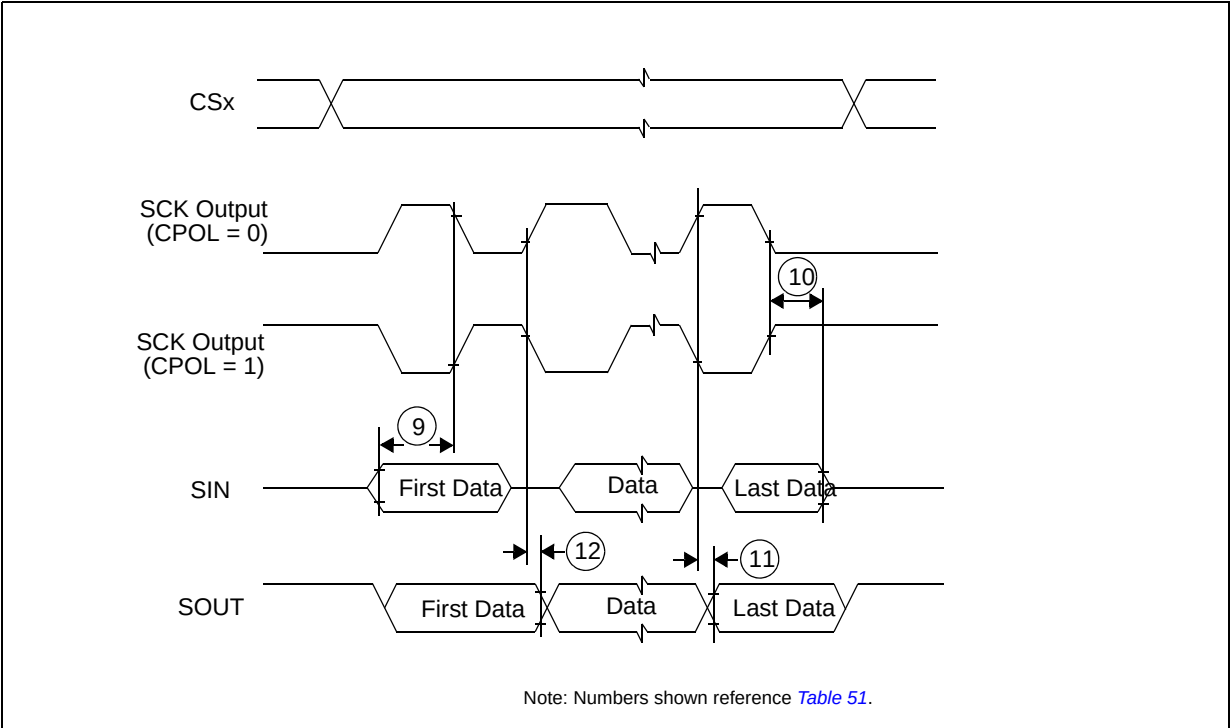


Figure 27. DSPI classic SPI timing-master, CPHA = 1

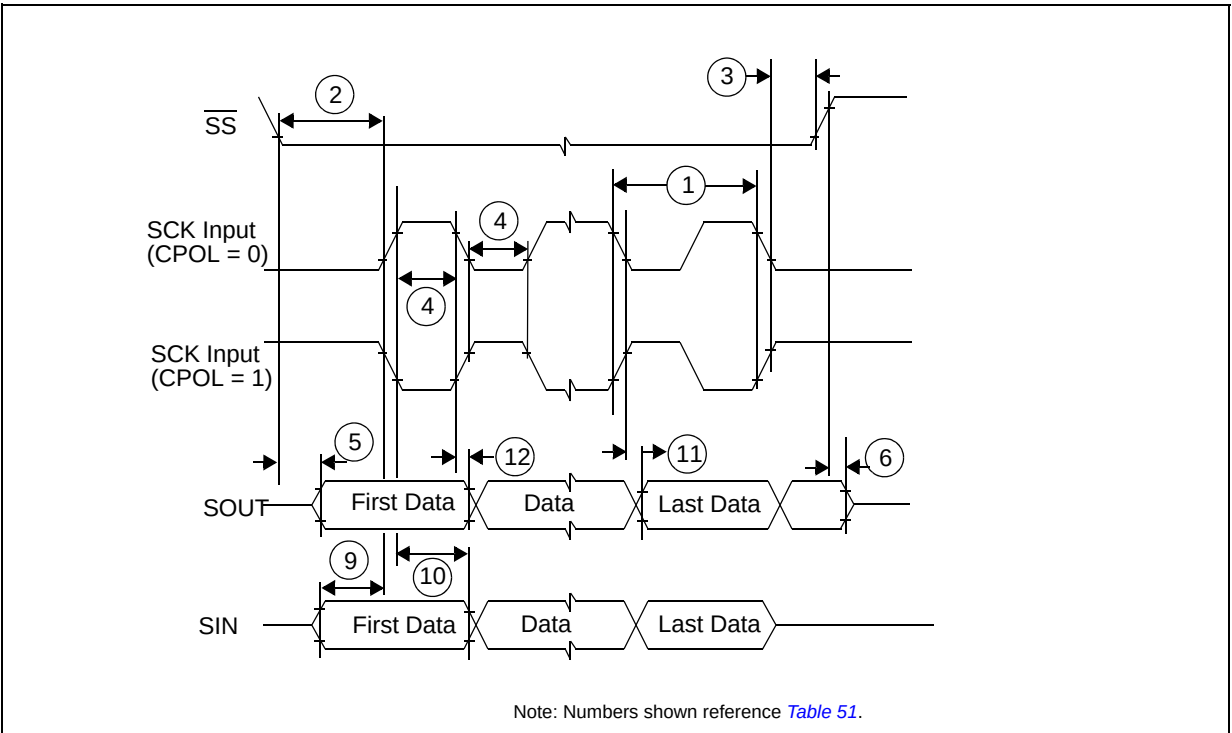


Figure 28. DSPI classic SPI timing–slave, CPHA = 0

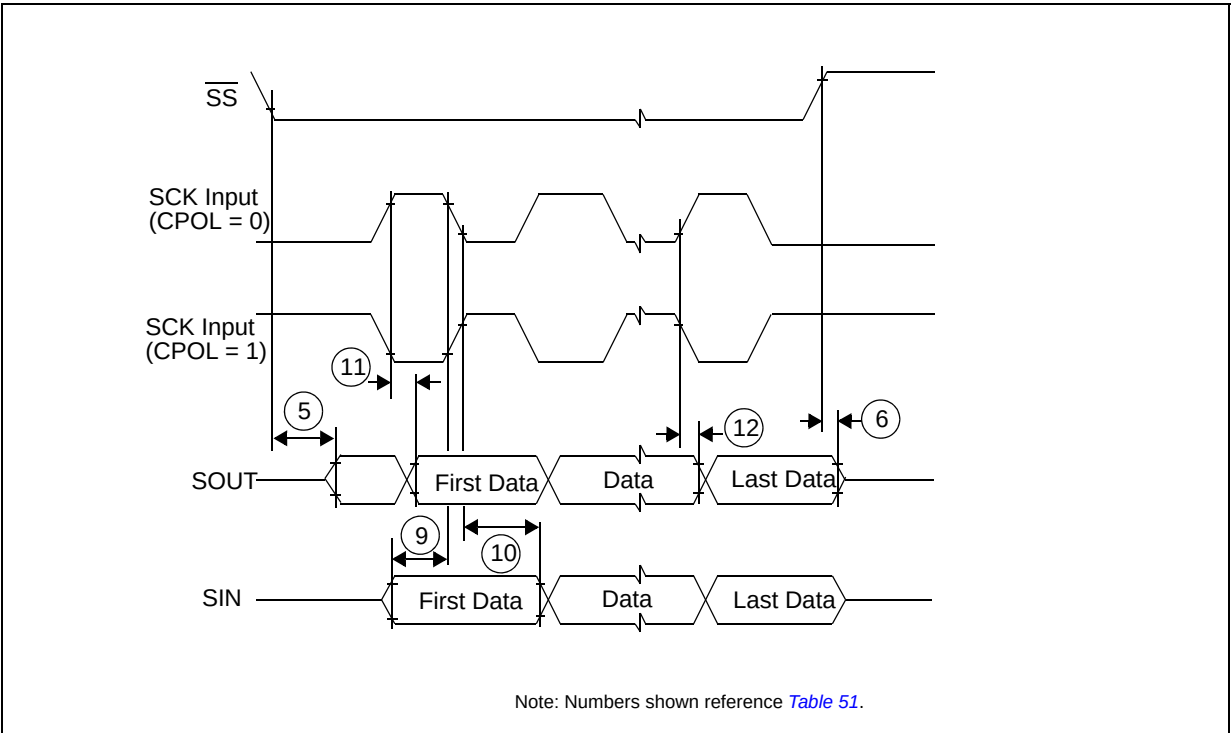


Figure 29. DSPI classic SPI timing–slave, CPHA = 1

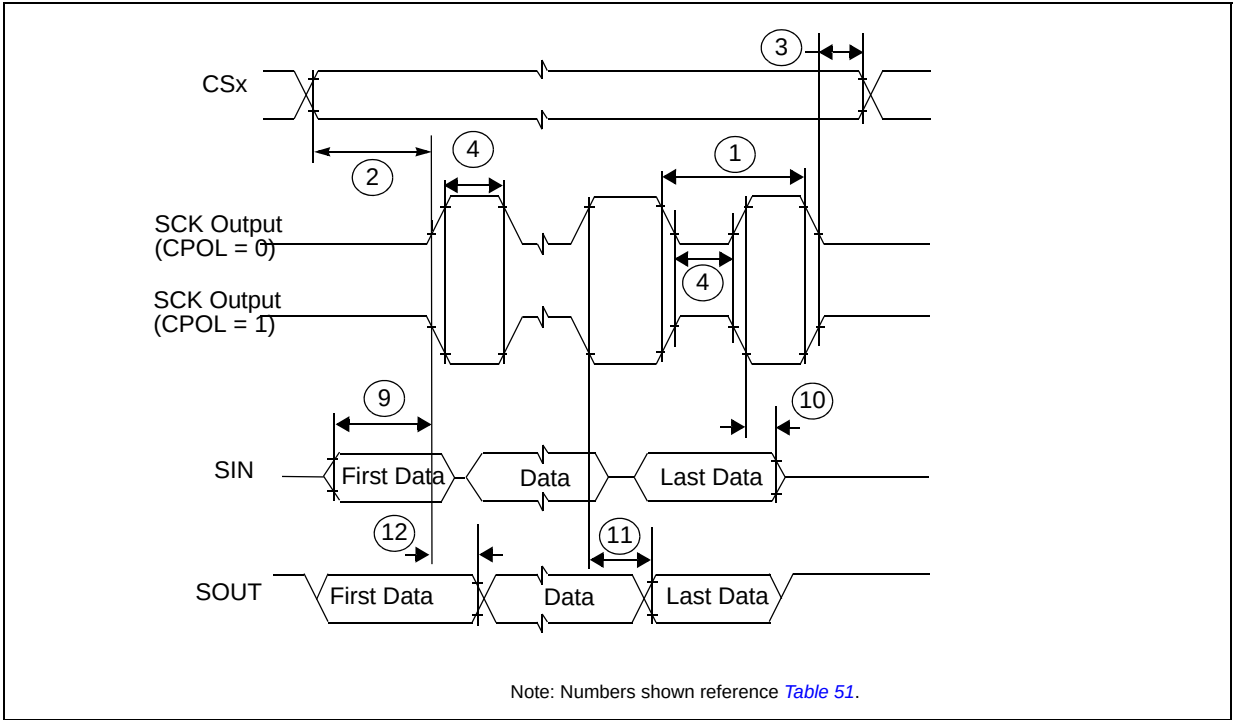


Figure 30. DSPI modified transfer format timing-master, CPHA = 0

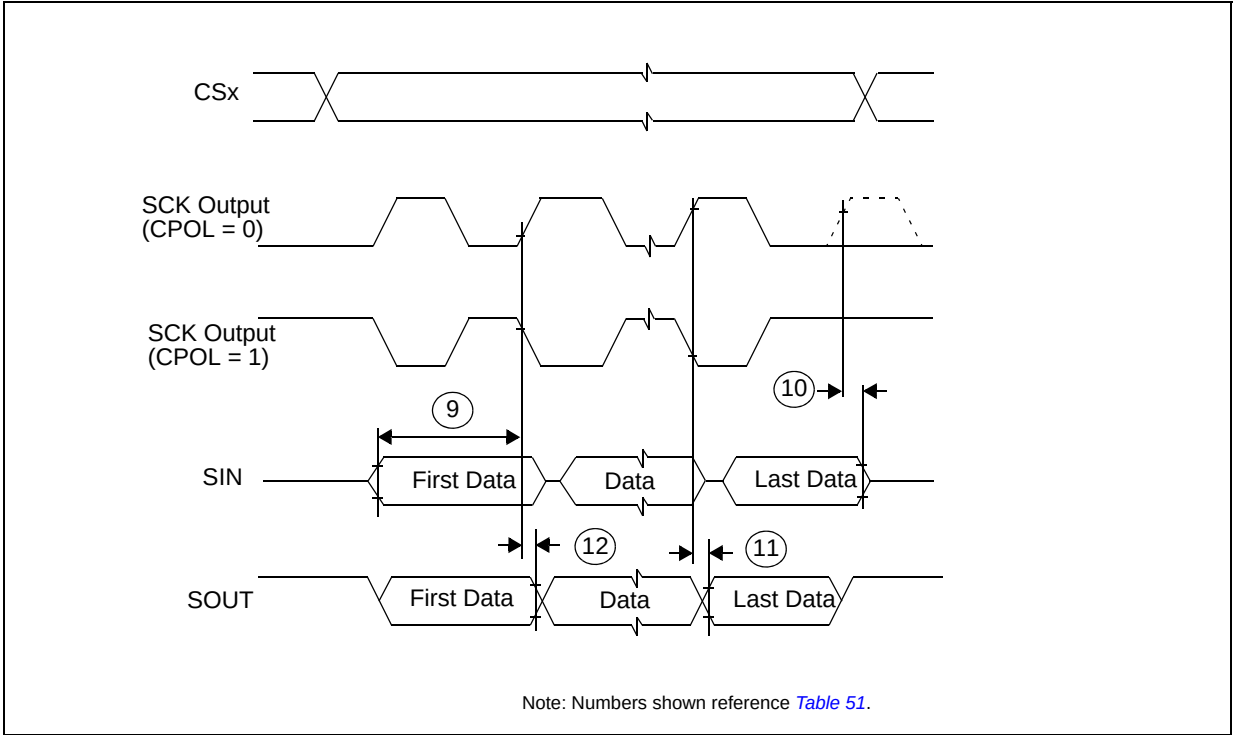


Figure 31. DSPI modified transfer format timing-master, CPHA = 1

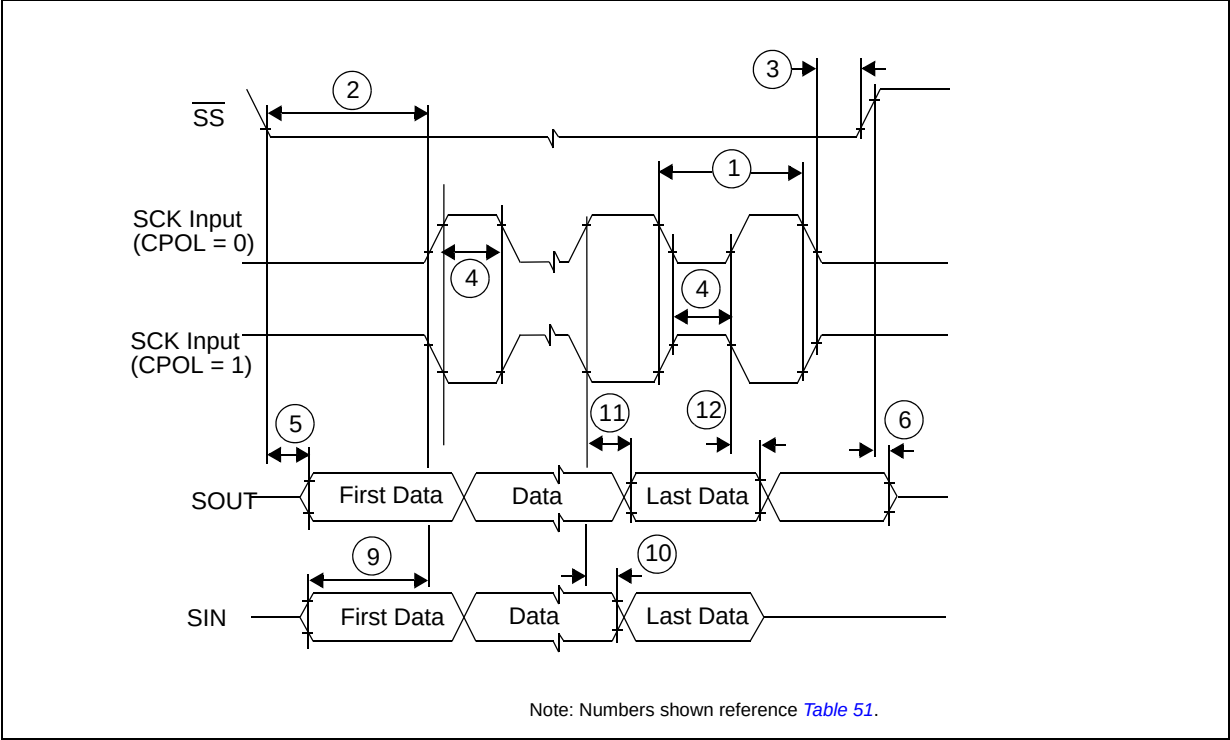


Figure 32. DSPI modified transfer format timing–slave, CPHA = 0

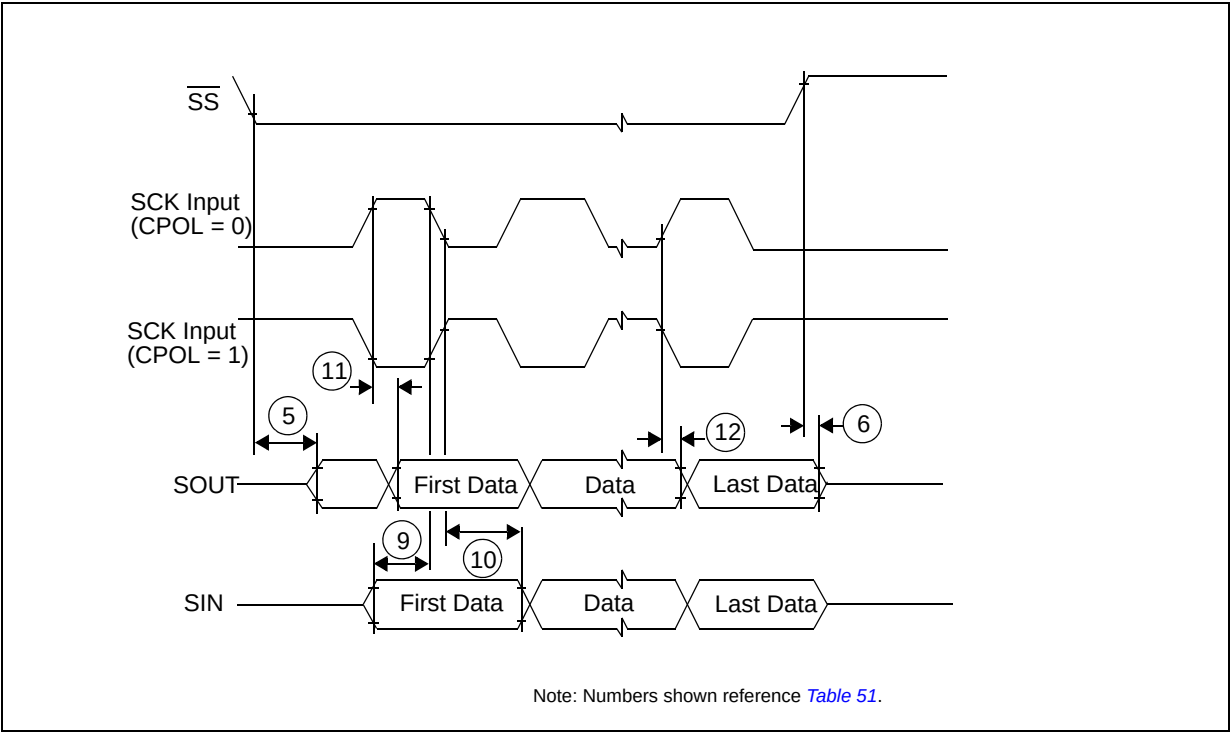
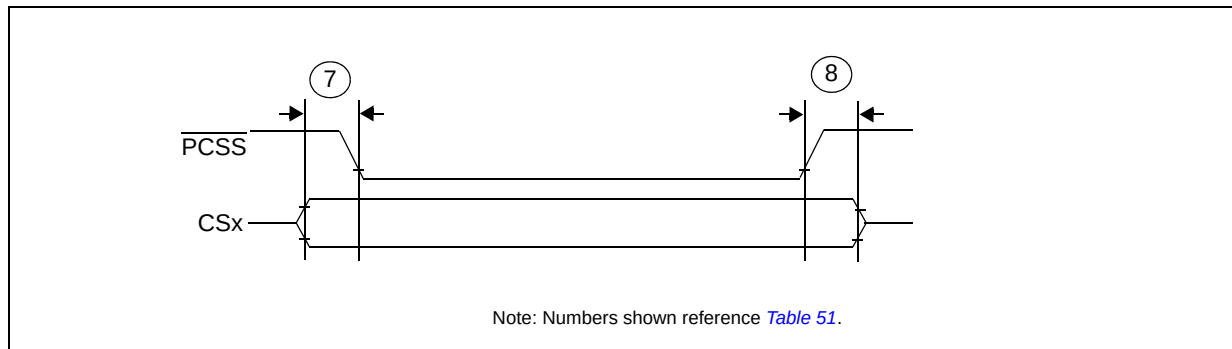


Figure 33. DSPI modified transfer format timing–slave, CPHA = 1

Figure 34. DSPI PCS strobe ($\overline{\text{PCSS}}$) timing

3.19.3 Nexus characteristics

Table 52. Nexus debug port timing⁽¹⁾

Spec	Characteristic	Symbol	Min	Max	Unit
1	MCKO Cycle Time ⁽²⁾	t_{MCCYC}	16.3	—	ns
2	MCKO Duty Cycle	t_{MDC}	40	60	%
3	MCKO Low to MDO, $\overline{\text{MSEO}}$, $\overline{\text{EVT0}}$ Data Valid ⁽³⁾	t_{MDOV}	-0.1	0.25	t_{MCCYC}
4	$\overline{\text{EVTI}}$ Pulse Width	t_{EVTIPW}	4.0	—	t_{TCCYC}
5	$\overline{\text{EVT0}}$ Pulse Width	t_{EVTOPW}	1	—	t_{MCCYC}
6	TCK Cycle Time ⁽⁴⁾	t_{TCCYC}	40	—	ns
7	TCK Duty Cycle	t_{TDC}	40	60	%
8	TDI, TMS Data Setup Time	$t_{\text{NTDIS}}, t_{\text{NTMSS}}$	8	—	ns
9	TDI, TMS Data Hold Time	$t_{\text{NTDIH}}, t_{\text{NTMSH}}$	5	—	ns
10	TCK Low to TDO Data Valid	t_{JOV}	0	25	ns

1. JTAG specifications in this table apply when used for debug functionality. All Nexus timing relative to MCKO is measured from 50% of MCKO and 50% of the respective signal. Nexus timing specified at $V_{\text{DDE}} = 4.0 - 5.5 \text{ V}$, $T_{\text{A}} = T_{\text{L}}$ to T_{H} , and $C_{\text{L}} = 30 \text{ pF}$ with $\text{SRC} = 0b11$.
2. MCKO can run up to 1/2 of full system frequency. It can also run at system frequency when it is <60 MHz.
3. MDO, $\overline{\text{MSEO}}$, and $\overline{\text{EVT0}}$ data is held valid until next MCKO low cycle.
4. The system clock frequency needs to be three times faster than the TCK frequency.

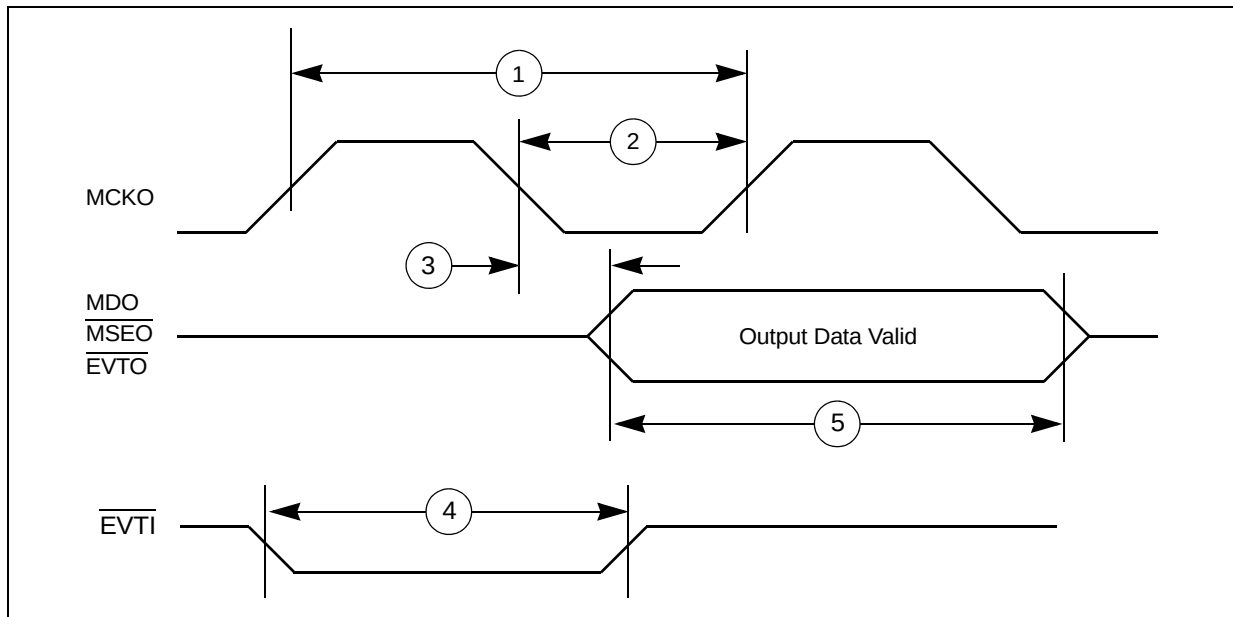


Figure 35. Nexus output timing

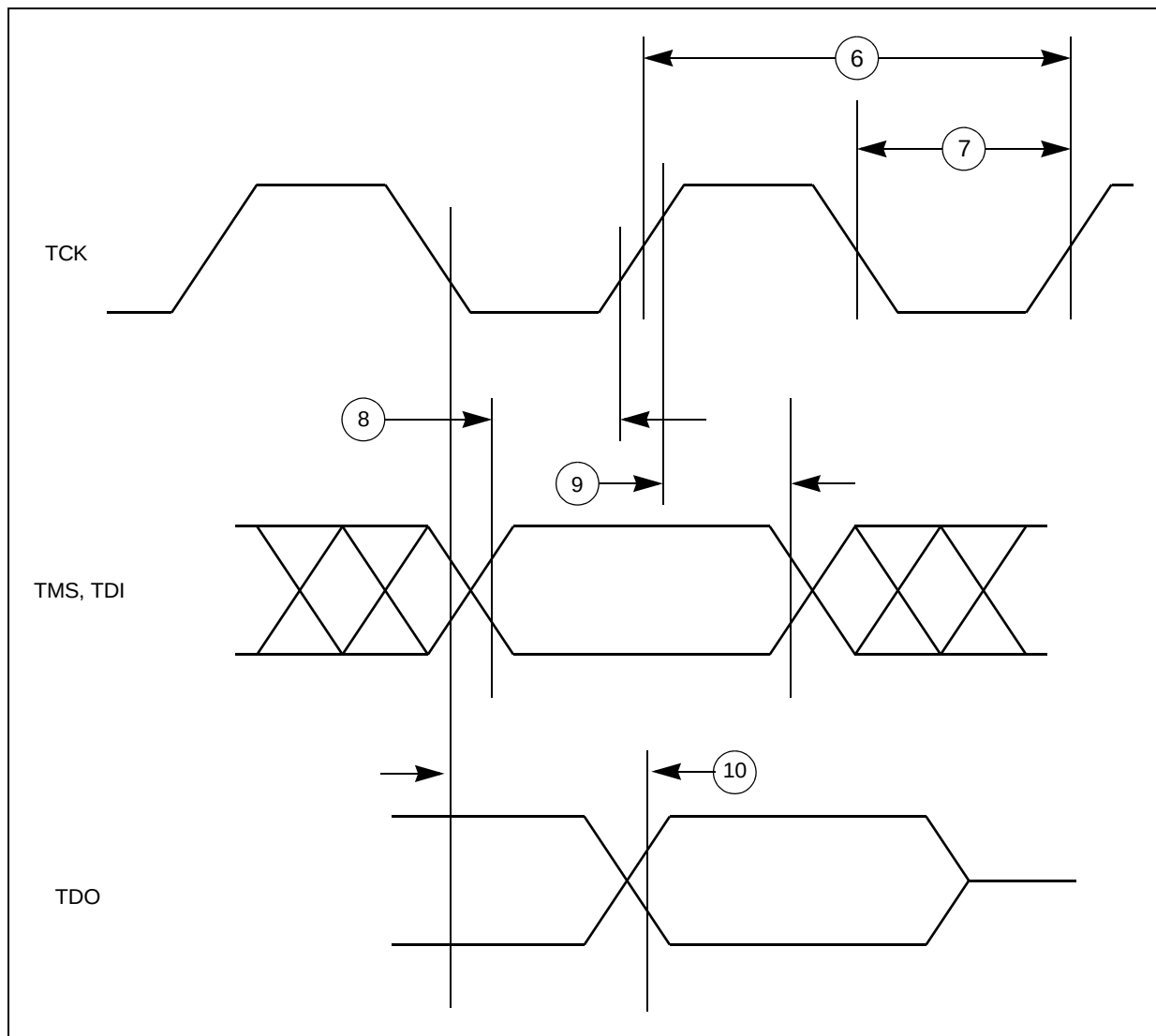


Figure 36. Nexus TDI, TMS, TDO timing

3.19.4 JTAG characteristics

Table 53. JTAG characteristics

No.	Symbol	C	Parameter	Value			Unit
				Min	Typ	Max	
1	t_{JCYC}	CC	D	TCK cycle time	64	—	ns
2	t_{TDIS}	CC	D	TDI setup time	10	—	ns
3	t_{TDIH}	CC	D	TDI hold time	5	—	ns
4	t_{TMSS}	CC	D	TMS setup time	10	—	ns
5	t_{TMSH}	CC	D	TMS hold time	5	—	ns

Table 53. JTAG characteristics (continued)

No.	Symbol		C	Parameter	Value			Unit
					Min	Typ	Max	
6	t _{TDOV}	CC	D	TCK low to TDO valid	—	—	33	ns
7	t _{TDOI}	CC	D	TCK low to TDO invalid	6	—	—	ns
—	t _{TDC}	CC	D	TCK Duty Cycle	40	—	60	%
—	t _{TCKRISE}	CC	D	TCK Rise and Fall Times	—	—	3	ns

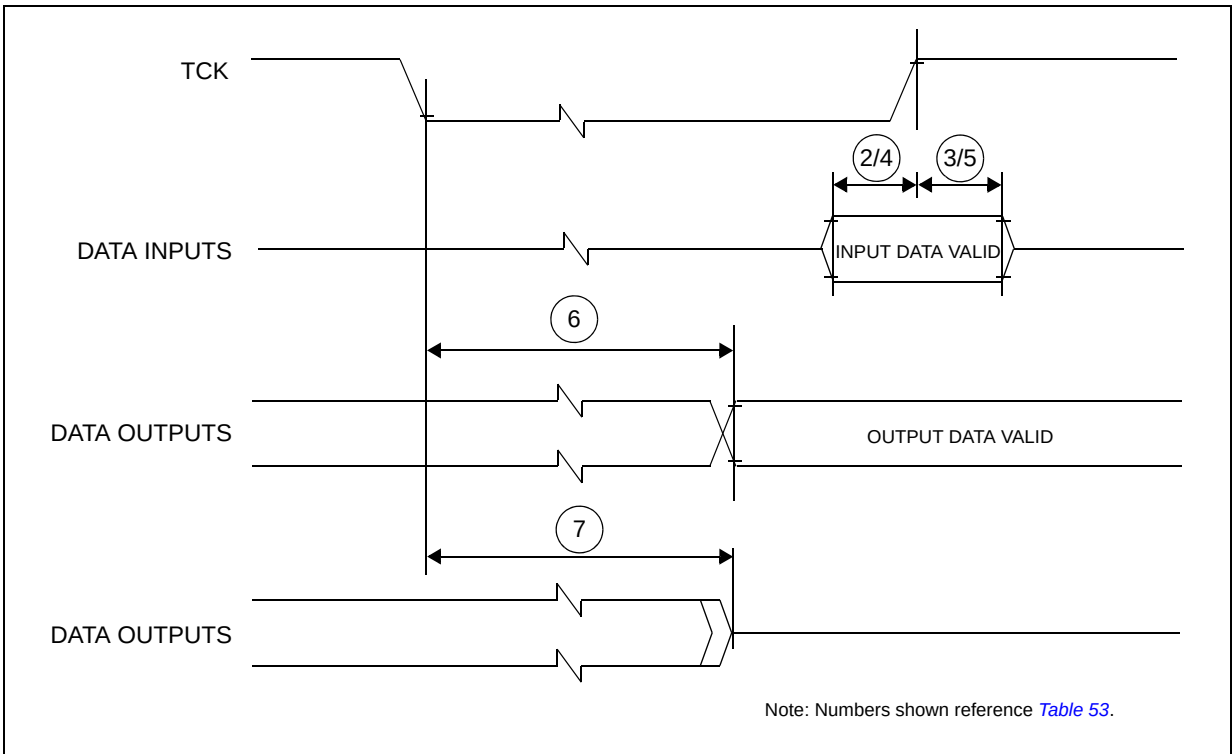


Figure 37. Timing diagram - JTAG boundary scan

4 Package characteristics

4.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.2 Package mechanical data

4.2.1 LQFP176 package mechanical drawing

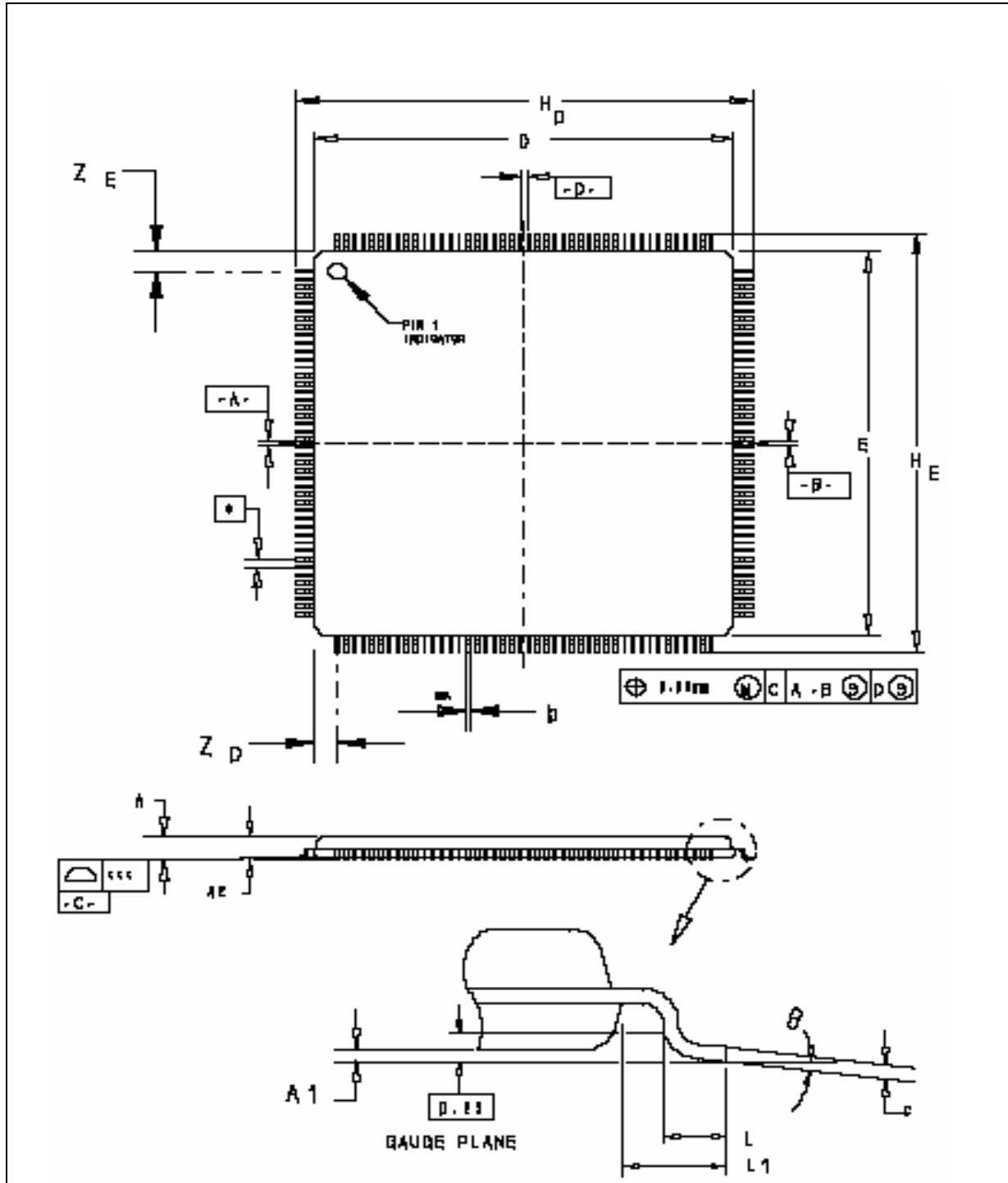


Figure 38. LQFP176 package mechanical drawing

Table 54. LQFP176 mechanical data⁽¹⁾

Symbol	mm			inches ⁽²⁾		
	Min	Typ	Max	Min	Typ	Max
A	1.400		1.600			0.063
A1	0.050		0.150	0.002		
A2	1.350		1.450	0.053		0.057
b	0.170		0.270	0.007		0.011
C	0.090		0.200	0.004		0.008
D	23.900		24.100	0.941		0.949
E	23.900		24.100	0.941		0.949
e		0.500			0.020	
HD	25.900		26.100	1.020		1.028
HE	25.900		26.100	1.020		1.028
L ⁽³⁾	0.450		0.750	0.018		0.030
L1		1.000			0.039	
ZD		1.250			0.049	
ZE		1.250			0.049	
q	0 °		7 °	0 °		7 °
Tolerance	mm			inches		
ccc	0.080			0.0031		

1. Controlling dimension: millimeter

2. Values in inches are converted from mm and rounded to 4 decimal digits.

3. L dimension is measured at gauge plane at 0.25 mm above the seating plane

4.2.2 LQFP208 package mechanical drawing

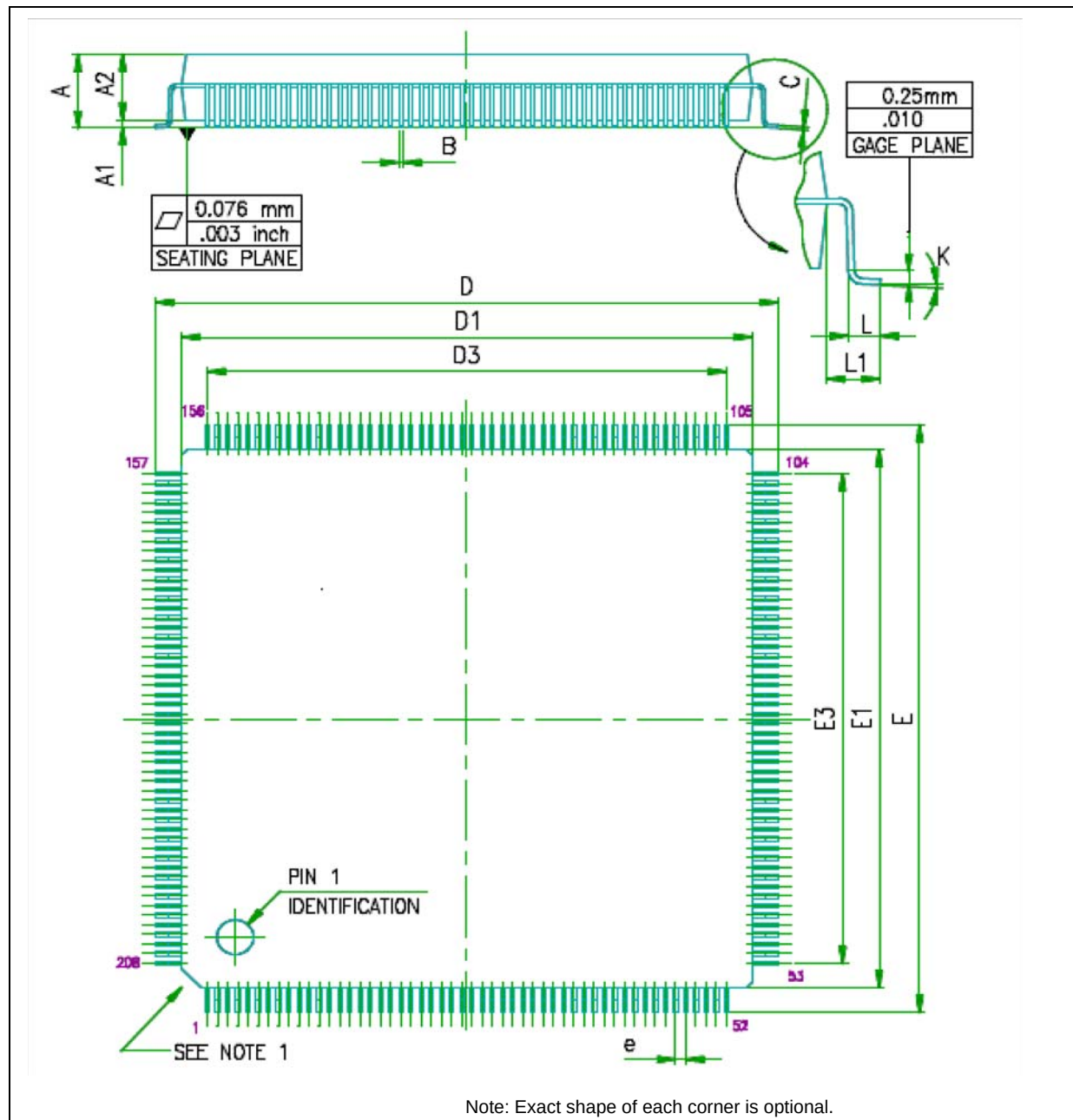


Figure 39. LQFP208 mechanical drawing

Table 55. LQFP208 mechanical data

Ref	mm			mm		
	Min	Typ	Max	Min	Typ	Max
A			1.6			1.6
A1	0.05		0.15	0.05	0.1	0.15
A2	1.3	1.35	1.45	1.3	1.35	1.45
B	0.17		0.27	0.17	0.22	0.27
c	0.09		0.2	0.11	0.15	0.19
D		30		29.8	30	30.2
D1		28		27.8	28	28.2
D3		25.5			25.5	
e		0.5			0.5	
E		30		29.8	30	30.2
E1		28		27.8	28	28.2
E3		25.5			25.5	
L	0.45	0.6	0.75	0.4	0.5	0.6
L1		1		1		
K	0 °	3.5 °	7.0 °	1 °	3 °	5 °

4.2.3 LBGA208 package mechanical drawing

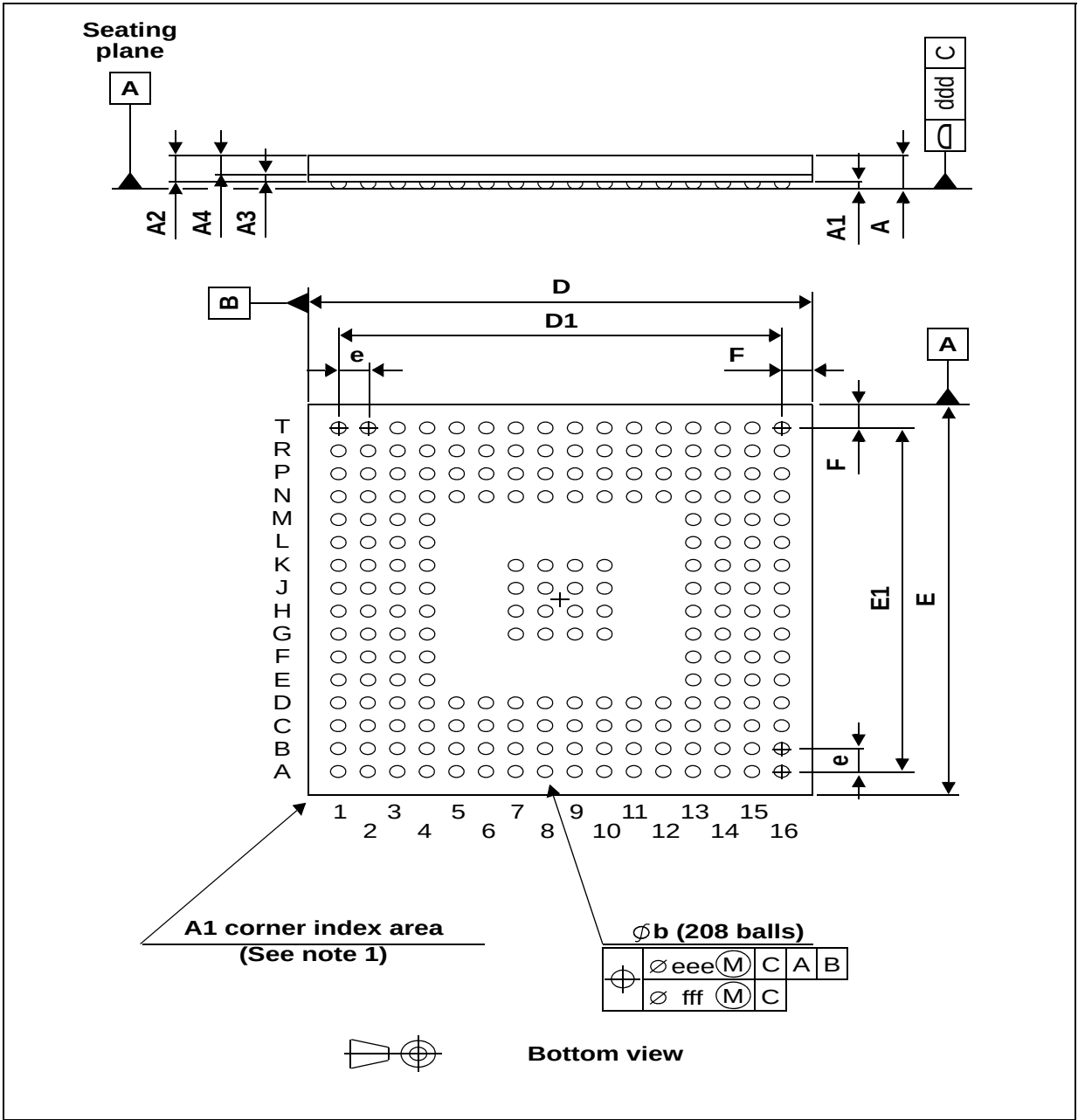


Figure 40. LBGA208 package mechanical drawing

¹ The terminal A1 corner must be identified on the top surface by using a corner chamfer, ink or metallized markings, or other feature of package body or integral heatslug. A distinguishing feature is allowable on the bottom surface of the package to identify the terminal A1 corner. Exact shape of each corner is optional.

Table 56. LBGA208 mechanical data

Symbol	mm			inches ⁽¹⁾			Notes
	Min	Typ	Max	Min	Typ	Max	
A			1.70			0.0669	(2)
A1	0.30			0.0118			
A2		1.085			0.0427		
A3		0.30			0.0118		
A4			0.80			0.0315	
b	0.50	0.60	0.70	0.0197	0.0236	0.0276	(3)
D	16.80	17.00	17.20	0.6614	0.6693	0.6772	
D1		15.00			0.5906		
E	16.80	17.00	17.20	0.6614	0.6693	0.6772	
E1		15.00			0.5906		
e		1.00			0.0394		
F		1.00			0.0394		
ddd			0.20			0.0079	
eee			0.25			0.0098	(4)
fff			0.10			0.0039	(5)

- Values in inches are converted from mm and rounded to 4 decimal digits.
- LBGA stands for **Low profile Ball Grid Array**.
 - Low profile: The total profile height (Dim A) is measured from the seating plane to the top of the component
 - The maximum total package height is calculated by the following methodology:
 $A2\ Typ + A1\ Typ + \sqrt{(A1^2 + A3^2 + A4^2)}$ tolerance values)
 - Low profile: $1.20\text{mm} < A \leq 1.70\text{ mm}$
- The typical ball diameter before mounting is 0.60 mm.
- The tolerance of position that controls the location of the pattern of balls with respect to datums A and B.
 For each ball there is a cylindrical tolerance zone eee perpendicular to datum C and located on true position with respect to datums A and B as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone.
- The tolerance of position that controls the location of the balls within the matrix with respect to each other.
 For each ball there is a cylindrical tolerance zone fff perpendicular to datum C and located on true position as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone.
 Each tolerance zone fff in the array is contained entirely in the respective zone eee above.
 The axis of each ball must lie simultaneously in both tolerance zones.

4.2.4 LBGA256 package mechanical drawing

Figure 41. LBGA256 mechanical drawing

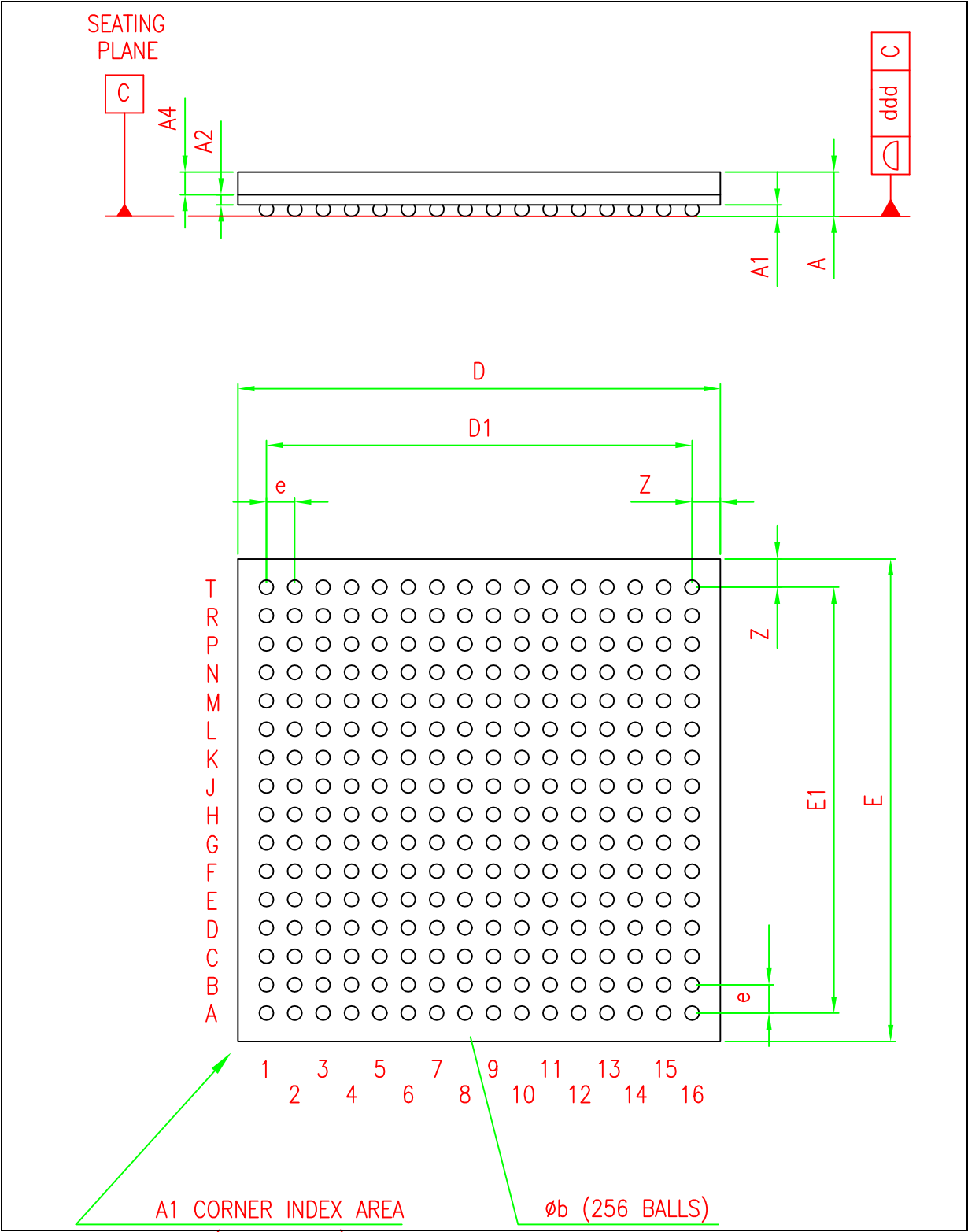


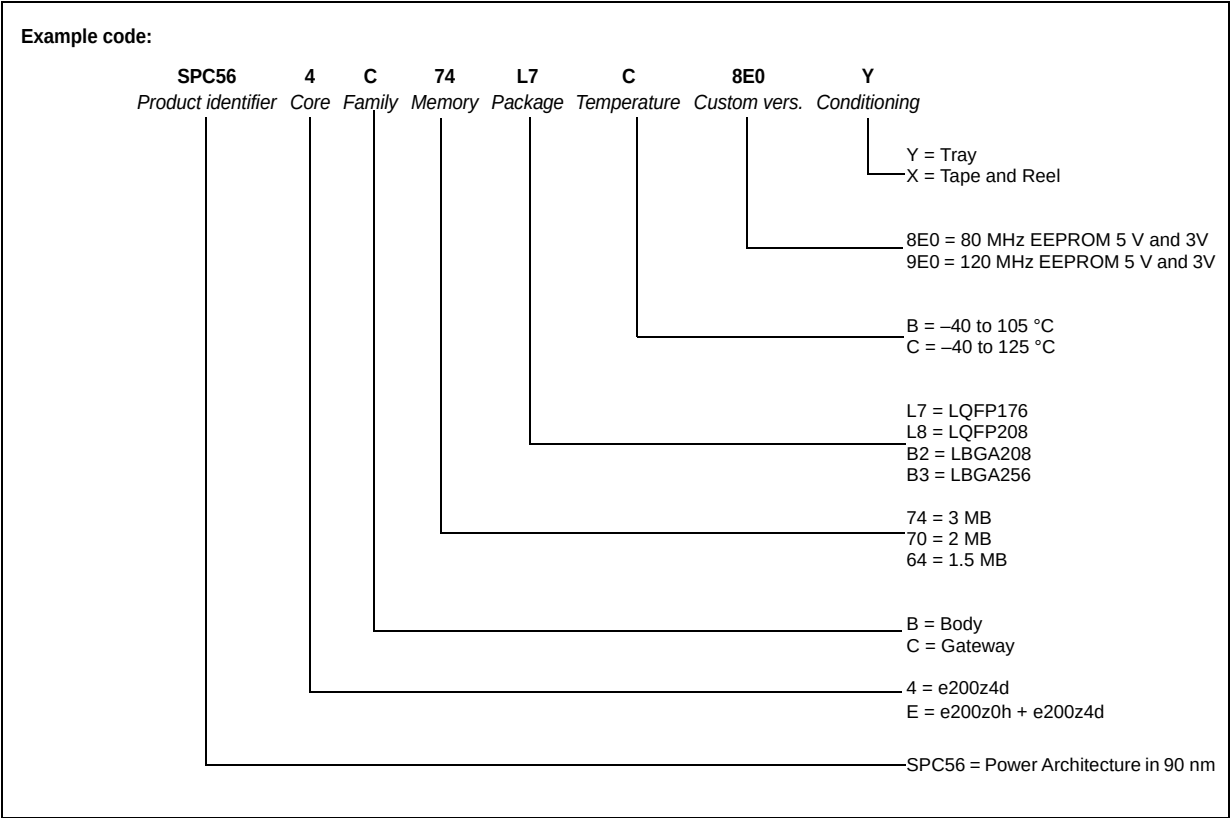
Table 57. LBGA256 mechanical data

Ref	mm		
	Min	Typ	Max
A	1.210		1.700
A1	0.300		
A2		0.300	
A4			0.800
b	0.400	0.500	0.600
D	16.800	17.000	17.200
D1		15.000	
E	16.800	17.000	17.200
E1		15.000	
e	0.900	1.000	1.100
Z	0.750	1.000	1.250
ddd			0.200

Note: The package is designed according to the Jedec standard No 95-1 Section 14 dedicated to Ball Grid Array Package Design Guide.

5 Ordering information

Figure 42. Ordering information scheme



Appendix A Abbreviations

[Table 58](#) lists abbreviations used but not defined elsewhere in this document.

Table 58. Abbreviations

Abbreviation	Meaning
CS	Chip select
EVTO	Event out
MCKO	Message clock out
MDO	Message data out
MSEO	Message start/end out
MTFE	Modified timing format enable
SCK	Serial communications clock
SOUT	Serial data out
TBD	To be defined
TCK	Test clock input
TDI	Test data input
TDO	Test data output
TMS	Test mode select

Revision history

[Table 59](#) summarizes revisions to this document.

Table 59. Revision history

Date	Revision	Changes
01-Jun-2010	1	Initial Release
17-Dec-2010	2	– Editing and formatting updates throughout the document. – Updated Voltage regulator capacitance connection figure. – Added a new sub-section “V_{DD_BV} Options” – Program and erase specifications: Updated Tdwprogram TYP to 22 us Updated T128Kpperase Max to 5000 ms Added t_{ESUS} parameter – Added recommendation in the Voltage regulator electrical characteristics section. – Added Crystal description table in Fast external crystal oscillator (4 to 140 MHz) electrical characteristics section and corrected the cross-reference to the same. – Added new sections - Pad types, System pins and functional ports – Updated TYP numbers in the Flash program and erase specifications table – Added a new table: Program and erase specifications (Data Flash) – Flash read access timing table: Added Data flash memory numbers – Flash power supply DC electrical characteristics table: Updated IDFREAD and IDFMOD values for Data flash, Removed IDFLPW parameter – Updated feature list. – SPC564Bxx and SPC56ECxx family comparison table: Updated ADC channels and added ADC footnotes. – SPC564Bxx and SPC56ECxx block diagram: Updated ADC channels and added legends. – SPC564Bxx and SPC56ECxx series block summary: Added new blocks. – Functional Port Pin Descriptions table: Added OSC32k_XTAL and OSC32k_EXTAL function at PB8 and PB9 port pins. – Electrical Characteristics: Replaced VSS with VSS_HV throughout the section. – Absolute maximum ratings, Recommended operating conditions (3.3 V) and Recommended operating conditions (5.0 V) tables: VRC_CTRL min is updated to "0". – Recommended operating conditions (3.3 V) and Recommended operating conditions (5.0 V) tables: Clarified VIN parameter, clarified footnote 2 in both tables. – LQFP thermal characteristics section: Added numbers for LQFP packages. – Low voltage power domain electrical characteristics table: Clarified footnotes based upon review comments. – Code flash memory—Program and erase specifications: Updated t_{ESRT} to 20 ms. – ADC electrical characteristics section: Replace ADC0 with ADC_0 and ADC1 with ADC_1 throughout the document. – DSPI characteristics section: Replaced PCSx with CSx in all figures and tables.

Table 59. Revision history (continued)

Date	Revision	Changes
28-Apr-2011	3	– Replaced VIL min from –0.4 V to –0.3 V in the following tables: - I/O input DC electrical characteristics - Reset electrical characteristics - Fast external crystal oscillator (4 to 40 MHz) electrical characteristics – Updated Crystal oscillator and resonator connection scheme figure – Specified NPN transistor as the recommended BCP68 transistor throughout the document – Code and Data flash memory—Program and erase specifications tables: Renamed the parameter t_{ESUS} to T_{eslat} – Revised the footnotes in the “Functional port pin descriptions” table. – In the “System pin descriptions” table, added a footnote to the A pads regarding not using IBE. – For ports PB[12–15], changed ANX to ADC0_X. – Revised the presentation of the ADC functions on the following ports: PB[4–7] PD[0–11] – ADC conversion characteristics (10-bit ADC_0) table and Conversion characteristics (12-bit ADC_1) table- Updated footnote 5 and 7 respectively for the definition of the conversion time. – Data flash memory—Program and erase specifications: Updated $T_{wprogram}$ to 500 μs and $T_{16Kpperase}$ to 500 μs. Corrected Teslat classification from “C” to “D”. – Code flash memory—Program and erase specifications: Corrected Teslat classification from “C” to “D”. – Flash Start-up time/Switch-off time: Changed $T_{FLARSTEXIT}$ classification from “C” to “D”. – Functional port pin description: Added a footnote at the PB [9] port pin. – Absolute maximum ratings table: Added footnote 1. – Low voltage power domain electrical characteristics table: Updated IDDHALT, IDSTOP, IDDSTBY3, IDDSTBY2, IDDSTBY1. – Updated commercial product code structure. – Slow external crystal oscillator (32 kHz) electrical characteristics table: Updated g_{msXOSC}, V_{SXOSC}, $I_{SXOSCBias}$ and I_{SXOSC}. – FMPLL electrical characteristics table: Updated Δt_{LTJIT}. – Fast internal RC oscillator (16 MHz) electrical characteristics table: Updated TFIRCSU and IFIRCPWD. – MII serial management channel timing table: Updated M12 – JTAG characteristics table: Updated t_{TDOV}. – Low voltage monitor electrical characteristics table: Updated VLVDHV3H, VLVDHV3L, VLVDHV5H, VLVDHV5L. – DSPI electricals table: Updated spec 1, 5, 6. Updated footnote 2 and 3. Added Δt_{CSC}, Δt_{ASC}, t_{SUSS}, t_{HSS}. – IO consumption table: Updated all parameter values. – DSPI electricals: Updated Δt_{CSC} max to 115 ns. – Low voltage power domain electrical characteristics table: Added footnote 9. – ADC electrical characteristics: Added 2 notes above 10-bit and 12-bit conversion tables.

Table 59. Revision history (continued)

Date	Revision	Changes
01-Dec-2011	4	– Interchanged the denominator with numerator in Equation 11 of Input impedance and ADC accuracy section – Removed the note (All ADC conversion characteristics described in the table below are applicable only for the precision channels. The data for semi-precision and extended channels is awaited and same will be subsequently updated in later revs.) in the ADC electrical characteristics section. – Table 50 (On-chip peripherals current consumption). Replaced IDD_HV_ADC with IDD_HV_ADC0 and IDD_HV_ADC1 values as per ADC specs – In Table 44, the minimum sample time of ADC0 changed to 500 at 32 MHz – In Table 44, removed the entry for sample time at 30 MHz – In Table 45, changed TUEX to TUES and INLX to INLS (Extended channels are not supported by the device. So, changed to standard channel.)
04-Mar-2013	5	– Updated the pins 23 and 24 of Figure 2: 176-pin LQFP configuration. – Updated unit of measure in Table 45: Conversion characteristics (12-bit ADC_1) – Modified the value to typical value in Table 50: On-chip peripherals current consumption – Added footnote to t_{ESRT} parameter in Table 27: Code flash memory—Program and erase specifications – Added footnote to t_{ESRT} parameter in Table 28: Data flash memory—Program and erase specifications – Updated Table 30: Flash memory read access timing. – Updated Notes 2 and Notes 3 of Table 10: Recommended operating conditions (3.3 V) and Table 11: Recommended operating conditions (5.0 V) respectively. – Updated the footnote1 of Table 10: Recommended operating conditions (3.3 V) and Table 11: Recommended operating conditions (5.0 V) – Updated V_{DD_HV_A} to V_{DD_BV} for C_{DEC2} and I_{DD_HV_A} in Table 24: Voltage regulator electrical characteristics and deleted footnote3 – Updated the dedicated number of channels for 12-bit ADC in family comparison tables – Updated the values of f_{SIRC}, parameters and conditions of Δ_{SIRCVAR} in Table 42: Slow internal RC oscillator (128 kHz) electrical characteristics – Updated second footnote in Table 11: Recommended operating conditions (5.0 V), – Updated the value of t_{ADC0_PU} in Table 44: ADC conversion characteristics (10-bit ADC_0) – Updated the IDD values in Table 26: Low voltage power domain electrical characteristics – Added footnote to Table 26: Low voltage power domain electrical characteristics related to current drawn from V_{DD_HV_A} and V_{DD_HV_B} – Updated entire Section : Input impedance and ADC accuracy – Updated the values of VLPREG in Table 24: Voltage regulator electrical characteristics. – Updated the values of V_LPREG in Table 24: Voltage regulator electrical characteristics. – Added T_A = 25 °C, min and max values of V_{MREG} in Table 24: Voltage regulator electrical characteristics – Added T_A = 25 °C, min and max values of V_LPREG in Table 24: Voltage regulator electrical characteristics

Table 59. Revision history (continued)

Date	Revision	Changes
04-Mar-2013	5 (cont.)	- Updated the min, max and typical values of $V_{LVDLVCORL}$ and $V_{LVDLVBKPL}$ in Table 25: Low voltage monitor electrical characteristics - Updated values of g_{mFXOSC} in Table 37: Fast external crystal oscillator (4 to 40 MHz) electrical characteristics - Updated values of g_{mSXOSC} in Table 39: Slow external crystal oscillator (32 kHz) electrical characteristics - Updated the footnote 5 for T_{ADC0_C} in Table 44: ADC conversion characteristics (10-bit ADC_0) - Updated the footnotes of Table 26: Low voltage power domain electrical characteristics
17-Sep-2013	6	Updated Disclaimer
28-Nov-2014	7	- Removed occurrences of 208BGA from Table 2: SPC564Bxx and SPC56ECxx family comparison. - Added PM[3] and PM[4] in the figure note 1 of Figure 5: 256-pin BGA configuration. - Added a table note in Table 21: I/O supplies. - Updated Figure 9: Voltage regulator capacitance connection and added a note in this figure. - Removed before trimming value for V_{MREG}, updated after trimming min value of V_{MREG} from 1.24 V to 1.20 V, updated after trimming min value of V_{LPREG} from 1.225 V to 1.17 V, updated after trimming typical value of V_{LPREG} from 1.25 V to 1.27 V and updated after trimming max value of V_{LPREG} from 1.275 V to 1.32 V in Table 24: Voltage regulator electrical characteristics. - Changed min value of $V_{LVDLVCORL}$ and $V_{LVDLVBKPL}$ from 1.12 V to 1.08 V, and removed typical value of $V_{LVDLVCORL}$ and $V_{LVDLVBKPL}$ in Table 25: Low voltage monitor electrical characteristics - Updated max values at 120 MHz for I_{DDRUN} from 200 mA to 208 mA and from 270 mA to 280 mA; updated max value at $T_A = 125\text{ }^{\circ}\text{C}$ for I_{DDHALT} from 80 mA to 100 mA; updated max value at $T_A = 25\text{ }^{\circ}\text{C}$ for I_{DDSTOP} from 1.2 mA to 5 mA and at $T_A = 125\text{ }^{\circ}\text{C}$ from 60 mA to 72 mA; updated max value at $T_A = 25\text{ }^{\circ}\text{C}$ for $I_{DDSTDBY3}$ from 75 μA to 96 μA and at $T_A = 125\text{ }^{\circ}\text{C}$ from 1200 μA to 2400 μA; updated max value at $T_A = 25\text{ }^{\circ}\text{C}$ for $I_{DDSTDBY2}$ from 70 μA to 92 μA and at $T_A = 125\text{ }^{\circ}\text{C}$ from 1100 μA to 2000 μA; updated max value at $T_A = 25\text{ }^{\circ}\text{C}$ for $I_{DDSTDBY1}$ from 65 μA to 85 μA and at $T_A = 125\text{ }^{\circ}\text{C}$ from 650 μA to 1100 μA; updated 1st footnote in Table 26: Low voltage power domain electrical characteristics. - Added a footnote below Table 30: Flash memory read access timing. - Updated the formula in Eq. 11 in Section : Input impedance and ADC accuracy. - Updated legend in Figure 17: Input equivalent circuit (precise channels) - Updated min and max values for g_{mFXOSC} at $V_{DD} = 5.0\text{ V} \pm 10\%$ from 4 mA/V to 6.5 mA/V and from 20 mA/V to 25 mA/V in Table 37: Fast external crystal oscillator (4 to 40 MHz) electrical characteristics - Added Figure 18: Input equivalent circuit (extended channels). - Updated t_{ADC0_PU} value to 1.5 as max and added footnote for I_{INJ} in Table 44: ADC conversion characteristics (10-bit ADC_0).

Table 59. Revision history (continued)

Date	Revision	Changes
28-Nov-2014	7 (cont.)	– Added Category column in Table 45: Conversion characteristics (12-bit ADC_1). – Added the IDD_HV_ADC0 values in Table 50: On-chip peripherals current consumption.

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