

SN54LS604, SN54LS606, SN54LS607, SN74LS604, SN74LS606, SN74LS607 OCTAL 2-INPUT MULTIPLEXED LATCHES

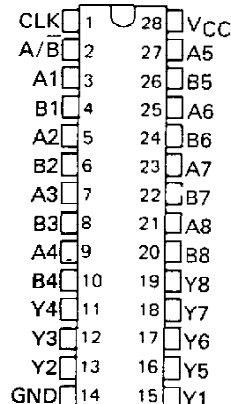
SDLS183

D2545, JULY 1979 - REVISED MARCH 1988

(TIM99604, TIM99606, TIM99607)

- **Choice of Outputs:**
Three State ('LS604, 'LS606)
Open-Collector ('LS607)
- **16 D-Type Registers, One for Each Data Input**
- **Multiplexer Selects Stored Data from Either A Bus or B Bus**
- **Application Oriented:**
Maximum Speed ('LS604)
Glitch-Free Operation ('LS606, 'LS607)

SN54LS604, SN54LS606, SN54LS607 . . . JD PACKAGE
SN74LS604, SN74LS606, SN74LS607 . . . JD OR N PACKAGE
(TOP VIEW)



description

The 'LS604, 'LS606, and 'LS607 multiplexed latches are ideal for storing data from two input buses, A and B, and providing the output bus with stored data from either the A or B register.

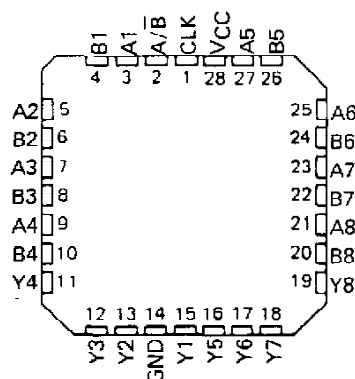
The clock loads data on the positive-going (low-level to high-level) transition. The clock pin also controls the active and high-impedance states of the outputs. When the clock pin is low, the outputs are in the high-impedance or off state. When the clock pin is high, the outputs are enabled.

The 'LS604 is optimized for high-speed operation. The 'LS606 and 'LS607 are especially designed to eliminate decoding voltage spikes.

These functions are ideal for interface from a 16-bit microprocessor to a 64K RAM board. The row and column addresses can be loaded as one word from the microprocessor and then multiplexed sequentially to the RAM during the time that RAS and CAS are active.

The SN54LS604, SN54LS606, and SN54LS607 are characterized for operation over the full military temperature range of -55°C to 125°C; the SN74LS604, SN74LS606, and SN74LS607 are characterized for operation from 0°C to 70°C.

SN54LS604, SN54LS606, SN54LS607 . . . FK PACKAGE
(TOP VIEW)



FUNCTION TABLE

INPUTS				OUTPUTS Y1-Y8
A1-A8	B1-B8	SELECT A/B	CLOCK	
A data	B data	L	↑	B data
A data	B data	H	↑	A data
X	X	X	L	Z or Off
X	X	L	H	B register stored data
X	X	H	H	A register stored data

H = high level (steady state)

L = low level (steady state)

X = irrelevant

Z = high-impedance state

Off = H if pull-up resistor is connected to open-collector output

↑ = transition from low to high level

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

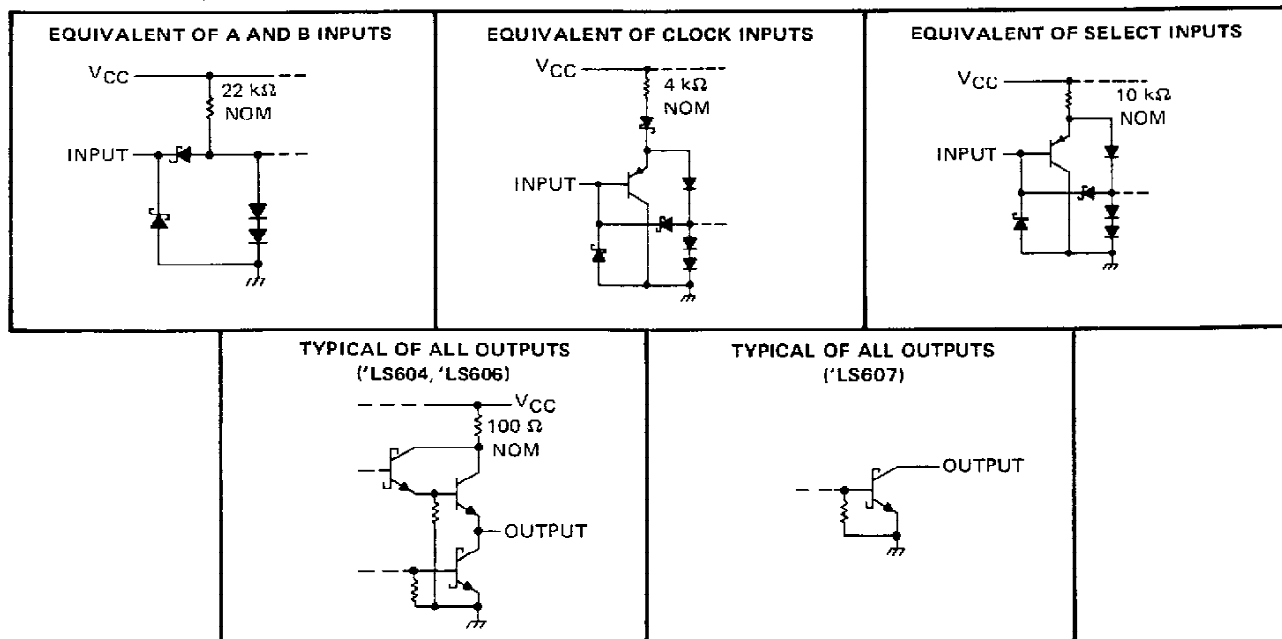
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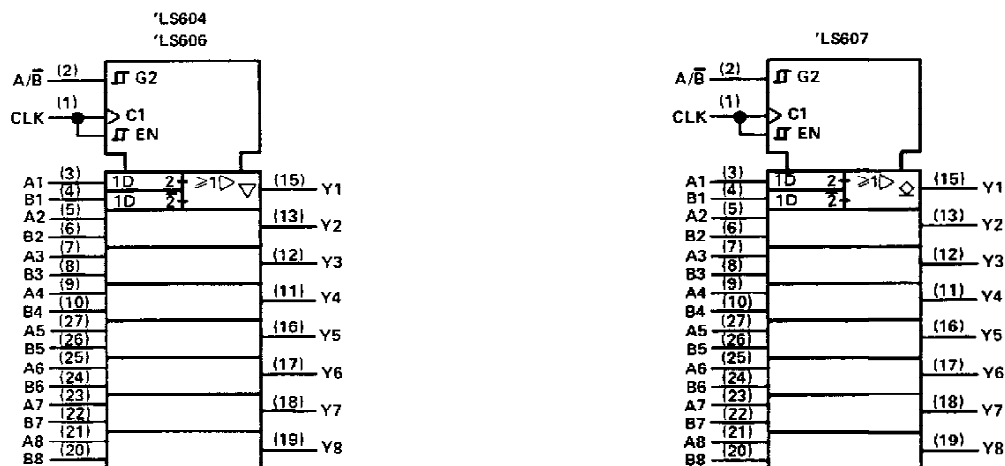
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OCTAL 2-INPUT MULTIPLEXED LATCHES

schematics of inputs and outputs



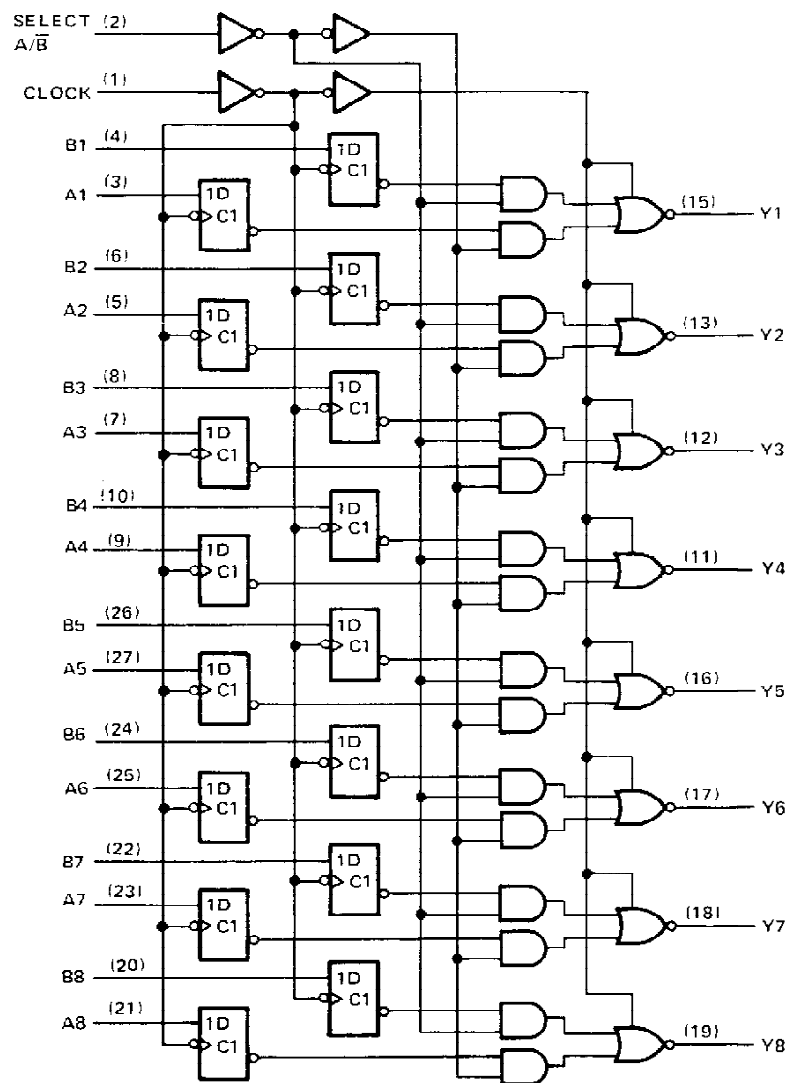
logic symbols†



†These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
Pin numbers shown are for JD and N packages.

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OCTAL 2-INPUT MULTIPLEXED LATCHES

logic diagram (positive logic)



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SN54LS604, SN54LS606, SN74LS604, SN74LS606

OCTAL 2-INPUT MULTIPLEXED LATCHES WITH 3-STATE OUTPUTS

recommended operating conditions

	SN54LS604 SN54LS606			SN74LS604 SN74LS606			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-1			-2.6	mA
Low-level output current, I_{OL}			12			24	mA
Width of clock pulse, t_W	20			20			ns
Setup time, t_{SU}	20†			20†			ns
Hold time, t_H	0†			0†			ns
Operating free-air temperature, T_A	-55		125	0		70	°C

NOTE 1: Voltage values are with respect to network ground terminal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS604 SN54LS606			SN74LS604 SN74LS606			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage				0.7			0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OH} = \text{MAX}$	2.4	3.1		2.4	3.1		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OL} = 12 \text{ mA}$ $I_{OL} = 24 \text{ mA}$		0.25	0.4		0.25	0.4	V
I_{OZH} Off-state output current, high-level voltage applied	$V_{CC} = \text{MAX}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, V_O = 2.7 \text{ V}$			20			20	µA
I_{OZL} Off-state output current, low-level voltage applied	$V_{CC} = \text{MAX}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, V_O = 0.4$			-20			-20	µA
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$			0.1			0.1	mA
				0.1			0.1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			20			20	µA
				20			20	µA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-0.4			-0.4	mA
				-0.2			-0.2	mA
I_{OS} Short-circuit output current§	$V_{CC} = \text{MAX}$	-30		-130	-30		-130	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}, \text{ See Note 2}$		55	70		55	70	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Note more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 2: I_{CC} is tested with all inputs grounded and all outputs open.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER	FROM (INPUT)	TEST CONDITIONS	'LS604			'LS606			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Select A/B (Data: A = H, B = L)	$C_L = 45 \text{ pF}, R_L = 667 \Omega,$ See Note 3		15	25		36	50	ns
t_{PHL}	Select A/B (Data: A = H, B = L)			23	35		16	30	ns
t_{PLH}	Select A/B (Data: A = L, B = H)			31	45		22	35	ns
t_{PHL}	Select A/B (Data: A = L, B = H)			19	30		22	35	ns
t_{PZH}	Clock	$C_L = 5 \text{ pF}, R_L = 667 \Omega,$ See Note 3		19	30		27	40	ns
t_{PZL}	Clock			28	40		35	50	ns
t_{PHZ}	Clock			20	30		20	30	ns
t_{PLZ}	Clock			15	25		15	25	ns

t_{PLH} ≡ propagation delay time, low-to-high-level output

t_{PHL} ≡ propagation delay time, high-to-low-level output

t_{PZH} ≡ output enable time to high level

t_{PZL} ≡ output enable time to low level

t_{PHZ} ≡ output disable time from high level

t_{PLZ} ≡ output disable time from low level

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

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SN54LS607, SN74LS607

OCTAL 2-INPUT MULTIPLEXED LATCHES WITH OPEN-COLLECTOR OUTPUTS

recommended operating conditions

	SN54LS607			SN74LS607			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}			5.5			5.5	V
Low-level output current, I_{OL}			12			24	mA
Width of clock pulse, t_W	20			20			ns
Setup time, t_{SU}	20†			20†			ns
Hold time, t_H	0†			0†			ns
Operating free-air temperature, T_A	-55		125	0		70	°C

NOTE 1: Voltage values are with respect to network ground terminal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS607			SN74LS607			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage				0.7			0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V
I_{OH} High-level output current	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, V_{OH} = 5.5 \text{ V}$			250			250	µA
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}$	0.25	0.4		0.25	0.4		V
				$I_{OL} = 12 \text{ mA}$			$I_{OL} = 24 \text{ mA}$	
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$	0.1	0.1		0.1	0.1		mA
				A, B			CLK, SELECT	
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$	20	20		20	20		µA
				A, B			CLK, SELECT	
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$	-0.4	-0.2		-0.4	-0.2		mA
				A, B			CLK, SELECT	
I_{CC} Supply current	$V_{CC} = \text{MAX}, \text{ See Note 2}$	40	60		40	60		mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

NOTE 2: I_{CC} is tested with all inputs grounded and all outputs open.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER	FROM (INPUT)	TEST CONDITIONS	'LS607			UNIT
			MIN	TYP	MAX	
tPLH	Select A/B	CL = 45 pF, RL = 667 Ω, See Note 3		51	70	ns
tPHL	(Data: A = H, B = L)			21	30	
tPLH	Select A/B			28	40	ns
tPHL	(Data: A = L, B = H)			28	40	
tPLH	Clock			30	45	ns
tPHL				32	45	

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

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