

## SN65LBC172A, SN75LBC172A Quadruple RS-485 Differential Line Drivers

### 1 Features

- Designed for TIA/EIA-485, TIA/EIA-422, and ISO 8482 applications
- Signaling Rates<sup>†</sup> up to 30Mbps
- Propagation delay times <11 ns
- Low standby power consumption 1.5mA max
- Output ESD protection 12 kV
- Driver positive- and negative-current limiting
- Power-up and power-down glitch-free for live insertion applications
- Thermal shutdown protection
- Industry standard pin-out, compatible with SN75172, AM26LS31, DS96172, LTC486, and MAX3045

### 2 Applications

- Motor drives
- Factory automation and control

### 3 Description

The SN65LBC172A and SN75LBC172A are quadruple differential line drivers with 3-state outputs, designed for TIA/EIA-485 (RS-485), TIA/EIA-422 (RS-422), and ISO 8482 applications.

These devices are optimized for balanced multipoint bus transmission at signaling rates up to 30 million bits per second. The transmission media may be

printed-circuit board traces, backplanes, or cables. The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media and the noise coupling to the environment.

Each driver features current limiting and thermal-shutdown circuitry making it suitable for high-speed multipoint data transmission applications in noisy environments. These devices are designed using LinBiCMOS, facilitating low power consumption and robustness.

The G and  $\bar{G}$  inputs provide driver enable control using either positive or negative logic. When disabled or powered off, the driver outputs present a high-impedance to the bus for reduced system loading.

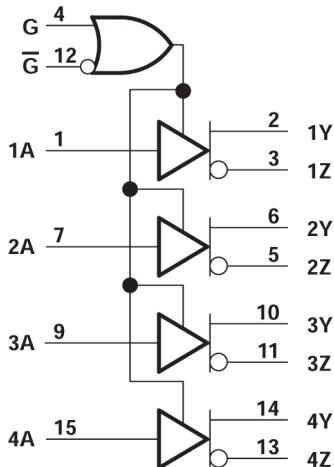
The SN75LBC172A is characterized for operation over the temperature range of 0°C to 70°C. The SN65LBC172A is characterized over the temperature range from -40°C to 85°C.

### Package Information

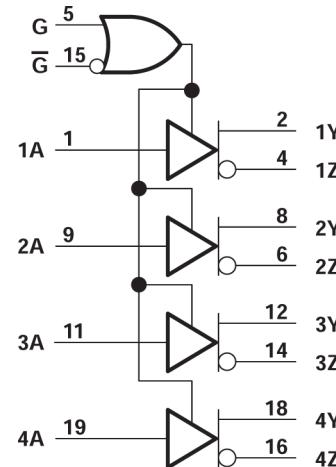
PART NUMBER	PACKAGE <sup>(1)</sup>	PACKAGE SIZE <sup>(2)</sup>
SN65LBC172A	SOIC (DW, 16)	10.3mm × 10.3mm
SN75LBC172A	SOIC (DW, 20)	12.8mm × 10.3mm
	PDIP (N, 16)	19.3mm × 9.4mm

(1) For more information, see [Section 11](#).

(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Logic Diagram (Positive Logic)



Logic Diagram (Positive Logic)

<sup>†</sup> The signaling rate of a line is the number of voltage transitions that are made per second expressed in the units bps (bits per second).



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

## Table of Contents

<b>1 Features</b> .....	<b>1</b>	<b>7 Detailed Description</b> .....	<b>13</b>
<b>2 Applications</b> .....	<b>1</b>	7.1 Device Functional Modes.....	<b>13</b>
<b>3 Description</b> .....	<b>1</b>	<b>8 Application and Implementation</b> .....	<b>14</b>
<b>4 Pin Configuration and Functions</b> .....	<b>3</b>	8.1 Application Information.....	<b>14</b>
<b>5 Specifications</b> .....	<b>4</b>	<b>9 Device and Documentation Support</b> .....	<b>15</b>
5.1 Absolute Maximum Ratings .....	4	9.1 Documentation Support.....	<b>15</b>
5.2 ESD Ratings.....	4	9.2 Receiving Notification of Documentation Updates.....	<b>15</b>
5.3 Dissipation Rating Table.....	4	9.3 Support Resources.....	<b>15</b>
5.4 Recommended Operating Conditions.....	4	9.4 Trademarks.....	<b>15</b>
5.5 Thermal Information.....	5	9.5 Electrostatic Discharge Caution.....	<b>15</b>
5.6 Electrical Characteristics.....	5	9.6 Glossary.....	<b>15</b>
5.7 Switching Characteristics.....	6	<b>10 Revision History</b> .....	<b>15</b>
5.8 Typical Characteristics.....	7	<b>11 Mechanical, Packaging, and Orderable</b> <b>Information</b> .....	<b>15</b>
<b>6 Parameter Measurement Information</b> .....	<b>8</b>		

## 4 Pin Configuration and Functions

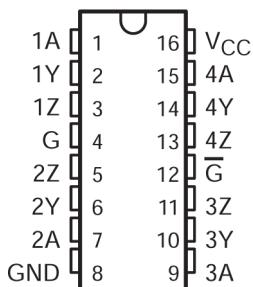


Figure 4-1. N Package (Top View)

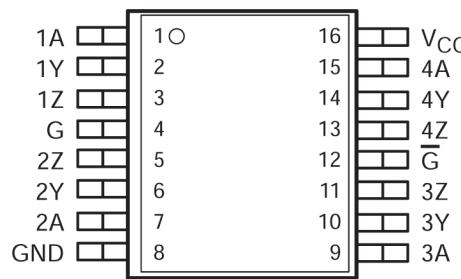


Figure 4-2. 16-DW Package (Top View)

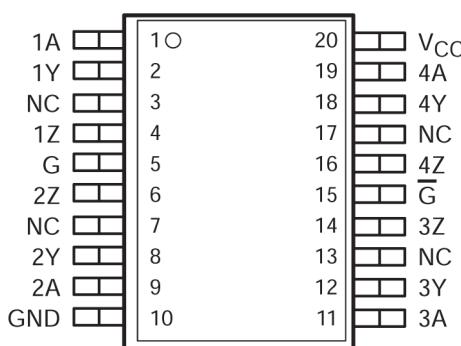


Figure 4-3. 20-DW Package (Top View)

## 5 Specifications

### 5.1 Absolute Maximum Ratings

See Note <sup>(1)</sup>

			MIN	MAX	UNIT
$V_{CC}$	Supply voltage range		-0.3	6	V
$V_O$	Output voltage range	at any bus (steady state)	-10	15	V
$V_O$	Output voltage range	at any bus (transient pulse through $100\Omega$ , see Figure 6-8)	-30	30	V
$V_I$	Input voltage range	at any A, G, or $\bar{G}$ terminal	-0.5	$V_{CC} + 0.5$	V
$T_{STG}$	Storage temperature range		-65	150	°C
$P_D$	Continuous power dissipation		See Dissipation Rating Table		
$T_{LEAD}$	Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds			260	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 <sup>(1)</sup>	$Y, Z$ , and GND	$\pm 12000$
		All pins	$\pm 5000$	V
		Charged device model (CDM), per AEC Q100-011 <sup>(2)</sup>	All pins	
			$\pm 1000$	

(1) Tested in accordance with JEDEC standard 22, Test Method A114-A.

(2) Tested in accordance with JEDEC standard 22, Test Method C101.

### 5.3 Dissipation Rating Table

PACKAGE	JEDEC BOARD MODEL	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR <sup>(1)</sup> ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING
16-PIN DW	Low K	1200mW	9.6mW/°C	769mW	625mW
	High K	2240mW	17.9mW/°C	1434mW	1165mW
20-PIN DW	Low K	1483mW	11.86mW/°C	949mW	771mW
	High K	2753mW	22mW/°C	1762mW	1432mW
16-PIN N	Low K	1150mW	9.2mW/°C	736mW	598mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted with no air flow.

### 5.4 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Supply voltage, $V_{CC}$		4.75	5	5.25	V
Voltage at any bus terminal	$Y, Z$	-7	12		V
High-level input voltage, $V_{IH}$	A, G, $\bar{G}$	2	$V_{CC}$		V
Low-level input voltage, $V_{IL}$		0	0.8		
Output current		-60	60		mA
Operating free-air temperature, $T_A$	SN75LBC172A	0	70		°C
	SN65LBC172A	-40	85		

## 5.5 Thermal Information

THERMAL METRIC <sup>(1)</sup>	N (PDIP)	DW (SOIC)	DW (SOIC)	UNIT
	16 PINS	16 PINS	20 PINS	
$R_{\theta JA}$ Junction-to-ambient thermal resistance	60.6	71.1	66.8	°C/W
$R_{\theta JC(\text{top})}$ Junction-to-case (top) thermal resistance	48.1	37.4	34.4	°C/W
$R_{\theta JB}$ Junction-to-board thermal resistance	40.6	36.8	39.7	°C/W
$\Psi_{JT}$ Junction-to-top characterization parameter	27.5	13.3	8.9	°C/W
$\Psi_{JB}$ Junction-to-board characterization parameter	40.3	36.4	39	°C/W
$R_{\theta JC(\text{bot})}$ Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics application report](#).

## 5.6 Electrical Characteristics

over recommended operating conditions

PARAMETER	TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
$V_{IK}$ Input clamp voltage	$I_I = -18\text{mA}$	-1.5	-0.77		V
$V_O$ Open-circuit output voltage	Y or Z, No load	0		$V_{CC}$	V
$ V_{OD(\text{ss})} $ Steady-state differential output voltage magnitude <sup>(2)</sup>	No load (open circuit)	3		$V_{CC}$	V
	$R_L = 54\Omega$ , see <a href="#">Figure 6-1</a>	1	1.6	2.5	
	With common-mode loading, see <a href="#">Figure 6-2</a>	1	1.6	2.5	
$\Delta V_{OD(\text{ss})}$ Change in steady-state differential output voltage between logic states	See <a href="#">Figure 6-1</a>	-0.1		0.1	V
$V_{OC(\text{ss})}$ Steady-state common-mode output voltage	See <a href="#">Figure 6-3</a>	2	2.4	2.8	V
$\Delta V_{OC(\text{ss})}$ Change in steady-state common-mode output voltage between logic states	See <a href="#">Figure 6-3</a>	-0.02		0.02	V
$I_I$ Input current	A, G, $\bar{G}$	-50		50	$\mu\text{A}$
$I_{os}$ Short-circuit output current	$V_{TEST} = -7\text{V}$ to $12\text{V}$ , See <a href="#">Figure 6-7</a>	$V_I = 0\text{V}$	-200	200	mA
$I_{oz}$ High-impedance-state output current		$V_I = V_{CC}$			
$I_{O(OFF)}$ Output current with power off		G at $0\text{V}$ , $\bar{G}$ at $V_{CC}$	-50	50	$\mu\text{A}$
$I_{CC}$ Supply current	$V_I = 0\text{V}$ or $V_{CC}$ , No load	$V_{CC} = 0\text{V}$	-10	10	
		All drivers enabled		23	mA
		All drivers disabled		1.5	

(1) All typical values are at  $V_{CC} = 5\text{V}$  and  $25^\circ\text{C}$ .

(2) The minimum  $V_{OD}$  may not fully comply with TIA/EIA-485-A at operating temperatures below  $0^\circ\text{C}$ . System designers should take the possibility of lower output signal into account in determining the maximum signal transmission distance.

## 5.7 Switching Characteristics

over recommended operating conditions

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}$	$R_L = 54\Omega$ , $C_L = 50\text{pF}$ , see <a href="#">Figure 6-4</a>	5.5	8	11	ns
$t_{PHL}$		5.5	8	11	ns
$t_r$		2	7.5	11	ns
$t_f$		2	7.5	11	ns
$t_{sk(p)}$		0.6	2	ns	
$t_{sk(o)}$			2	ns	
$t_{sk(pp)}$			3	ns	
$t_{PZH}$	<a href="#">See Figure 6-5</a>		25	ns	
$t_{PHZ}$			25	ns	
$t_{PZL}$	<a href="#">See Figure 6-6</a>		30	ns	
$t_{PLZ}$			20	ns	

(1) Output skew ( $t_{sk(o)}$ ) is the magnitude of the time delay difference between the outputs of a single device with all of the inputs connected together.

(2) Part-to-part skew ( $t_{sk(pp)}$ ) is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same input signals, the same supply voltages, at the same temperature, and have identical packages and test circuits.

## 5.8 Typical Characteristics

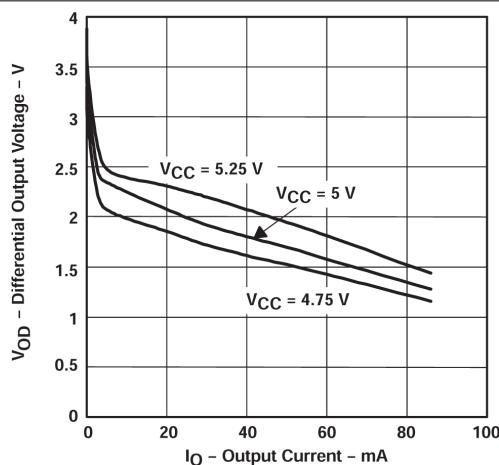


Figure 5-1. Differential Output Voltage vs Output Current

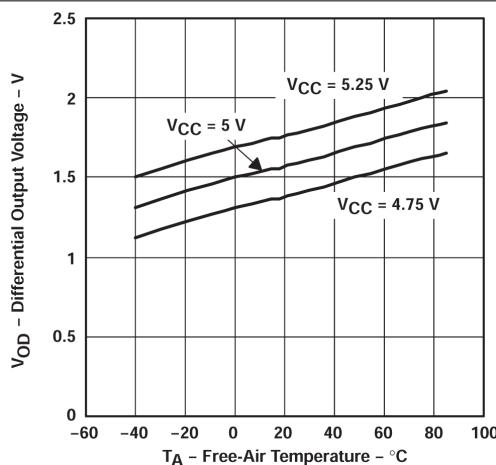


Figure 5-2. Differential Output Voltage vs Free-air Temperature

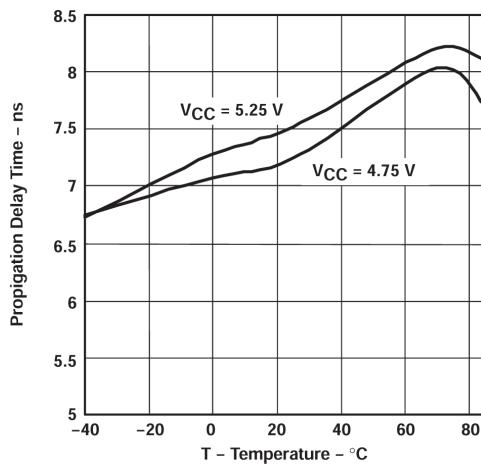


Figure 5-3. Propagation Delay Time vs Temperature

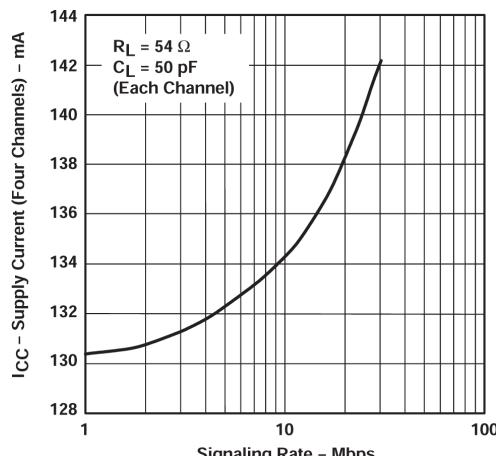


Figure 5-4. Supply Current (Four Channels) vs Signaling Rate

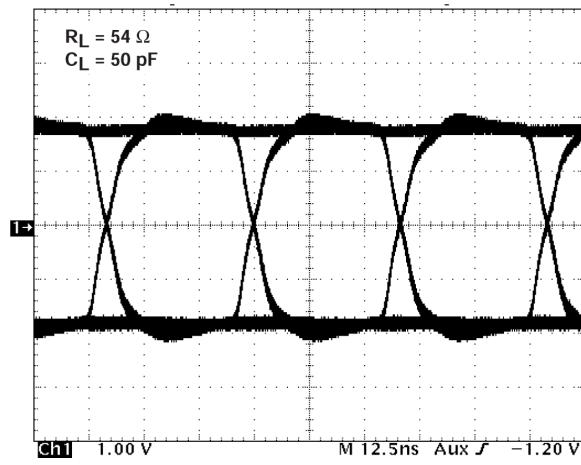


Figure 5-5. Eye Pattern, Pseudorandom Data at 30Mbps

## 6 Parameter Measurement Information

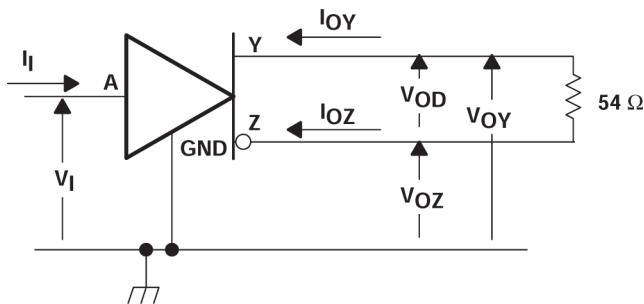


Figure 6-1. Test Circuit,  $V_{OD}$  Without Common-Mode Loading

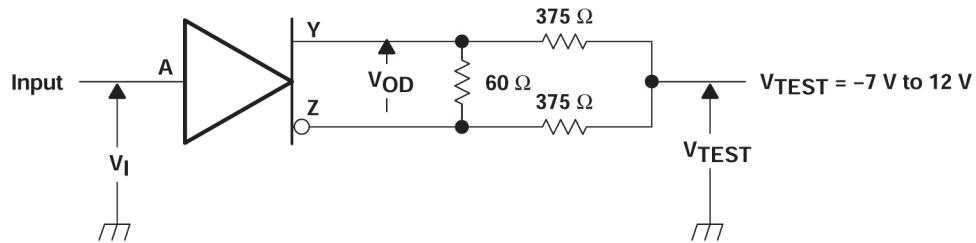


Figure 6-2. Test Circuit,  $V_{OD}$  With Common-Mode Loading

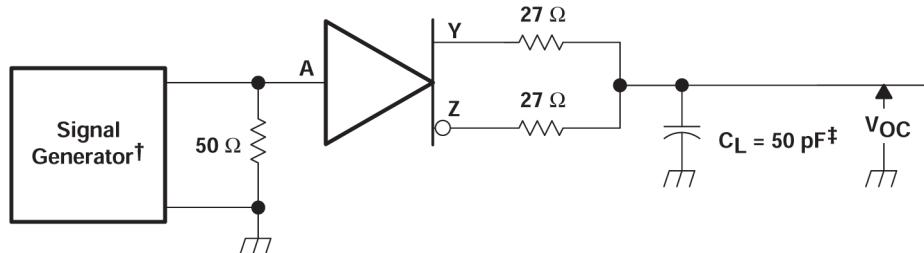
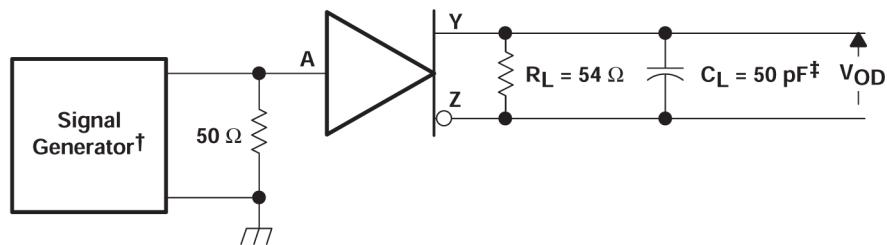


Figure 6-3.  $V_{OC}$  Test Circuit



<sup>†</sup> PRR = 1 MHz, 50% duty cycle,  $t_r < 6 \text{ ns}$ ,  $t_f < 6 \text{ ns}$ ,  $Z_O = 50 \Omega$

<sup>‡</sup> Includes probe and jig capacitance

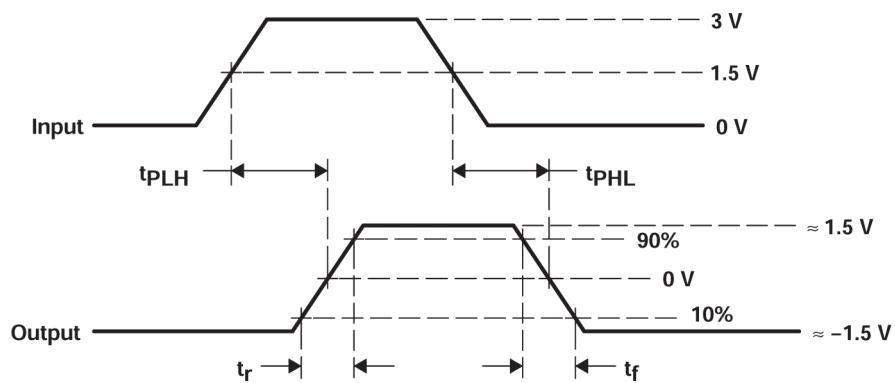
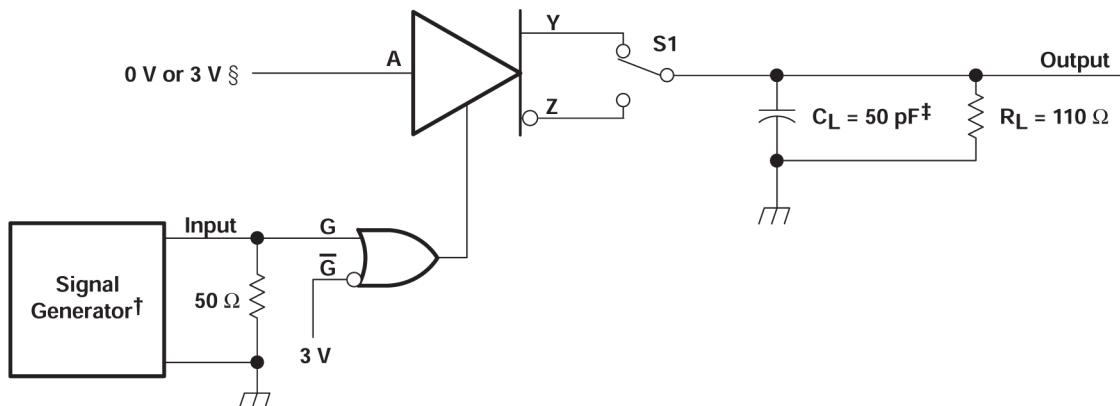


Figure 6-4. Output Switching Test Circuit and Waveforms



† PRR = 1 MHz, 50% duty cycle,  $t_r < 6$  ns,  $t_f < 6$  ns,  $Z_O = 50 \Omega$

‡ Includes probe and jig capacitance

§ 3-V if testing Y output, 0 V if testing Z output

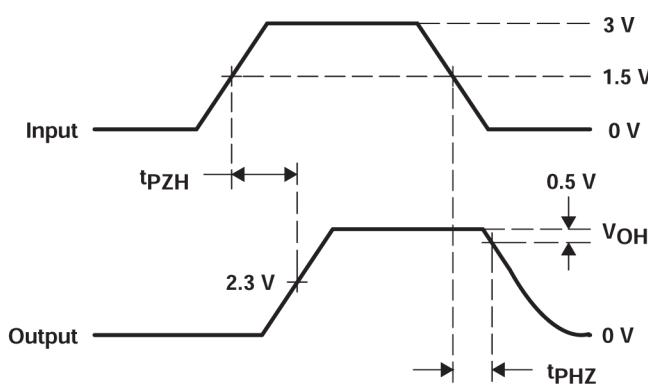
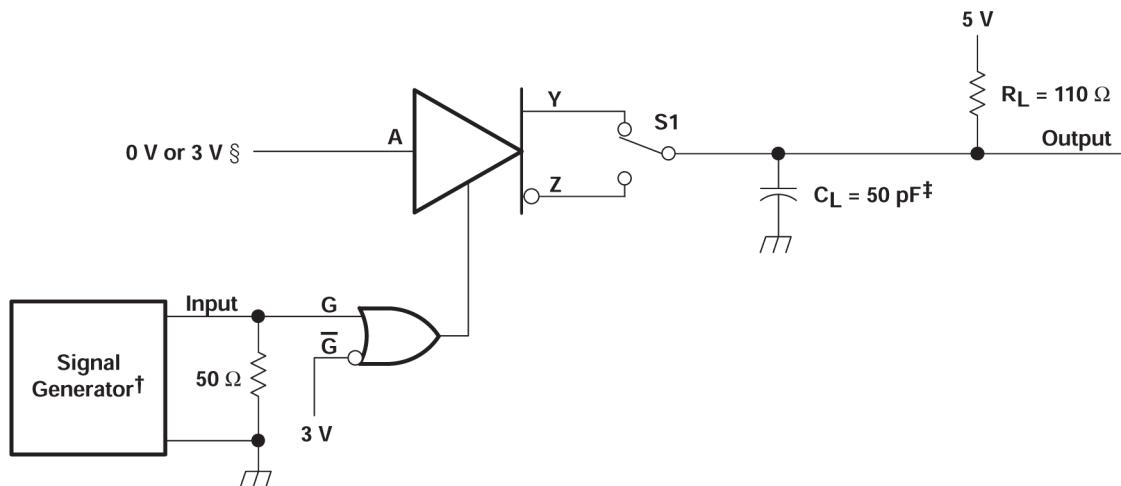


Figure 6-5. Enable Timing Test Circuit and Waveforms,  $t_{PZH}$  and  $t_{PHZ}$



† PRR = 1 MHz, 50% duty cycle,  $t_r < 6$  ns,  $t_f < 6$  ns,  $Z_O = 50$   $\Omega$

‡ Includes probe and jig capacitance

§ 3-V if testing Y output, 0 V if testing Z output

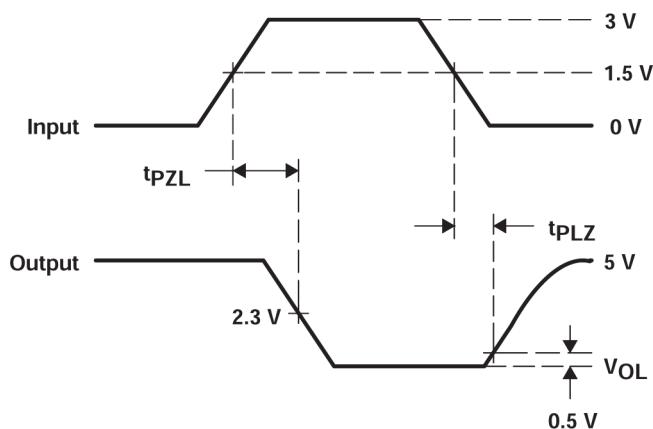


Figure 6-6. Enable Timing Test Circuit and Waveforms,  $t_{PZL}$  and  $t_{PLZ}$

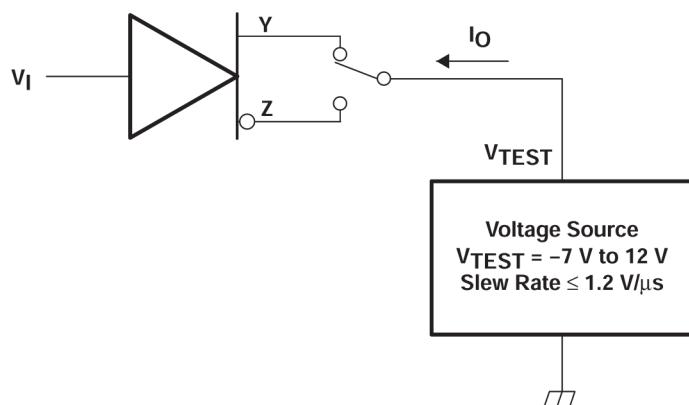
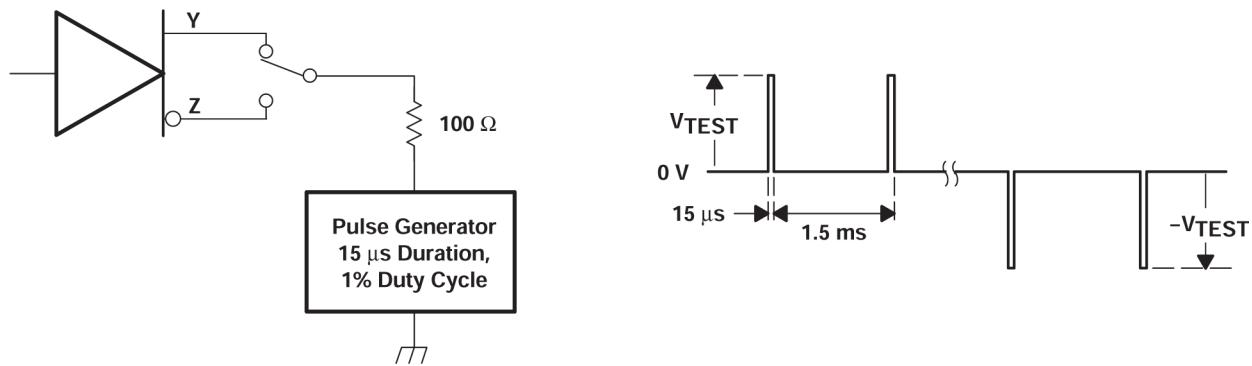


Figure 6-7. Test Circuit, Short-Circuit Output Current



**Figure 6-8. Test Circuit and Waveform, Transient Over-Voltage**

## 7 Detailed Description

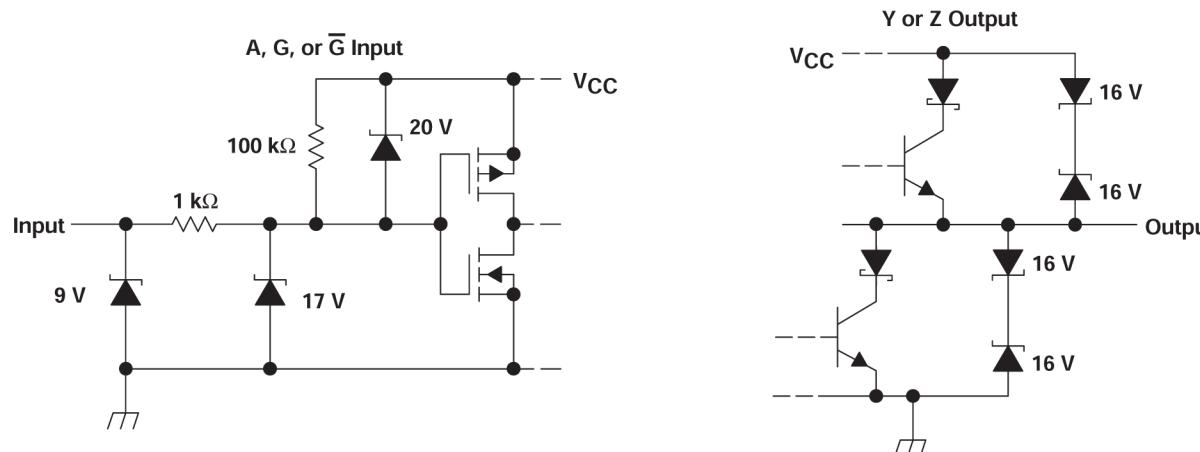
### 7.1 Device Functional Modes

### 7.1.1 Function Table

**Table 7-1. (Each Driver)**

INPUT	ENABLES		OUTPUTS	
A	G	$\bar{G}$	Y	Z
L	H	X	L	H
L	X	L	L	H
H	H	X	H	L
H	X	L	H	L
OPEN	H	X	H	L
OPEN	X	L	H	L
H	OPEN	X	H	L
L	OPEN	X	L	H
X	L	H	Z	Z
X	L	OPEN	Z	Z

### 7.1.2 Equivalent Input and Output Schematic Diagrams



## 8 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 8.1 Application Information

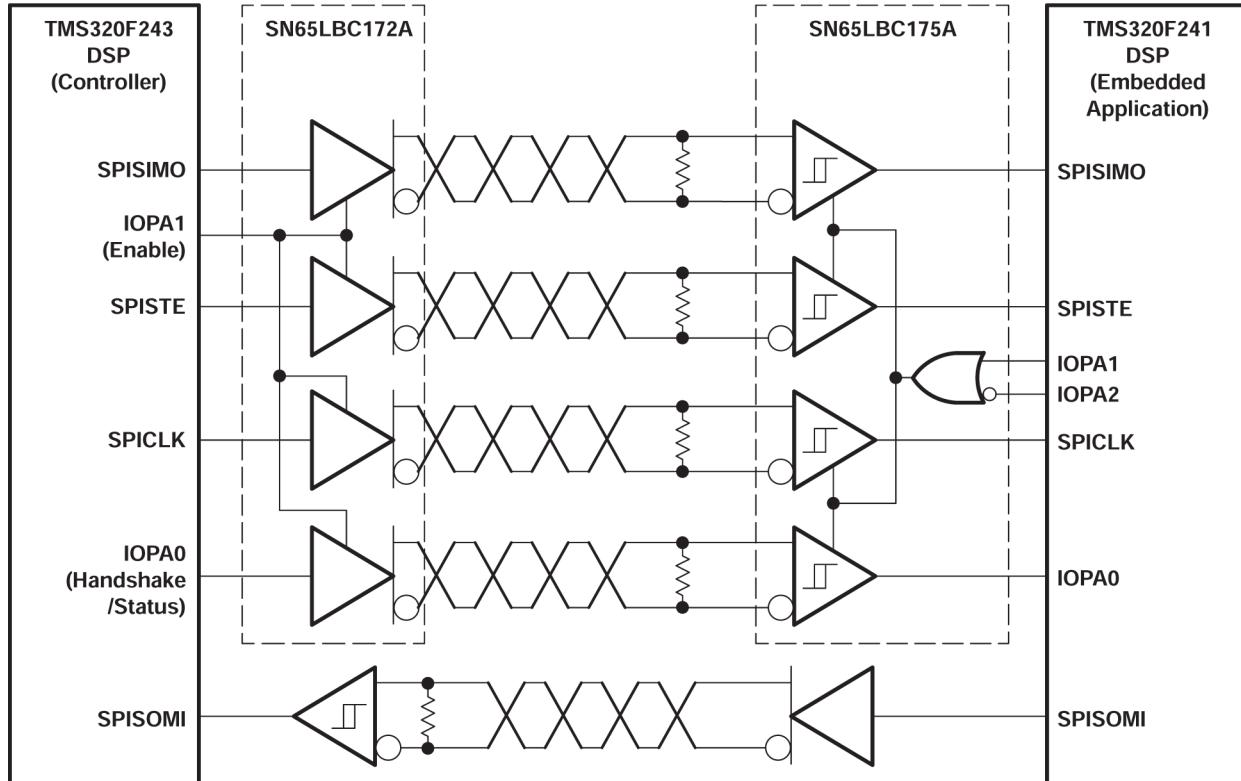


Figure 8-1. Typical Application Circuit, DSP-to-DSP Link via Serial Peripheral Interface

## 9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 9.1 Documentation Support

#### 9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

#### 9.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

#### 9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

#### 9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

#### 9.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision C (August 2008) to Revision D (April 2024)</b>	<b>Page</b>
• Changed the numbering format for tables, figures, and cross-references throughout the document.....	1
• Added the <i>Thermal Information</i> table .....	5

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">SN65LBC172A16DW</a>	Obsolete	Production	SOIC (DW)   16	-	-	Call TI	Call TI	-40 to 85	65LBC172A
<a href="#">SN65LBC172A16DWR</a>	Active	Production	SOIC (DW)   16	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65LBC172A
<a href="#">SN65LBC172A16DWR.A</a>	Active	Production	SOIC (DW)   16	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65LBC172A
<a href="#">SN65LBC172ADW</a>	Obsolete	Production	SOIC (DW)   20	-	-	Call TI	Call TI	-40 to 85	65LBC172A
<a href="#">SN65LBC172ADWR</a>	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65LBC172A
<a href="#">SN65LBC172ADWR.A</a>	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65LBC172A
<a href="#">SN65LBC172AN</a>	Active	Production	PDIP (N)   16	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	65LBC172A
<a href="#">SN65LBC172AN.A</a>	Active	Production	PDIP (N)   16	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	65LBC172A
<a href="#">SN65LBC172ANE4</a>	Active	Production	PDIP (N)   16	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	65LBC172A
<a href="#">SN75LBC172A16DW</a>	Obsolete	Production	SOIC (DW)   16	-	-	Call TI	Call TI	0 to 70	75LBC172A
<a href="#">SN75LBC172A16DWR</a>	Obsolete	Production	SOIC (DW)   16	-	-	Call TI	Call TI	0 to 70	75LBC172A
<a href="#">SN75LBC172ADW</a>	Obsolete	Production	SOIC (DW)   20	-	-	Call TI	Call TI	0 to 70	75LBC172A
<a href="#">SN75LBC172ADWR</a>	Obsolete	Production	SOIC (DW)   20	-	-	Call TI	Call TI	0 to 70	75LBC172A
<a href="#">SN75LBC172AN</a>	Obsolete	Production	PDIP (N)   16	-	-	Call TI	Call TI	0 to 70	75LBC172A

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

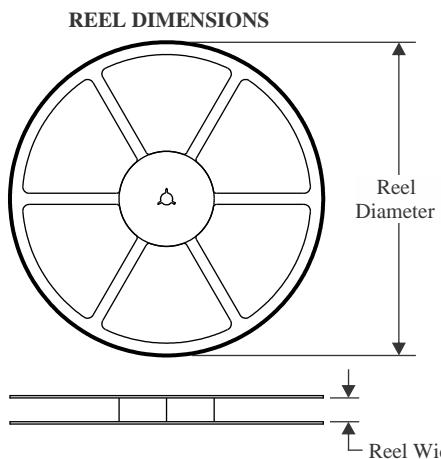
<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

---

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

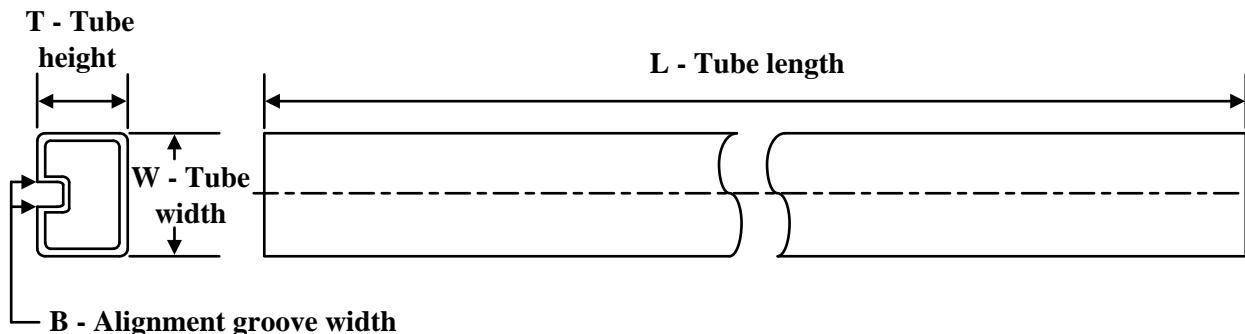

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LBC172A16DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
SN65LBC172ADWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LBC172A16DWR	SOIC	DW	16	2000	350.0	350.0	43.0
SN65LBC172ADWR	SOIC	DW	20	2000	356.0	356.0	45.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN65LBC172AN	N	PDIP	16	25	506	13.97	11230	4.32
SN65LBC172AN.A	N	PDIP	16	25	506	13.97	11230	4.32
SN65LBC172ANE4	N	PDIP	16	25	506	13.97	11230	4.32

# GENERIC PACKAGE VIEW

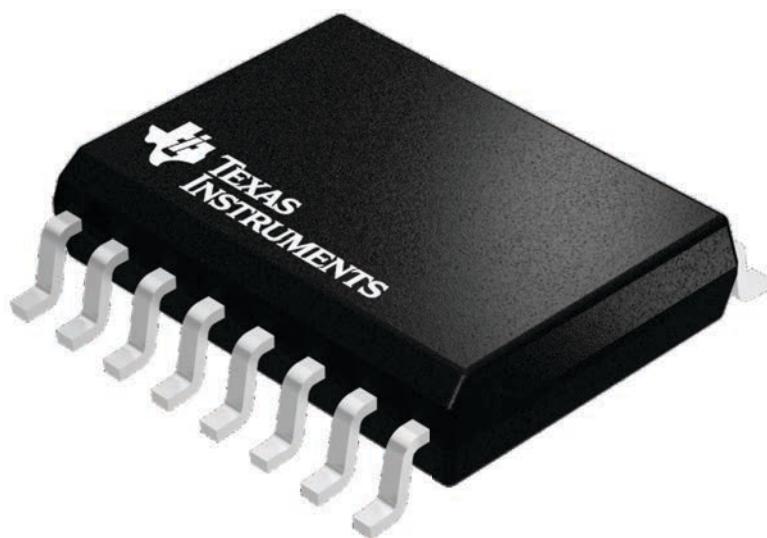
**DW 16**

**SOIC - 2.65 mm max height**

**7.5 x 10.3, 1.27 mm pitch**

**SMALL OUTLINE INTEGRATED CIRCUIT**

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4224780/A

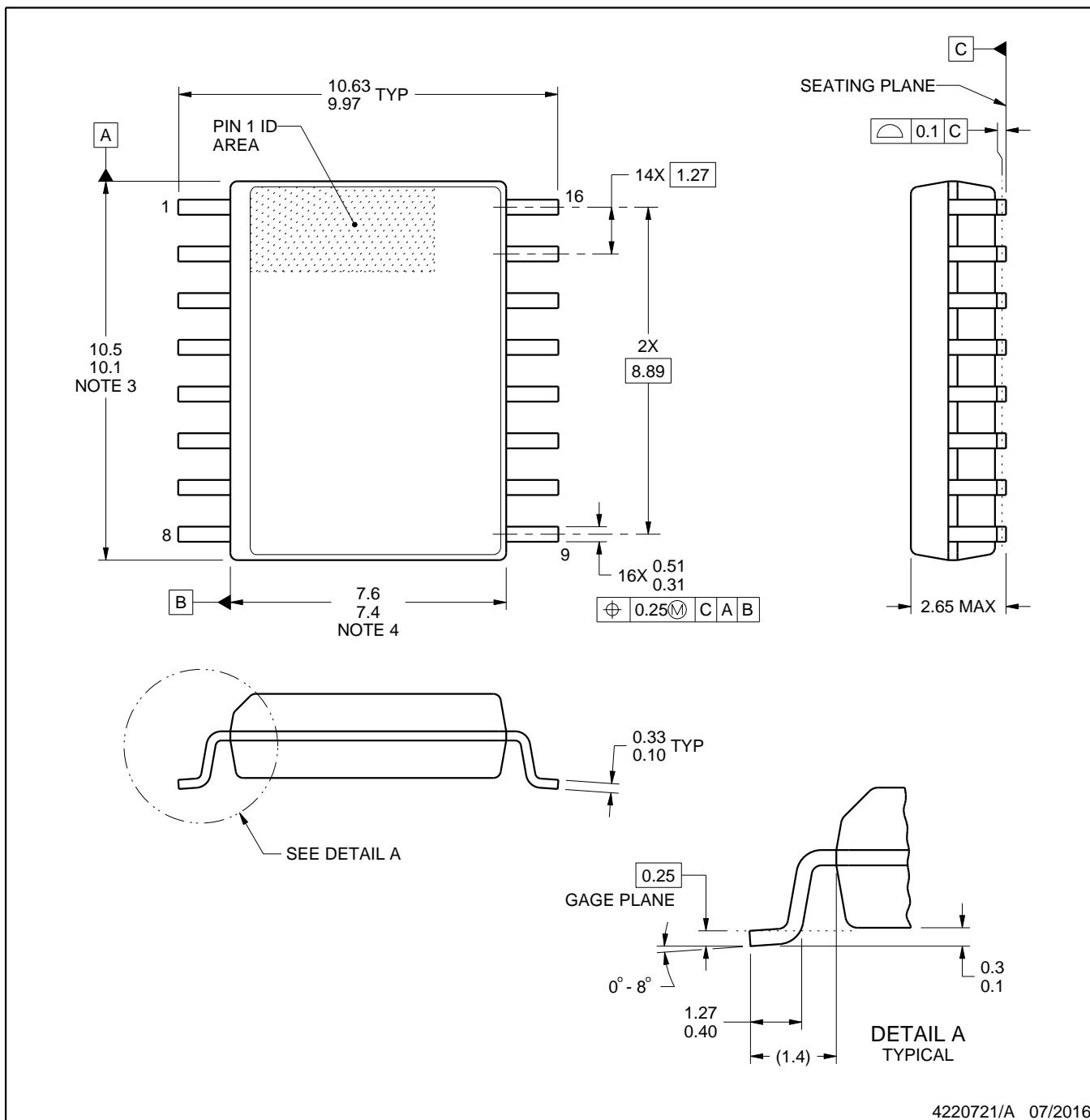


# PACKAGE OUTLINE

DW0016A

SOIC - 2.65 mm max height

SOIC



4220721/A 07/2016

## NOTES:

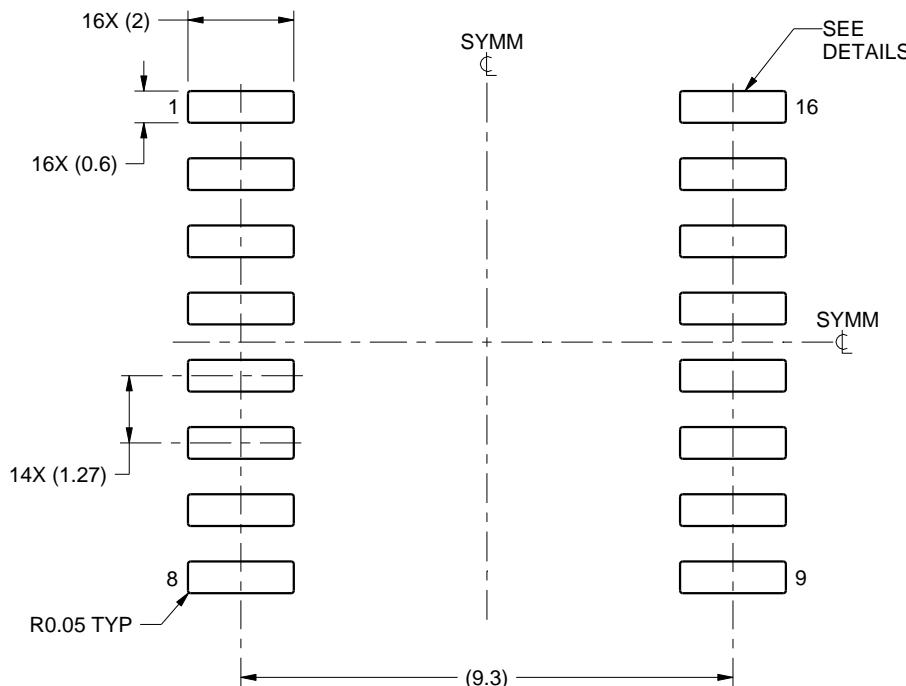
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

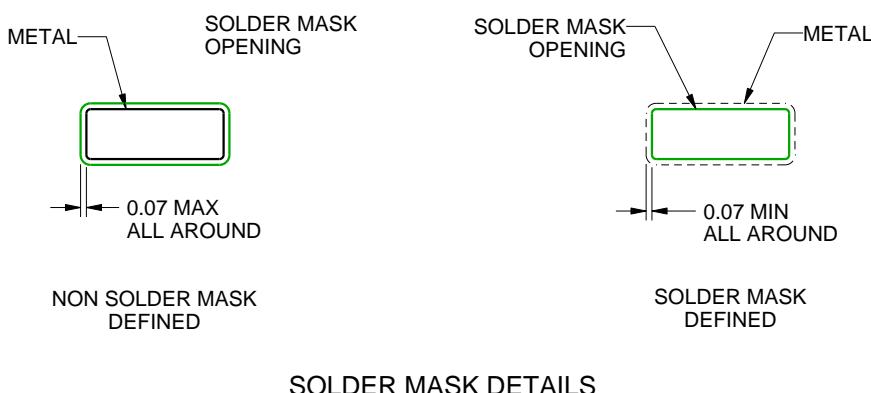
DW0016A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:7X



4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

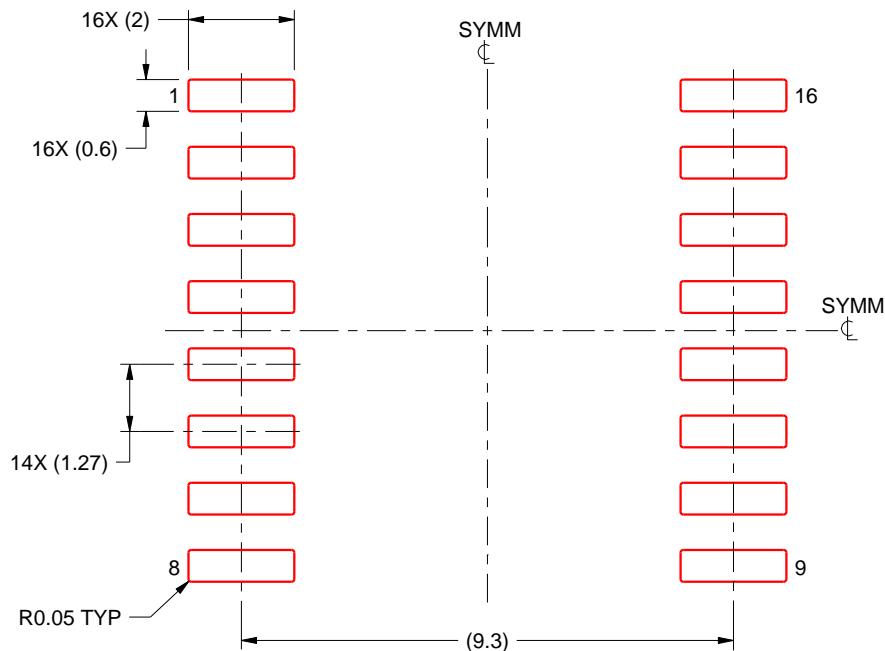
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0016A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:7X

4220721/A 07/2016

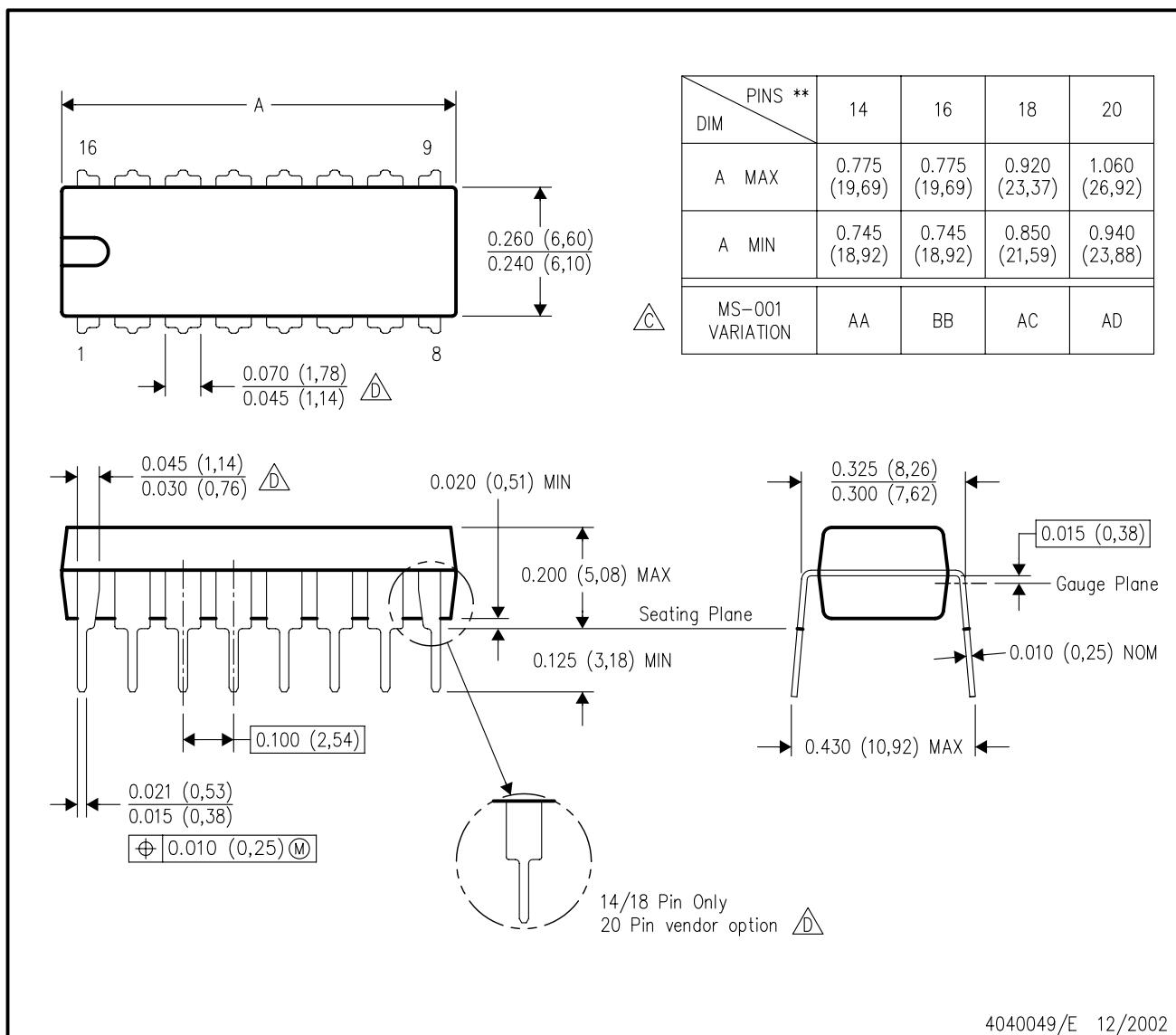
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.

△ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

△ The 20 pin end lead shoulder width is a vendor option, either half or full width.

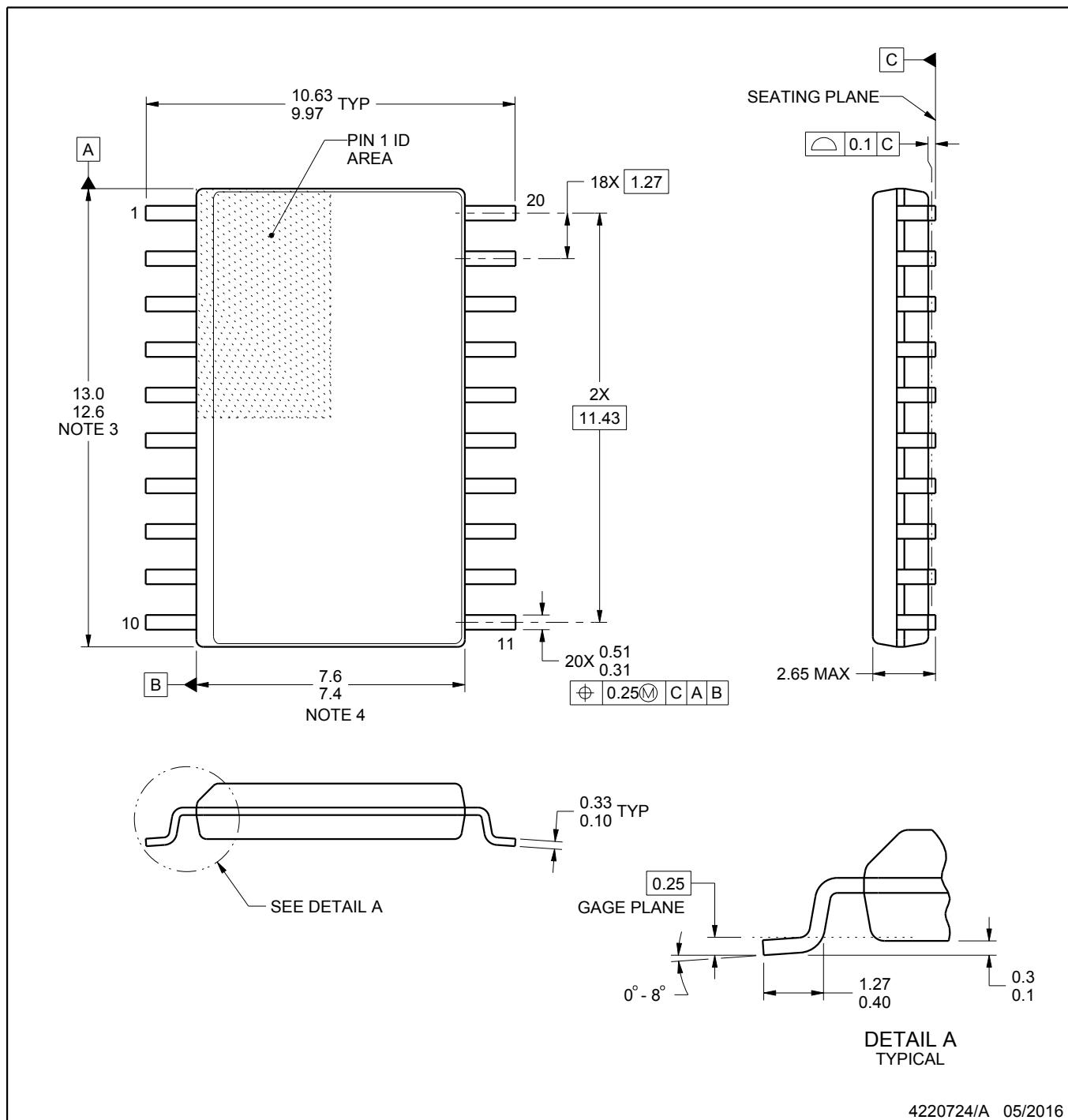


## PACKAGE OUTLINE

**DW0020A**

## **SOIC - 2.65 mm max height**

SOIG



## NOTES:

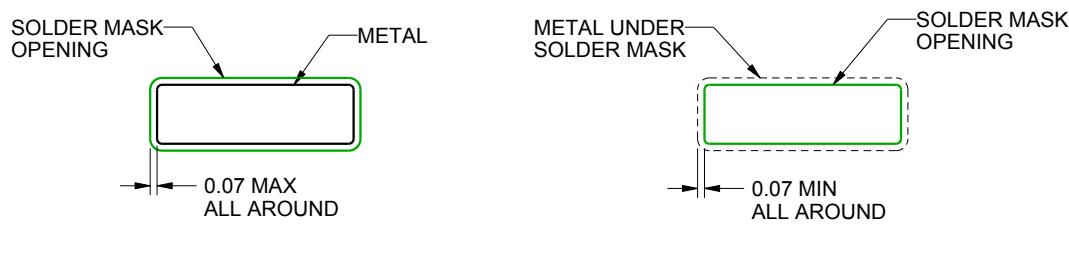
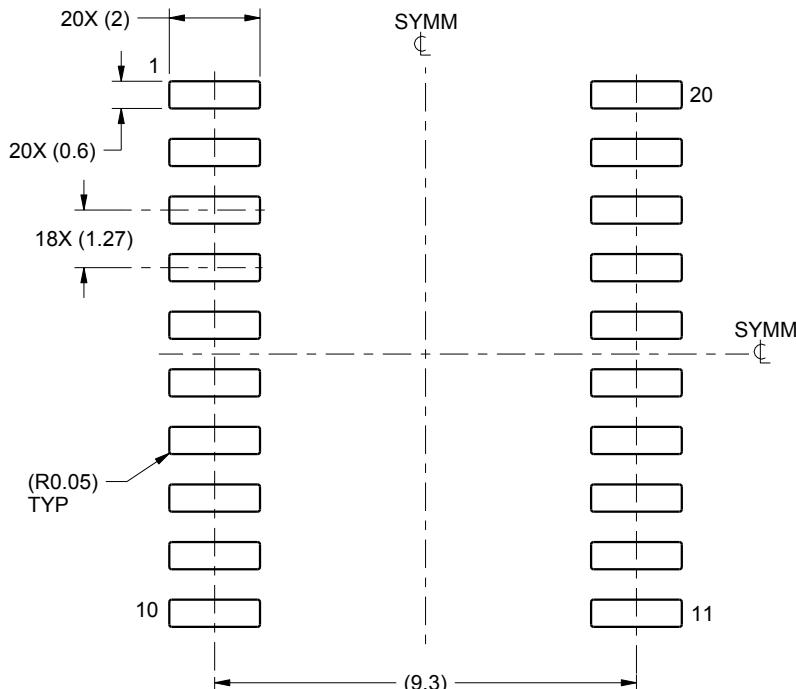
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

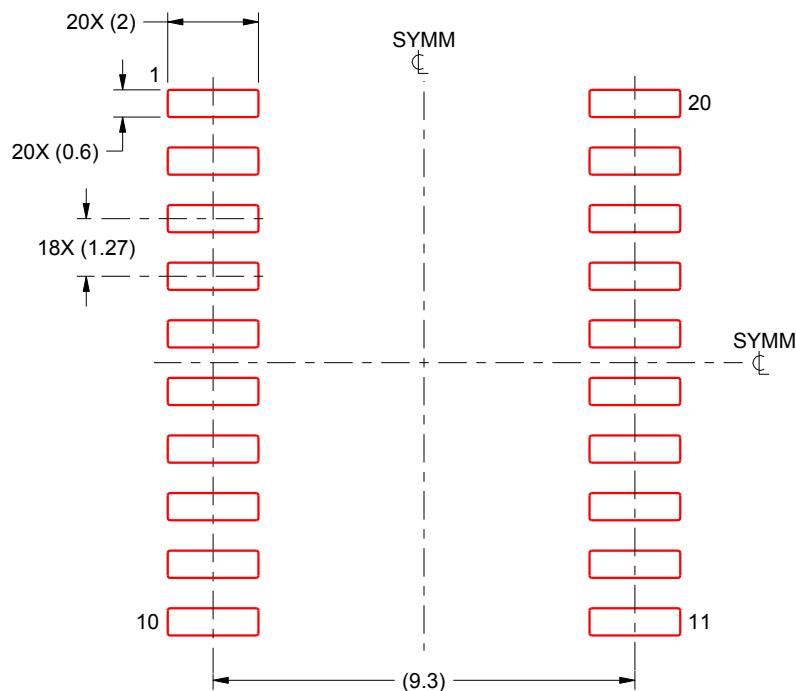
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2025, Texas Instruments Incorporated