# 4 X 11 W SINGLE-ENDED OR 2 X 22 W POWER AMPLIFIER

## GENERAL DESCRIPTION

The TDA1554Q is an integrated class-B output amplifier in a 17-lead single-in-line (SIL) plastic power package. The circuit contains 4 x 11 W single-ended or 2 x 22 W bridge amplifiers. The device is primarily developed for car radio applications.

### Features

- Requires very few external components
- Flexibility in use – Quad single-ended or stereo BTL
- High output power
- Low offset voltage at outputs (important for BTL)
- Fixed gain
- Good ripple rejection
- Mute/stand-by switch
- Load dump protection
- AC and DC short-circuit-safe to ground and $V_P$
- Thermally protected
- Reverse polarity safe
- Capability to handle high energy on outputs ($V_P$ = 0 V)
- Protected against electrostatic discharge
- No switch-on/switch-off plop
- Low thermal resistance
- Identical inputs (inverting and non-inverting)
- Flexible leads

## QUICK REFERENCE DATA

| parameter | conditions | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|---|
| Supply voltage range operating | | $V_P$ | 6.0 | 14.4 | 18.0 | V |
| Repetitive peak output current | | $I_{ORM}$ | – | – | 4 | A |
| Total quiescent current | | $I_{tot}$ | – | 80 | 160 | mA |
| Stand-by current | | $I_{sb}$ | – | 0.1 | 100 | μA |
| **Stereo BTL application** | | | | | | |
| Output power | $R_L$ = 4 Ω; THD = 10% | $P_o$ | 20 | 22 | – | W |
| Supply voltage ripple rejection | | RR | 48 | – | – | dB |
| Noise output voltage (RMS value) | $R_S$ = 0 Ω | $V_{no(rms)}$ | – | 70 | – | μV |
| Input impedance | | $\|Z_I\|$ | 25 | 30 | 38 | kΩ |
| DC output offset voltage | | $\|\Delta V_O\|$ | – | – | 100 | mV |
| **Quad single-ended application** | | | | | | |
| Output power | THD = 10% | | | | | |
| | $R_L$ = 4 Ω | $P_o$ | – | 6 | – | W |
| | $R_L$ = 2 Ω | $P_o$ | – | 11 | – | W |
| Supply voltage ripple rejection | | RR | 48 | – | – | dB |
| Noise output voltage (RMS value) | $R_S$ = 0 Ω | $V_{no(rms)}$ | – | 50 | – | μV |
| Input impedance | | $\|Z_I\|$ | 50 | 60 | 75 | kΩ |

## PACKAGE OUTLINE

17-lead SIL-bent-to-DIL; plastic power (SOT243R).

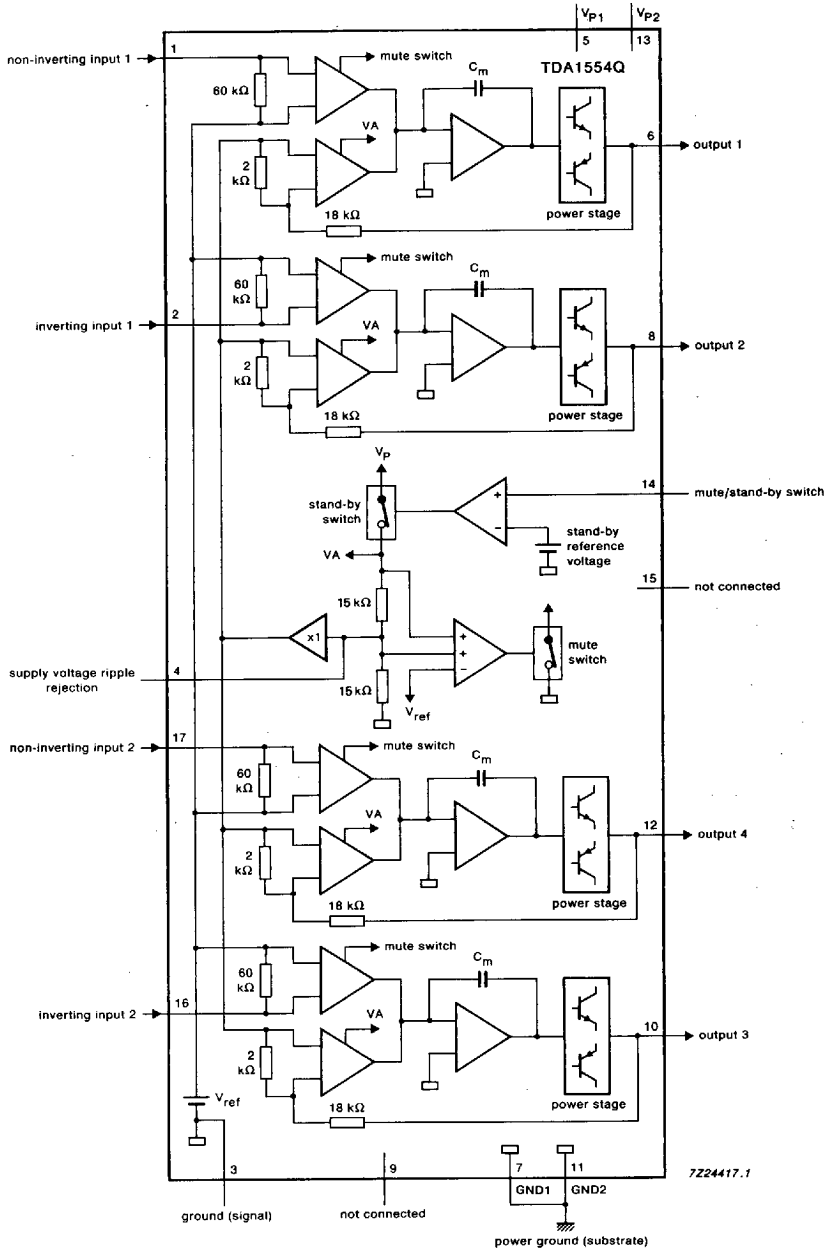


Fig.1 Block diagram.

## PINNING

| | | |
|---|---|---|
| 1 | NINV1 | non-inverting input 1 |
| 2 | INV1 | inverting input 1 |
| 3 | GND | ground (signal) |
| 4 | RR | supply voltage ripple rejection |
| 5 | $V_{P1}$ | positive supply voltage 1 |
| 6 | OUT1 | output 1 |
| 7 | GND1 | power ground 1 (substrate) |
| 8 | OUT2 | output 2 |
| 9 | n.c. | not connected |
| 10 | OUT3 | output 3 |
| 11 | GND2 | power ground 2 (substrate) |
| 12 | OUT4 | output 4 |
| 13 | $V_{P2}$ | positive supply voltage 2 |
| 14 | M/SS | mute/stand-by switch |
| 15 | n.c. | not connected |
| 16 | INV2 | inverting input 2 |
| 17 | NINV2 | non-inverting input 2 |

## FUNCTIONAL DESCRIPTION

The TDA1554Q contains four identical amplifiers with differential input stages (two inverting and two non-inverting) and can be used for single-ended or bridge applications. The gain of each amplifier is fixed at 20 dB (26 dB in BTL). A special feature of this device is:

**Mute/stand-by switch**

- low stand-by current ($< 100\ \mu A$)
- low mute/stand-by switching current (low cost supply switch)
- mute facility

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| parameter | conditions | symbol | min. | max. | unit |
|---|---|---|---|---|---|
| Supply voltage | | | | | |
| operating | | $V_P$ | – | 18 | V |
| non-operating | | $V_P$ | – | 30 | V |
| load dump protected | during 50 ms; $t_r \geqslant 2.5$ ms | $V_P$ | – | 45 | V |
| Non-repetitive peak output current | | $I_{OSM}$ | – | 6 | A |
| Repetitive peak output current | | $I_{ORM}$ | – | 4 | A |
| Storage temperature range | | $T_{stg}$ | −55 | + 150 | °C |
| Junction temperature | | $T_j$ | – | 150 | °C |
| AC and DC short-circuit-safe voltage | | $V_{PSC}$ | – | 18 | V |
| Energy handling capability at outputs | $V_P = 0$ V | | – | 200 | mJ |
| Reverse polarity | | $V_{PR}$ | – | 6 | V |
| Total power dissipation | see Fig.2 | $P_{tot}$ | – | 60 | W |

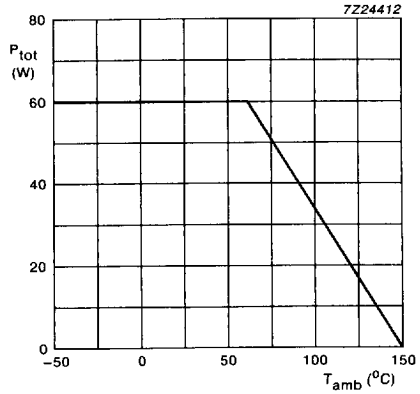


Fig.2 Power derating curve.

## DC CHARACTERISTICS

$V_P$ = 14.4 V; $T_{amb}$ = 25 °C; measurements taken using Fig.4; unless otherwise specified

| parameter | conditions | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|---|
| **Supply** | | | | | | |
| Supply voltage range | note 1 | $V_P$ | 6.0 | 14.4 | 18.0 | V |
| Total quiescent current | | $I_{tot}$ | – | 80 | 160 | mA |
| DC output voltage | note 2 | $V_O$ | – | 6.9 | – | V |
| DC output offset voltage | | $\lvert\Delta V_O\rvert$ | – | – | 100 | mV |
| **Mute/stand-by switch** | | | | | | |
| Switch-on voltage level | | $V_{ON}$ | 8.5 | – | – | V |
| **Mute condition** | | $V_{mute}$ | 3.3 | – | 6.4 | V |
| Output signal in mute position | $V_I$ = 1 V (max); f = 1 kHz | $V_O$ | – | – | 2 | mV |
| DC output offset voltage (between pins 6 to 8 and 10 to 12) | | $\lvert\Delta V_O\rvert$ | – | – | 100 | mV |
| **Stand-by condition** | | $V_{sb}$ | 0 | – | 2 | V |
| DC current in stand-by condition | | $I_{sb}$ | – | – | 100 | μA |
| Switch-on current | | $I_{sw}$ | – | 12 | 40 | μA |

## AC CHARACTERISTICS

$V_P$ = 14.4 V; $R_L$ = 4 Ω; f = 1 kHz; $T_{amb}$ = 25 °C; measurements taken using Fig.3 for stereo BTL application and Fig.4 for quad single-ended application unless otherwise specified

| parameter | conditions | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|---|
| **Stereo BTL application** | | | | | | |
| Output power | THD = 0.5% | $P_O$ | 15 | 17 | – | W |
| | THD = 10% | $P_O$ | 20 | 22 | – | W |
| Output power at $V_P$ = 13.2 V | THD = 0.5% | $P_O$ | – | 12 | – | W |
| | THD = 10% | $P_O$ | – | 17 | – | W |
| Total harmonic distortion | $P_O$ = 1 W | THD | – | 0.1 | – | % |
| Power bandwidth | THD = 0.5%<br>$P_O$ = −1 dB<br>w.r.t. 15 W | $B_W$ | – | 20 to 15 000 | – | Hz |
| Low frequency roll-off | note 3<br>−1 dB | $f_L$ | – | 45 | – | Hz |
| High frequency roll-off | −1 dB | $f_H$ | 20 | – | – | kHz |
| Closed loop voltage gain | | $G_V$ | 25 | 26 | 27 | dB |
| Supply voltage ripple rejection | note 4 | | | | | |
| ON | | RR | 48 | – | – | dB |
| mute | | RR | 48 | – | – | dB |
| stand-by | | RR | 80 | – | – | dB |
| Input impedance | | $\|Z_i\|$ | 25 | 30 | 38 | kΩ |
| Noise output voltage (RMS value) | | | | | | |
| ON | $R_S$ = 0 Ω; note 5 | $V_{no(rms)}$ | – | 70 | – | μV |
| ON | $R_S$ = 10 kΩ; note 5 | $V_{no(rms)}$ | – | 100 | 200 | μV |
| mute | notes 5 and 6 | $V_{no(rms)}$ | – | 60 | – | μV |
| Channel separation | $R_S$ = 10 kΩ | α | 40 | – | – | dB |
| Channel unbalance | | $\|\Delta G_V\|$ | – | – | 1 | dB |

| parameter | conditions | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|---|
| **Quad single-ended application** | | | | | | |
| Output power | note 7 | | | | | |
| | THD = 0.5% | $P_o$ | 4 | 5 | – | W |
| | THD = 10% | $P_o$ | 5.5 | 6 | – | W |
| Output power at $R_L$ = 2 Ω | note 7 | | | | | |
| | THD = 0.5% | $P_o$ | 7.5 | 8.5 | – | W |
| | THD = 10% | $P_o$ | 10 | 11 | – | W |
| Total harmonic distortion | $P_o$ = 1 W | THD | – | 0.1 | – | % |
| Low frequency roll-off | note 3 | | | | | |
| | −3 dB | $f_L$ | – | 45 | – | Hz |
| High frequency roll-off | −1 dB | $f_H$ | 20 | – | – | kHz |
| Closed loop voltage gain | | $G_v$ | 19 | 20 | 21 | dB |
| Supply voltage ripple rejection | note 4 | | | | | |
| ON | | RR | 48 | – | – | dB |
| mute | | RR | 48 | – | – | dB |
| stand-by | | RR | 80 | – | – | dB |
| Input impedance | | $\|Z_i\|$ | 50 | 60 | 75 | kΩ |
| Noise output voltage (RMS value) | | | | | | |
| ON | $R_S$ = 0 Ω; note 5 | $V_{no(rms)}$ | – | 50 | – | μV |
| ON | $R_S$ = 10 kΩ; note 5 | $V_{no(rms)}$ | – | 70 | 100 | μV |
| mute | notes 5 and 6 | $V_{no(rms)}$ | – | 50 | – | μV |
| Channel separation | $R_S$ = 10 kΩ | α | 40 | – | – | dB |
| Channel unbalance | | $\|\Delta G_v\|$ | – | – | 1 | dB |

**Notes to the characteristics**

1. The circuit is DC adjusted at $V_P$ = 6 V to 18 V and AC operating at $V_P$ = 8.5 V to 18 V.
2. At 18 V < $V_P$ < 30 V the DC output voltage ⩽ $V_P/2$.
3. Frequency response externally fixed.
4. Ripple rejection measured at the output with a source impedance of 0 Ω (maximum ripple amplitude of 2 V) and a frequency between 100 Hz and 10 kHz.
5. Noise voltage measured in a bandwidth of 20 Hz to 20 kHz.
6. Noise output voltage independent of $R_S$ ($V_I$ = 0 V).
7. Output power is measured directly at the output pins of the IC.

## APPLICATION INFORMATION

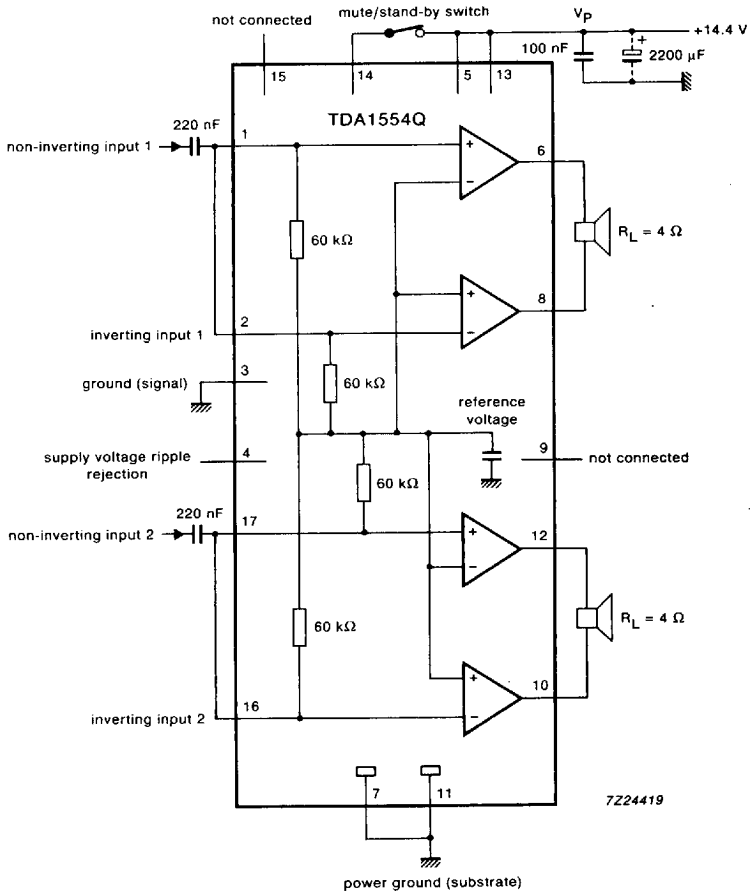


Fig.3 Stereo BTL application circuit diagram.

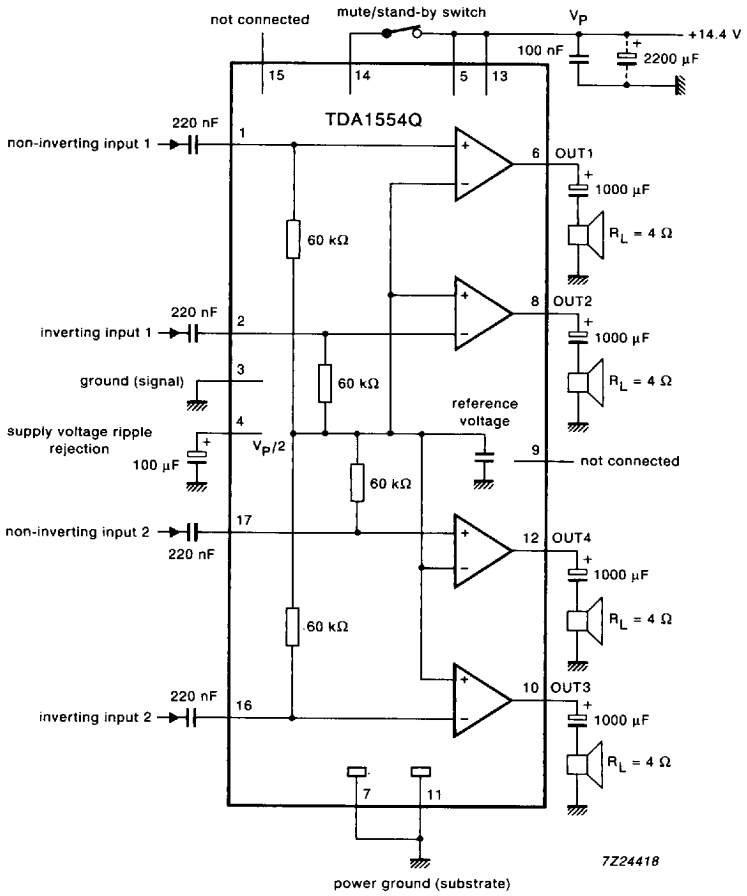


Fig.4 Quad single-ended application circuit diagram.