CS5342

105 dB, 192 kHz, Multi-bit Audio A/D Converter

Features

- Advanced Multi-bit Delta-Sigma Architecture
- 24-bit Conversion
- Supports all audio sample rates including 192 kHz.
- 105 dB Dynamic Range at 5 V
- -98 dB THD+N
- High-pass Filter to Remove DC Offsets
- Analog/Digital Core Supplies From 3.3 V to 5 V
- Supports logic levels between 2.5 V and 5 V.
- Low-latency Digital Filter
- Automatic Mode Selection
- Supports 384x MCLK/LRCK Ratios.

General Description

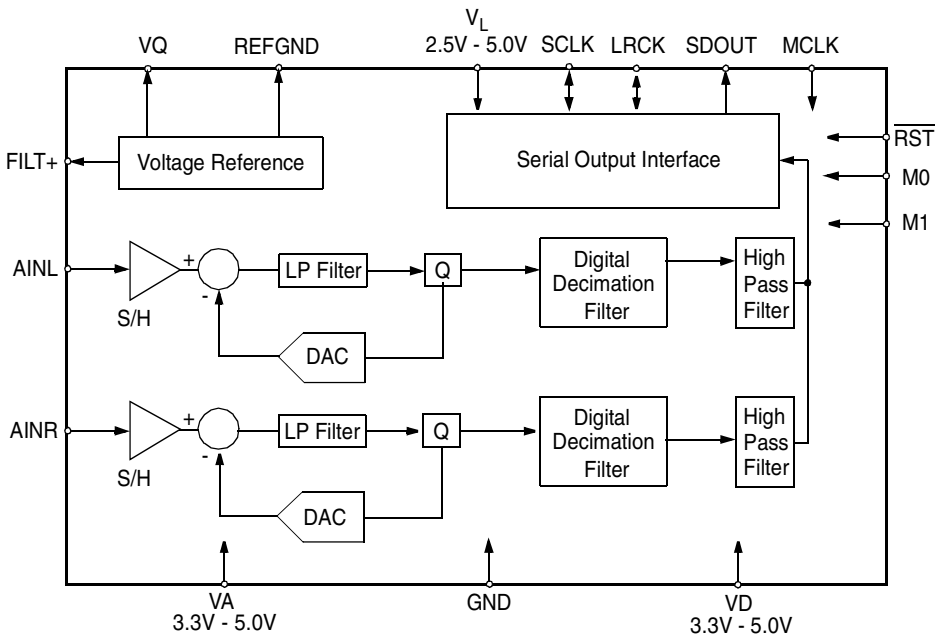
The CS5342 is a complete analog-to-digital converter for digital audio systems. It performs sampling, analog-to-digital conversion and anti-alias filtering, generating 24-bit values for both left and right inputs in serial form at sample rates up to 200 kHz per channel.

The CS5342 uses a 5th-order, multi-bit Delta-Sigma modulator followed by digital filtering and decimation, which removes the need for an external anti-alias filter.

The CS5342 is ideal for audio systems requiring wide dynamic range, negligible distortion and low noise, such as set-top boxes, DVD-karaoke players, DVD recorders, A/V receivers, and automotive applications.

ORDERING INFORMATION

CS5342-CZZ	Lead-free	-10° to 70° C	16-pin TSSOP
CS5342-DZZ	Lead-free	-40° to 85° C	16-pin TSSOP
CDB5342			Evaluation Board



Preliminary Product Information | This document contains information for a new product. Cirrus Logic reserves the right to modify this product without notice.

TABLE OF CONTENTS

Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative.
To find one nearest you go to **www.cirrus.com/**

LIST OF FIGURES

LIST OF TABLES

1 CHARACTERISTICS AND SPECIFICATIONS

(All Min/Max characteristics and specifications are guaranteed over the Specified Operating Conditions. Typical performance characteristics and specifications are derived from measurements taken at typical supply voltages and T_A = 25°C.)

SPECIFIED OPERATING CONDITIONS

(GND = 0 V, all voltages with respect to 0 V.)

Parameter		Symbol	Min	Typ	Max	Unit
Power Supplies (Notes 2, 3)	Analog	VA	3.14	(Note 1)	5.25	V
	Digital	VD	3.14	3.3	5.25	V
	Logic	VL	2.38	3.3	5.25	V
Ambient Operating Temperature	Commercial (-CZZ)	T_{AC}	-10	-	70	°C

Notes: 1. This part is specified at typical analog voltages of 3.3 V and 5.0 V. See *Analog Characteristics (CS5342-CZZ)* below for details.

2. In Quad-Speed Slave Mode, the CS5342 is only specified for operation with VA and VD at 5 V, ±5%.

ABSOLUTE MAXIMUM RATINGS

(GND = 0 V, All voltages with respect to ground.) (Note 3)

Parameter		Symbol	Min	Max	Units
DC Power Supplies:	Analog	VA	-0.3	+6.0	V
	Logic	VL	-0.3	+6.0	V
	Digital	VD	-0.3	+6.0	V
Input Current	(Note 4)	I_{in}	-	±10	mA
Analog Input Voltage	(Note 5)	V_{IN}	GND-0.7	VA+0.7	V
Digital Input Voltage	(Note 5)	V_{IND}	-0.7	VL+0.7	V
Ambient Operating Temperature (Power Applied)		T_A	-50	+95	°C
Storage Temperature		T_{stg}	-65	+150	°C

Notes: 3. Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

4. Any pin except supplies. Transient currents of up to ±100 mA on the analog input pins will not cause SRC latch-up.

5. The maximum over/under voltage is limited by the input current.

ANALOG CHARACTERISTICS (CS5342-CZZ) Test conditions (unless otherwise specified):

Input test signal is a 1 kHz sine wave; measurement bandwidth is 10 Hz to 20 kHz.

Parameter		Symbol	Min	Typ	Max	Unit
VA = 3.3 V						
Single Speed Mode Fs = 48 kHz						
Dynamic Range	A-weighted		96	102	-	dB
	unweighted		93	99	-	dB
Total Harmonic Distortion + Noise	(Note 6)	THD+N				
	-1 dB		-	-95	-89	dB
	-20 dB		-	-79	-	dB
	-60 dB		-	-39	-	dB
Double Speed Mode Fs = 96 kHz						
Dynamic Range	A-weighted		96	102	-	dB
	unweighted		93	99	-	dB
40 kHz bandwidth	unweighted		-	96	-	dB
Total Harmonic Distortion + Noise	(Note 6)	THD+N				
	-1 dB		-	-95	-89	dB
	-20 dB		-	-79	-	dB
	-60 dB		-	-39	-	dB
40 kHz bandwidth	-1 dB		-	-87	-	dB
Quad Speed Mode (Note 2) Fs = 192 kHz						
Dynamic Range	A-weighted		96	102	-	dB
	unweighted		93	99	-	dB
40 kHz bandwidth	unweighted		-	96	-	dB
Total Harmonic Distortion + Noise	(Note 6)	THD+N				
	-1 dB		-	-95	-89	dB
	-20 dB		-	-79	-	dB
	-60 dB		-	-39	-	dB
40 kHz bandwidth	-1 dB		-	-87	-	dB
VA = 5.0 V						
Single Speed Mode Fs = 48 kHz						
Dynamic Range	A-weighted		99	105	-	dB
	unweighted		96	102	-	dB
Total Harmonic Distortion + Noise	(Note 6)	THD+N				
	-1 dB		-	-98	-92	dB
	-20 dB		-	-82	-	dB
	-60 dB		-	-42	-	dB
Double Speed Mode Fs = 96 kHz						
Dynamic Range	A-weighted		99	105	-	dB
	unweighted		96	102	-	dB
40 kHz bandwidth	unweighted		-	99	-	dB
Total Harmonic Distortion + Noise	(Note 6)	THD+N				
	-1 dB		-	-98	-92	dB
	-20 dB		-	-82	-	dB
	-60 dB		-	-42	-	dB
40 kHz bandwidth	-1 dB		-	-95	-	dB

Quad Speed Mode (Note 2) Fs = 192 kHz						
Dynamic Range	A-weighted		99	105	-	dB
	unweighted		96	102	-	dB
40 kHz bandwidth	unweighted		-	99	-	dB
Total Harmonic Distortion + Noise	(Note 6)	THD+N				
	-1 dB		-	-98	-92	dB
	-20 dB		-	-82	-	dB
	-60 dB		-	-42	-	dB
40 kHz bandwidth	-1 dB		-	-95	-	dB
Dynamic Performance for All Modes						
Interchannel Isolation			-	90	-	dB
DC Accuracy						
Interchannel Gain Mismatch			-	0.1	-	dB
Gain Error			-3	-	3	%
Gain Drift			-	±100	-	ppm/°C
Analog Input Characteristics						
Full-scale Input Voltage			0.54*VA	0.56*VA	0.58*VA	Vpp
Input Impedance			18	-	-	kΩ

Note: 6. Referred to the typical full-scale input voltage

DIGITAL FILTER CHARACTERISTICS

Parameter (Note 7)	Symbol	Min	Typ	Max	Unit
Single Speed Mode					
Passband (-0.1 dB)		0	-	0.4896	Fs
Passband Ripple		-0.1	-	0.035	dB
Stopband		0.5688	-	-	Fs
Stopband Attenuation		70	-	-	dB
Total Group Delay (Fs = Output Sample Rate)	t_{gd}	-	12/Fs	-	s
Double Speed Mode					
Passband (-0.1 dB)		0	-	0.4896	Fs
Passband Ripple		-0.1	-	0.058	dB
Stopband		0.5604	-	-	Fs
Stopband Attenuation		69	-	-	dB
Total Group Delay (Fs = Output Sample Rate)	t_{gd}	-	9/Fs	-	s
Quad Speed Mode **(Note 2)**					
Passband (-0.1 dB)		0	-	0.2604	Fs
Passband Ripple		-0.1	-	0.058	dB
Stopband		0.5000	-	-	Fs
Stopband Attenuation		60	-	-	dB
Total Group Delay (Fs = Output Sample Rate)	t_{gd}	-	5/Fs	-	s
High Pass Filter Characteristics					
Frequency Response -3.0 dB		-	1	-	Hz
-0.13 dB (Note 7)			20	-	Hz
Phase Deviation @ 20 Hz (Note 7)		-	10	-	Deg
Passband Ripple		-	-	0	dB
Filter Settling Time			10^5/Fs		s

Note: 7. Response is clock dependent and will scale with Fs. Note that the response plots (Figures 1 to 12) are normalized to Fs and can be de-normalized by multiplying the X-axis scale by Fs.

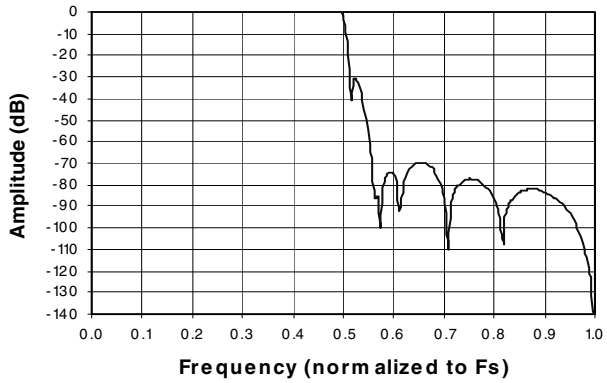


Figure 1. Single Speed Stopband Rejection

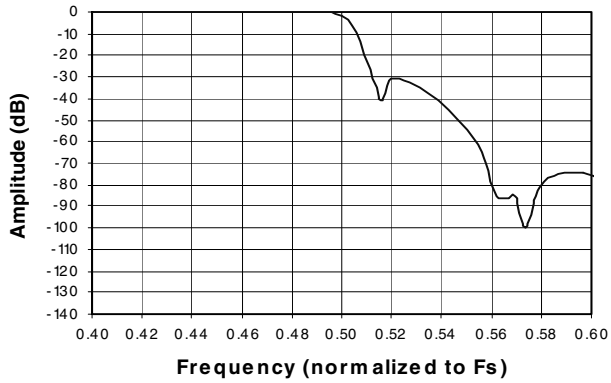


Figure 2. Single Speed Stopband Rejection (detail)

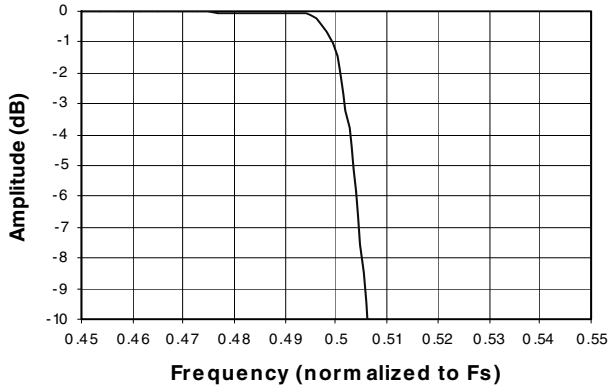


Figure 3. Single Speed Transition Band (detail)

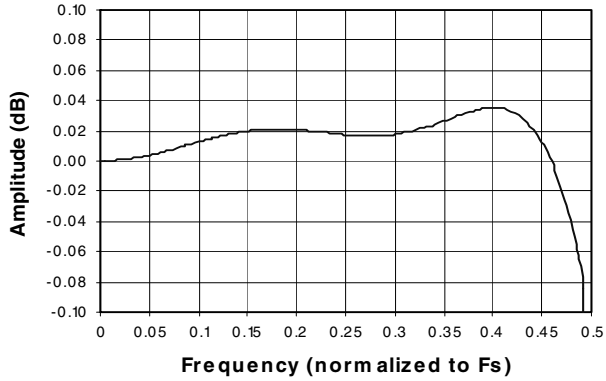


Figure 4. Single Speed Passband Ripple

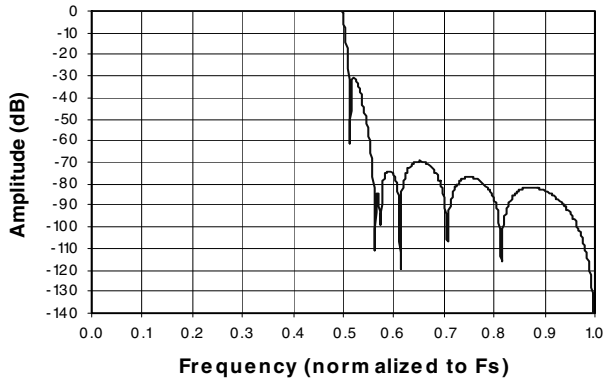


Figure 5. Double Speed Stopband Rejection

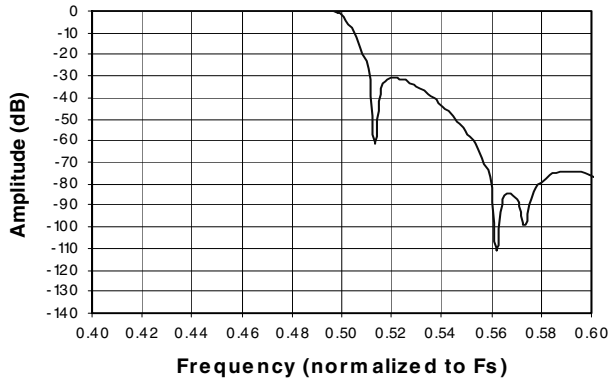


Figure 6. Double Speed Stopband Rejection (detail)

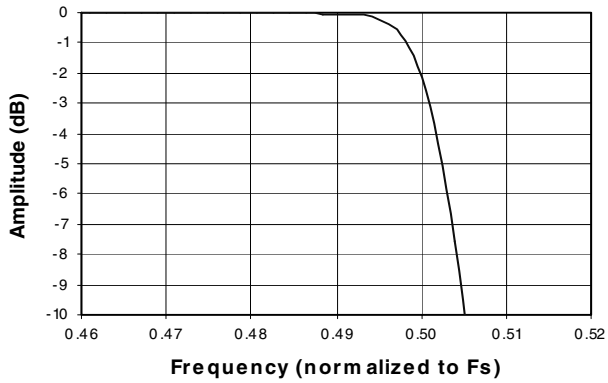


Figure 7. Double Speed Transition Band (detail)

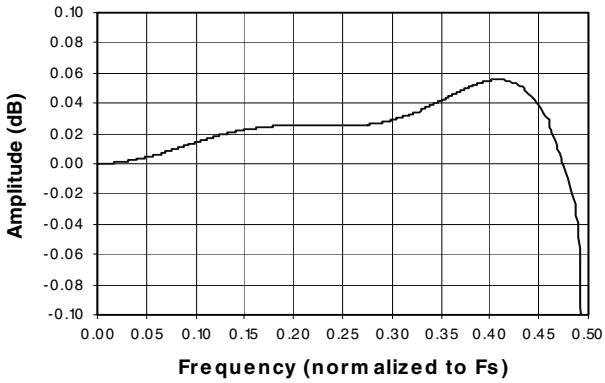


Figure 8. Double Speed Passband Ripple

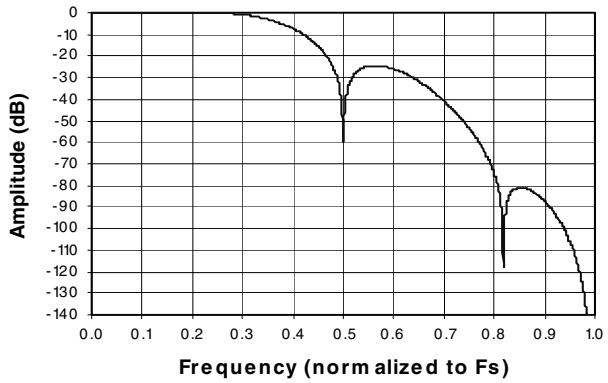


Figure 9. Quad Speed Stopband Rejection

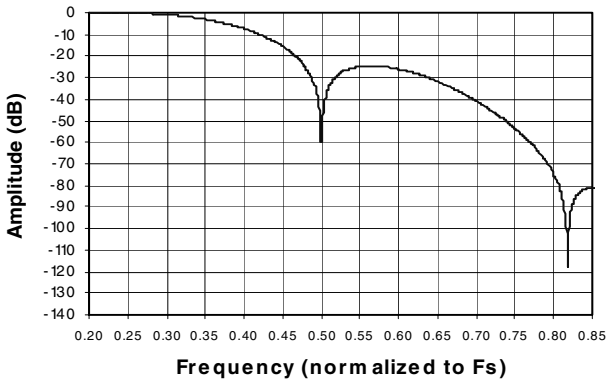


Figure 10. Quad Speed Stopband Rejection (detail)

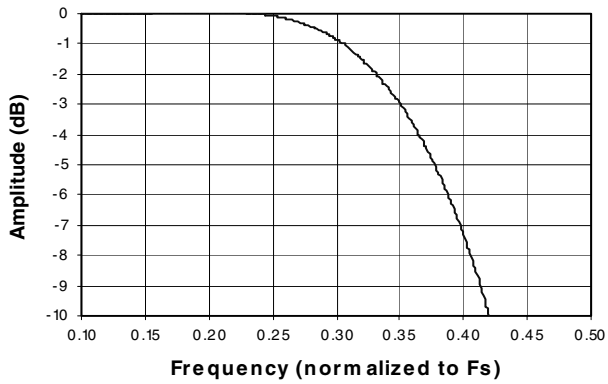


Figure 11. Quad Speed Transition Band (detail)

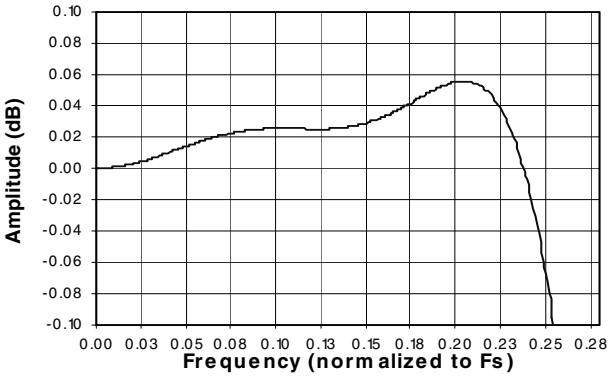


Figure 12. Quad Speed Passband Ripple

DC ELECTRICAL CHARACTERISTICS (GND = 0 V, all voltages with respect to 0 V. MCLK=18.432 MHz; Master Mode; refer to Note 2)

Parameter		Symbol	Min	Typ	Max	Unit
DC Power Supplies:	Positive Analog	VA	3.14	-	5.25	V
	Positive Digital	VD	3.14	-	5.25	V
	Positive Logic	VL	2.38	-	5.25	V
Power Supply Current	VA = 5 V	I_A	-	21	23.1	mA
(Normal Operation)	VA = 3.3 V	I_A	-	18.2	20	mA
	VL,VD = 5 V	I_D	-	15	16.5	mA
	VL,VD = 3.3 V	I_D	-	9	10	mA
Power Supply Current	VA = 5 V	I_A	-	1.5	-	mA
(Power-down Mode) (Note 8)	VL,VD=5 V	I_D	-	0.4	-	mA
Power Consumption	VL, VD, VA = 5 V	-	-	180	198	mW
(Normal Operation)	VL, VD, VA = 3.3 V	-	-	90	100	mW
	(Power-Down Mode)	-	-	9.5	-	mW
Power Supply Rejection Ratio (1 kHz)	(Note 9)	PSRR	-	65	-	dB
V_Q Nominal Voltage			-	VA÷2	-	V
Output Impedance			-	25	-	kΩ
Filt+ Nominal Voltage			-	VA	-	V
Output Impedance			-	36	-	kΩ
Maximum allowable DC current source/sink			-	0.01	-	mA

Notes: 8. Power-down Mode is defined as $\overline{RST}$ = Low with all clocks and data lines held static.

9. Valid with the recommended capacitor values on FILT+ and VQ as shown in the “Typical Connection Diagram”.

DIGITAL CHARACTERISTICS

Parameter		Symbol	Min	Typ	Max	Units
High-level Input Voltage	(% of VL)	V_{IH}	70%	-	-	V
Low-level Input Voltage	(% of VL)	V_{IL}	-	-	30%	V
High-level Output Voltage at I_o = 100 µA	(% of VL)	V_{OH}	70%	-	-	V
Low-level Output Voltage at I_o =100 µA	(% of VL)	V_{OL}	-	-	15%	V
Input Leakage Current		I_{in}	-	-	±10	µA

THERMAL CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Allowable Junction Temperature		-	-	135	°C
Junction-to-ambient Thermal Impedance	θ_{JA}	-	75	-	°C/W

SWITCHING CHARACTERISTICS - SERIAL AUDIO PORT (Logic "0" = GND = 0 V; Logic "1" = VL, C_L = 20 pF)

Parameter	Symbol	Min	Typ	Max	Unit
MCLK Specifications					
MCLK Period	t_{clkw}	26	-	31	ns
		52	-	1303	ns
MCLK Pulse Duty Cycle		40	-	60	%
Master Mode					
SCLK falling to LRCK	t_{mslr}	-20	-	20	ns
SCLK falling to SDOUT valid	t_{sdo}	-	-	32	ns
SCLK Duty Cycle Single-Speed		-	50	-	%
Double-Speed		-	50	-	%
Quad-Speed		-	33	-	%
Slave Mode					
Single Speed*					
LRCK Duty Cycle		40	-	60	%
SCLK Period	t_{sclkw}	290	-	-	ns
SCLK Duty Cycle		45	-	55	%
SDOUT valid before SCLK rising	t_{stp}	10	-	-	ns
SDOUT valid after SCLK rising	t_{hld}	5	-	-	ns
SCLK falling to LRCK edge	t_{slrd}	-20	-	20	ns
Double Speed*					
LRCK Duty Cycle		40	-	60	%
SCLK Period (Note 9)	t_{sclkw}	193	-	-	ns
SCLK Duty Cycle		45	-	55	%
SDOUT valid before SCLK rising	t_{stp}	10	-	-	ns
SDOUT valid after SCLK rising	t_{hld}	5	-	-	ns
SCLK falling to LRCK edge	t_{slrd}	-20	-	20	ns
Quad Speed* **(Note 2)**					
LRCK Duty Cycle		40	-	60	%
SCLK Period (Note 9)	t_{sclkw}	104	-	-	ns
SCLK Duty Cycle		40	-	50	%
SDOUT valid before SCLK rising	t_{stp}	10	-	-	ns
SDOUT valid after SCLK rising	t_{hld}	5	-	-	ns
SCLK falling to LRCK edge	t_{slrd}	-8	-	8	ns

* For a description of Speed Modes, please refer to Table 1 on page 15

Notes: 9. SCLK must be derived synchronously from MCLK and the ratio of SCLK/LRCK must be equal to 48.

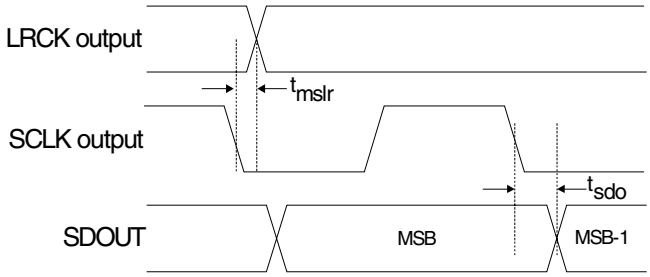


Figure 13. Master Mode, Left Justified SAI

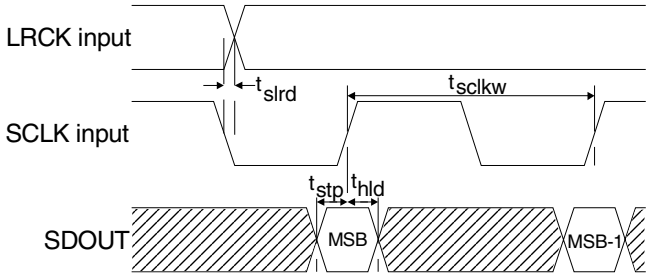


Figure 14. Slave Mode, Left Justified SAI

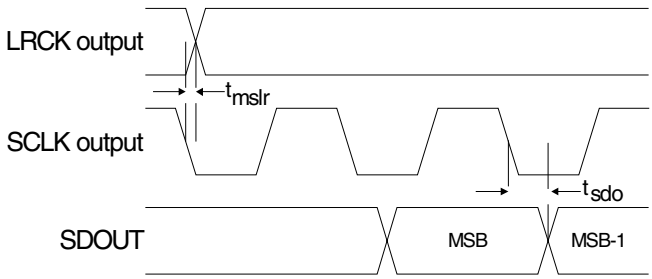


Figure 15. Master Mode, I^2S SAI

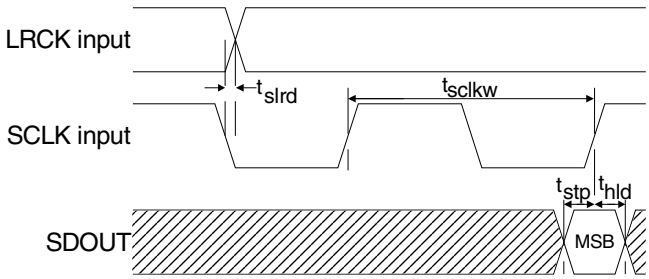
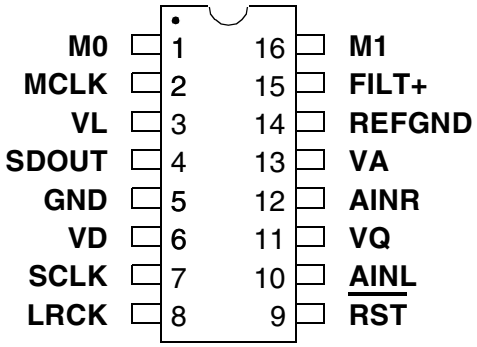


Figure 16. Slave Mode, I^2S SAI

2 PIN DESCRIPTION



Pin Name	#	Pin Description
M0 **M1**	1 16	**Mode Selection** (*Input*) - Determines the operational mode of the device.
MCLK	2	**Master Clock** (*Input*) - Clock source for the delta-sigma modulator and digital filters.
VL	3	**Logic Power** (*Input*) **-** Positive power for the digital input/output.
SDOUT	4	**Serial Audio Data Output** (*Output*) - Output for two's complement serial audio data.
GND	5	**Ground** (*Input*) - Ground reference. Must be connected to analog ground.
VD	6	**Digital Power** (*Input*) **-** Positive power supply for the digital section.
SCLK	7	**Serial Clock** (*Input*/*Output*) - Serial clock for the serial audio interface.
LRCK	8	**Left Right Clock** (*Input*/*Output*) - Determines which channel, Left or Right, is currently active on the serial audio data line.
$\overline{\text{RST}}$	9	**Reset** (*Input*) - The device enters a low power mode when low.
AINL **AINR**	10 12	**Analog Input** (*Input*) - The full scale analog input level is specified in the Analog Characteristics specification table.
VQ	11	**Quiescent Voltage** *(Output)* **-** Filter connection for the internal quiescent reference voltage.
VA	13	**Analog Power** (*Input*) **-** Positive power supply for the analog section.
REFGND	14	**Reference Ground** (*Output*) **-** Ground reference for the internal sampling circuits.
FILT+	15	**Positive Voltage Reference** (*Output*) **-** Positive reference voltage for the internal sampling circuits.

3 TYPICAL CONNECTION DIAGRAM

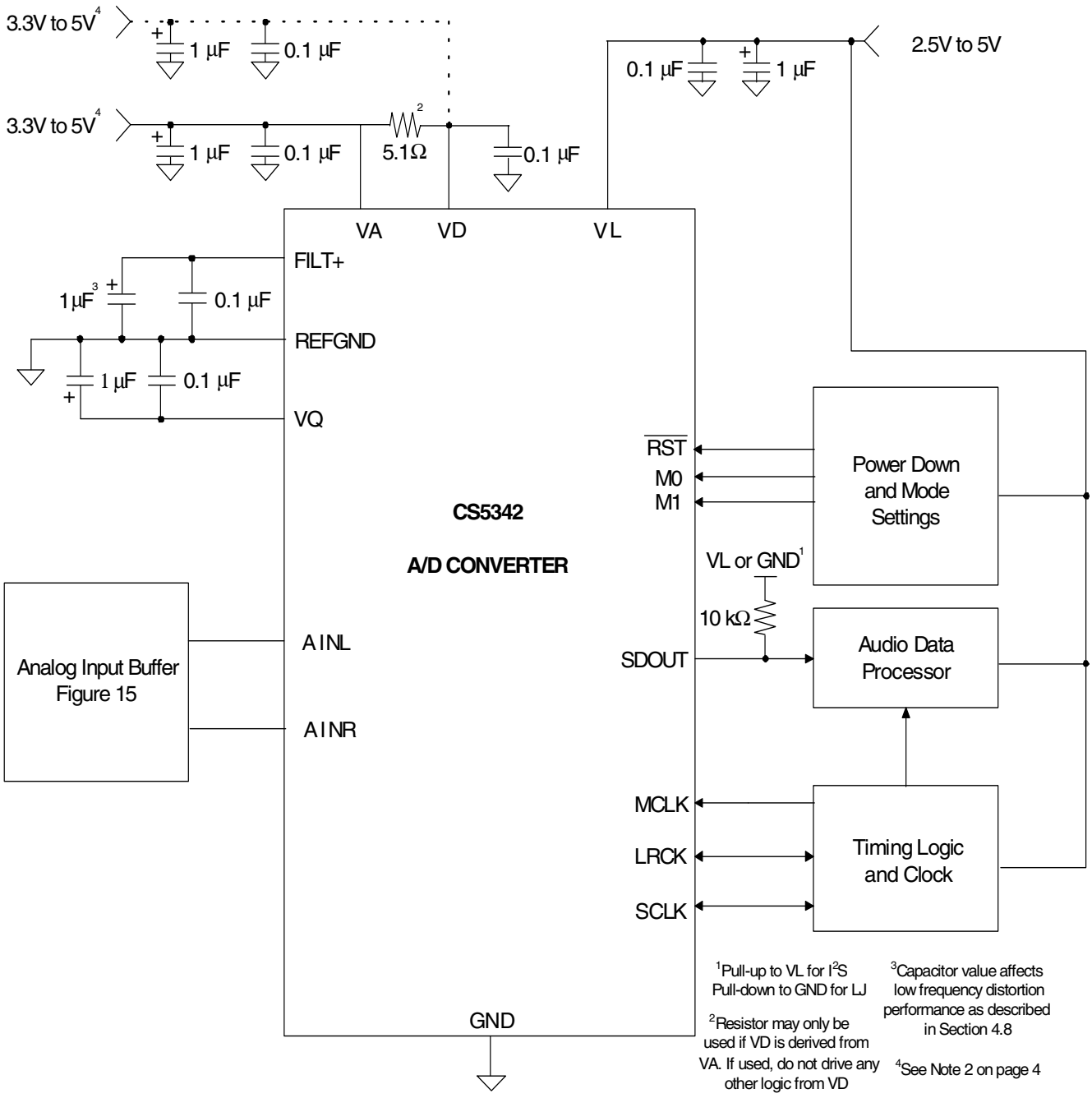


Figure 17. Typical Connection Diagram

4 APPLICATIONS

4.1 Single, Double, and Quad Speed Modes

The CS5342 can support output sample rates from 2 kHz to 200 kHz. The proper speed mode can be determined by the desired output sample rate and the external MCLK/LRCK ratio, as shown in Table 1.

Speed Mode	MCLK/LRCK Ratio	Output Sample Rate Range (kHz)
Single Speed Mode	768x	43 - 54
	384x	2 - 54
Double Speed Mode	384x	86 - 108
	192x	50 - 108
Quad Speed Mode	192x	172 - 200
	96x*	100 - 200

* Quad Speed Mode, 96x only available in Master Mode.

Table 1. Speed Modes and the Associated Output Sample Rates (Fs)

4.2 Operation as Either a Clock Master or Slave

The CS5342 supports operation as either a clock master or slave. As a clock master, the LRCK and SCLK pins are outputs with the left/right and serial clocks synchronously generated on-chip. As a clock slave, the LRCK and SCLK pins are inputs and require the left/right and serial clocks to be externally generated. The selection of clock master or slave is made via the Mode pins as shown in Table 2.

M1 (Pin 16)	M0 (Pin 1)	MODE
0	0	Clock Master, Single Speed Mode
0	1	Clock Master, Double Speed Mode
1	0	Clock Master, Quad Speed Mode
1	1	Clock Slave, All Speed Modes

Table 2. CS5342 Mode Control

4.2.1 Operation as a Clock Master

As a clock master, LRCK and SCLK operate as outputs. The left/right and serial clocks are internally derived from the master clock with the left/right clock equal to Fs and the serial clock equal to 64x Fs, as shown in Figure 18.

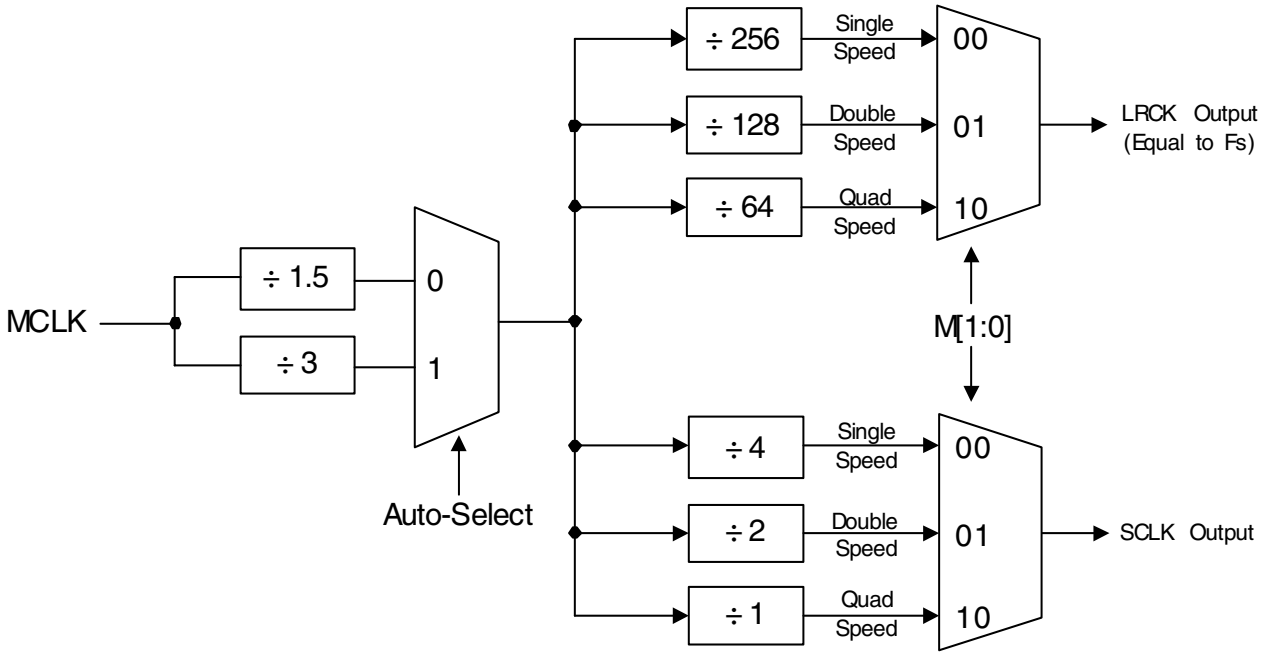


Figure 18. CS5342 Master Mode Clocking

4.2.2 Operation as a Clock Slave

LRCK and SCLK operate as inputs in clock slave mode. It is recommended that the left/right clock be synchronously derived from the master clock and must be equal to Fs. It is also recommended that the serial clock be synchronously derived from the master clock and equal to 48x Fs or 64x Fs in Single-Speed Mode. In Double-Speed and Quad-Speed Modes the serial clock must be derived synchronously from the master clock and equal to 48x Fs. Additionally, Quad-Speed Slave Mode is only specified for operation with a VA and VD at 5 V, ±5%.

A unique feature of the CS5342 is the automatic selection of either Single, Double or Quad speed mode when operating as a clock slave. The auto-mode select feature negates the need to configure the Mode pins to correspond to the desired mode. The auto-mode selection feature supports all standard audio sample rates from 2 to 200 kHz. However, there are ranges of non-standard audio sample rates that are not supported when operating with a fast MCLK (768x, 384x, and 192x for Single, Double, and Quad Speed Modes respectively). Please refer to Table 1 on page 15 for supported sample rate ranges.

4.2.3 Master Clock

The CS5342 requires a Master clock (MCLK) which runs the internal sampling circuits and digital filters. There is also an internal MCLK divider which is automatically activated based on the frequency of the MCLK. Table 3 shows a listing of the external MCLK/LRCK ratios that are required. Table 4 lists some common audio output sample rates and the required MCLK frequency. Please note that not all of the listed sample rates are supported when operating with a fast MCLK (768x, 384x, 192x for Single, Double, and Quad Speed Modes respectively).

	Single Speed Mode	Double Speed Mode	Quad Speed Mode
MCLK/LRCK Ratio	384x, 768x	192x, 384x	96x*, 192x

* Quad Speed, 96x only available in Master Mode.

Table 3. Master Clock (MCLK) Ratios

SAMPLE RATE (kHz)	MCLK (MHz)
32	12.288
44.1	16.9344 33.8688
48	18.432 36.864
64	12.288
88.2	16.9344 33.8688
96	18.432 36.864
192	36.864

Table 4. Master Clock (MCLK) Frequencies for Standard Audio Sample Rates

4.3 Serial Audio Interface

The CS5342 supports both I^2S and Left Justified serial audio formats. Upon start-up, the CS5342 will detect the logic level on SDOUT (pin 4). A 10 kΩ pull-up resistor to VL is needed to select I^2S format, and a 10 kΩ pull-down resistor to GND is needed to select Left Justified format. Please see Figures 13 through 16 on page 12, for more information on the required timing for the two serial audio interface formats.

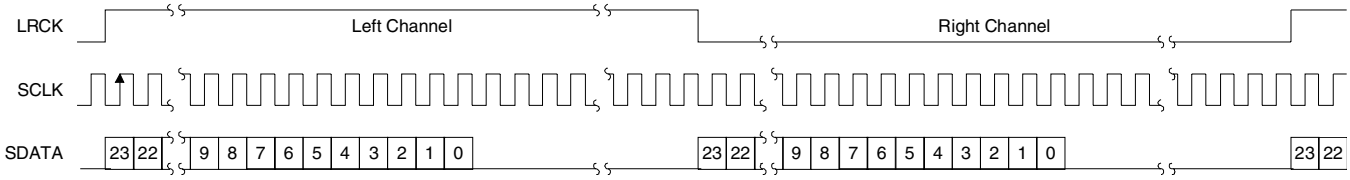


Figure 19. Left-Justified Serial Audio Interface

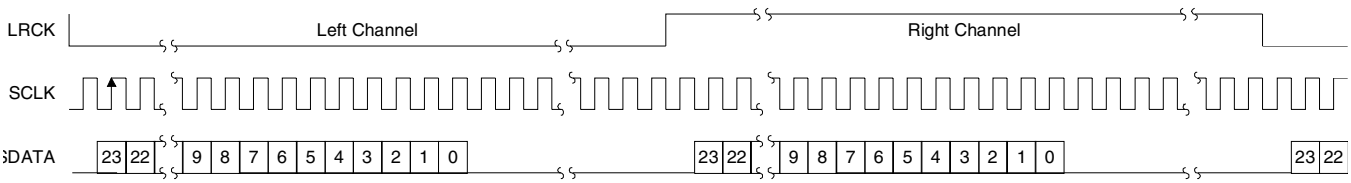


Figure 20. I^2S Serial Audio Interface

4.4 Power-up Sequence

Reliable power-up can be accomplished by keeping the device in reset until the power supplies, clocks and configuration pins are stable. It is also recommended that reset be enabled if the analog or digital supplies drop below the minimum specified operating voltages to prevent power glitch related issues.

4.5 Analog Connections

The analog modulator samples the input at 6.144 MHz. The digital filter will reject signals within the stopband of the filter. However, there is no rejection for input signals which are multiples of the input sampling frequency (n × 6.144 MHz), where n=0,1,2,... Refer to Figure 15 which shows the suggested filter that will attenuate any noise energy at 6.144 MHz, in addition to providing the optimum source impedance for the modulators. The use of capacitors which have a large voltage coefficient (such as general purpose ceramics) must be avoided since these can degrade signal linearity.

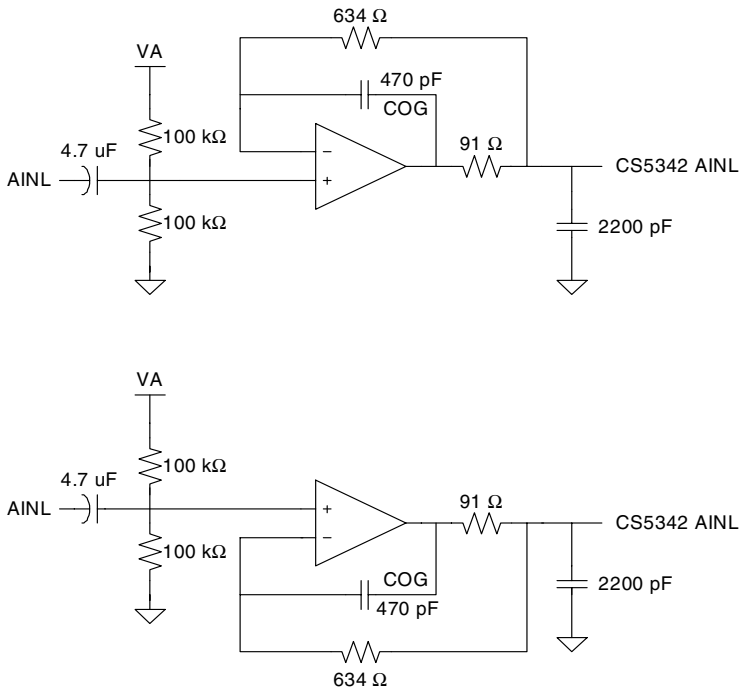


Figure 21. CS5342 Recommended Analog Input Buffer

4.6 Grounding and Power Supply Decoupling

As with any high resolution converter, the CS5342 requires careful attention to power supply and grounding arrangements if its potential performance is to be realized. Figure 17 shows the recommended power arrangements, with VA and VL connected to clean supplies. VD, which powers the digital filter, may be run from the system logic supply or may be powered from the analog supply via a resistor. In this case, no additional devices should be powered from VD. Decoupling capacitors should be as near to the ADC as possible, with the low value ceramic capacitor being the nearest. All signals, especially clocks, should be kept away from the FILT+ and VQ pins in order to avoid unwanted coupling into the modulators. The FILT+ and VQ decoupling capacitors, particularly the 0.1 µF, must be positioned to minimize the electrical path from FILT+ and REF_GND. The CDB5342 evaluation board demonstrates the optimum layout and power supply arrangements. To minimize digital noise, connect the ADC digital outputs only to CMOS inputs.

4.7 Synchronization of Multiple Devices

In systems where multiple ADCs are required, care must be taken to achieve simultaneous sampling. To ensure synchronous sampling, the MCLK and LRCK must be the same for all of the CS5342's in the system.

4.8 Capacitor Size on the Reference Pin (FILT+)

The CS5342 requires an external capacitance on the internal reference voltage pin, FILT+. The size of this decoupling capacitor will affect the low frequency distortion performance as shown in Figure 22, with larger capacitor values used to optimize low frequency distortion performance. The THD+N curves in Figure 22 were measured with VA = VD = VL = 5 V in Single-Speed Master Mode using a 1 kHz input tone of magnitude -1 dB Full-Scale.

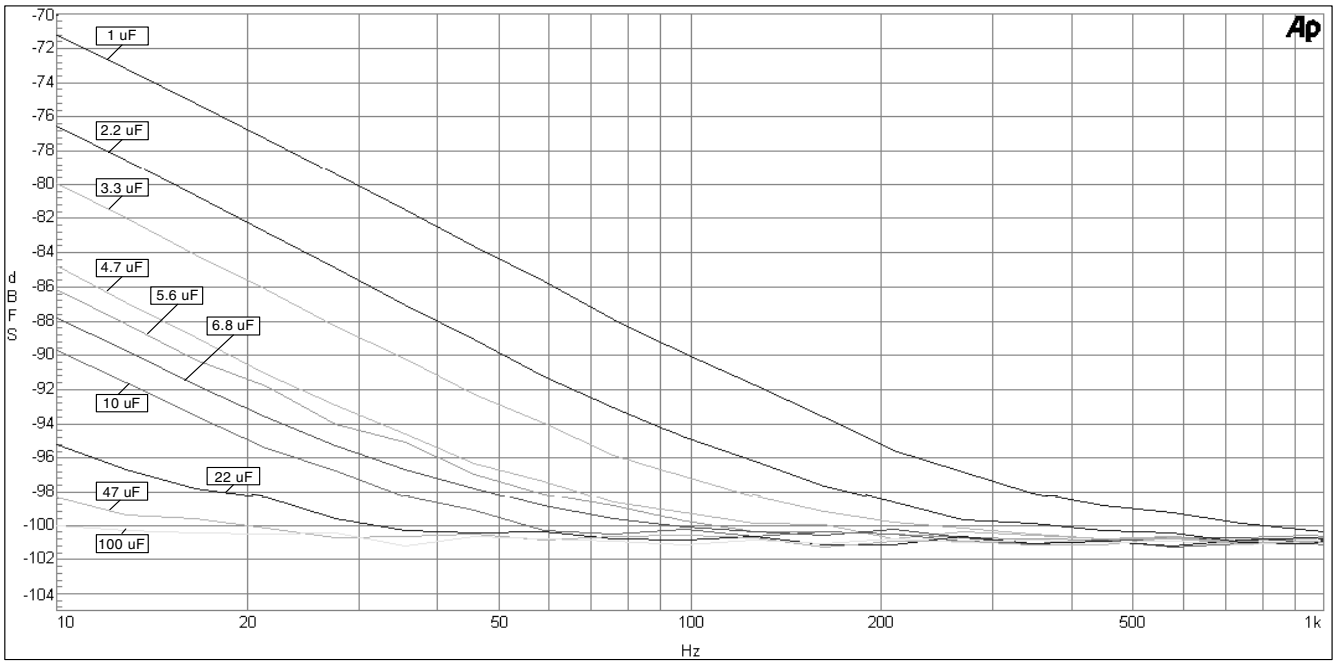


Figure 22. CS5342 THD+N versus Frequency

5 PARAMETER DEFINITIONS

Dynamic Range

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth. Dynamic Range is a signal-to-noise ratio measurement over the specified bandwidth made with a -60 dBFS signal. 60 dB is added to resulting measurement to refer the measurement to full-scale. This technique ensures that the distortion components are below the noise level and do not affect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17-1991, and the Electronic Industries Association of Japan, EIAJ CP-307. Expressed in decibels.

Total Harmonic Distortion + Noise

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth (typically 10 Hz to 20 kHz), including distortion components. Expressed in decibels. Measured at -1 and -20 dBFS as suggested in AES17-1991 Annex A.

Frequency Response

A measure of the amplitude response variation from 10 Hz to 20 kHz relative to the amplitude response at 1 kHz. Units in decibels.

Interchannel Isolation

A measure of crosstalk between the left and right channels. Measured for each channel at the converter's output with no signal to the input under test and a full-scale signal applied to the other channel. Units in decibels.

Interchannel Gain Mismatch

The gain difference between left and right channels. Units in decibels.

Gain Error

The deviation from the nominal full-scale analog input for a full-scale digital output.

Gain Drift

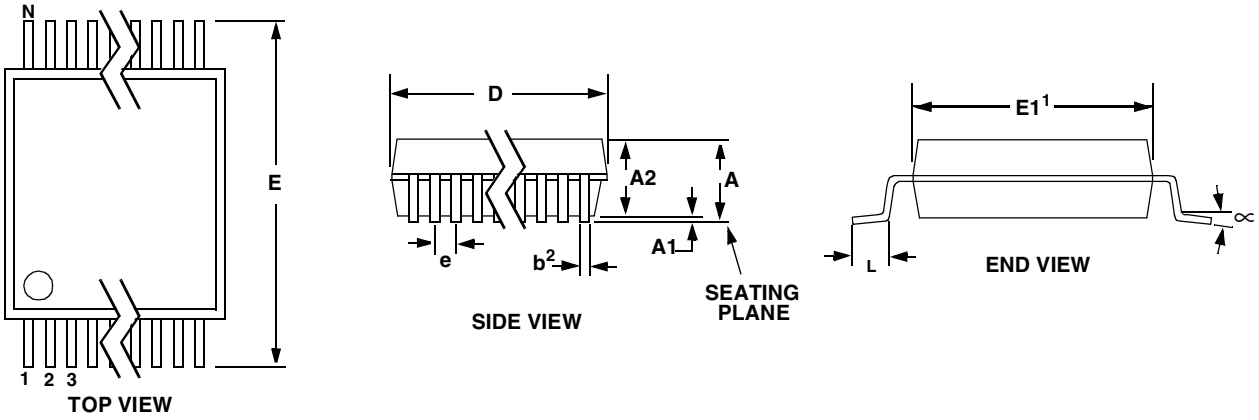
The change in gain value with temperature. Units in ppm/°C.

Offset Error

The deviation of the mid-scale transition (111...111 to 000...000) from the ideal. Units in mV.

6 PACKAGE DIMENSIONS

16L TSSOP (4.4 mm BODY) PACKAGE DRAWING



	INCHES			MILLIMETERS			NOTE
DIM	MIN	NOM	MAX	MIN	NOM	MAX	
A	--	--	0.043	--	--	1.10	
A1	0.002	0.004	0.006	0.05	--	0.15	
A2	0.03346	0.0354	0.037	0.85	0.90	0.95	
b	0.00748	0.0096	0.012	0.19	0.245	0.30	2,3
D	0.193	0.1969	0.201	4.90	5.00	5.10	1
E	0.248	0.2519	0.256	6.30	6.40	6.50	
E1	0.169	0.1732	0.177	4.30	4.40	4.50	1
e	--	0.026 BSC	--	--	0.065 BSC	--	
L	0.020	0.024	0.028	0.50	0.60	0.70	
∝	0°	4°	8°	0°	4°	8°	

JEDEC #: MO-153

Controlling Dimension is Millimeters

Notes: 1. "D" and "E1" are reference datums and do not included mold flash or protrusions, but do include mold mismatch and are measured at the parting line, mold flash or protrusions shall not exceed 0.20 mm per side.

2. Dimension "b" does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.13 mm total in excess of "b" dimension at maximum material condition. Dambar intrusion shall not reduce dimension "b" by more than 0.07 mm at least material condition.

3. These dimensions apply to the flat section of the lead between 0.10 and 0.25 mm from lead tips.

7. REVISION HISTORY

Release	Date	Changes
A1	April 2003	-Initial Advance Release.
A2	July 2003	-Modify serial port timing specs. -Add Applications section on speed mode detect.
PP1	August 2004	-Change 2700 pF capacitors to 2200 pF in analog input buffer diagram. -Update Output Sample Range table. -Add new Applications section about capacitor on FILT+ pin. -Correct Max MCLK period under “Switching Characteristics.” -Replace MCLK low/high timing specifications with duty cycle specification. -Redefine slave mode timing specifications under “Switching Characteristics.” -Add requirement of SCLK/LRCK = 48x in Double and Quad Speed Modes. -Increase minimum VL specification from 1.7 V to 2.38 V. -Specify VA and VD at 5 V, ±5% for Quad-Speed Slave Mode. -Reduce gain error specification under Analog Characteristics. -Improve minimum and maximum specifications for full-scale input voltage. -Initial Preliminary Release.
PP2	Aug 2004	Update to include lead-free device ordering information.

Table 5. Revision History