TOSHIBA PHOTOCOUPLER GaAℓAs IRED & PHOTO-IC

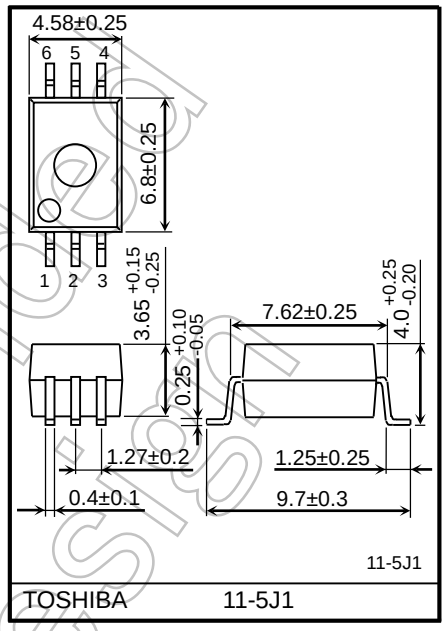
TLP715

Isolated Bus Drivers

High Speed Line Receivers

Microprocessor System Interfaces

Unit: mm



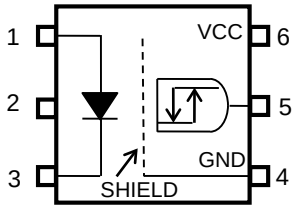
Weight: 0.26 g (typ.)

The Toshiba TLP715 consists of a GaAℓAs light-emitting diode and an integrated high-gain, high-speed photodetector. This unit is a 6-pin SDIP. The TLP715 is 50% smaller than the 8-PIN DIP and meets the reinforced insulation class requirements of international safety standards. Therefore the mounting area can be reduced in equipment requiring safety standard certification. The detector has a totem pole output stage to provide both source and sink driving. The detector IC has an internal shield that provides a guaranteed common-mode transient immunity. The TLP715 is buffer logic type. For inverter logic type, the TLP718 is in line-up.

- Buffer logic output (totem pole output)
- Guaranteed performance over temperature: -40 to 100°C
- Power supply voltage: 4.5 to 20 V
- Input current: I_{FLH} = 3 mA (max)
- Switching time (t_{pLH} / t_{pHL}): 250 ns (max)
- Common-mode transient immunity: ±10 kV / μs (min)
- Isolation voltage: 5000 Vrms (min)
- UL recognized: UL1577, File No.E67349
- cUL recognized: CSA Component Acceptance Service No. 5A
  File No.E67349
- Option (D4) VDE approved :
  EN60747-5-5 EN60065 EN60950-1 (Note 1)
  EN62368-1(Pending)

Note 1: When a EN60747-5-5 approved type is needed, Please designate "Option(D4)"

Pin Configuration (Top View)

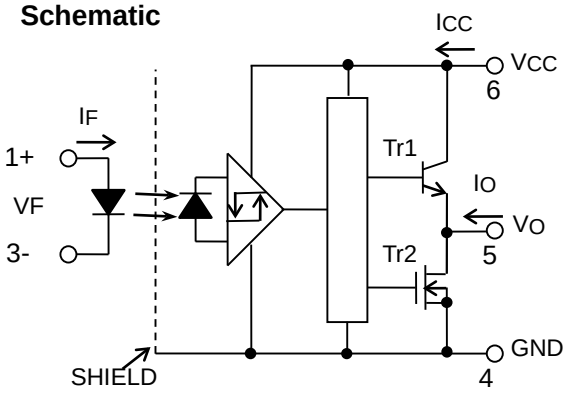


1: ANODE
2: N.C.
3: CATHODE
4: GND
5: V_O (Output)
6: V_{CC}

Truth Table

Input	LED	Tr1	Tr2	Output
H	ON	ON	OFF	H
L	OFF	OFF	ON	L

Schematic



Note: 0.1 μF bypass capacitor must be connected between pins 6 and 4.

Start of commercial production
2008-11

Absolute Maximum Ratings (Ta = 25°C)

CHARACTERISTIC			SYMBOL	RATING	UNIT
LED	Forward Current (Ta ≤ 83°C)		I_F	20	mA
	Forward Current Derating (Ta ≥ 83°C)		$\Delta I_F/\Delta Ta$	-0.48	mA/°C
	Peak Transient Forward Current	(Note 1)	I_{FPT}	1	A
	Reverse Voltage		V_R	5	V
	Diode power dissipation		P_D	40	mW
	Diode power dissipation derating (Ta ≥ 83°C)		ΔP_D/°C	-0.95	mW/°C
	Junction Temperature		Tj	125	°C
DETECTOR	Output Current 1 (Ta ≤ 25°C)		I_{O1}	25 / -15	mA
	Output Current 2 (Ta ≤ 100°C)		I_{O2}	13 / -13	mA
	Output Voltage		V_O	-0.5 to 20	V
	Supply Voltage		V_{CC}	-0.5 to 20	V
	Power dissipation		P_C	75	mW
	Power dissipation derating (Ta ≥ 25°C)		ΔP_C / °C	-0.75	mW / °C
	Junction Temperature		Tj	125	°C
Operating Temperature Range			Topr	-40 to 100	°C
Storage Temperature Range			Tstg	-55 to 125	°C
Lead Solder Temperature (10 s)			Tsol	260	°C
Isolation Voltage (AC,60 s, R.H. ≤ 60%)		(Note 2)	BV_S	5000	Vrms

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Pulse width PW ≤ 1μs, 300pps.

Note 2: Device Considered a two terminal device: pins 1, 2 and 3 shorted together and pins 4, 5 and 6 shorted together.

Recommended Operating Conditions

CHARACTERISTIC		SYMBOL	MIN	TYP.	MAX	UNIT
Input Current, ON		$I_{F(ON)}$	4.5	-	10	mA
Input Voltage, OFF		$V_{F(OFF)}$	0	-	0.8	V
Supply Voltage	(Note 1)	V_{CC}	4.5	-	20	V
Operating Temperature		T_{opr}	-40	-	100	°C

Note 1: This item denotes operating ranges, not meaning of recommended operating conditions.

Note: Recommended operating conditions are given as a design guideline to obtain expected performance of the device. Additionally, each item is an independent guideline respectively. In developing designs using this product, please confirm specified characteristics shown in this document.

Electrical Characteristics
(Unless otherwise specified, Ta =-40 to 100°C, V_{CC} = 4.5 to 20 V)

CHARACTERISTIC	SYMBOL	TEST CIRCUIT	CONDITION		MIN	TYP.	MAX	UNIT
Input forward voltage	V_F	-	I_F = 5 mA , Ta = 25°C		1.4	1.6	1.7	V
Temperature coefficient of	$\Delta V_F/\Delta Ta$	-	I_F = 5 mA		-	-2.0	-	mV/°C
Input reverse current	I_R	-	V_R = 5 V , Ta = 25°C		-	-	10	μA
Input capacitance	C_T	-	V = 0 V, f = 1 MHz, Ta = 25°C		-	45	-	pF
Logic LOW output voltage	V_{OL}	1	I_{OL} = 3.5 mA, V_F = 0.8 V		-	0.2	0.6	V
Logic HIGH output voltage	V_{OH} (Note 1)	2	I_{OH} = -2.6 mA, I_F=5 mA	V_{CC} = 4.5 V	2.7	3.5	-	V
				V_{CC} = 20 V	17.4	19	-	
Logic LOW supply current	I_{CCL}	3	V_F = 0V		-	-	3.0	mA
Logic HIGH supply current	I_{CCH}	4	I_F = 5 mA		-	-	3.0	mA
Logic LOW short circuit output current (Note 2)	I_{OSL}	5	V_F = 0V	V_{CC} = V_O = 5.5 V	15	80	-	mA
				V_{CC} = V_O = 20 V	20	90	-	
Logic HIGH short circuit output current (Note2)	I_{OSH}	6	I_F = 5mA, V_O = GND	V_{CC} = 5.5 V	-5	-15	-	mA
				V_{CC} = 20 V	-10	-20	-	
Input current logic HIGH	I_{FLH}	-	I_O = -2.6 mA, V_O > 2.4 V		-	0.4	3	mA
Input voltage logic LOW	V_{FHL}	-	I_O = 3.5 mA, V_O < 0.6V		0.8	-	-	V
Input current hysteresis	I_{HYS}	-	V_{CC} = 5 V		-	0.05	-	mA

Note: All typical values are at Ta=25°C, V_{CC}=5 V.

Note : A ceramic capacitor (0.1 μF) should be connected from pin 6 to pin 4 to stabilize the operation of the high gain linear amplifier. Failure to provide the bypassing may impair the switching property. The total lead length between capacitor and coupler should not exceed 1 cm.

Note 1: V_{OH} = V_{CC} –V_O [V]

Note 2: Duration of output short circuit time should not exceed 10 ms.

Isolation Characteristics (Ta = 25°C)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN	TYP.	MAX	UNIT
Capacitance input to output	C_S	V_S = 0 V, f = 1 MHz (Note 1)	-	1.0	-	pF
Isolation resistance	R_S	R.H. ≤ 60%, V_S = 500 V (Note 1)	1×10^{12}	10^{14}	-	Ω
Isolation voltage	BV_S	AC, 60 s	5000	-	-	Vrms
		AC, 1 s, in oil	-	10000	-	
		DC, 60 s, in oil	-	10000	-	Vdc

Note 1: Device Considered a two terminal device: pins 1, 2 and 3 shorted together and pins 4, 5 and 6 shorted together.

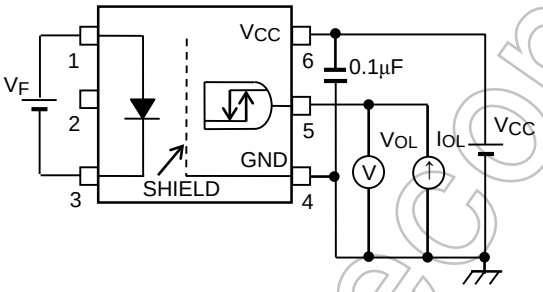
Switching Characteristics

(Unless otherwise specified, Ta = -40 to 100°C, V_{CC} = 4.5 to 20 V)

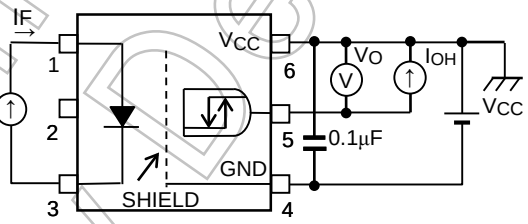
CHARACTERISTIC	SYMBOL	TEST CIRCUIT	CONDITION	MIN	TYP. *	MAX	UNIT
Propagation delay time to logic HIGH output	t_{pLH}	7 8	I_F = 0 → 3 mA	30	120	250	ns
Propagation delay time to logic LOW output	t_{pHL}		I_F = 3 → 0 mA	30	120	250	ns
Switching time dispersion between ON and OFF	$\|t_{pLH}-t_{pHL}\|$		-	-	-	220	ns
Rise Time (10 – 90 %)	t_r		I_F = 0 → 3 mA, V_{CC} = 5 V	-	30	-	ns
Fall Time (90 – 10 %)	t_f		I_F = 3 → 0 mA, V_{CC} = 5 V	-	30	-	ns
Common-mode transient Immunity at HIGH level output	CM_H	9	V_{CM} = 1000 V_{p-p}, I_F = 5 mA, V_{CC} = 20 V, Ta = 25°C	10000	-	-	V/μs
Common-mode transient Immunity at LOW level output	CM_L		V_{CM} = 1000 V_{p-p}, I_F = 0 mA, V_{CC} = 20 V, Ta = 25°C	-10000	-	-	V/μs

*All typical values are at Ta = 25°C.

TEST CIRCUIT 1: V_{OL}

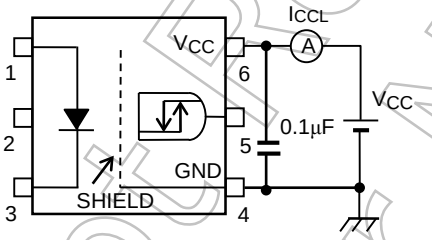


TEST CIRCUIT 2: V_{OH}

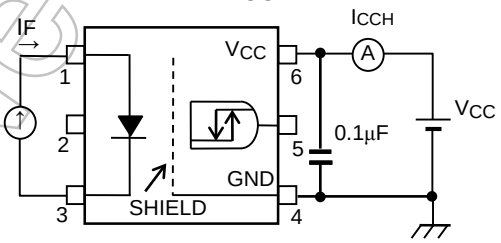


$V_{OH}=V_{CC}-V_O$ [V]

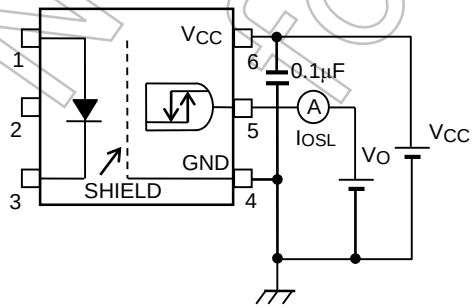
TEST CIRCUIT 3: I_{CCL}



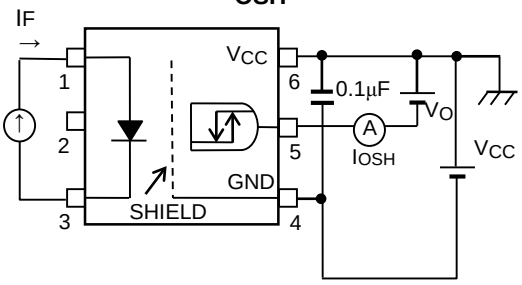
TEST CIRCUIT 4: I_{CCH}



TEST CIRCUIT 5: I_{OSL}

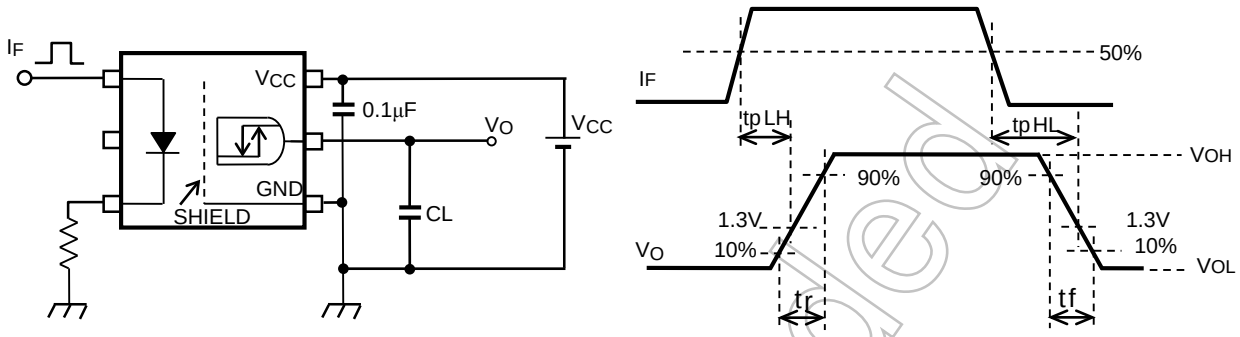


TEST CIRCUIT 6: I_{OSH}



TEST CIRCUIT 7: Switching Time Test Circuit

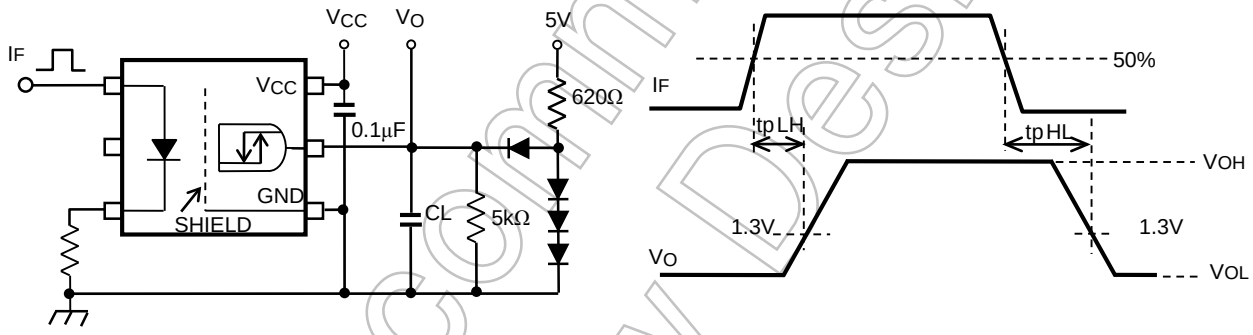
I_F=3 mA(P.G)
(f=50 kHz, duty=50%, less than tr = tf = 5ns)



CL: stray capacitance of probe and wiring (to 15 pF)

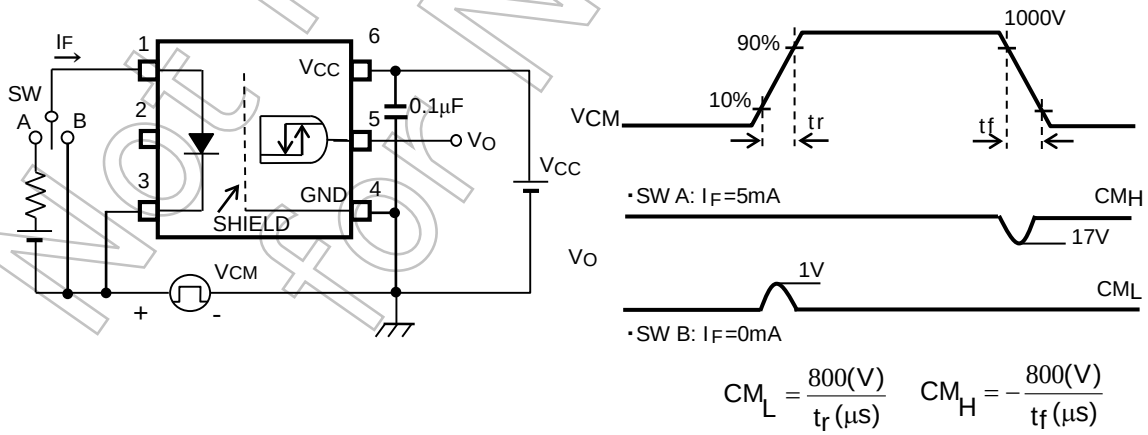
TEST CIRCUIT 8: Switching Time Test Circuit

I_F=3 mA(P.G)
(f=50 kHz, duty=50%, less than tr = tf = 5ns)



CL: stray capacitance of probe and wiring (to 15 pF)

TEST CIRCUIT 9: Common-Mode Transient Immunity Test Circuit



$$CM_L = \frac{800(V)}{t_r(\mu s)} \qquad CM_H = -\frac{800(V)}{t_f(\mu s)}$$

Note: CM_H (CM_L) is the maximum rate of rise (fall) of the common mode voltage that can be sustained with the output voltage in the high (low) state.

EN60747-5-5 Option (D4) Specification

Types : TLP715

Type designations for “option: (D4)”, which are tested under EN60747 requirements.

Ex.: TLP715 (D4-TP,F)
D4 : EN60747 option
TP : Standard tape & reel type
F : [[G]]/RoHS COMPATIBLE (Note 1)

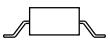
Note: Use TOSHIBA standard type number for safety standard application.
Ex.: TLP715 (D4-TP,F) → TLP715

Note 1: Please contact your Toshiba sales representative for details on environmental information such as the product's RoHS compatibility.
RoHS is the Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment.

EN60747 Isolation Characteristics

Description		Symbol	Rating	Unit
Application classification for rated mains voltage≤300V_{rms} for rated mains voltage≤600V_{rms}			 I-IV I-III	—
Climatic classification			40/ 100 / 21	—
Pollution degree			2	—
Maximum operating insulation voltage	TLPxxx type	V_{IORM}	890	Vpk
	TLPxxxFtype		1140	
Input to output test voltage, method A Vpr=1.6×V_{IORM}, type and sample test tp=10 s, partial discharge<5pC	TLPxxx type	Vpr	1424	Vpk
	TLPxxxFtype		1824	
Input to output test voltage, method B Vpr=1.875×V_{IORM}, 100% production test t_p=1 s, partial discharge<5pC	TLPxxx type	Vpr	1670	Vpk
	TLPxxxFtype		2140	
Highest permissible overvoltage (transient overvoltage, t_{pr} = 60 s)		V_{TR}	8000	Vpk
Safety limiting values (max. permissible ratings in case of fault, also refer to thermal derating curve) current (input current I_F, P_{si} = 0) power (output or total power dissipation) temperature		 Isi Psi Ts	 300 700 150	 mA mW °C
Insulation resistance, input-output	V_{IO} =500V, Ta=25°C V_{IO} =500V, Ta=100°C V_{IO} =500V, Ta=Ts	Rsi	≥10^{12} ≥10^{11} ≥10^{9}	Ω

Insulation Related Specifications

		 7.62mm pitch TLPxxx type	 10.16mm pitch TLPxxxF type
Minimum creepage distance	Cr	7.0mm	8.0mm
Minimum clearance	Cl	7.0mm	8.0mm
Minimum insulation thickness	ti	0.4mm	
Comperative tracking index	CTI	175	

1. If a printed circuit is incorporated, the creepage distance and clearance may be reduced below this value. If this is not permissible, the user shall take suitable measures.
2. This photocoupler is suitable for ‘safe electrical isolation’ only within the safety limit data. Maintenance of the safety data shall be ensured by means of protective circuits.

Marking on product for EN60747 Option:(D4): 4

Marking Example

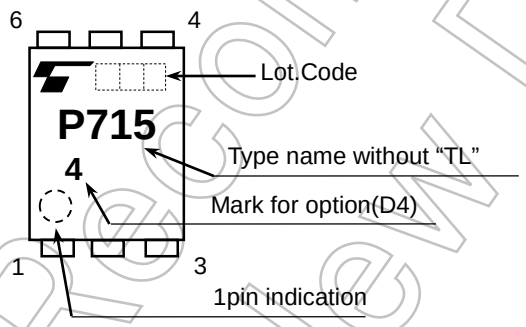


Figure 1 Partial discharge measurement procedure according to EN60747
Destructive test for qualification and sampling tests.

Method A

(for type and sampling tests, destructive tests)

t_1, t_2	= 1 to 10 s
t_3, t_4	= 1 s
t_p(Measuring time for partial discharge)	= 10 s
t_b	= 12 s
t_{ini}	= 60 s

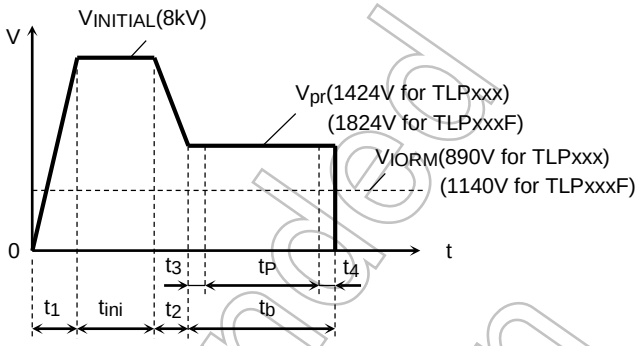


Figure 2 Partial discharge measurement procedure according to EN60747
Non-destructive test for100% inspection.

Method B

(for sample test,non-destructive test)

t_3, t_4	= 0.1 s
t_p(Measuring time for partial discharge)	= 1 s
t_b	= 1.2 s

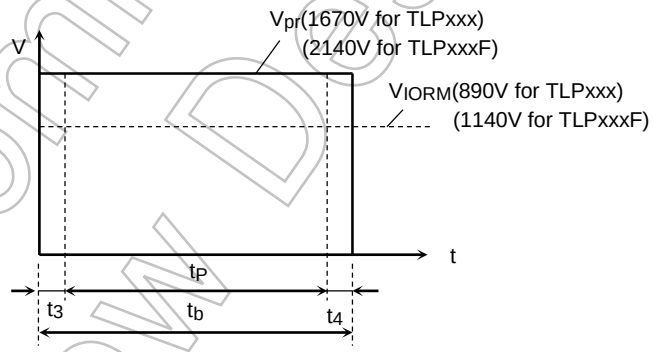
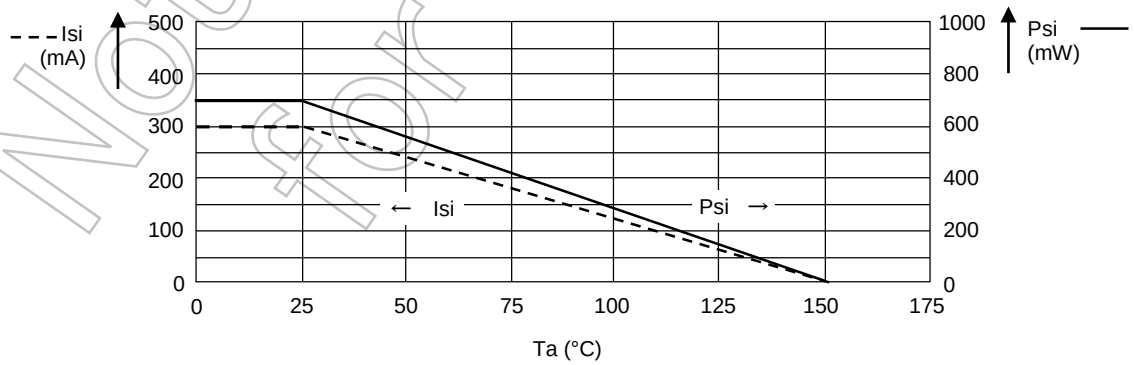


Figure 3 Dependency of maximum safety ratings on ambient temperature (for photodetector failure)



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