

## Field Programmable Blank Oscillator

Series **CPPL**

- Programmed with the PG-2000P, PG-3000 field oscillator programming instrument within seconds
- Can be programmed twice
- Provides a sealed finished custom oscillator
- Standard Package Options
- Ultra low jitter @ 1 million samples
- Power down and Tri-State options



Part Numbering Example: CPPL C 1 L Z - A5 B6 - XX.XXXX TS

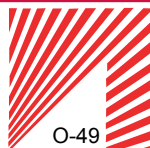
| CPPL   | C                   | 1                                                                                         | L                       | Z                                             | A5                                                        | B6                                            | XX.XXXX           | TS                            |
|--------|---------------------|-------------------------------------------------------------------------------------------|-------------------------|-----------------------------------------------|-----------------------------------------------------------|-----------------------------------------------|-------------------|-------------------------------|
| SERIES | OUTPUT              | PACKAGE STYLE                                                                             | VOLTAGE                 | ADDED FEATURES                                | OPERATING TEMP.                                           | STABILITY                                     | FREQUENCY         | TRI-STATE                     |
| CPPL   | C = CMOS<br>T = TTL | 1 = Full Size<br>4 = Half Size<br>5 = 3.2X5 Ceramic<br>7 = 5X7 Ceramic<br>8 = PLASTIC SMD | Blank = 5V<br>L = 3.3 V | Blank = Bulk<br>T = Tube<br>Z = Tape and Reel | Blank = 0°C +70°C<br>A5 = -20°C +70°C<br>A7 = -40°C +85°C | B6 = ±100 ppm<br>BP = ±50 ppm<br>BR = ±25 ppm | 1.000~133.000 MHz | TS = Tri-State<br>PD=PowerDwn |

## Specifications:

| Description                                                            | Min                | Typ        | Max               | Unit              |
|------------------------------------------------------------------------|--------------------|------------|-------------------|-------------------|
| <b>Frequency Range:</b><br>Programmable to Any Discrete Frequency      | 1.000              |            | 133.000           | MHz               |
| <b>Available Stability Options:</b>                                    | -100<br>-50<br>-25 |            | 100<br>50<br>25   | ppm<br>ppm<br>ppm |
| <b>Programmable Input Voltage:</b><br>(1~133 MHz)<br>(1~100 MHz)       | 4.5<br>3.0         | 5.0<br>3.3 | 5.5<br>3.6        | V<br>V            |
| <b>Operating Temperature Range Options:</b>                            | 0<br>-20<br>-40    |            | +70<br>+70<br>+85 | °C<br>°C<br>°C    |
| <b>Storage Temperature:</b>                                            | -55                |            | +125              | °C                |
| Aging (PPM/Year)<br>Ta=25°C, Vdd=5/3.3V                                |                    |            | ±5                |                   |
| <b>Programmable Output Level:</b> TTL/CMOS                             |                    |            |                   |                   |
| <b>Packaging:</b> Tape and Reel (1K per Reel)<br>Tube<br>Bulk Shipping |                    |            |                   |                   |

## Operating Load Conditions:

| Description                                                                                                                                                            | Min | Max                  | Unit                 |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|----------------------|----------------------|
| Vdd Supply Voltage                                                                                                                                                     | 3.0 | 5.5                  | V                    |
| CTTL Max Capacitive Load on outputs for TTL levels<br>4.5V~5.5V Vdd ≤ 40 MHz<br>4.5V~5.5V Vdd > 40~133 MHz                                                             |     | 50<br>25             | pF<br>pF             |
| CCMOS Max Capacitive Load on outputs for CMOS levels<br>4.5V~5.5V Vdd, ≤ 66 MHz<br>4.5V~5.5V Vdd, >66~133 MHz<br>3.0V~3.6V Vdd, ≤ 40 MHz<br>3.0V~3.6V Vdd, >40~100 MHz |     | 50<br>25<br>30<br>15 | pF<br>pF<br>pF<br>pF |



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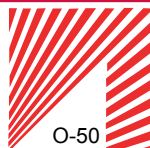
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## Electrical Characteristics

| Description                                                                 | TEST CONDITIONS                                                                                         | Min                                          | Typ        | Max                       | Unit     |
|-----------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------|----------------------------------------------|------------|---------------------------|----------|
| <b>Input Characteristics (Pin 1):</b>                                       |                                                                                                         |                                              |            |                           |          |
| V <sub>IL</sub> , Low-Level Input Voltage<br>TO TRI-STATE OR POWER DOWN     | 4.5–5.5V V <sub>dd</sub><br>3.0–3.6V V <sub>dd</sub>                                                    |                                              |            | 0.8<br>0.2V <sub>dd</sub> | V<br>V   |
| V <sub>IH</sub> , High-Level Input Voltage<br>TO ENABLE OUTPUT OR open      | 4.5–5.5V V <sub>dd</sub><br>3.0–3.6V V <sub>dd</sub>                                                    | 2.0<br>0.7 V <sub>dd</sub>                   |            |                           | V<br>V   |
| I <sub>IL</sub> , Input Low Current<br>I <sub>IH</sub> , Input High Current | V <sub>IN</sub> = 0V<br>V <sub>IN</sub> = V <sub>dd</sub>                                               |                                              |            | 10<br>5                   | μA<br>μA |
| <b>Output Characteristics:</b>                                              |                                                                                                         |                                              |            |                           |          |
| V <sub>OL</sub> , Low-Level Output Voltage                                  | 4.5V–5.5V V <sub>dd</sub> , 16 mA I <sub>OL</sub><br>3.0V–3.6V V <sub>dd</sub> , 8 mA I <sub>OL</sub>   |                                              |            | 0.4<br>0.4                | V<br>V   |
| V <sub>OHTTL</sub> ,<br>High-level Output Voltage TTL                       | 4.5V–5.5V V <sub>dd</sub> , -16 mA I <sub>OL</sub>                                                      | 2.4                                          |            |                           | V        |
| V <sub>OHCMOS</sub> ,<br>High-level CMOS Voltage                            | 4.5V–5.5V V <sub>dd</sub> , -16 mA I <sub>OL</sub><br>3.0V–3.6V V <sub>dd</sub> , -8 mA I <sub>OL</sub> | V <sub>dd</sub> -0.4<br>V <sub>dd</sub> -0.4 |            |                           | V<br>V   |
| <b>Power Supply Current:<br/>(unloaded)</b>                                 | 4.5–5.5 V <sub>dd</sub> , OUTPUT FREQ ≤ 133 MHz<br>3.0–3.6 V <sub>dd</sub> , OUTPUT FREQ ≤ 100 MHz      |                                              |            | 45<br>25                  | mA<br>mA |
| <b>Standby Current:</b>                                                     |                                                                                                         |                                              | 10         | 50                        | μA       |
| <b>Tristate pull up</b>                                                     | 4.5–5.5 V <sub>dd</sub> , V <sub>IN</sub> = 0V<br>4.5–5.5 V <sub>dd</sub> , V <sub>IN</sub> = 0.7V      | 1.1<br>50                                    | 3.0<br>100 | 8.0<br>200                | MΩ<br>KΩ |
| <b>Tri-State Leakage Current</b>                                            | 5.0 V <sub>dd</sub>                                                                                     |                                              | 20         |                           | μA       |
| <b>Output Enable Mode:</b>                                                  | Output is Tri-Stated                                                                                    |                                              |            |                           |          |
| <b>Power Down Mode:</b>                                                     | Output is Tri-Stated.                                                                                   |                                              |            |                           |          |

"Tristate internal pull up. Output active when high"



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## Output Clock Switching Characteristics

| Description                                                      | TEST CONDITIONS                                              | Min | Typ | Max        | Unit |
|------------------------------------------------------------------|--------------------------------------------------------------|-----|-----|------------|------|
| <b>Duty Cycle:</b><br>TTL @ 1.4 V<br>4.5-5.5 Vdd                 | $\leq 50$ MHz, $C_L = 50$ pF                                 | 45  |     | 55         | %    |
|                                                                  | 50–66 MHz, $C_L = 15$ pF                                     | 45  |     | 55         | %    |
|                                                                  | 66–125 MHz, $C_L = 25$ pF                                    | 40  |     | 60         | %    |
|                                                                  | 125–133 MHz, $C_L = 15$ pF                                   | 40  |     | 60         | %    |
| <b>Duty Cycle:</b><br>CMOS @ Vdd/2<br>4.5-5.5 Vdd<br>3.0–3.6 Vdd | $\leq 66$ MHz, $C_L \leq 25$ pF                              | 45  |     | 55         | %    |
|                                                                  | 66–125 MHz, $C_L \leq 25$ pF                                 | 40  |     | 60         | %    |
|                                                                  | 125–133 MHz, $C_L \leq 15$ pF                                | 40  |     | 60         | %    |
|                                                                  | $\leq 40$ MHz, $C_L \leq 30$ pF                              | 45  |     | 55         | %    |
|                                                                  | 40-100 MHz, $C_L \leq 15$ pF                                 | 40  |     | 60         | %    |
| <b>Output Clock Rise/Fall</b>                                    | 0.8V–2.0V, 4.5-5.5 Vdd, $C_L = 50$                           |     |     | 1.8        | ns   |
|                                                                  | 0.8V–2.0V, 4.5-5.5 Vdd, $C_L = 25$                           |     |     | 1.2        | ns   |
|                                                                  | 0.8V–2.0V, 4.5-5.5 Vdd, $C_L = 15$                           |     |     | 0.9        | ns   |
|                                                                  | 0.2–0.8Vdd, 4.5-5.5 Vdd, $C_L = 50$                          |     |     | 3.4        | ns   |
|                                                                  | 0.2–0.8Vdd, 3.0–3.6 Vdd, $C_L = 30$                          |     |     | 4.0        | ns   |
|                                                                  | 0.2–0.8Vdd, 3.0–3.6 Vdd, $C_L = 15$                          |     |     | 2.4        | ns   |
| <b>Start Up Time</b>                                             | From power on                                                |     |     | 2          | ms   |
| <b>Power Down Delay Time</b><br>Synchronous<br>Asynchronous      | PWR_DWN pin LOW to output Hi-Z                               |     | T/2 | T+10       | ns   |
|                                                                  |                                                              |     | 10  | 15         | ns   |
| <b>Output Disable Time</b><br>Synchronous<br>Asynchronous        | OE pin LOW to output Hi-Z<br>T = Frequency oscillator period |     | T/2 | T+10       | ns   |
|                                                                  |                                                              |     | 10  | 15         | ns   |
| <b>Output Enable Time</b>                                        |                                                              |     | T   | 1.5 T + 25 | ns   |
| <b>RMS Period Jitter:</b>                                        | 1 – 133 MHz                                                  |     | 8   | 11         | ps   |
| Peak to Peak *                                                   | $\leq 33.000$ MHz                                            |     | 65  | 99         | ps   |
|                                                                  | $> 33.000$ MHz                                               |     | 65  | 80         | ps   |

\* Jitter tested at > 1,000,000 samples, exceeding JEDEC std JESD65.

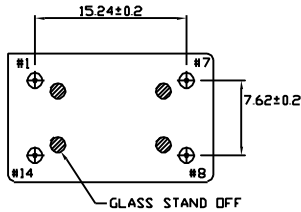
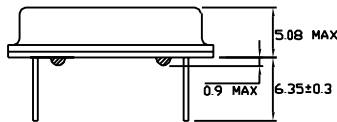
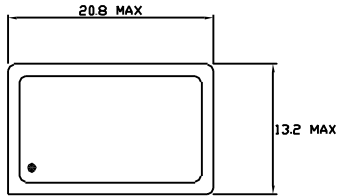


# Field Programmable Blank Oscillator

**Note:** *Bypass Vdd to GND with a 0.01  $\mu$ F capacitor*

## Style 1 Full Size 14 Pin Dip

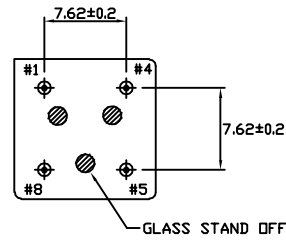
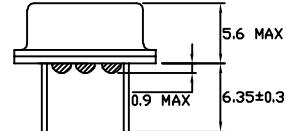
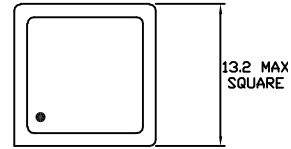
STYLE 1 FULL SIZE 14 PIN DIP



**PIN FUNCTION**  
1 CONTROL  
7 GND  
8 OUTPUT  
14 Vdd

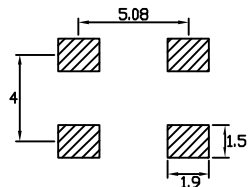
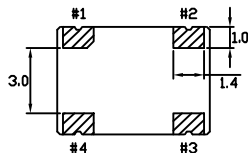
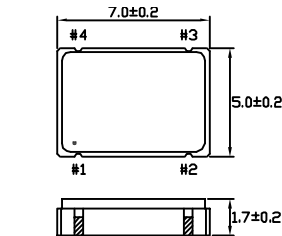
## Style 4 Half Size 8 Pin Dip

STYLE 4 HALFSIZE 8 PIN DIP



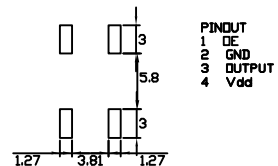
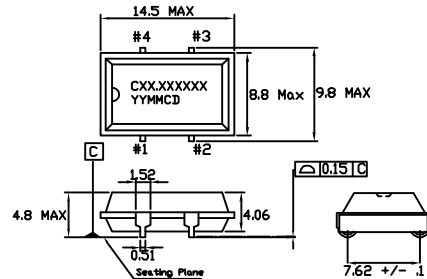
**PIN FUNCTION**  
1 CONTROL  
4 GND  
5 OUTPUT  
8 Vdd

## Style 7 5x7 Ceramic SMD



**PIN FUNCTION**  
1 CONTROL  
2 GND  
3 OUTPUT  
4 Vdd

## Style 8 Plastic SMD



**PINOUT**  
1 OE  
2 GND  
3 OUTPUT  
4 Vdd

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**Note:** *Bypass Vdd to GND with a 0.01  $\mu$ F capacitor*

## Style 5 3.2x5 Ceramic SMD

