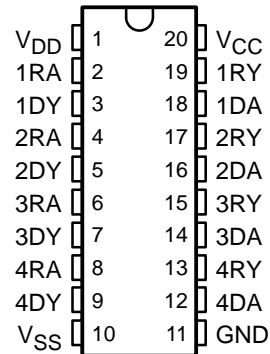


SN65C1154, SN75C1154 QUADRUPLE LOW-POWER DRIVERS/RECEIVERS

SLLS151D – DECEMBER 1988 – REVISED APRIL 2003

- Meet or Exceed the Requirements of TIA/EIA-232-F and ITU Recommendation V.28
- Very Low Power Consumption . . . 5 mW Typ
- Wide Driver Supply Voltage . . . ± 4.5 V to ± 15 V
- Driver Output Slew Rate Limited to 30 V/ μ s Max
- Receiver Input Hysteresis . . . 1000 mV Typ
- Push-Pull Receiver Outputs
- On-Chip Receiver 1- μ s Noise Filter

SN65C1154 . . . N PACKAGE
SN75C1154 . . . DW, N, OR NS PACKAGE
(TOP VIEW)



description/ordering information

The SN65C1154 and SN75C1154 are low-power BiMOS devices containing four independent drivers and receivers that are used to interface data terminal equipment (DTE) with data circuit-terminating equipment (DCE). These devices are designed to conform to TIA/EIA-232-F. The drivers and receivers of the SN65C1154 and SN75C1154 are similar to those of the SN75C188 quadruple driver and SN75C189A quadruple receiver, respectively. The drivers have a controlled output slew rate that is limited to a maximum of 30 V/ μ s and the receivers have filters that reject input noise pulses of shorter than 1 μ s. Both these features eliminate the need for external components.

The SN65C1154 and SN75C1154 have been designed using low-power techniques in a BiMOS technology. In most applications, the receivers contained in these devices interface to single inputs of peripheral devices such as ACEs, UARTs, or microprocessors. By using sampling, such peripheral devices usually are insensitive to the transition times of the input signals. If this is not the case, or for other uses, it is recommended that the SN65C1154 and SN75C1154 receiver outputs be buffered by single Schmitt input gates or single gates of the HCMOS, ALS, or 74F logic families.

ORDERING INFORMATION

| T _A | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|-----------|--------------|-----------------------|------------------|
| -40°C to 85°C | PDIP (N) | Tube of 20 | SN65C1154N | SN65C1154N |
| 0°C to 70°C | PDIP (N) | Tube of 20 | SN75C1154N | SN75C1154N |
| | SOIC (DW) | Tube of 25 | SN75C1154DW | SN75C1154 |
| | | Reel of 2500 | SN75C1154DWR | |
| | SOP (NS) | Reel of 2000 | SN75C1154NSR | SN75C1154 |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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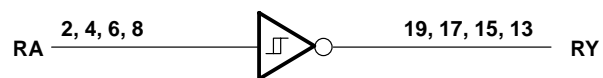
SN65C1154, SN75C1154

QUADRUPLE LOW-POWER DRIVERS/RECEIVERS

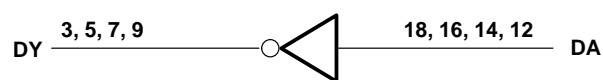
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logic diagram (positive logic)

Typical of Each Receiver



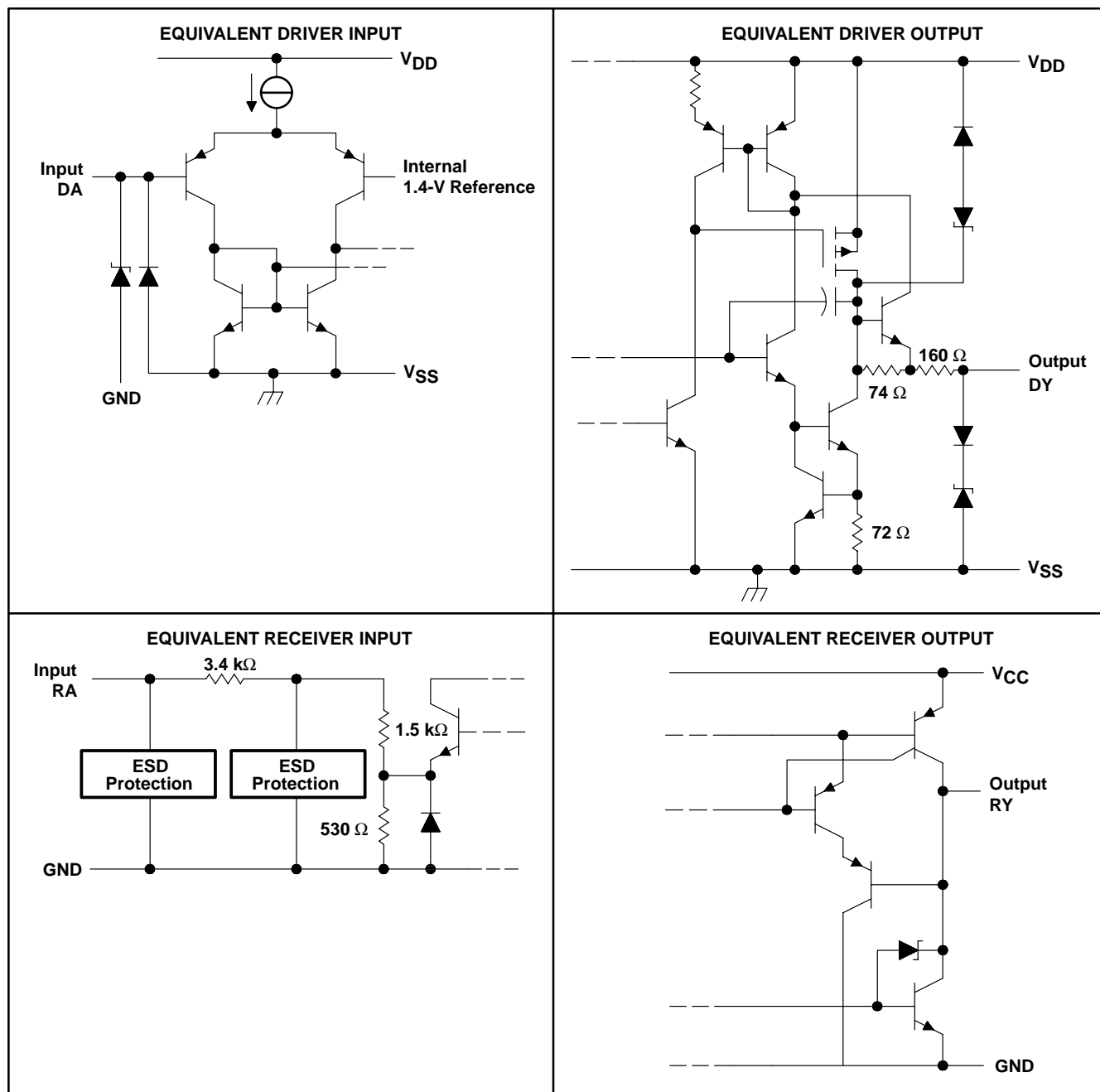
Typical of Each Driver



SN65C1154, SN75C1154 QUADRUPLE LOW-POWER DRIVERS/RECEIVERS

SLLS151D – DECEMBER 1988 – REVISED APRIL 2003

schematics of inputs and outputs



Resistor values shown are nominal.

SN65C1154, SN75C1154

QUADRUPLE LOW-POWER DRIVERS/RECEIVERS

SLLS151D – DECEMBER 1988 – REVISED APRIL 2003

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

| | |
|--|--|
| Supply voltage: V_{DD} (see Note 1) | 15 V |
| V_{SS} | –15 V |
| V_{CC} | 7 V |
| Input voltage range, V_I : Driver | V_{SS} to V_{DD} |
| Receiver | –30 V to 30 V |
| Output voltage range, V_O : Driver | ($V_{SS} - 6$ V) to ($V_{DD} + 6$ V) |
| Receiver | –0.3 V to ($V_{CC} + 0.3$ V) |
| Package thermal impedance, θ_{JA} (see Notes 2 and 3): DW package | 58°C/W |
| N package | 69°C/W |
| NS package | 60°C/W |
| Operating virtual junction temperature, T_J | 150°C |
| Storage temperature range, T_{stg} | –65°C to 150°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | 260°C |

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. All voltage s are with respect to the network GND terminal.
 2. Maximum power dissipation is a function of $T_J(\text{max})$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(\text{max}) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
 3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

| | | | MIN | NOM | MAX | UNIT |
|-----------------|--------------------------------|-----------|---------------------|-----|-----------------|------|
| V _{DD} | Supply voltage | | 4.5 | 12 | 15 | V |
| V _{SS} | Supply voltage | | −4.5 | −12 | −15 | V |
| V _{CC} | Supply voltage | | 4.5 | 5 | 6 | V |
| V _I | Input voltage | Driver | V _{SS} + 2 | | V _{DD} | V |
| | | Receiver | | | ±25 | |
| V _{IH} | High-level input voltage | Driver | 2 | | | V |
| V _{IL} | Low-level input voltage | Driver | | | 0.8 | V |
| I _{OH} | High-level output current | Receiver | | | −1 | mA |
| I _{OL} | High-level output current | Receiver | | | 3.2 | mA |
| T _A | Operating free-air temperature | SN65C1154 | −40 | | 85 | °C |
| | | SN75C1154 | 0 | | 70 | |



SN65C1154, SN75C1154 QUADRUPLE LOW-POWER DRIVERS/RECEIVERS

SLLS151D – DECEMBER 1988 – REVISED APRIL 2003

DRIVER SECTION

electrical characteristics over operating free-air temperature range, $V_{DD} = 12\text{ V}$, $V_{SS} = -12\text{ V}$, $V_{CC} = 5\text{ V} \pm 10\%$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | | MIN | TYP† | MAX | UNIT | |
|---------------------|---|---|----------------|-------------------------|-------|------|------|-------|----|
| VOH | High-level output voltage | VIL = 0.8 V, See Figure 1 | RL = 3 kΩ, | VDD = 5 V, VSS = −5 V | 4 | 4.5 | V | | |
| | | | | VDD = 12 V, VSS = −12 V | 10 | 10.8 | | | |
| VOL | Low-level output voltage (see Note 4) | VIH = 2 V, See Figure 1 | RL = 3 kΩ, | VDD = 5 V, VSS = −5 V | −4.4 | −4 | V | | |
| | | | | VDD = 12 V, VSS = −12 V | −10.7 | −10 | | | |
| IIH | High-level input current | VI = 5 V, | See Figure 2 | | | | 1 | μA | |
| IIL | Low-level input current | VI = 0, | See Figure 2 | | | | −1 | μA | |
| I _{OS} (H) | High-level short-circuit output current‡ | VI = 0.8 V, | VO = 0 or VSS, | See Figure 1 | | −7.5 | −12 | −19.5 | mA |
| I _{OS} (L) | Low-level short-circuit output current‡ | VI = 2 V, | VO = 0 or VDD, | See Figure 1 | | 7.5 | 12 | 19.5 | mA |
| IDD | Supply current from VDD | No load, All inputs at 2 V or 0.8 V | | VDD = 5 V, VSS = −5 V | | 115 | 250 | μA | |
| | | | | VDD = 12 V, VSS = −12 V | | 115 | 250 | | |
| ISS | Supply current from VSS | No load, All inputs at 2 V or 0.8 V | | VDD = 5 V, VSS = −5 V | | −115 | −250 | μA | |
| | | | | VDD = 12 V, VSS = −12 V | | −115 | −250 | | |
| ro | Output resistance | VDD = VSS = VCC = 0, VO = −2 V to 2 V, See Note 5 | | | 300 | 400 | | Ω | |

† All typical values are at $T_A = 25^\circ\text{C}$.

‡ Not more than one output should be shorted at one time.

NOTES: 4. The algebraic convention, where the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic levels only.

5. Test conditions are those specified by TIA/EIA-232-F.

switching characteristics, $V_{DD} = 12\text{ V}$, $V_{SS} = -12\text{ V}$, $V_{CC} = 5\text{ V} \pm 10\%$, $T_A = 25^\circ\text{C}$ (see Figure 3)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|--|------|-----|-----|------------------|
| t_{PLH} Propagation delay time, low- to high-level output§ | $R_L = 3$ to $7\text{ k}\Omega$, $C_L = 15\text{ pF}$ | | 1.2 | 3 | μs |
| t_{PHL} Propagation delay time, high- to low-level output§ | $R_L = 3$ to $7\text{ k}\Omega$, $C_L = 15\text{ pF}$ | | 2.5 | 3.5 | μs |
| t_{TLH} Transition time, low- to high-level output¶ | $R_L = 3$ to $7\text{ k}\Omega$, $C_L = 15\text{ pF}$ | 0.53 | 2 | 3.2 | μs |
| t_{THL} Transition time, high- to low-level output¶ | $R_L = 3$ to $7\text{ k}\Omega$, $C_L = 15\text{ pF}$ | 0.53 | 2 | 3.2 | μs |
| t_{TLH} Transition time, low- to high-level output# | $R_L = 3$ to $7\text{ k}\Omega$, $C_L = 2500\text{ pF}$ | | 1 | 2 | μs |
| t_{THL} Transition time, high- to low-level output# | $R_L = 3$ to $7\text{ k}\Omega$, $C_L = 2500\text{ pF}$ | | 1 | 2 | μs |
| SR Output slew rate | $R_L = 3$ to $7\text{ k}\Omega$, $C_L = 15\text{ pF}$ | 4 | 10 | 30 | V/ μs |

§ t_{PHL} and t_{PLH} include the additional time due to on-chip slew rate control and are measured at the 50% points.

¶ Measured between 10% and 90% points of output waveform

Measured between 3 V and -3 V points of output waveform (TIA/EIA-232-F conditions) with all unused inputs tied either high or low



SN65C1154, SN75C1154

QUADRUPLE LOW-POWER DRIVERS/RECEIVERS

SLLS151D – DECEMBER 1988 – REVISED APRIL 2003

RECEIVER SECTION

electrical characteristics over operating free-air temperature range, $V_{DD} = 12\text{ V}$, $V_{SS} = -12\text{ V}$, $V_{CC} = 5\text{ V} \pm 10\%$ (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP† | MAX | UNIT |
|--|---|--|-------|------|---------------|
| V_{IT+} Positive-going input threshold voltage | See Figure 5 | 1.7 | 2.1 | 2.55 | V |
| V_{IT-} Negative-going input threshold voltage | See Figure 5 | 0.65 | 1 | 1.25 | V |
| V_{hys} Input hysteresis voltage ($V_{IT+} - V_{IT-}$) | | 600 | 1000 | | mV |
| V_{OH} High-level output voltage | $V_I = 0.75\text{ V}$, $I_{OH} = -20\text{ }\mu\text{A}$, See Figure 5 and Note 6 | 3.5 | | | V |
| | $V_I = 0.75\text{ V}$, $I_{OH} = -1\text{ mA}$, See Figure 5, $V_{CC} = 4.5\text{ V}$ | 2.8 | 4.4 | | |
| | $V_I = 0.75\text{ V}$, $I_{OH} = -1\text{ mA}$, See Figure 5, $V_{CC} = 5\text{ V}$ | 3.8 | 4.9 | | |
| | $V_I = 0.75\text{ V}$, $I_{OH} = -1\text{ mA}$, See Figure 5, $V_{CC} = 5.5\text{ V}$ | 4.3 | 5.4 | | |
| V_{OL} Low-level output voltage | $V_I = 3\text{ V}$, $I_{OL} = 3.2\text{ mA}$, See Figure 5 | | 0.17 | 0.4 | V |
| I_{IH} High-level input current | $V_I = 25\text{ V}$ | 3.6 | 4.6 | 8.3 | mA |
| | $V_I = 3\text{ V}$ | 0.43 | 0.55 | 1 | |
| I_{IL} Low-level input current | $V_I = -25\text{ V}$ | -3.6 | -5 | -8.3 | mA |
| | $V_I = -3\text{ V}$ | -0.43 | -0.55 | -1 | |
| $I_{OS(H)}$ Short-circuit output at high level | $V_I = 0.75\text{ V}$, $V_O = 0$, See Figure 4 | | -8 | -15 | mA |
| $I_{OS(L)}$ Short-circuit output at low level | $V_I = V_{CC}$, $V_O = V_{CC}$, See Figure 4 | | 13 | 25 | mA |
| I_{CC} Supply current from V_{CC} | No load, All inputs at 0 or 5 V | $V_{DD} = 5\text{ V}$, $V_{SS} = -5\text{ V}$ | 400 | 600 | μA |
| | | $V_{DD} = 12\text{ V}$, $V_{SS} = -12\text{ V}$ | 400 | 600 | |

† All typical values are at $T_A = 25^\circ\text{C}$.

NOTE 6: If the inputs are left unconnected, the receiver interprets this as an input low and the receiver outputs will remain in the high state.

switching characteristics, $V_{DD} = 12\text{ V}$, $V_{SS} = -12\text{ V}$, $V_{CC} = 5\text{ V} \pm 10\%$, $T_A = 25^\circ\text{C}$

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|--|-----|-----|-----|---------------|
| t_{PLH} Propagation delay time, low- to high-level output | $C_L = 50\text{ pF}$, $R_L = 5\text{ k}\Omega$, See Figure 6 | | 3 | 4 | μs |
| t_{PHL} Propagation delay time, high- to low-level output | $C_L = 50\text{ pF}$, $R_L = 5\text{ k}\Omega$, See Figure 6 | | 3 | 4 | μs |
| t_{TLH} Transition time, low- to high-level output | $C_L = 50\text{ pF}$, $R_L = 5\text{ k}\Omega$, See Figure 6 | | 300 | 450 | ns |
| t_{THL} Transition time, high- to low-level output | $C_L = 50\text{ pF}$, $R_L = 5\text{ k}\Omega$, See Figure 6 | | 100 | 300 | ns |
| $t_{w(N)}$ Duration of longest pulse rejected as noise‡ | $C_L = 50\text{ pF}$, $R_L = 5\text{ k}\Omega$ | 1 | | 4 | μs |

‡ The receiver ignores any positive- or negative-going pulse that is less than the minimum value of $t_{w(N)}$ and accepts any positive- or negative-going pulse greater than the maximum of $t_{w(N)}$.



PARAMETER MEASUREMENT INFORMATION

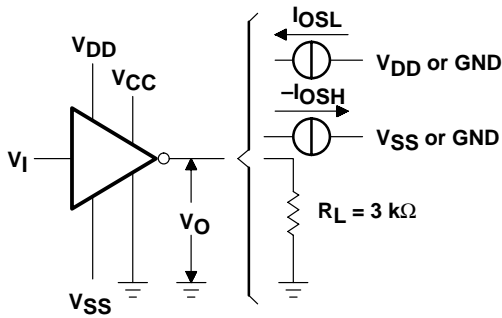


Figure 1. Driver Test Circuit (V_{OH} , V_{OL} , I_{OSL} , I_{OSH})

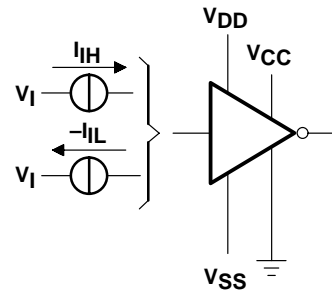
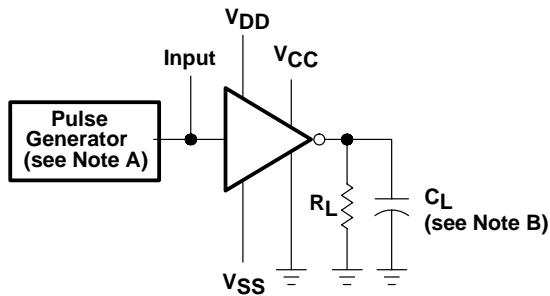
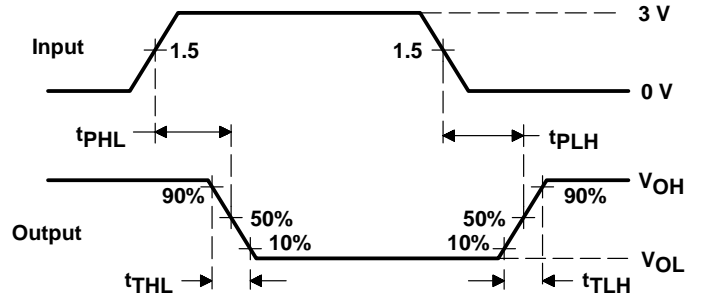


Figure 2. Driver Test Circuit (I_{IL} , I_{IH})



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: $t_W = 25 \mu s$, $PRR = 20 \text{ kHz}$, $Z_O = 50 \Omega$, $t_r = t_f < 50 \text{ ns}$.
B. C_L includes probe and jig capacitance.

Figure 3. Driver Test Circuit and Voltage Waveforms

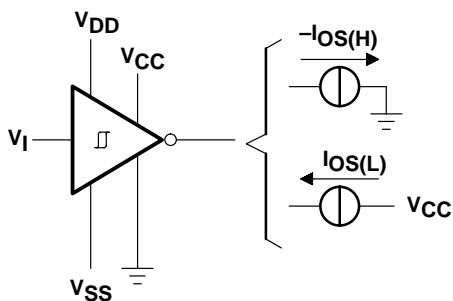


Figure 4. Receiver Test Circuit (I_{OSH} , I_{OSL})

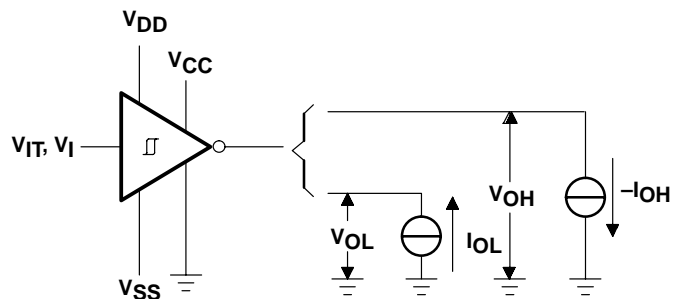
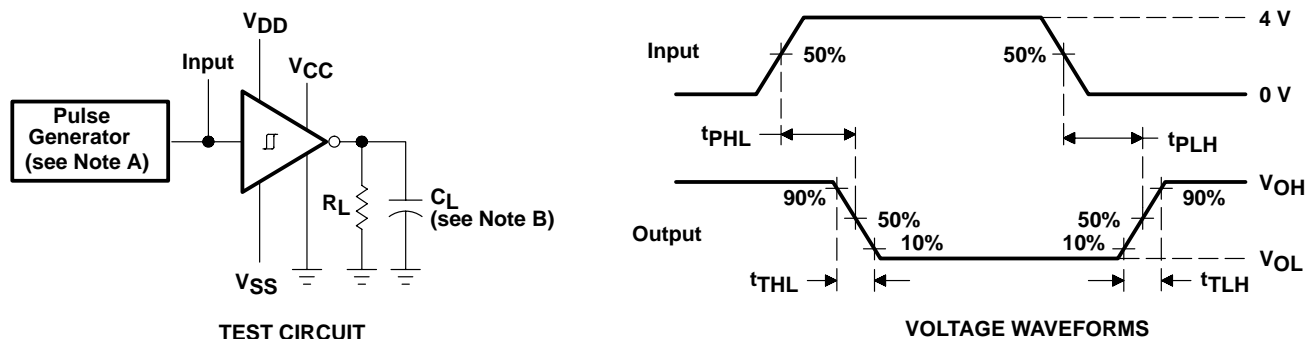


Figure 5. Receiver Test Circuit (V_{IT} , V_{OL} , V_{OH})

SN65C1154, SN75C1154 QUADRUPLE LOW-POWER DRIVERS/RECEIVERS

SLLS151D – DECEMBER 1988 – REVISED APRIL 2003

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics: $t_W = 25 \mu s$, $PRR = 20 \text{ kHz}$, $Z_O = 50 \Omega$, $t_r = t_f < 50 \text{ ns}$.
B. C_L includes probe and jig capacitance.

Figure 6. Receiver Test Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| SN65C1154DW | OBSOLETE | SOIC | DW | 20 | | TBD | Call TI | Call TI | | | |
| SN65C1154DWR | OBSOLETE | SOIC | DW | 20 | | TBD | Call TI | Call TI | | | |
| SN65C1154N | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -40 to 85 | SN65C1154N | Samples |
| SN65C1154NE4 | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -40 to 85 | SN65C1154N | Samples |
| SN75C1154DW | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | SN75C1154 | Samples |
| SN75C1154DWG4 | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | SN75C1154 | Samples |
| SN75C1154DWR | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | SN75C1154 | Samples |
| SN75C1154N | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | SN75C1154N | Samples |
| SN75C1154NE4 | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | SN75C1154N | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN75C1154DWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



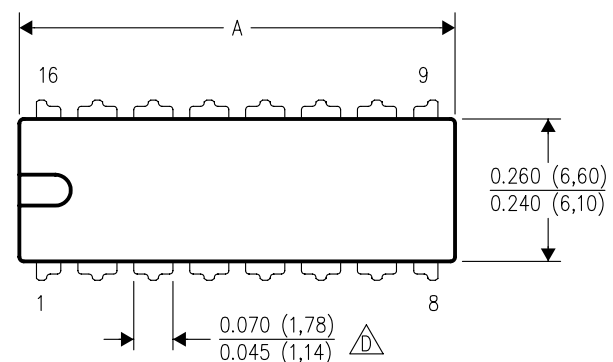
*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN75C1154DWR | SOIC | DW | 20 | 2000 | 367.0 | 367.0 | 45.0 |

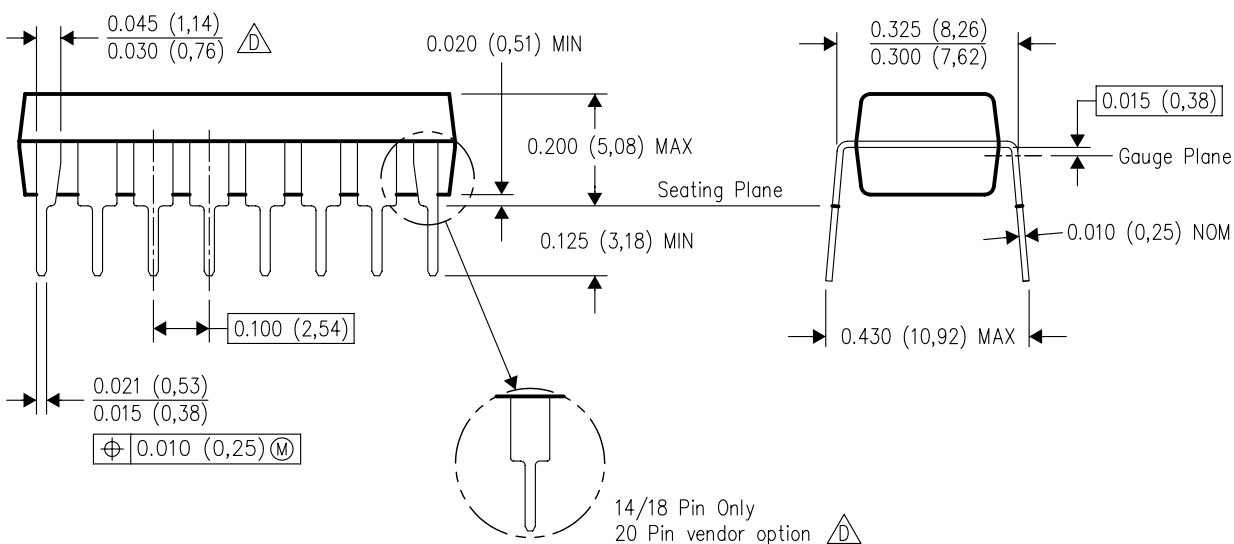
N (R-PDIP-T**)

16 PINS SHOWN



PLASTIC DUAL-IN-LINE PACKAGE



| PINS ** DIM | 14 | 16 | 18 | 20 |
|---------------------|------------------|------------------|------------------|------------------|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS-001 VARIATION | AA | BB | AC | AD |

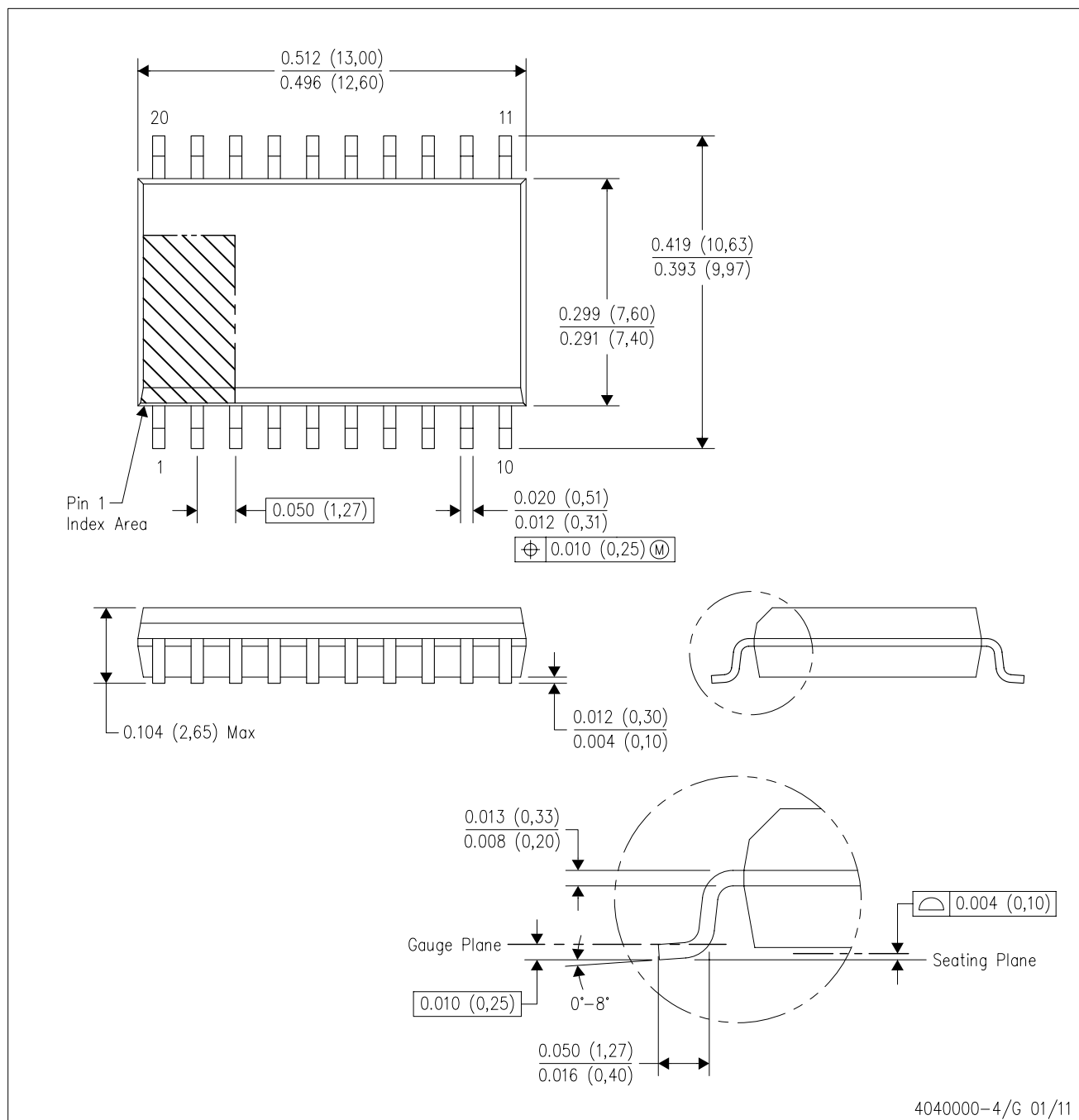


4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 -  The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-013 variation AC.

DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Refer to IPC7351 for alternate board design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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