



0.9Ω, Low-Voltage, Single-Supply Quad SPST Analog Switches

General Description

The MAX4751/MAX4752/MAX4753 are low on-resistance, low-voltage, quad, single-pole/single-throw (SPST) analog switches that operate from a single +1.6V to +3.6V supply. These devices have fast switching speeds ($t_{ON} = 30\text{ns}$, $t_{OFF} = 25\text{ns}$), handle Rail-to-Rail® analog signals, and consume less than $1\mu\text{W}$ of quiescent power. The MAX4753 has break-before-make switching.

When powered from a +3V supply, the MAX4751/MAX4752/MAX4753 feature low 0.9Ω (max) on-resistance (R_{ON}), with 0.12Ω (max) R_{ON} matching and 0.1Ω (max) R_{ON} flatness. The digital input is 1.8V CMOS compatible when using a single +3V supply.

The MAX4751 has four normally open (NO) switches, the MAX4752 has four normally closed (NC) switches, and the MAX4753 has two NO and two NC switches. The MAX4751/MAX4752/MAX4753 are available in $3\text{mm} \times 3\text{mm}$, 16-pin QFN and 14-pin TSSOP packages.

Applications

Power Routing
Battery-Powered Systems
Audio and Video Signal Routing
Low-Voltage Data-Acquisition Systems
Communications Circuits
PCMCIA Cards
Cellular Phones
Modems
Hard Drives

Features

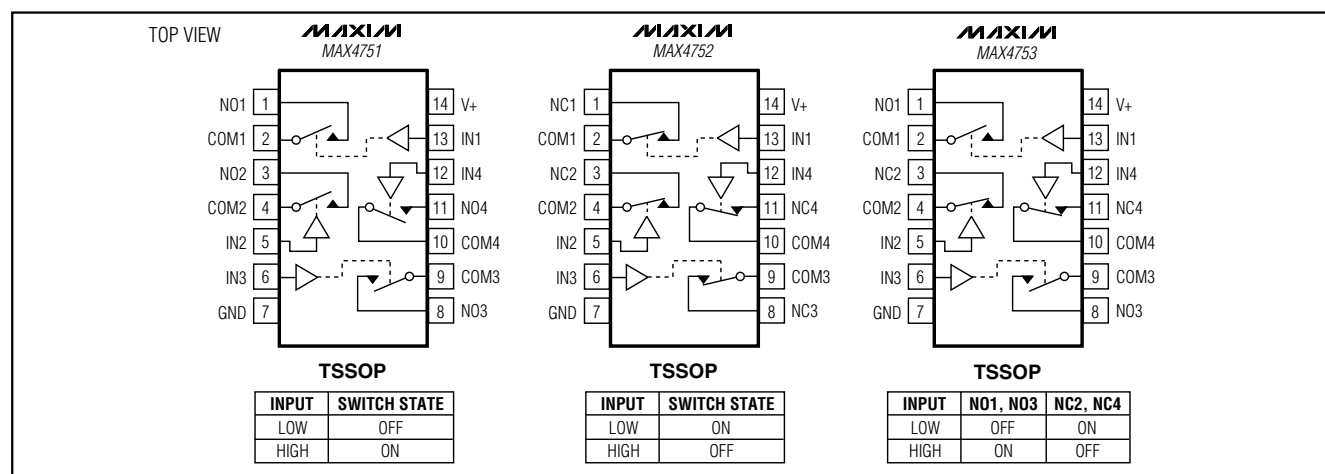
- ◆ **Low R_{ON}**
 0.9Ω max (+3V Supply)
 2.5Ω max (+1.8V Supply)
- ◆ **On-Resistance Flatness: 0.1Ω max (+3V)**
- ◆ **R_{ON} Matching**
 0.12Ω max (+3V Supply)
 0.25Ω max (+1.8V Supply)
- ◆ **+1.6V to +3.6V Single-Supply Operation**
- ◆ **Available in 16-Pin QFN and $3\text{mm} \times 3\text{mm}$ Packages**
- ◆ **1.8V CMOS Logic Compatible (+3V Supply)**
- ◆ **High Current-Handling Capacity (100mA Continuous)**
- ◆ **Fast Switching: $t_{ON} = 30\text{ns}$, $t_{OFF} = 25\text{ns}$**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX4751EUD	-40°C to +85°C	14 TSSOP	—
MAX4751EGE	-40°C to +85°C	16 QFN ($3\text{mm} \times 3\text{mm}$)	AAC
MAX4752EUD	-40°C to +85°C	14 TSSOP	—
MAX4752EGE	-40°C to +85°C	16 QFN ($3\text{mm} \times 3\text{mm}$)	AAD
MAX4753EUD	-40°C to +85°C	14 TSSOP	—
MAX4753EGE	-40°C to +85°C	16 QFN ($3\text{mm} \times 3\text{mm}$)	AAE

Rail-to-Rail is a registered trademark of Nippon Motorola, Ltd.

Pin Configurations/Functional Diagrams/Truth Tables



Pin Configurations/Functional Diagrams/Truth Tables continued at end of data sheet.



Maxim Integrated Products 1

For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

MAX4751/MAX4752/MAX4753

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ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to GND

V+, IN_ -0.3V to +4V

COM_, NO_, NC_ (Note 1) -0.3V to (V+ + 0.3V)

Continuous Current (COM_, NO_, NC_) $\pm 100\text{mA}$

Peak Current COM_, NO_, NC_ (pulsed at 1ms 10% duty cycle) $\pm 200\text{mA}$

Continuous Power Dissipation (T_A = +70°C)

14-Pin TSSOP (derate 9.1W/°C above +70°C) 727mW

16-Pin QFN (derate 16.9W/°C above +70°C) 1349mW

Operating Temperature Range -40°C to +85°C

Junction Temperature +150°C

Storage Temperature Range -65°C to +150°C

Lead Temperature (soldering, 10s) +300°C

Note 1: Signals on COM_, NO_, or NC_ exceeding V+ or GND are clamped by internal diodes. Limit forward diode current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Single +3V Supply

(V+ = +2.7V to +3.6V, V_{IHL} = +1.4V, V_{IL} = +0.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V+ = +3.0V, T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	T _A	MIN	TYP	MAX	UNITS
ANALOG SWITCH							
Analog Signal Range	V _{COM_} , V _{NO_} , V _{NC_}			0		V+	V
On-Resistance (Note 4)	R _{ON}	V+ = 2.7V, I _{COM_} = 100mA, V _{NO_} or V _{NC_} = 1.5V	+25°C		0.6	0.9	Ω
			T _{MIN} to T _{MAX}			1	
On-Resistance Match Between Channels (Notes 4, 5)	ΔR_{ON}	V+ = 2.7V, I _{COM_} = 100mA, V _{NO_} or V _{NC_} = 1.5V	+25°C		0.03	0.12	Ω
			T _{MIN} to T _{MAX}			0.15	
On-Resistance Flatness (Note 6)	R _{FLAT(ON)}	V+ = 2.7V, I _{COM_} = 100mA, V _{NO_} or V _{NC_} = 1V, 1.5V, 2V	+25°C		0.04	0.1	Ω
			T _{MIN} to T _{MAX}			0.12	
NO_ or NC_ Off-Leakage Current (Note 7)	I _{NO_(OFF)} , I _{NC_(OFF)}	V+ = 3.6V, V _{COM_} = 0.3V, 3.6V, V _{NO_} or V _{NC_} = 3.6V, 0.3V	+25°C	-2.5	0.002	+2.5	nA
			T _{MIN} to T _{MAX}	-5		+5	
COM_ Off-Leakage Current (Note 7)	I _{COM_(OFF)}	V+ = 3.6V, V _{COM_} = 0.3V, 3.6V, V _{NO_} or V _{NC_} = 3.6V, 0.3V	+25°C	-2.5	0.002	+2.5	nA
			T _{MIN} to T _{MAX}	-5		+5	
COM_ On-Leakage Current (Note 7)	I _{COM_(ON)}	V+ = 3.6V, V _{COM_} = 0.3V, 3.6V, V _{NO_} or V _{NC_} = 0.3V, 3.6V, or floating	+25°C	-2.5	0.002	+2.5	nA
			T _{MIN} to T _{MAX}	-5		+5	

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MAX4751/MAX4752/MAX4753

ELECTRICAL CHARACTERISTICS—Single +3V Supply (continued)

(V+ = +2.7V to +3.6V, V_{IH} = +1.4V, V_{IL} = +0.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V+ = +3.0V, T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	T _A	MIN	TYP	MAX	UNITS
SWITCH DYNAMIC CHARACTERISTICS							
Turn-On Time	t _{ON}	V _{NO} or V _{NC} = 1.5V, R _L = 50Ω, C _L = 35pF, Figure 1	+25°C	6	30		ns
			T _{MIN} to T _{MAX}		30		
Turn-Off Time	t _{OFF}	V _{NO} or V _{NC} = 1.5V, R _L = 50Ω, C _L = 35pF, Figure 1	+25°C	10	25		ns
			T _{MIN} to T _{MAX}		25		
Break-Before-Make (Note 8) (MAX4753 Only)	t _{BBM}	V _{NO} and V _{NC} = 1.5V, R _L = 50Ω, C _L = 35pF, Figure 1	+25°C	7			ns
			T _{MIN} to T _{MAX}	2			
Charge Injection	Q	V _{GEN} = 0, R _{GEN} = 0, C _L = 1.0nF, Figure 2	+25°C	21			pC
NO ₋ or NC ₋ Off-Capacitance	C _{OFF}	f = 1MHz, Figure 3	+25°C	31			pF
COM ₋ Off-Capacitance	C _{COM} (OFF)	f = 1MHz, Figure 3	+25°C	30			pF
COM ₋ On-Capacitance	C _{COM} (ON)	f = 1MHz, Figure 3	+25°C	75			pF
Off-Isolation (Note 9)	V _{ISO}	R _L = 50Ω, C _L = 5pF, Figure 4	f = 10MHz +25°C	-51			dB
			f = 1MHz +25°C	-65			
Crosstalk		R _L = 50Ω, C _L = 5pF, Figure 4	f = 10MHz +25°C	-70			dB
			f = 1MHz +25°C	-80			
Total Harmonic Distortion	THD	f = 20Hz to 20kHz, V _{COM} = 2V _{P-P} , R _L = 32Ω	+25°C	0.031			%
DIGITAL I/O							
Input Logic High	V _{IH}		T _{MIN} to T _{MAX}	1.4			V
Input Logic Low	V _{IL}		T _{MIN} to T _{MAX}			0.5	V
Input Leakage Current	I _{IN}	V _{IN} = 0 or V+	T _{MIN} to T _{MAX}	-1	0.0005	+1	μA
POWER SUPPLY							
Power-Supply Range	V+			+1.6		+3.6	V
Positive Supply Current	I+	V+ = 3.6V, V _{IN} = 0 or V+				1	μA

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ELECTRICAL CHARACTERISTICS—Single +1.8V Supply

(V₊ = +1.8V, V_{IH} = +1V, V_{IL} = +0.4V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	T _A	MIN	TYP	MAX	UNITS
ANALOG SWITCH							
Analog Signal Range	V _{COM} _, V _{NO} _, V _{NC} _			0		V+	V
On-Resistance (Note 4)	R _{ON}	V+ = 1.8V, I _{COM} = 10mA, V _{NO} _ or V _{NC} _ = 0.9V	+25°C		1.4	2.5	Ω
			T _{MIN} to T _{MAX}			3	
On-Resistance Match Between Channels (Notes 4, 5)	ΔR _{ON}	V+ = 1.8V, I _{COM} = 10mA, V _{NO} _ or V _{NC} _ = 0.9V	+25°C		0.05	0.25	Ω
			T _{MIN} to T _{MAX}			0.25	
SWITCH DYNAMIC CHARACTERISTICS							
Turn-On Time	t _{ON}	V _{NO} _ or V _{NC} _ = 1.0V, R _L = 50Ω, C _L = 35pF, Figure 1	+25°C		25	35	ns
			T _{MIN} to T _{MAX}			35	
Turn-Off Time	t _{OFF}	V _{NO} _ or V _{NC} _ = 1.0V, R _L = 50Ω, C _L = 35pF, Figure 1	+25°C		20	25	ns
			T _{MIN} to T _{MAX}			30	
Charge Injection	Q	V _{GEN} = 0, R _{GEN} = 0, C _L = 1.0nF, Figure 2	+25°C		8		pC
DIGITAL I/O							
Input Logic High	V _{IH} _		T _{MIN} to T _{MAX}		1.0		V
Input Logic Low	V _{IL} _		T _{MIN} to T _{MAX}			0.4	V
Input Leakage Current	I _{IN} _	V _{IN} _ = 0 or V+	T _{MIN} to T _{MAX}	-1	0.0005	+1	μA
POWER SUPPLY							
Power-Supply Range	V+			+1.6		+3.6	V
Positive Supply Current	I+	V _{IN} _ = 0 or V+				1	μA

Note 2: The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.

Note 3: Parts are tested at +85°C and guaranteed by design and correlation over the full temperature range.

Note 4: R_{ON} and Δ R_{ON} matching specifications for QFN-packaged parts are guaranteed by design.

Note 5: Δ R_{ON} = R_{ON}(MAX) - R_{ON}(MIN)

Note 6: Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges.

Note 7: Leakage parameters are 100% tested at the maximum-rated hot operating temperature and guaranteed by correlation at T_A = +25°C.

Note 8: Guaranteed by design, not production tested.

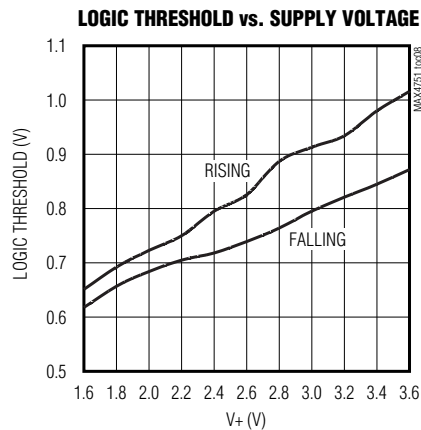
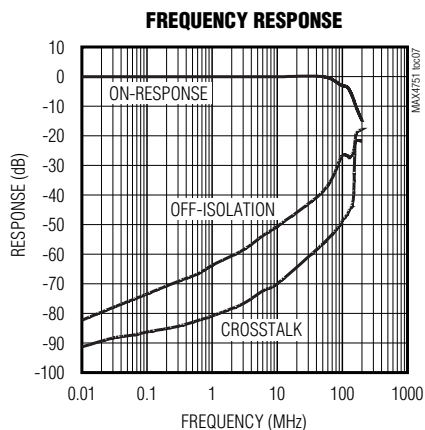
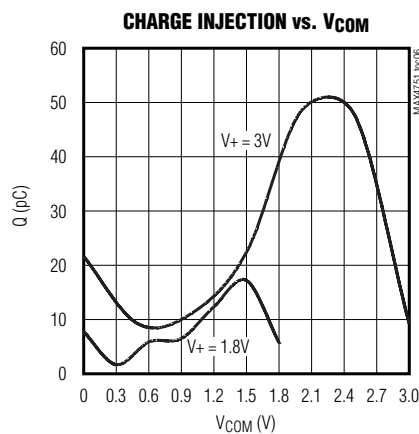
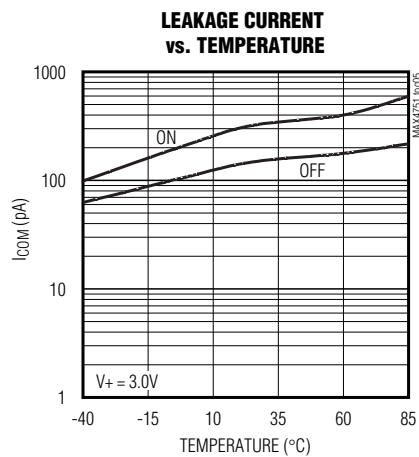
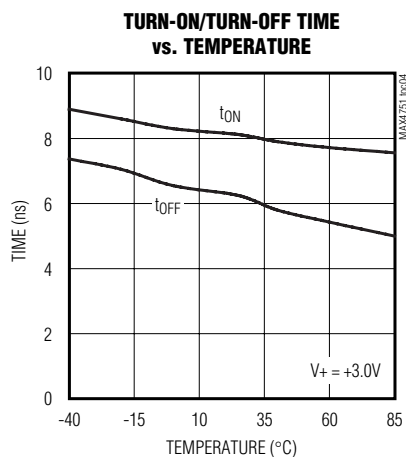
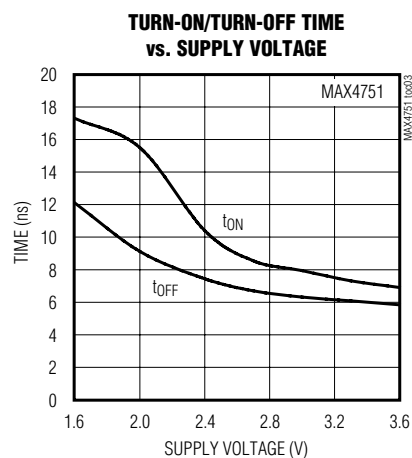
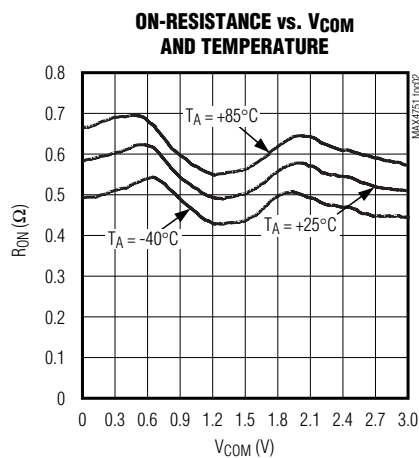
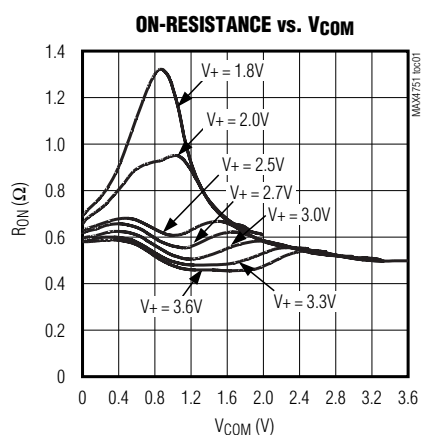
Note 9: Off-Isolation = 20log₁₀[V_{COM} / (V_{NC} or V_{NO})], V_{COM} = output, V_{NC} or V_{NO} = input to off switch.

0.9Ω, Low-Voltage, Single-Supply Quad SPST Analog Switches

Typical Operating Characteristics

(V+ = +3V and T_A = +25°C, unless otherwise noted.)

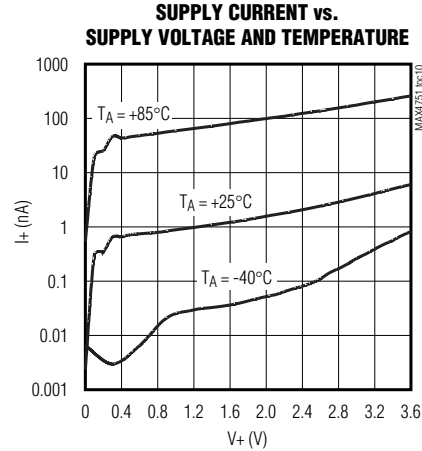
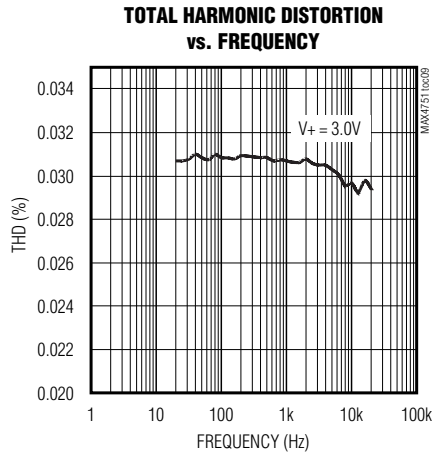
MAX4751/MAX4752/MAX4753



0.9Ω, Low-Voltage, Single-Supply Quad SPST Analog Switches

Typical Operating Characteristics (continued)

(V+ = +3V and T_A = +25°C, unless otherwise noted.)



Pin Description

PIN						NAME	FUNCTION
MAX4751		MAX4752		MAX4753			
TSSOP	QFN	TSSOP	QFN	TSSOP	QFN		
1, 3, 8, 11	15, 1, 7, 11	—	—	—	—	NO1, NO2, NO3, NO4	Switch Normally Open Terminals
—	—	1, 3, 8, 11	15, 1, 7, 11	—	—	NC1, NC2, NC3, NC4	Switch Normally Closed Terminals
—	—	—	—	3, 11	1, 11	NC2, NC4	Switch Normally Closed Terminals
—	—	—	—	1, 8	15, 7	NO1, NO3	Switch Normally Open Terminals
2, 4, 9, 10	16, 2, 8, 9	2, 4, 9, 10	16, 2, 8, 9	2, 4, 9, 10	16, 2, 8, 9	COM1, COM2, COM3, COM4	Switch Common Terminals
7	6	7	6	7	6	GND	Ground
13, 5, 6, 12	13, 4, 5, 12	13, 5, 6, 12	13, 4, 5, 12	13, 5, 6, 12	13, 4, 5, 12	IN1, IN2, IN3, IN4	Logic Control Inputs
14	14	14	14	14	14	V+	Positive Supply Voltage
—	3, 10	—	3, 10	—	3, 10	N.C.	No Connection. Not internally connected.

0.9Ω, Low-Voltage, Single-Supply Quad SPST Analog Switches

Test Circuits/Timing Diagrams

MAX4751/MAX4752/MAX4753

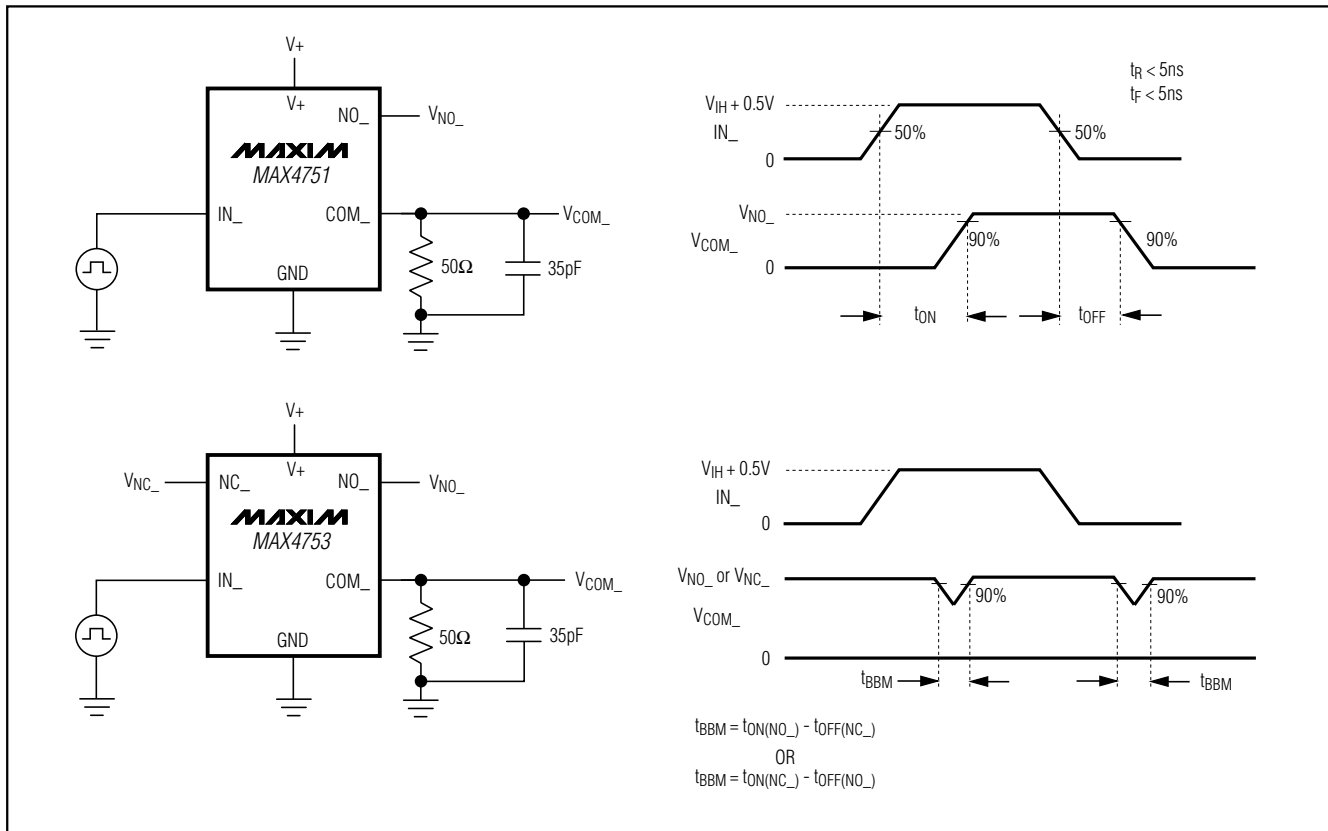


Figure1. Switching Times

0.9Ω, Low-Voltage, Single-Supply Quad SPST Analog Switches

Test Circuits/Timing Diagrams (continued)

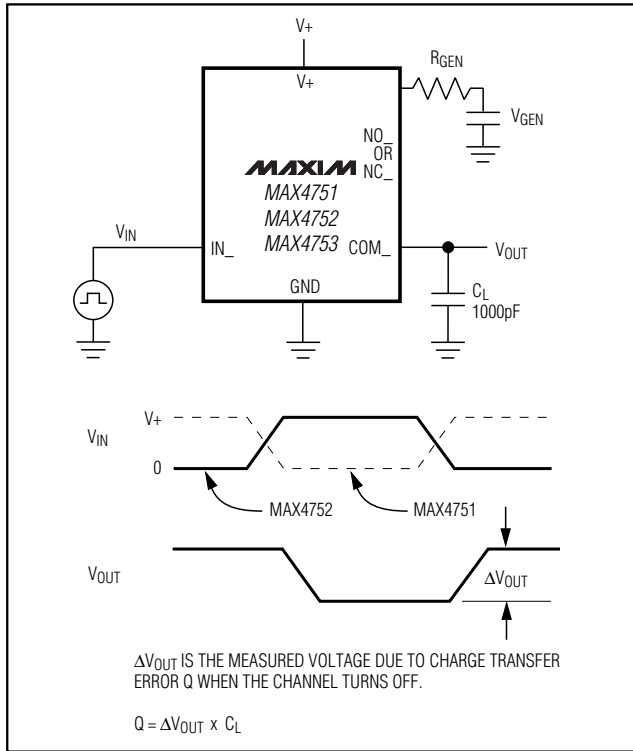


Figure 2. Charge Injection

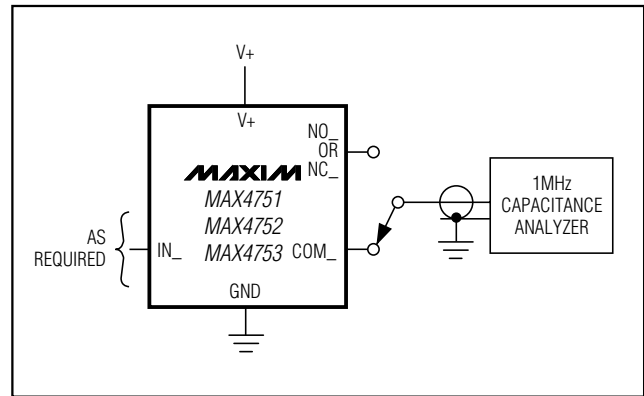


Figure 3. NO_, NC_, and COM_ Capacitance

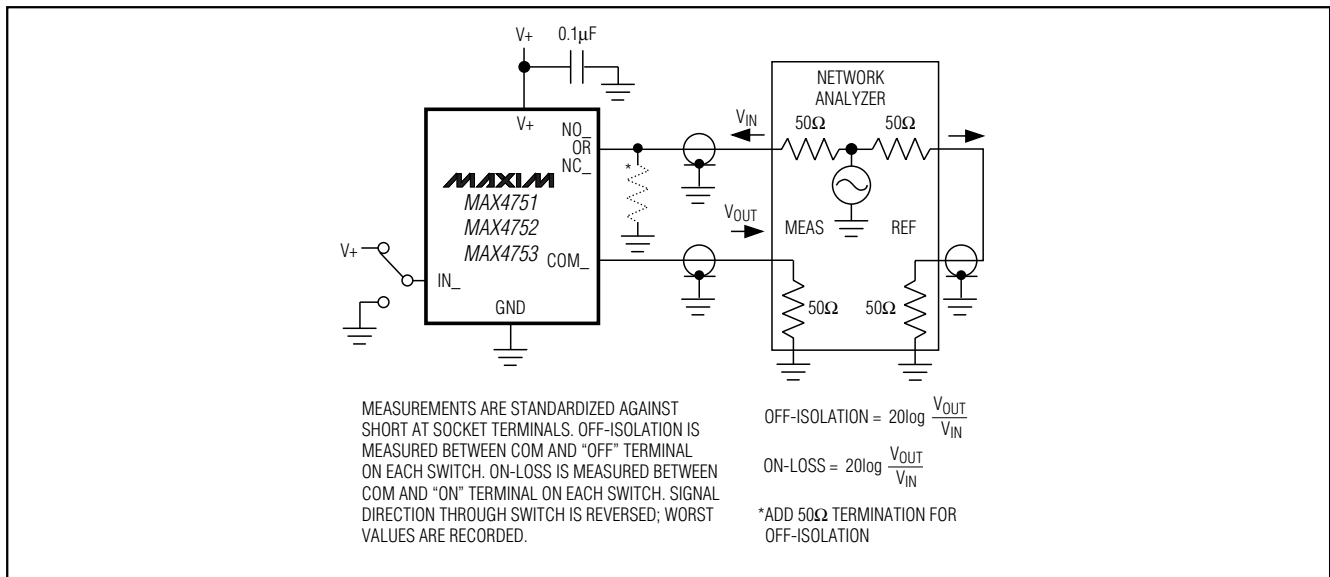


Figure 4. Off-Isolation, On-Loss, and Crosstalk

0.9Ω, Low-Voltage, Single-Supply Quad SPST Analog Switches

Detailed Description

The MAX4751/MAX4752/MAX4753 are low 0.9Ω max (at $V_+ = 3V$) on-resistance, low-voltage quad analog switches that operate from a +1.6V to +3.6V single supply. CMOS construction allows switching analog signals that are within the supply voltage range (GND to V_+).

When powered from a +3V supply, the 0.9Ω (max) R_{ON} allows high continuous currents to be switched in a variety of applications.

Applications Information

Proper power-supply sequencing is recommended for all CMOS devices. Do not exceed the absolute maximum ratings because stresses beyond the listed ratings can cause permanent damage to the devices. Always sequence V_+ on first, followed by $NO_$, $NC_$, or $COM_$. If power-supply sequencing is not possible, add two small-signal diodes (D1, D2) in series with the supply pins for overvoltage protection (Figure 5). Adding these diodes reduces the analog signal by one diode drop below V_+ and one diode drop above GND, but does not affect the low switch resistance and low leakage characteristics of the device. Device operation is unchanged, and the difference between V_+ and GND should not exceed 4V.

Power-supply bypassing is needed to improve noise margin and to prevent switching noise propagation from the V_+ supply to other components. A 0.1μF capacitor, connected from V_+ to GND, is adequate for most applications.

Logic Inputs

The MAX4751/MAX4752/MAX4753 logic inputs can be driven up to +3.6V regardless of the supply voltage. For example, with a +1.8V supply, $IN_$ may be driven low to GND and high to +3.6V. Driving $IN_$ rail-to-rail minimizes power consumption.

Analog Signal Levels

Analog signals that range over the entire supply voltage (V_+ to GND) can be passed with very little change in on-

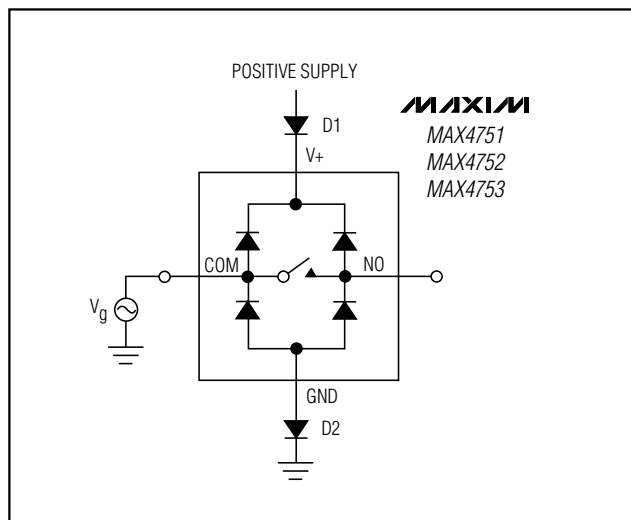


Figure 5. Overvoltage Protection Using Two External Blocking Diodes

resistance (see the *Typical Operating Characteristics*). The switches are bidirectional, so the $NO_$, $NC_$, and $COM_$ pins can be used as either inputs or outputs.

Layout

High-speed switches require proper layout and design procedures for optimum performance. Reduce stray inductance and capacitance by keeping traces short and wide. Ensure that bypass capacitors are as close to the device as possible. Use large ground planes where possible.

Chip Information

TRANSISTOR COUNT: 228

PROCESS: CMOS

MAX4751/MAX4752/MAX4753

0.9Ω, Low-Voltage, Single-Supply Quad SPST Analog Switches

Pin Configurations/Functional Diagrams/Truth Tables (continued)

TOP VIEW

QFN

MAX4751	
INPUT	SWITCH STATE
LOW	OFF
HIGH	ON

QFN

MAX4752	
INPUT	SWITCH STATE
LOW	ON
HIGH	OFF

QFN

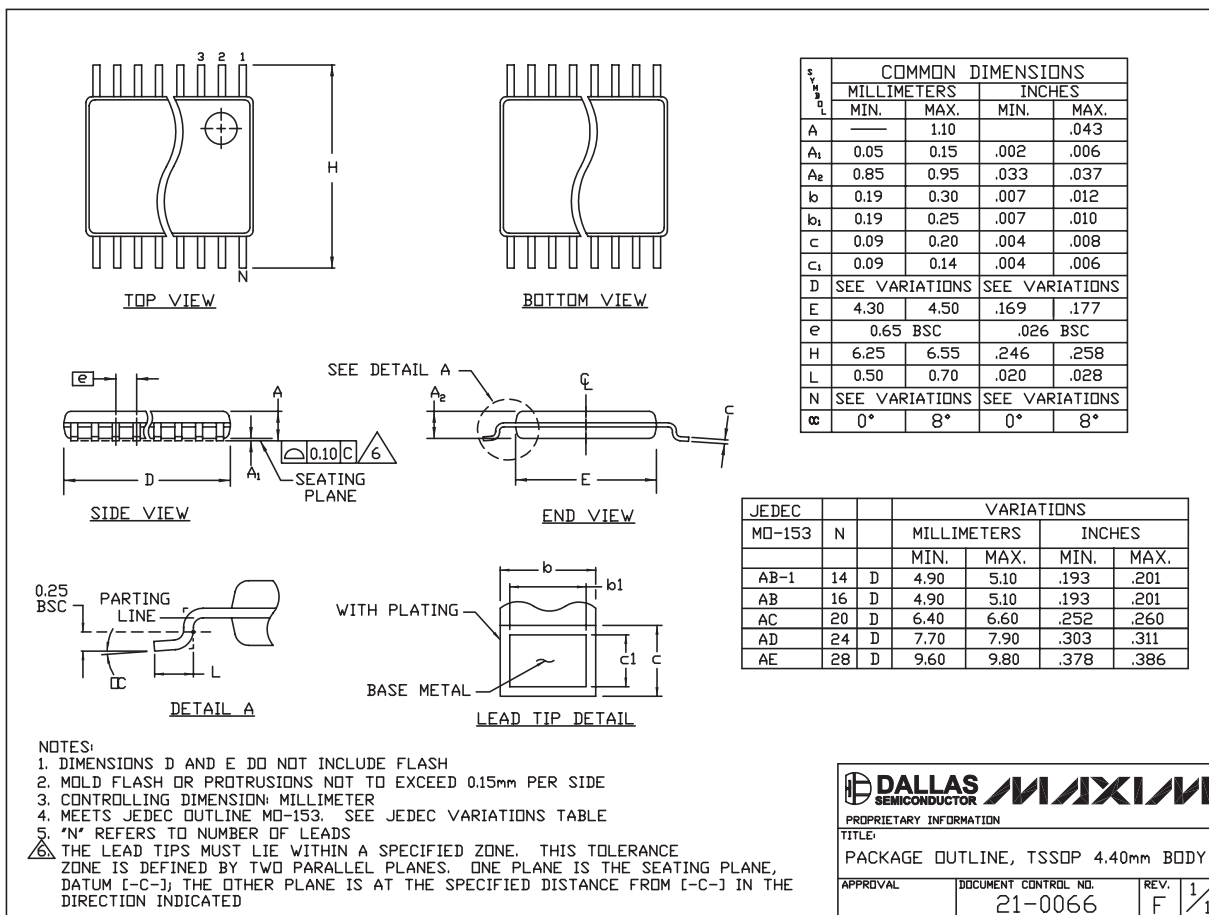
MAX4753		
INPUT	SWITCHES 1, 8	SWITCHES 2, 4
LOW	OFF	ON
HIGH	ON	OFF

0.9Ω, Low-Voltage, Single-Supply Quad SPST Analog Switches

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)

MAX4751/MAX4752/MAX4753

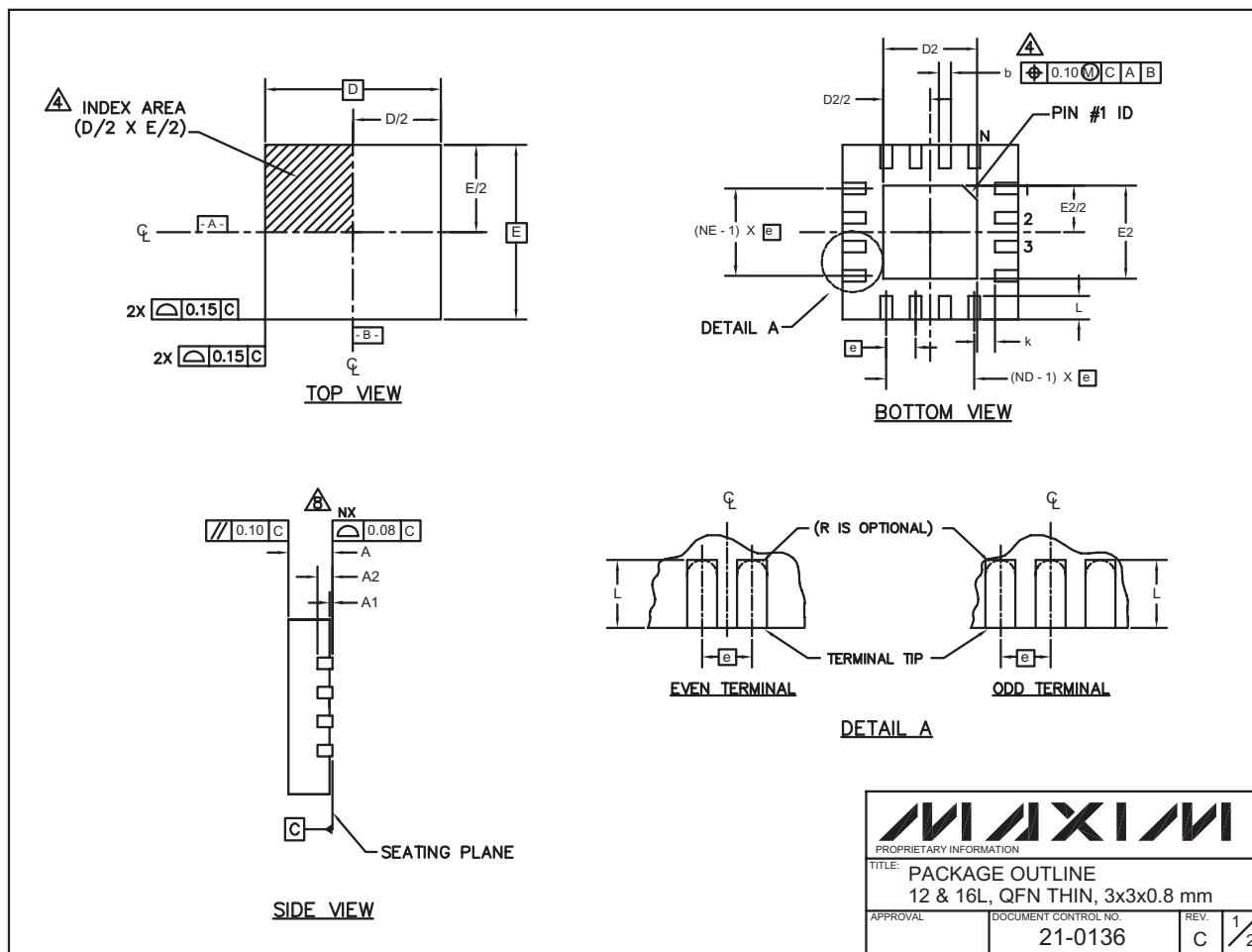


0.9 Ω , Low-Voltage, Single-Supply Quad SPST Analog Switches

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)

12x16L QFN THIN.EPS



0.9Ω, Low-Voltage, Single-Supply Quad SPST Analog Switches

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)

PKG	12L 3x3			16L 3x3		
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80
b	0.20	0.25	0.30	0.20	0.25	0.30
D	2.90	3.00	3.10	2.90	3.00	3.10
E	2.90	3.00	3.10	2.90	3.00	3.10
e	0.50 BSC.			0.50 BSC.		
L	0.45	0.55	0.65	0.30	0.40	0.50
N	12			16		
ND	3			4		
NE	3			4		
A1	0	0.02	0.05	0	0.02	0.05
A2	0.20 REF			0.20 REF		
k	0.25	-	-	0.25	-	-

EXPOSED PAD VARIATIONS								
PKG. CODES	D2			E2			PIN ID	JEDEC
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.		
T1233-1	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-1
T1633-1	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-2
T1633F-3	0.65	0.80	0.95	0.65	0.80	0.95	0.225 x 45°	-

NOTES:

- DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
- ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
- N IS THE TOTAL NUMBER OF TERMINALS.
- THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JEDEC 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
- DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.20 mm AND 0.25 mm FROM TERMINAL TIP.
- ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
- DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
- COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
- DRAWING CONFORMS TO JEDEC MO220 REVISION C.

			
PROPRIETARY INFORMATION			
TITLE: PACKAGE OUTLINE			
12 & 16L, QFN THIN, 3x3x0.8 mm			
APPROVAL	DOCUMENT CONTROL NO.	REV.	2/2
	21-0136	C	

MAX4751/MAX4752/MAX4753

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