Lattice®
Semiconductor
Corporation

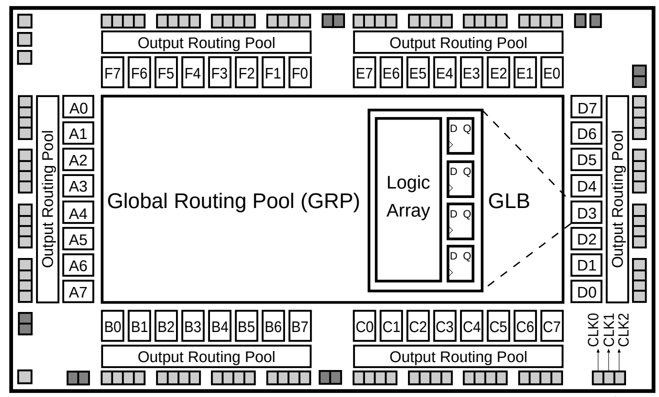
ispLSI® 2192VL

2.5V In-System Programmable SuperFAST™ High Density PLD

Features

- **SuperFAST HIGH DENSITY IN-SYSTEM PROGRAMMABLE LOGIC**
  - **— 8000 PLD Gates**
  - **— 96 I/O Pins, Nine Dedicated Inputs**
  - **— 192 Registers**
  - **— High Speed Global Interconnect**
  - **— Wide Input Gating for Fast Counters, State Machines, Address Decoders, etc.**
  - **— Small Logic Block Size for Random Logic**
  - **— Pinout Compatible with ispLSI 2096V and 2096VE**
- **2.5V LOW VOLTAGE ARCHITECTURE**
  - **— Interfaces with Standard 3.3V Devices (Inputs and I/Os are 3.3V Tolerant)**
  - **— 175 mA Typical Active Current**
- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - **— f_{max} = 150 MHz Maximum Operating Frequency**
  - **— t_{pd} = 6.0 ns Propagation Delay**
  - **— Electrically Erasable and Reprogrammable**
  - **— Non-Volatile**
  - **— 100% Tested at Time of Manufacture**
  - **— Unused Product Term Shutdown Saves Power**
- **IN-SYSTEM PROGRAMMABLE**
  - **— 2.5V In-System Programmability (ISP™) Using Boundary Scan Test Access Port (TAP)**
  - **— Open-Drain Output Option for Flexible Bus Interface Capability, Allowing Easy Implementation of Wired-OR Bus Arbitration Logic**
  - **— Increased Manufacturing Yields, Reduced Time-to-Market and Improved Product Quality**
  - **— Reprogram Soldered Devices for Faster Prototyping**
- **100% IEEE 1149.1 BOUNDARY SCAN TESTABLE**
- **THE EASE OF USE AND FAST SYSTEM SPEED OF PLDs WITH THE DENSITY AND FLEXIBILITY OF FPGAS**
  - **— Enhanced Pin Locking Capability**
  - **— Three Dedicated Clock Input Pins**
  - **— Synchronous and Asynchronous Clocks**
  - **— Programmable Output Slew Rate Control**
  - **— Flexible Pin Placement**
  - **— Optimized Global Routing Pool Provides Global Interconnectivity**

Functional Block Diagram



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Description

The ispLSI 2192VL is a High Density Programmable Logic Device containing 192 Registers, nine Dedicated Input pins, three Dedicated Clock Input pins, two dedicated Global OE input pins and a Global Routing Pool (GRP). The GRP provides complete interconnectivity between all of these elements. The ispLSI 2192VL features in-system programmability through the Boundary Scan Test Access Port (TAP) and is 100% IEEE 1149.1 Boundary Scan Testable. The ispLSI 2192VL offers non-volatile reprogrammability of the logic, as well as the interconnect to provide truly reconfigurable systems.

The basic unit of logic on the ispLSI 2192VL device is the Generic Logic Block (GLB). The GLBs are labeled A0, A1 .. F7 (see Figure 1). There are a total of 48 GLBs in the ispLSI 2192VL device. Each GLB is made up of four macrocells. Each GLB has 18 inputs, a programmable AND/OR/Exclusive OR array, and four outputs which can be configured to be either combinatorial or registered. Inputs to the GLB come from the GRP and dedicated inputs. All of the GLB outputs are brought back into the GRP so that they can be connected to the inputs of any GLB on the device.

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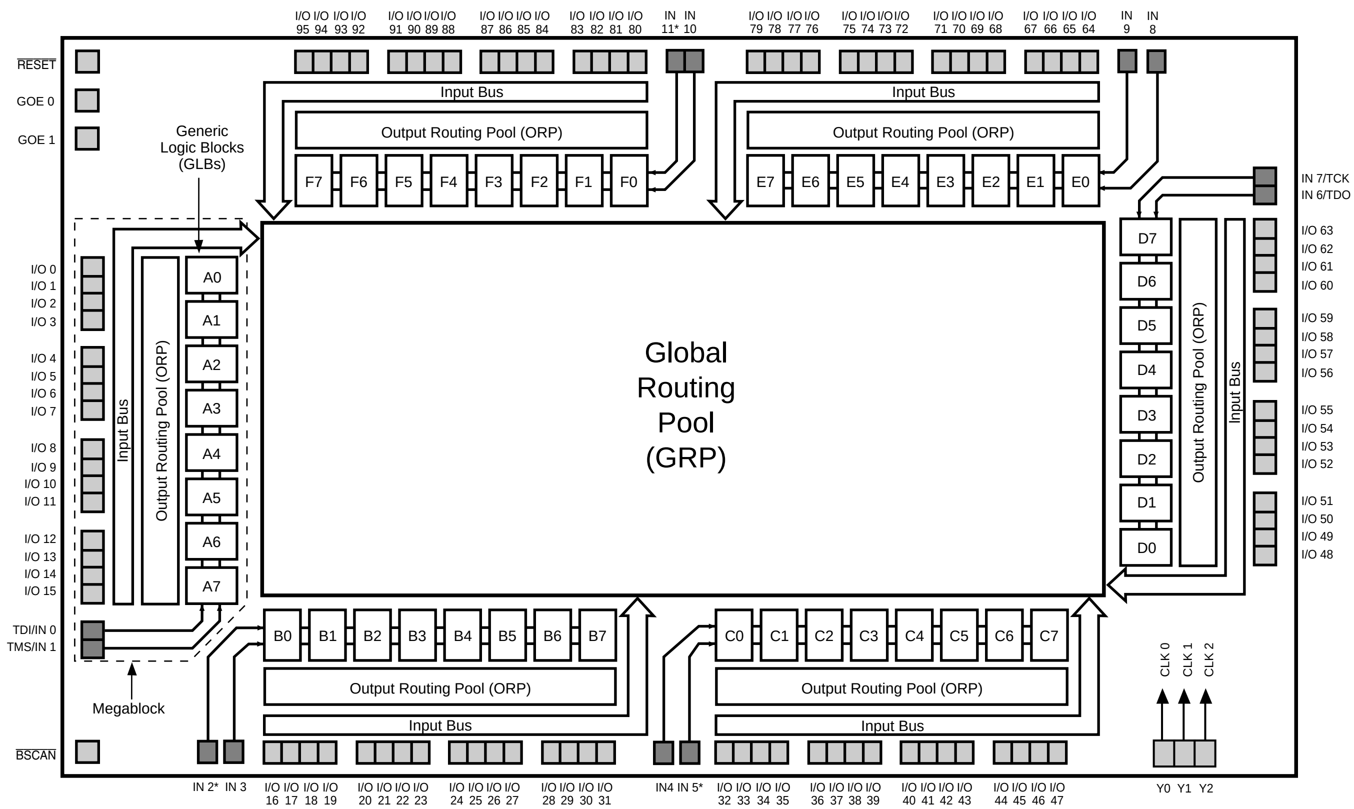
Functional Block Diagram

Figure 1. ispLSI 2192VL Functional Block Diagram



*Note: Dedicated Inputs 2, 5 and 11 are not available with 128-pin packages.

2192VL Block.eps

The 2192VL contains 96 I/O cells. Each I/O cell is directly connected to an I/O pin and can be individually programmed to be a combinatorial input, output or bi-directional I/O pin with 3-state control, and the output drivers can source 4mA or sink 8mA. Each output can be programmed independently for fast or slow output slew rate to minimize overall output switching noise. Device pins can be safely driven to 3.3V signal levels to support mixed-voltage systems.

Eight GLBs, 16 I/O cells, two dedicated inputs and an ORP are connected together to make a Megablock (see Figure 1). The outputs of the eight GLBs are connected to a set of 16 universal I/O cells by the ORPs. Each ispLSI 2192VL device contains six Megablocks.

The GRP has as its inputs, the outputs from all of the GLBs and all of the inputs from the bi-directional I/O cells. All of these signals are made available to the inputs of the GLBs. Delays through the GRP have been equalized to minimize timing skew.

Clocks in the ispLSI 2192VL device are selected using the dedicated clock pins. Three dedicated clock pins (Y0, Y1, Y2) or an asynchronous clock can be selected on a GLB basis. The asynchronous or Product Term clock can be generated in any GLB for its own clock.

Programmable Open-Drain Outputs

In addition to the standard output configuration, the outputs of the ispLSI 2192VL are individually programmable, either as a standard totem-pole output or an open-drain output. The totem-pole output drives the specified Voh and Vol levels, whereas the open-drain output drives only the specified Vol. The Voh level on the open-drain output depends on the external loading and pull-up. This output configuration is controlled by a programmable fuse. The default configuration is a totem-pole configuration. The open-drain/totem-pole option is selectable through the Lattice software tools.

Absolute Maximum Ratings [1]

Supply Voltage V_{cc} .... -0.5 to +4.05V

Input Voltage Applied .... -0.5 to +4.05V

Off-State Output Voltage Applied .... -0.5 to +4.05V

Storage Temperature .... -65 to 150°C

Case Temp. with Power Applied .... -55 to 125°C

Max. Junction Temp. (T_J) with Power Applied ... 150°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

DC Recommended Operating Condition

SYMBOL	PARAMETER			MIN.	MAX.	UNITS
V_{CC}	Supply Voltage	Commercial	T_A = 0°C to + 70°C	2.3	2.7	V
		Industrial	T_A = -40°C to + 85°C	2.3	2.7	V
V_{IL}	Input Low Voltage			-0.3	0.7	V
V_{IH}	Input High Voltage			1.7	3.6	V

Table 2-0005/2192VL

Capacitance (T_A=25°C, f=1.0 MHz)

SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
C_1	Dedicated Input Capacitance	8	pf	V_{CC} = 2.5V, V_{IN} = 0.0V
C_2	I/O Capacitance	6	pf	V_{CC} = 2.5V, $V_{I/O}$ = 0.0V
C_3	Clock and Global Output Enable Capacitance	10	pf	V_{CC} = 2.5V, V_Y = 0.0V

Table 2-0006/2192VL

Erase Reprogram Specifications

PARAMETER	MINIMUM	MAXIMUM	UNITS
Erase/Reprogram Cycles	10,000	—	Cycles

Table 2-0008/2192VL

Switching Test Conditions

Input Pulse Levels	GND to V_{CC}
Input Rise and Fall Time	≤ 1.5ns 10% to 90%
Input Timing Reference Levels	$V_{CC}/2$
Output Timing Reference Levels	$V_{CC}/2$
Output Load	See Figure 2

3-state levels are measured 0.15V from steady-state active level.

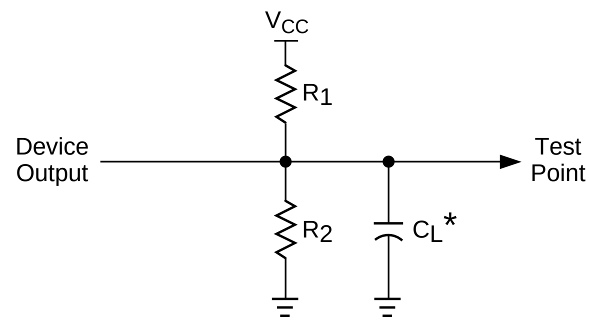
Table 2 - 0003/2192VL

Output Load Conditions (see Figure 2)

TEST CONDITION		R1	R2	CL
A		250Ω	218Ω	35pF
B	Active High	∞	218Ω	35pF
	Active Low	250Ω	∞	35pF
C	Active High to Z at V_{OH}-0.15V	∞	218Ω	5pF
	Active Low to Z at V_{OL}+0.15V	250Ω	∞	5pF

Table 2-0004/2192VL

Figure 2. Test Load



*C_L includes Test Fixture and Probe Capacitance.

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DC Electrical Characteristics

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[3]	MAX.	UNITS
V_{OL}	Output Low Voltage	I_{OL} = 100µA	—	—	0.2	V
		I_{OL} = 8mA	—	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -100µA	V_{CC} - 0.2	—	—	V
		I_{OH} = -1mA	2.0	—	—	V
		I_{OH} = -4mA	1.8	—	—	V
I_{IL}[5]	Input or I/O Low Leakage Current	0V ≤ V_{IN} ≤ V_{IL} (Max.)	—	—	-10	µA
I_{IH}	Input or I/O High Leakage Current	V_{IH} (min) ≤ V_{IN} ≤ 3.6V	—	—	10	µA
$I_{IL\text{-}isp}$	$\overline{\text{BSCAN}}$ Input Pull-Up Current	0V ≤ V_{IN} ≤ V_{IL}	—	—	-150	µA
$I_{IL\text{-}PU}$	I/O Active Pull-Up Current	0V ≤ V_{IN} ≤ V_{IL}	—	—	-150	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 2.5V, V_{OUT} = 0.5V	—	—	-100	mA
I_{CC}[2, 4]	Operating Power Supply Current	V_{IL} = 0.0V, V_{IH} = 2.5V f_{CLK} = 1 MHz	—	175	—	mA

Table 2-0007/2192VL

1. One output at a time for a maximum duration of one second. V_{OUT} = 0.5V was selected to avoid test problems by tester ground degradation. Characterized but not 100% tested.
2. Measured using 12 16-bit counters.
3. Typical values are at V_{CC} = 2.5V and T_A = 25°C.
4. Maximum I_{CC} varies widely with specific device configuration and operating frequency. Refer to Power Consumption section of this data sheet and Thermal Management section of the Lattice Semiconductor Data Book or CD-ROM to estimate maximum I_{CC}.
5. With no pull-up resistors.

External Timing Parameters

Over Recommended Operating Conditions

PARAMETER	TEST COND.[3]	#	DESCRIPTION[1]	-150		-135		-100		UNITS
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{pd1}	A	1	Data Propagation Delay, 4PT Bypass, ORP Bypass	—	6.0	—	7.5	—	10.0	ns
t_{pd2}	A	2	Data Propagation Delay	—	8.5	—	10.0	—	13.0	ns
f_{max}	A	3	Clock Frequency with Internal Feedback[2]	150	—	135	—	100	—	MHz
f_{max} (Ext.)	—	4	Clock Frequency with External Feedback $\left(\frac{1}{tsu2 + tco1}\right)$	111	—	95	—	77	—	MHz
f_{max} (Tog.)	—	5	Clock Frequency, Max. Toggle	166	—	143	—	100	—	MHz
t_{su1}	—	6	GLB Reg. Setup Time before Clock, 4 PT Bypass	4.0	—	5.0	—	6.5	—	ns
t_{co1}	A	7	GLB Reg. Clock to Output Delay, ORP Bypass	—	4.0	—	4.5	—	5.0	ns
t_{h1}	—	8	GLB Reg. Hold Time after Clock, 4 PT Bypass	0.0	—	0.0	—	0.0	—	ns
t_{su2}	—	9	GLB Reg. Setup Time before Clock	5.0	—	6.0	—	8.0	—	ns
t_{co2}	A	10	GLB Reg. Clock to Output Delay	—	5.0	—	5.5	—	6.0	ns
t_{h2}	—	11	GLB Reg. Hold Time after Clock	0.0	—	0.0	—	0.0	—	ns
t_{r1}	A	12	Ext. Reset Pin to Output Delay, ORP Bypass	—	6.0	—	8.0	—	13.5	ns
t_{rw1}	—	13	Ext. Reset Pulse Duration	5.0	—	5.5	—	6.5	—	ns
t_{ptoeen}	B	14	Input to Output Enable	—	10.0	—	12.0	—	15.0	ns
$t_{ptoedis}$	C	15	Input to Output Disable	—	10.0	—	12.0	—	15.0	ns
t_{goeen}	B	16	Global OE Output Enable	—	6.0	—	7.0	—	9.0	ns
t_{goedis}	C	17	Global OE Output Disable	—	6.0	—	7.0	—	9.0	ns
t_{wh}	—	18	External Synchronous Clock Pulse Duration, High	3.0	—	3.5	—	5.0	—	ns
t_{wl}	—	19	External Synchronous Clock Pulse Duration, Low	3.0	—	3.5	—	5.0	—	ns

Table 2-0030C/2192VL

1. Unless noted otherwise, all parameters use a GRP load of four, 20 PTXOR path, ORP and Y0 clock.
2. Standard 16-bit counter using GRP feedback.
3. Reference Switching Test Conditions section.

Internal Timing Parameters[1]

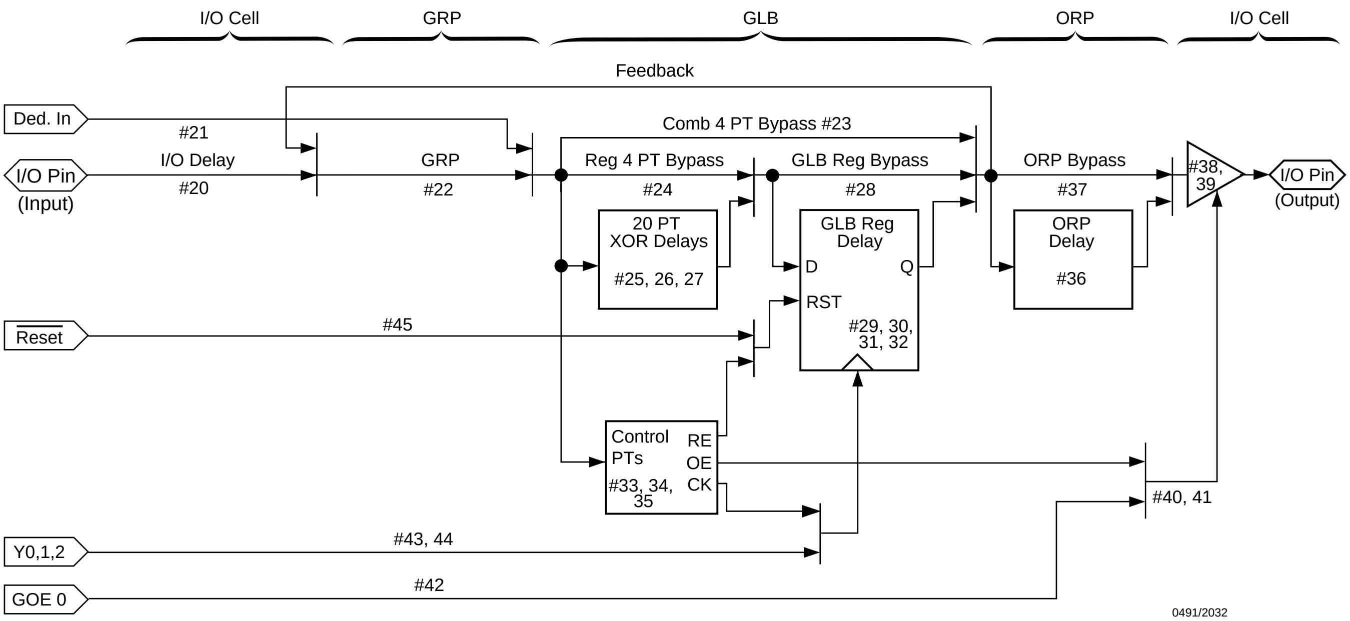
Over Recommended Operating Conditions

PARAMETER	#[2]	DESCRIPTION	-150 MIN.	-150 MAX.	-135 MIN.	-135 MAX.	-100 MIN.	-100 MAX.	UNITS
Inputs									
t_{io}	20	Input Buffer Delay	—	0.4	—	1.0	—	0.9	ns
t_{din}	21	Dedicated Input Delay	—	1.5	—	2.2	—	2.7	ns
GRP									
t_{grp}	22	GRP Delay	—	1.1	—	1.2	—	1.8	ns
GLB									
t_{4ptbpc}	23	4 Product Term Bypass Path Delay (Combinatorial)	—	2.5	—	3.2	—	5.2	ns
t_{4ptbpr}	24	4 Product Term Bypass Path Delay (Registered)	—	3.0	—	3.2	—	4.7	ns
t_{1ptxor}	25	1 Product Term/XOR Path Delay	—	4.0	—	4.2	—	6.2	ns
$t_{20ptxor}$	26	20 Product Term/XOR Path Delay	—	4.0	—	4.2	—	6.2	ns
t_{xoradj}	27	XOR Adjacent Path Delay[3]	—	4.0	—	4.2	—	6.2	ns
t_{gbp}	28	GLB Register Bypass Delay	—	0.0	—	0.5	—	1.0	ns
t_{gsu}	29	GLB Register Setup Time before Clock	1.2	—	1.7	—	1.7	—	ns
t_{gh}	30	GLB Register Hold Time after Clock	2.8	—	3.3	—	4.8	—	ns
t_{gco}	31	GLB Register Clock to Output Delay	—	0.3	—	0.3	—	0.3	ns
t_{gro}	32	GLB Register Reset to Output Delay	—	0.6	—	1.1	—	4.3	ns
t_{ptre}	33	GLB Product Term Reset to Register Delay	—	4.9	—	6.6	—	8.9	ns
t_{ptoe}	34	GLB Product Term Output Enable to I/O Cell Delay	—	5.0	—	5.8	—	7.4	ns
t_{ptck}	35	GLB Product Term Clock Delay	1.2	4.2	2.1	4.5	2.8	4.8	ns
ORP									
t_{orp}	36	ORP Delay	—	1.4	—	1.5	—	1.5	ns
t_{orpbp}	37	ORP Bypass Delay	—	0.4	—	0.5	—	0.5	ns
Outputs									
t_{ob}	38	Output Buffer Delay	—	1.6	—	1.6	—	1.6	ns
t_{sl}	39	Output Slew Limited Delay Adder	—	2.0	—	2.0	—	2.0	ns
t_{oen}	40	I/O Cell OE to Output Enabled	—	3.5	—	4.0	—	4.9	ns
t_{odis}	41	I/O Cell OE to Output Disabled	—	3.5	—	4.0	—	4.9	ns
t_{goe}	42	Global Output Enable	—	2.5	—	3.0	—	4.1	ns
Clocks									
t_{gy0}	43	Clock Delay, Y0 to Global GLB Clock Line (Ref. clock)	1.7	1.7	2.1	2.1	2.6	2.6	ns
$t_{gy1/2}$	44	Clock Delay, Y1 or Y2 to Global GLB Clock Line	1.9	1.9	2.3	2.3	2.8	2.8	ns
Global Reset									
t_{gr}	45	Global Reset to GLB	—	3.4	—	4.8	—	7.1	ns

Table 2-0036/2192VL

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. The XOR adjacent path can only be used by hard macros.

ispLSI 2192VL Timing Model



Derivations of **t**su, **t**h and **t**co from the Product Term Clock

tsu	=	Logic + Reg su - Clock (min)
	=	(**t**io + **t**grp + **t**20ptxor) + (**t**gsu) - (**t**io + **t**grp + **t**ptck(min))
	=	(#20 + #22 + #26) + (#29) - (#20 + #22 + #35)
4.0ns	=	(0.4 + 1.1 + 4.0) + (1.2) - (0.4 + 1.1 + 1.2)
th	=	Clock (max) + Reg h - Logic
	=	(**t**io + **t**grp + **t**ptck(max)) + (**t**gh) - (**t**io + **t**grp + **t**20ptxor)
	=	(#20 + #22 + #35) + (#30) - (#20 + #22 + #26)
3.0ns	=	(0.4 + 1.1 + 4.2) + (2.8) - (0.4 + 1.1 + 4.0)
tco	=	Clock (max) + Reg co + Output
	=	(**t**io + **t**grp + **t**ptck(max)) + (**t**gco) + (**t**orp + **t**ob)
	=	(#20 + #22 + #35) + (#31) + (#36 + #38)
9.0ns	=	(0.4 + 1.1 + 4.2) + (0.3) + (1.4 + 1.6)

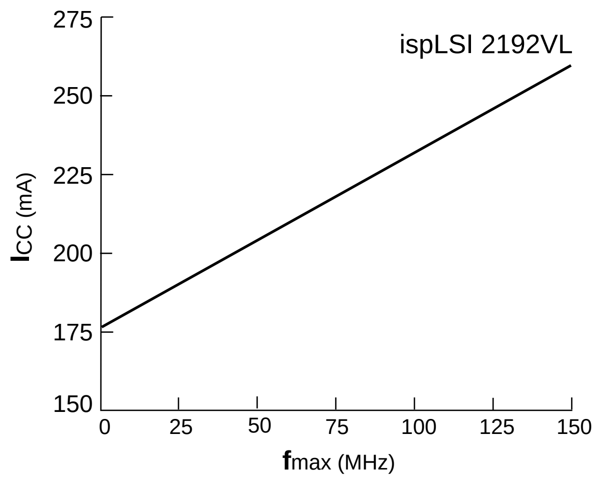
Note: Calculations are based upon timing specifications for the ispLSI 2192VL-150L.

Table 2-0042/2192VL

Power Consumption

Power consumption in the ispLSI 2192VL device depends on two primary factors: the speed at which the device is operating and the number of Product Terms used. Figure 3 shows the relationship between power and operating speed.

Figure 3. Typical Device Power Consumption vs fmax



Notes: Configuration of 12 16-bit counters
Typical current at 2.5V, 25° C

I_{CC} can be estimated for the ispLSI 2192VL using the following equation:

I_{CC} = 12 + (# of PTs * 0.44) + (# of nets * max freq * 0.0029)

Where:
- # of PTs = Number of Product Terms used in design
- # of nets = Number of Signals used in device
- Max freq = Highest Clock Frequency to the device (in MHz)

The I_{CC} estimate is based on typical conditions (V_{CC} = 2.5V, room temperature) and an assumption of two GLB loads on average exists. These values are for estimates only. Since the value of I_{CC} is sensitive to operating conditions and the program in the device, the actual I_{CC} should be verified.

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Signal Descriptions

Signal Name	Description
$\overline{\text{RESET}}$	Active Low (0) Reset pin resets all the registers in the device.
GOE 0, GOE1	Global Output Enable input pins.
Y0, Y1, Y2	Dedicated Clock Input – These clock inputs are connected to one of the clock inputs of all the GLBs in the device.
$\overline{\text{BSCAN}}$	Input – Dedicated in-system programming Boundary Scan enable input pin. This pin is brought low to enable the programming mode. The TMS, TDI, TDO and TCK controls become active.
TDI/IN 0	Input – This pin performs two functions. When $\overline{\text{BSCAN}}$ is logic low, it functions as a serial data input pin to load programming data into the device. When $\overline{\text{BSCAN}}$ is high, it functions as a dedicated input pin.
TCK/IN 7	Input – This pin performs two functions. When $\overline{\text{BSCAN}}$ is logic low, it functions as a clock pin for the Boundary Scan state machine. When $\overline{\text{BSCAN}}$ is high, it functions as a dedicated input pin.
TMS/IN 1	Input – This pin performs two functions. When $\overline{\text{BSCAN}}$ is logic low, it functions as a mode control pin for the Boundary Scan state machine. When $\overline{\text{BSCAN}}$ is high, it functions as a dedicated input pin.
TDO/IN 6	Output/Input – This pin performs two functions. When $\overline{\text{BSCAN}}$ is logic low, it functions as an output pin to read serial shift register data. When $\overline{\text{BSCAN}}$ is high, it functions as a dedicated input pin.
IN 2-5, IN 8-11	Dedicated Input Pins to the device.
GND	Ground (GND)
VCC	Vcc
NC[1]	No Connect
I/O	Input/Output Pins – These are the general purpose I/O pins used by the logic array.

1. NC pins are not to be connected to any active signals, VCC or GND.

Signal Locations

Signal Name	128-Pin TQFP	144-Ball fpBGA
$\overline{\text{RESET}}$	15	G4
GOE 0, GOE 1	80, 17	F12, G2
Y0, Y1, Y2	14, 83, 78	F3, F10, G11
$\overline{\text{BSCAN}}$	19	F1
TDI/IN 0	20	G3
TMS/IN 1	112	J6
TDO/IN 6	48	C7
TCK/IN 7	77	G12
IN 2-5, IN 8-11	—, 49, 82, —, 84, 113, 13, —	M7, J7, F9, G10, E12, B6, F2, E1
GND	18, 34, 50, 63, 79, 98, 111, 127	A1, A12, D4, D9, E5, E8, F6, F7, G6, G7, H5, H8, J4, J9, M1, M12
VCC	2, 16, 31, 47, 66, 81, 95, 114	B1, B12, E6, E7, F5, F8, G5, G8, H6, H7, L1, L12
NC[1]	—	K2

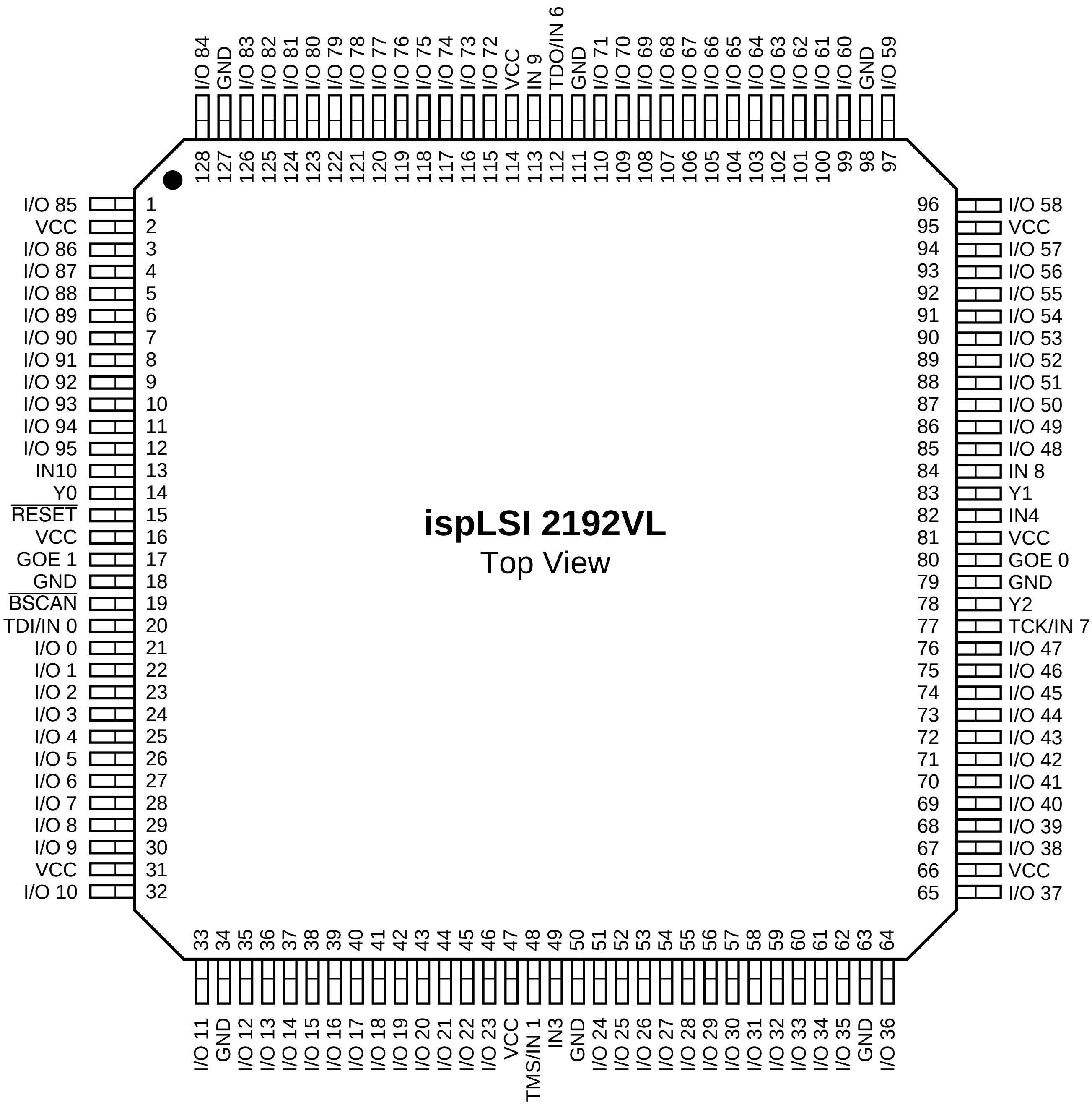
1. NC pins are not to be connected to any active signals, VCC or GND.

I/O Locations

Signal	128 TQFP	144 fpBGA	Signal	128 TQFP	144 fpBGA
I/O 0	21	H4	I/O 48	85	F11
I/O 1	22	G1	I/O 49	86	D12
I/O 2	23	H2	I/O 50	87	E9
I/O 3	24	H1	I/O 51	88	E10
I/O 4	25	H3	I/O 52	89	E11
I/O 5	26	J1	I/O 53	90	C12
I/O 6	27	J3	I/O 54	91	D10
I/O 7	28	K1	I/O 55	92	D11
I/O 8	29	J2	I/O 56	93	B11
I/O 9	30	M2	I/O 57	94	C11
I/O 10	32	L2	I/O 58	96	C10
I/O 11	33	L3	I/O 59	97	A11
I/O 12	35	K3	I/O 60	99	B10
I/O 13	36	M3	I/O 61	100	A10
I/O 14	37	L4	I/O 62	101	C9
I/O 15	38	K4	I/O 63	102	B9
I/O 16	39	M4	I/O 64	103	A9
I/O 17	40	J5	I/O 65	104	D8
I/O 18	41	M5	I/O 66	105	B8
I/O 19	42	K5	I/O 67	106	C8
I/O 20	43	L5	I/O 68	107	A8
I/O 21	44	M6	I/O 69	108	B7
I/O 22	45	L6	I/O 70	109	A7
I/O 23	46	K6	I/O 71	110	D7
I/O 24	51	L7	I/O 72	115	C6
I/O 25	52	K7	I/O 73	116	A6
I/O 26	53	J8	I/O 74	117	D6
I/O 27	54	M8	I/O 75	118	B5
I/O 28	55	L8	I/O 76	119	C5
I/O 29	56	K8	I/O 77	120	A5
I/O 30	57	M9	I/O 78	121	D5
I/O 31	58	L9	I/O 79	122	C4
I/O 32	59	K9	I/O 80	123	B4
I/O 33	60	M10	I/O 81	124	A4
I/O 34	61	L10	I/O 82	125	C3
I/O 35	62	M11	I/O 83	126	B3
I/O 36	64	K10	I/O 84	128	A3
I/O 37	65	K11	I/O 85	1	C2
I/O 38	67	L11	I/O 86	3	B2
I/O 39	68	K12	I/O 87	4	D2
I/O 40	69	J11	I/O 88	5	A2
I/O 41	70	J12	I/O 89	6	D3
I/O 42	71	J10	I/O 90	7	E2
I/O 43	72	H9	I/O 91	8	C1
I/O 44	73	H11	I/O 92	9	E3
I/O 45	74	H12	I/O 93	10	E4
I/O 46	75	H10	I/O 94	11	D1
I/O 47	76	G9	I/O 95	12	F4

Pin Configuration

ispLSI 2192VL 128-Pin TQFP Pinout Diagram



0124-2192VL

Pin Configuration

ispLSI 2192VL 144-Ball fpBGA Signal Diagram

	12	11	10	9	8	7	6	5	4	3	2	1	
A	GND	I/O 59	I/O 61	I/O 64	I/O 68	I/O 70	I/O 73	I/O 77	I/O 81	I/O 84	I/O 88	GND	A
B	VCC	I/O 56	I/O 60	I/O 63	I/O 66	I/O 69	IN 9	I/O 75	I/O 80	I/O 83	I/O 86	VCC	B
C	I/O 53	I/O 57	I/O 58	I/O 62	I/O 67	TDO/ IN 6	I/O 72	I/O 76	I/O 79	I/O 82	I/O 85	I/O 91	C
D	I/O 49	I/O 55	I/O 54	GND	I/O 65	I/O 71	I/O 74	I/O 78	GND	I/O 89	I/O 87	I/O 94	D
E	IN 8	I/O 52	I/O 51	I/O 50	GND	VCC	VCC	GND	I/O 93	I/O 92	I/O 90	IN 11	E
F	GOE 0	I/O 48	Y1	IN 4	VCC	GND	GND	VCC	I/O 95	Y0	IN 10	$\overline{\text{BSCAN}}$	F
G	TCK/ IN 7	Y2	IN 5	I/O 47	VCC	GND	GND	VCC	$\overline{\text{RESET}}$	TDI/ IN 0	GOE 1	I/O 1	G
H	I/O 45	I/O 44	I/O 46	I/O 43	GND	VCC	VCC	GND	I/O 0	I/O 4	I/O 2	I/O 3	H
J	I/O 41	I/O 40	I/O 42	GND	I/O 26	IN 3	TMS/ IN 1	I/O 17	GND	I/O 6	I/O 8	I/O 5	J
K	I/O 39	I/O 37	I/O 36	I/O 32	I/O 29	I/O 25	I/O 23	I/O 19	I/O 15	I/O 12	NC[1]	I/O 7	K
L	VCC	I/O 38	I/O 34	I/O 31	I/O 28	I/O 24	I/O 22	I/O 20	I/O 14	I/O 11	I/O 10	VCC	L
M	GND	I/O 35	I/O 33	I/O 30	I/O 27	IN 2	I/O 21	I/O 18	I/O 16	I/O 13	I/O 9	GND	M
	12	11	10	9	8	7	6	5	4	3	2	1	

144-BGA/2192VL

ispLSI 2192VL

Bottom View

[1]NCs are not to be connected to any active signals, VCC or GND.

Note: Ball A1 indicator dot on top side of package.

Part Number Description

ispLSI 2192VL - XXX X XXXX X

Device Family — ispLSI

Device Number — 2192VL

Speed — XXX
150 = 150 MHz fmax
135 = 135 MHz fmax
100 = 100 MHz fmax

Power — X
L = Low

Package — XXXX
T128 = 128-Pin TQFP
B144 = 144-Ball fpBGA

Grade — X
Blank = Commercial

0212A/2192VL

ispLSI 2192VL Ordering Information

COMMERCIAL

FAMILY	fmax (MHz)	tpd (ns)	ORDERING NUMBER	PACKAGE
ispLSI	150	6.0	ispLSI 2192VL-150LT128	128-Pin TQFP
	150	6.0	ispLSI 2192VL-150LB144	144-Ball fpBGA
	135	7.5	ispLSI 2192VL-135LT128	128-Pin TQFP
	135	7.5	ispLSI 2192VL-135LB144	144-Ball fpBGA
	100	10	ispLSI 2192VL-100LT128	128-Pin TQFP
	100	10	ispLSI 2192VL-100LB144	144-Ball fpBGA

Table 2-0041C/2192VL