MC1600 Series (-30°C to +85°C)

The requirement for digital systems with ever higher performance has increased the need for high-speed integrated circuits. The industry has recognized that the only economical way to obtain high operating system speed is through the use of emitter-coupled logic. Motorola offers a state-of-the-art, emitter-coupled logic family with sub-nanosecond propagation delays – MECL III.

MECL III circuit design is similar to that used in the popular MECL 10,000 family. In the MECL III line, as well as MECL 10,000, advanced processing techniques are employed and the capability for driving low-impedance terminated lines is provided. MECL III is recommended for new designs.

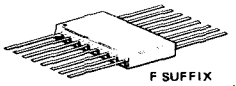
2

GENERAL FEATURES

- Gate Switching Speeds of 1.0 ns typical
- Capability of Driving Terminated Lines with Impedance as Low as 50 Ohms
- Flip-Flop Toggle Rate Greater Than 500 MHz
- Operation with Unused Inputs Left Open
- Multilayer Metalization for economy
- New Packages with Improved Electrical and Thermal Characteristics
- Compatibility with MECL 10,000 Series
- Counting Speeds to above 1 GHz

P SUFFIX
PLASTIC PACKAGE
CASE 646

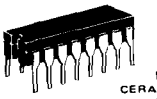
L SUFFIX
CERAMIC PACKAGE
CASE 632



F SUFFIX
CERAMIC PACKAGE
CASE 650

P SUFFIX
PLASTIC PACKAGE
CASE 648

F SUFFIX
CERAMIC PACKAGE
CASE 607



L SUFFIX
CERAMIC PACKAGE
CASE 620

FUNCTIONS AND CHARACTERISTICS (V_{CC} = 0, V_{EE} = -5.2 V, T_A = 25°C unless otherwise noted.)

Function	Type ① -30° to +85°C	Loading Factor # Each Output	Propagation Delay 50-ohm Load ns typ	Power Dissipation (No Load) mW typ/pkg	Case
Voltage Controlled Oscillator	MC1648	–	*225 MHz typ	150	607,632,646
Dual A/D Comparator	MC1650	70	3.5	275	620,650
Dual A/D Comparator	MC1651	70	3.0	275	620,650
Binary Counter	MC1654	70	*325 MHz typ	750 ⌐⌐⌐	620
Voltage-Controlled Multivibrator	MC1658	70	*150 MHz typ	125	620,648,650
Dual 4-Input OR/NOR Gate	MC1660	70	1.1	120	620,650
Quad 2-Input NOR Gate	MC1662	70	1.1	240	620,650
Quad 2-Input OR Gate	MC1664	70	1.1	240	620,650
Dual Clocked R-S Flip-Flop	MC1666	70	1.8	220	620,650
Dual Clocked Latch	MC1668	70	1.8	220	620,650
Master-Slave Type D Flip-Flop	MC1670	70	*350 MHz typ	220	620,650
Triple 2-Input Exclusive OR Gate	MC1672	70	1.3	220	620,650
Triple 2-Input Exclusive NOR Gate	MC1674	70	1.3	220	620,650
Bi-Quinary Counter	MC1678	70	*350 MHz typ	750 ⌐⌐⌐	620
Dual 4-5-Input OR/NOR Gate	MC1688	70	0.8	125	650
UHF Prescaler Type D Flip-Flop	MC1690	70	*500 MHz min	200	620,650
Quad Line Receiver	MC1692	70	1.1	220	620,650
4-Bit Shift Register	MC1694	70	*325 MHz typ	750 ⌐⌐⌐	620
1 GHz Divide-By-Ten Counter	MC1696	–	*1 GHz min	650	650

① L suffix denotes Dual In-Line Ceramic Package, F suffix denotes Ceramic Flat Package, P suffix denotes Dual In-Line Plastic Package. (i.e., MC1600L = Ceramic Dual In-Line Package, MC1600F = Ceramic Flat Package, MC1600P = Plastic Dual In-Line Package).

⌐⌐⌐ Requires Heat Sink – IERC-LIC-214A2WCB or equivalent.

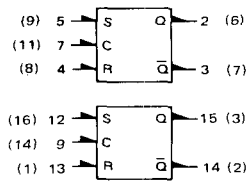
*Toggle Frequency

#DC Loading Factors are based on:

1. Full load output current, I_L = -25 mAdc max
2. Maximum input current, I_{in} = 350 μAdc

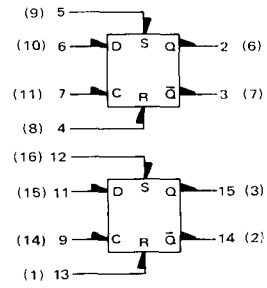
FLIP-FLOPS

MC1666
Dual Clocked R-S Flip-Flop



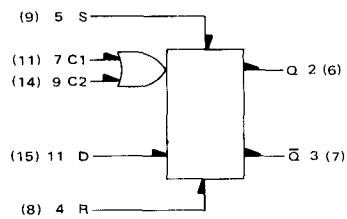
t_{pd} = 1.6 ns typ (510-ohm load)
= 1.8 ns typ (50-ohm load)
P_D = 220 mW typ/pkg (no-load)

MC1668
Dual Clocked Latch



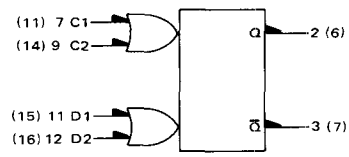
t_{pd} = 1.6 ns typ (510-ohm load)
= 1.8 ns typ (50-ohm load)
P_D = 220 mW typ/pkg (no-load)

MC1670
Master-Slave Type D Flip-Flop



f_{Tog} = 350 MHz typ
P_D = 220 mW typ/pkg (no load)

MC1690
UHF *Prescaler* Type D Flip-Flop



f_{Tog} = 500 MHz min
P_D = 200 mW typ/pkg (No Load)

MASTER-SLAVE
TYPE D FLIP-FLOP

MC1670

The MC1670 is a Type D Master-Slave Flip-Flop designed for use in high speed digital applications. Master slave construction renders the MC1670 relatively insensitive to the shape of the clock waveform, since only the voltage levels at the clock inputs control the transfer of information from data input (D) to output.

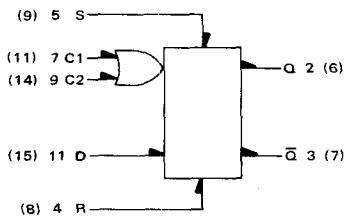
When both clock inputs (C1 and C2) are in the low state, the data input affects only the "Master" portion of the flip-flop. The data present in the "Master" is transferred to the "Slave" when clock inputs (C1 "OR" C2) are taken from a low to a high level. In other words, the output state of the flip-flop changes on the positive transition of the clock pulse.

While either C1 "OR" C2 is in the high state, the "Master" (and data input) is disabled.

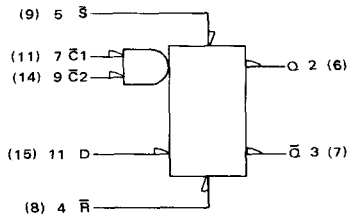
Asynchronous Set (S) and Reset (R) override Clock (C) and Data (D) inputs.

Input pulldown resistors eliminate the need to tie unused inputs to V_{EE}.

POSITIVE LOGIC



NEGATIVE LOGIC



Number at end of terminal denotes pin number for L package (Case 620).
Number in parenthesis denotes pin number for F package (Case 650).

V_{CC1} = Pin 1 (5)
V_{CC2} = Pin 16 (4)
V_{EE} = Pin 8 (12)

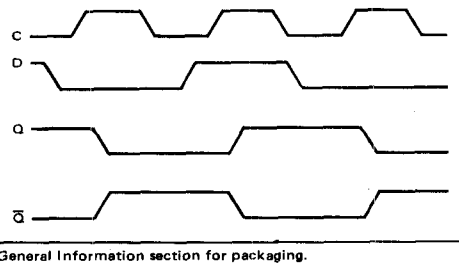
Power Dissipation = 220 mW typical (No Load)
f_{tog} = 350 MHz typ

TRUTH TABLE

R	S	D	C	Q_{n+1}
L	H	ϕ	ϕ	H
H	L	ϕ	ϕ	L
H	H	ϕ	ϕ	N.D.
L	L	L	L	Q_n
L	L	L	↗	L
L	L	L	H	Q_n
L	L	H	L	Q_n
L	L	H	↗	H
L	L	H	H	Q_n

ϕ = Don't Care
ND = Not Defined
C = C1 + C2

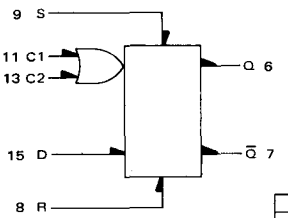
TIMING DIAGRAM

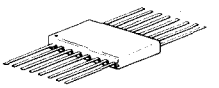


See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

This MECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. Air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or is mounted on a printed circuit board. Test procedures are shown for only one input and one output. The other inputs and outputs are tested in a similar manner. Outputs are tested with a 50-ohm resistor to -2.0 Vdc. See general information section for complete thermal data.

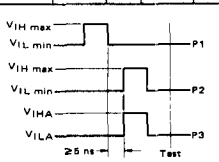




F SUFFIX
CERAMIC PACKAGE
CASE 650

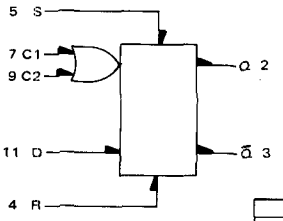
@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
-30°C	-0.875	-1.890	-1.180	-1.515	-5.2
+25°C	-0.810	-1.850	-1.095	-1.485	-5.2
+85°C	-0.700	-1.830	-1.025	-1.440	-5.2

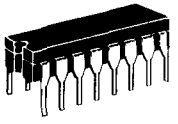
Characteristic	Symbol	Pin Under Test	MC1670F Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	P_1	P_2	P_3	(V_{CC}) Gnd
Power Supply Drain	I_E	12	–	–	–	48	–	–	mAdc	–	–	–	–	12	–	–	–	4,5
Input Current	$I_{in\ H}$	8	–	–	–	550	–	–	μAdc	8	–	–	–	12	–	–	–	4,5
		9	–	–	–	550	–	–		9	–	–	–		–	–	–	
		14	–	–	–	250	–	–		14	–	–	–		–	–	–	
		11	–	–	–	250	–	–		11	–	–	–		–	–	–	
		15	–	–	–	270	–	–		15	–	–	–		–	–	–	
	$I_{in\ L}$	8	–	–	0.5	–	–	–	μAdc	14	8	–	–	12	–	–	–	4,5
		9	–	–		–	–	–		14	9	–	–		–	–	–	
		14	–	–		–	–	–		11	14	–	–		–	–	–	
		11	–	–		–	–	–		14	11	–	–		–	–	–	
		15	–	–		–	–	–		14	15	–	–		–	–	–	
Logic "1" Output Voltage	V_{OH}	6	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	–	8,11,15	–	–	12	14	9	–	4,5
		7								15	9,14	–	–		11	8	–	
		6								15	9,11	–	–		8	14	–	
		7								–	8,14,15	–	–		9	11	–	
Logic "0" Output Voltage	V_{OL}	6	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	15	9,11	–	–	12	14	8	–	4,5
		7								–	8,14,15	–	–		11	9	–	
		6								–	8,11,15	–	–		9	14	–	
		7								15	9,14	–	–		8	11	–	
Logic "1" Threshold Voltage	V_{OHA}	6	-1.065	–	-0.980	–	-0.910	–	Vdc	–	8,11,15	–	–	12	14	–	9	4,5
		7		–		–		–		15	9,14	–	–		11	–	8	
		6		–		–		–		15	9,11	–	–		8	–	14	
		7		–		–		–		–	8,14,15	–	–		9	–	11	
		6		–		–		–		–	9,11	15	–		8	14	–	
		7		–		–		–		–	8,14	–	15		9	11	–	
Logic "0" Threshold Voltage	V_{OLA}	6	–	-1.630	–	-1.600	–	-1.555	Vdc	15	9,11	–	–	12	14	–	8	4,5
		7	–		–		–			–	8,14,15	–	–		11	–	9	
		6	–		–		–			–	8,11,15	–	–		9	–	14	
		7	–		–		–			15	9,14	–	–		8	–	11	
		6	–		–		–			–	8,11	–	15		9	14	–	
		7	–		–		–			–	9,14	15	–		8	11	–	
Switching Parameters			Min	Max	Min	Max	Min	Max						-3.2 Vdc				+2.0 Vdc
Clock to Output Delay	t_{11+6+}	14,6	1.0	2.7	1.1	2.5	1.1	2.9	ns	–	–	–	–	12	–	–	–	4,5
(See Figure 1)	t_{11-6-}	14,6								–	–	–	–		–	–	–	
	t_{11+7-}	14,7								–	–	–	–		–	–	–	
	t_{11-7+}	14,7								–	–	–	–		–	–	–	
Set to Output Delay	t_{9+6+}	9,6								–	–	–	–		–	–	–	
(See Figure 2)	t_{9+6-}	9,7								–	–	–	–		–	–	–	
Reset to Output Delay	t_{8+6-}	8,6								–	–	–	–		–	–	–	
(See Figure 2)	t_{8+7+}	8,7								–	–	–	–		–	–	–	
Output Rise Time	t_{6+7+}	6,7	0.9	2.7	1.0	2.5	1.0	2.9		–	–	–	–		–	–	–	
Fall Time (See Figure 2)	t_{6-7-}	6,7	0.5	2.1	0.6	1.9	0.6	2.3		–	–	–	–		–	–	–	
Set Up Time	t_s"1"	6	–	–	–	0.4	–	–		–	6	–	–		–	–	–	
(See Figure 3)	t_s"0"	6	–	–	–	0.5	–	–		–	6	–	–		–	–	–	
Hold Time	t_H"1"	6	–	–	–	0.3	–	–		–	6	–	–		–	–	–	
(See Figure 3)	t_H"0"	6	–	–	–	0.5	–	–		–	6	–	–		–	–	–	
Toggle Frequency (See Figure 4)	f_{Tog}	6	270	–	300	–	270	–	MHz	–	–	–	–	–	–	–	–	–



ELECTRICAL CHARACTERISTICS

This MECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The package should be housed in a suitable heat sink (IERC-14A2C8 or equivalent) or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or is mounted on a printed circuit board. *Test procedures are shown* for only one input and one output. The other inputs and outputs are tested in a similar manner. Outputs are tested with a 50-ohm resistor to −2.0 Vdc. See general information section for complete thermal data.





L SUFFIX
CERAMIC PACKAGE
CASE 620

@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
−30°C	−0.875	−1.890	−1.180	−1.515	−5.2
+25°C	−0.810	−1.850	−1.005	−1.485	−5.2
+85°C	−0.700	−1.830	−1.025	−1.440	−5.2

Characteristic	Symbol	Pin Under Test	MC1670L Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	P_1	P_2	P_3	(V_{CC}) Gnd
Power Supply Drain	I_E	8	–	–	–	48	–	–	mAdc	7,9	–	–	–	8	–	–	–	1,16
Input Current	$I_{in\ H}$	4	–	–	–	550	–	–	μAdc	4	–	–	–	8	–	–	–	1,16
		5	–	–	–	550	–	–		5	–	–	–		–	–	–	
		9	–	–	–	250	–	–		9	–	–	–		–	–	–	
		7	–	–	–	250	–	–		7	–	–	–		–	–	–	
		11	–	–	–	270	–	–		11	–	–	–		–	–	–	
	$I_{in\ L}$	4	–	–	0.5	–	–	–	μAdc	9	4	–	–	8	–	–	–	1,16
		5	–	–		–	–	–		9	5	–	–		–	–	–	
		9	–	–		–	–	–		7	9	–	–		–	–	–	
		7	–	–		–	–	–		9	7	–	–		–	–	–	
		11	–	–		–	–	–		9	11	–	–		–	–	–	
Logic "1" Output Voltage	V_{OH}	2	−1.045	−0.875	−0.960	−0.810	−0.890	−0.700	Vdc	–	4,7,11	–	–	8	9	5	–	1,16
		3								11	5,9	–	–		7	4	–	
		2								11	5,7	–	–		4	9	–	
		3								–	4,9,11	–	–		5	7	–	
Logic "0" Output Voltage	V_{OL}	2	−1.890	−1.650	−1.850	−1.620	−1.830	−1.575	Vdc	11	5,7	–	–	8	9	4	–	1,16
		3								–	4,9,11	–	–		7	5	–	
		2								–	4,7,11	–	–		5	9	–	
		3								11	5,9	–	–		4	7	–	
Logic "1" Threshold Voltage	V_{OHA}	2	−1.065	–	−0.980	–	−0.910	–	Vdc	–	4,7,11	–	–	8	9	–	5	1,16
		3		–		–		–		11	5,9	–	–		7	–	4	
		2		–		–		–		11	5,7	–	–		4	–	9	
		3		–		–		–		–	4,9,11	–	–		5	–	7	
		2		–		–		–		–	5,7	11	–		4	9	–	
		3		–		–		–		–	4,9	–	11		5	7	–	
Logic "0" Threshold Voltage	V_{OLA}	2	–	−1.630	–	−1.600	–	−1.555	Vdc	11	5,7	–	–	8	9	–	4	1,16
		3								–	4,9,11	–	–		7	–	5	
		2								–	4,7,11	–	–		5	–	9	
		3			–					11	5,9	–	–		4	–	7	
		2					–			–	4,7	11	–		5	9	–	
		3			–					–	5,9	11	–		4	7	–	
Switching Parameters			Min	Max	Min	Max	Min	Max						−3.2 Vdc				+2.0 Vdc
Clock to Output Delay (See Figure 1)	t_{7+2+}	9,2	1.0	2.7	1.1	2.5	1.1	2.9	ns	–	–	–	–	8	–	–	–	1,16
	t_{7-2-}	9,2								–	–	–	–		–	–	–	
	t_{7+3-}	9,3								–	–	–	–		–	–	–	
	t_{7-3+}	9,3								–	–	–	–		–	–	–	
Set to Output Delay (See Figure 2)	t_{5+2+}	5,2								–	–	–	–		–	–	–	
	t_{5+3-}	5,3								–	–	–	–		–	–	–	
Reset to Output Delay (See Figure 2)	t_{4+2-}	4,2								–	–	–	–		–	–	–	
	t_{4+3+}	4,3								–	–	–	–		–	–	–	
Output Rise Time	$t_{2+,3+}$	2,3	0.9	2.7	1.0	2.5	1.0	2.9		–	–	–	–		–	–	–	
Fall Time (See Figure 2)	$t_{2-,3-}$	2,3	0.5	2.1	0.6	1.9	0.6	2.3		–	–	–	–		–	–	–	
Set Up Time (See Figure 3)	t_{S}"1"	2	–	–	–	0.4	–	–		–	6	–	–		–	–	–	
	t_{S}"0"	2	–	–	–	0.5	–	–		–	6	–	–		–	–	–	
Hold Time (See Figure 3)	t_{H}"1"	2	–	–	–	0.3	–	–		–	6	–	–		–	–	–	
	t_{H}"0"	2	–	–	–	0.5	–	–		–	6	–	–		–	–	–	
Toggle Frequency (See Figure 4)	f_{Tog}	2	270		300	–	270	–	MHz	–	–	–	–	–	–	–	–	–

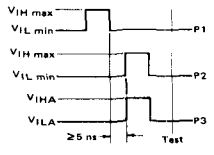


FIGURE 1 – PROPAGATION DELAY TEST CIRCUIT

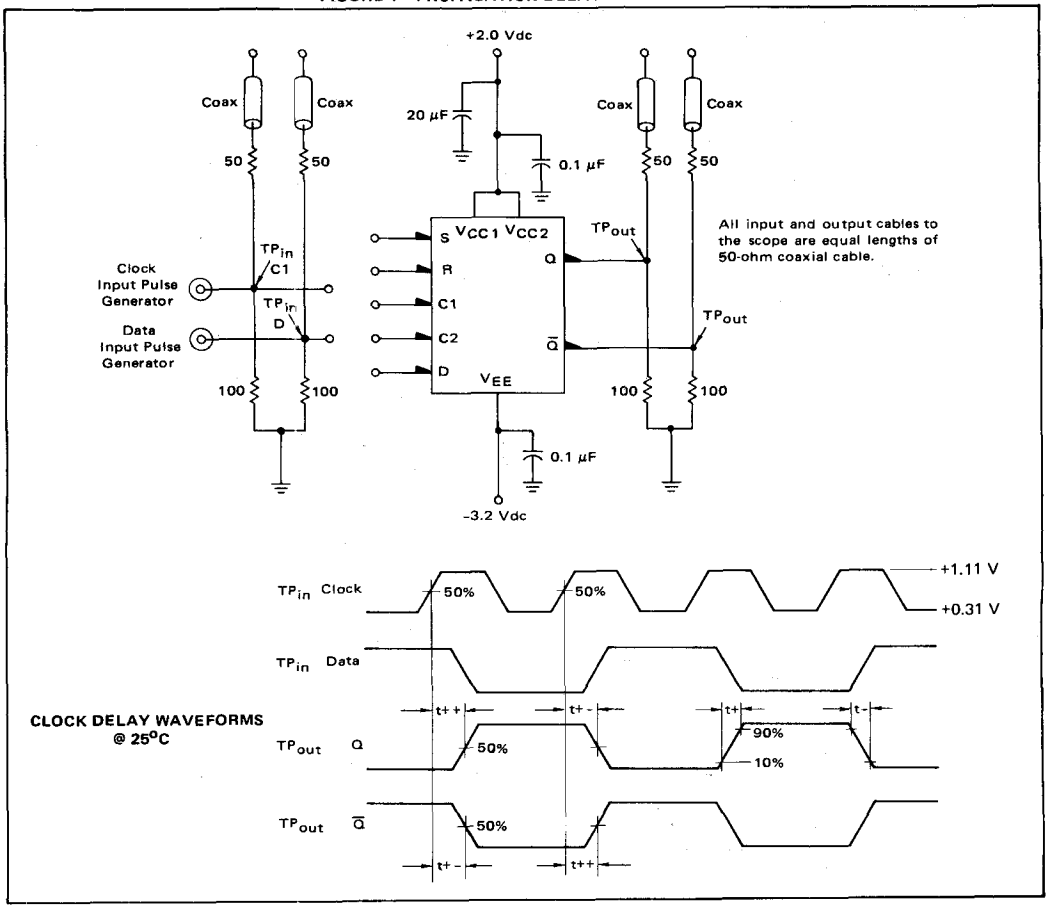


FIGURE 2 – SET-RESET DELAY WAVEFORMS @ 25°C

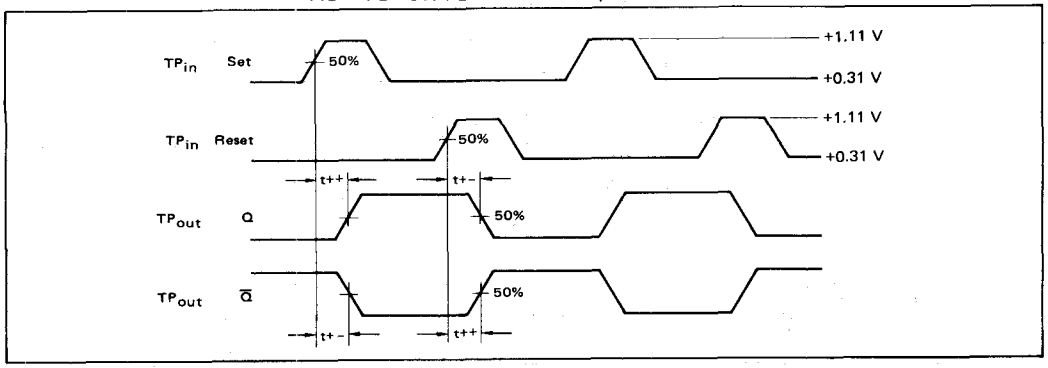
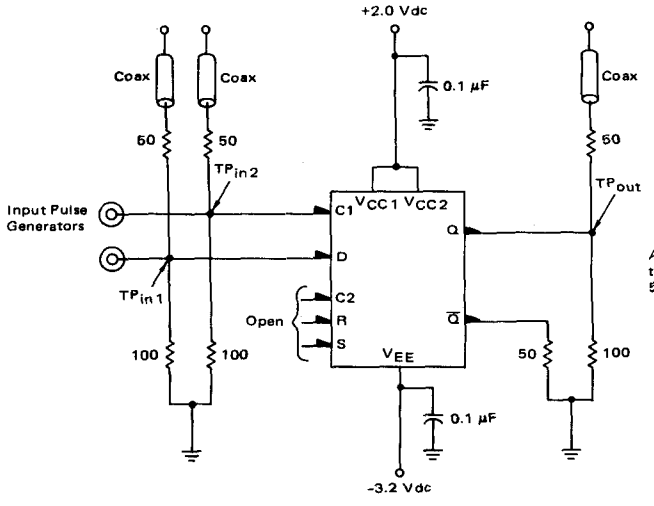
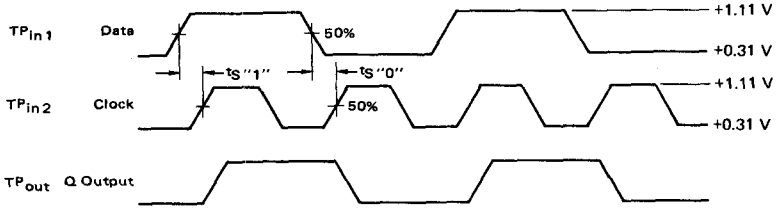


FIGURE 3 – SET UP AND HOLD TIME TEST CIRCUIT

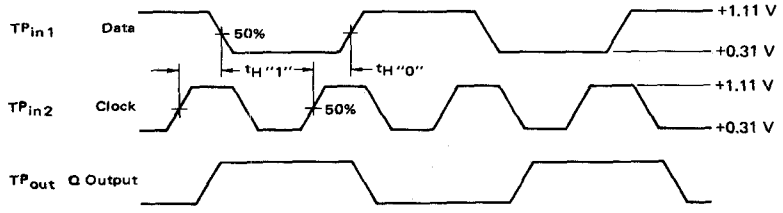


All input and output cables to the scope are equal lengths of 50-ohm coaxial cable.

SET UP TIME WAVEFORMS @ 25°C



HOLD TIME WAVEFORMS @ 25°C



Set up time is the minimum time before the positive transition of the clock pulse (C) that information must be present at the data (D) input.

Hold time is the minimum time after the positive transition of the clock pulse (C) that information must remain unchanged at the data (D) input.

FIGURE 4 – TOGGLE FREQUENCY TEST CIRCUIT

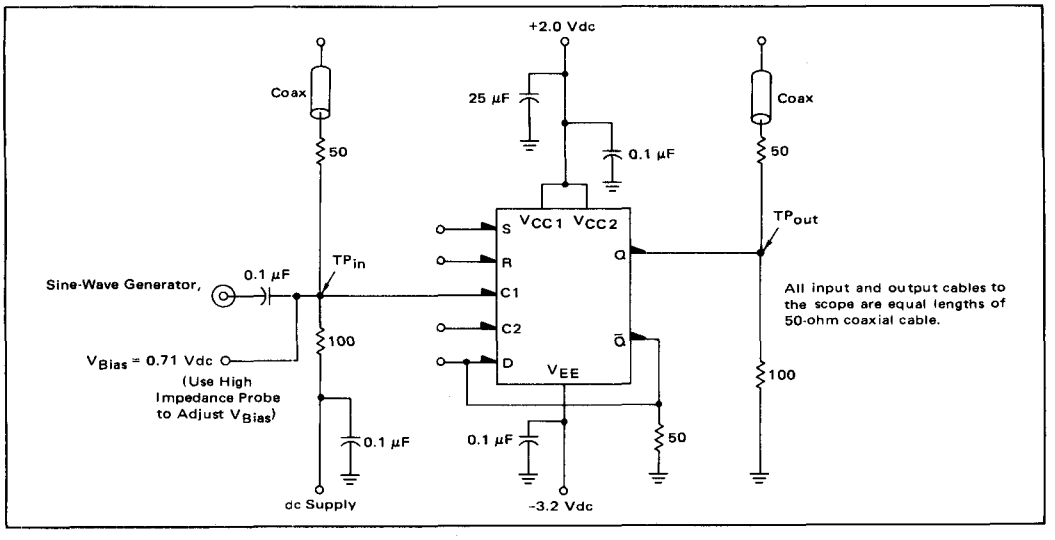


FIGURE 5 – TOGGLE FREQUENCY WAVEFORMS

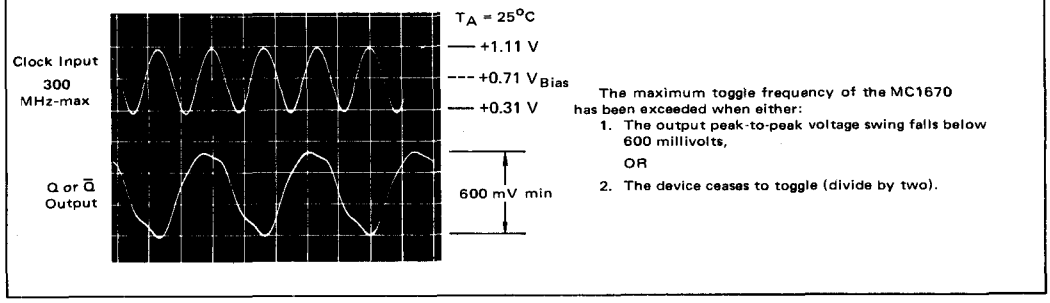


FIGURE 6 – MAXIMUM TOGGLE FREQUENCY (TYPICAL)

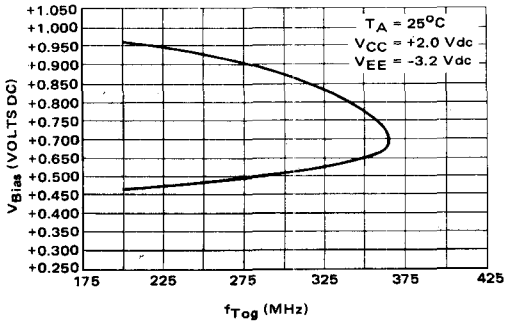
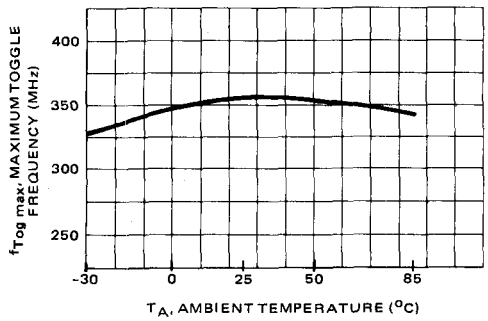


Figure 6 illustrates the variation in toggle frequency with the dc offset voltage (V_{Bias}) of the input clock signal. V_{Bias} is defined by the test circuit in Figure 4, and waveform Figure 5.

Figures 8 and 9 illustrate minimum clock pulse width recommended for reliable operation of the MC1670.

FIGURE 7 – TYPICAL MAXIMUM TOGGLE FREQUENCY versus TEMPERATURE



Temperature	-30°C	+25°C	+85°C
V_{Bias}	+0.660 Vdc	+0.710 Vdc	+0.765 Vdc

FIGURE 8 – MINIMUM "DOWN TIME" TO CLOCK
OUTPUT LOAD = 50 Ω

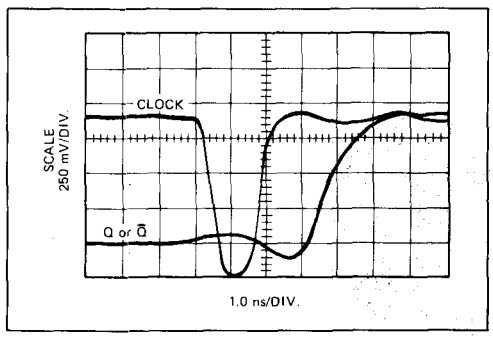
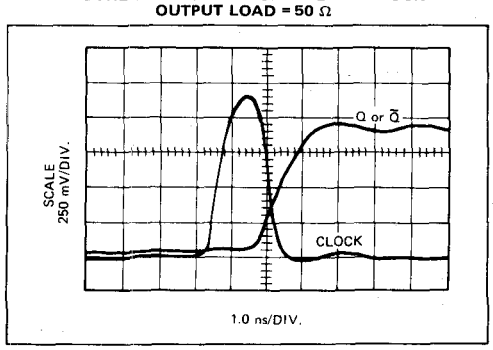


FIGURE 9 – MINIMUM "UP TIME" TO CLOCK
OUTPUT LOAD = 50 Ω



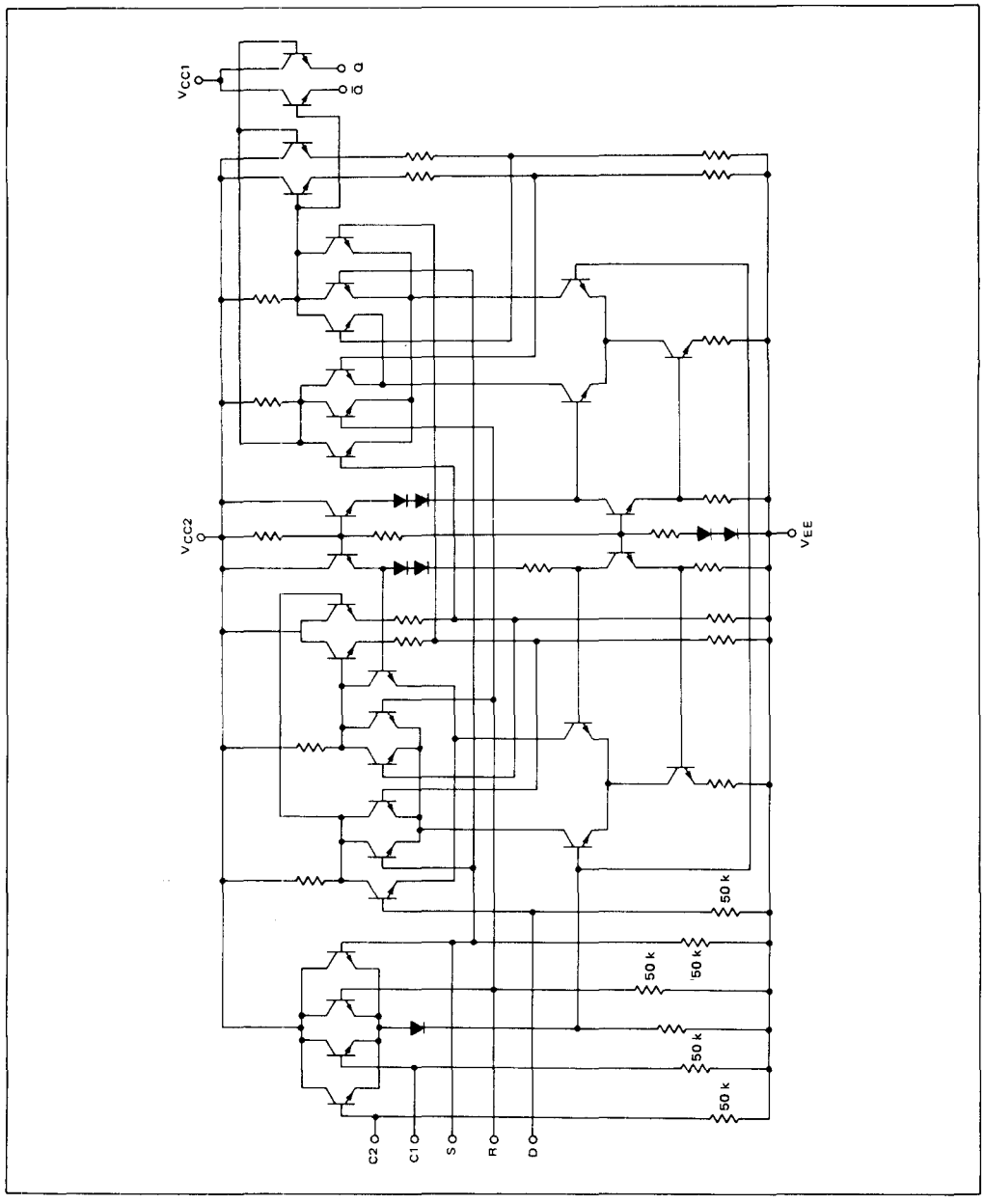


FIGURE 10 – MC1670 CIRCUIT SCHEMATIC

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