R8A20110BG (MARIE)

Network Signature Matching Co-Processor
(1 M-bit Full Ternary CAM)

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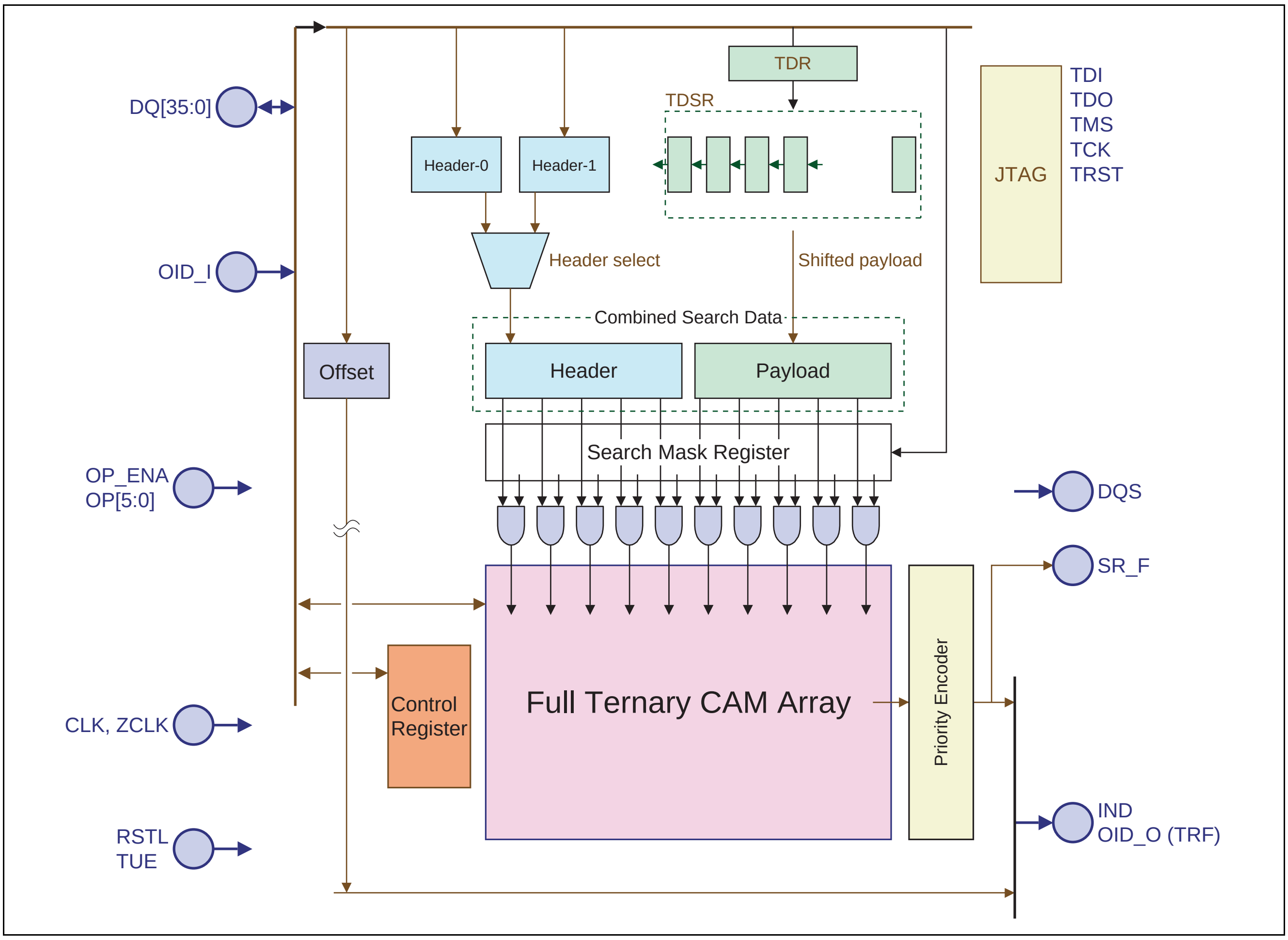
Description

"MARIE" is a new RENESAS Ternary CAM co-processor targeted for the network packet classification and signature matching application. MARIE's 1 M-bit special features, small package and reduced pin count interface makes it suitable for cost sensitive platforms. MARIE provides a 36-bit Data bus SSTL-2 interface and is able to achieve 100 Msps in Turbo Mode. During normal search mode MARIE performs 50 Msps at 144-bit lookup. A special shifted payload algorithm for the signature matching makes MARIE a perfect fit for IDS applications.

Features

- 1 M-bit full ternary CAM
- 100 Msps max. 144-bit LU/288-bit LU with Turbo Search
- 50 Msps max. 144-bit LU with Normal Search
- 25 Msps max. 288-bit LU with Normal Search
- Shifting payload for signature matching application.
- 36-bit DQ interface (reduced pin count interface)
- Priority encoder
- IEEE 1149.1 test port
- 2.5 V/1.5 V power supply
- SSTL-2 interface
- 1.7 × 1.7 mm, 1 mm pitch 256 PBGA

Block Diagram



Functional Description

1. Denser and Low power CAM
   MARIE is a new Network Signature Matching Co-Processor ideal for IDS applications. The specially designed custom SRAM cell takes advantage of space and power increasing MARIE's overall performance.

2. Half Sized Global Mask Search Register
   In a conventional TCAM the Global Mask Search Register consists of the same number of register bits as number of CAM bits. During a search command the Global Mask Search Register controls the bits that participate in the search. In MARIE's TCAM the Global Mask Search Register controls two CAM bits at the same time, making MARIE's GMSR one half the size of a conventional CAM. As a result range mask can be achieved, but bit mask is not supported. GMSR is only used during search.

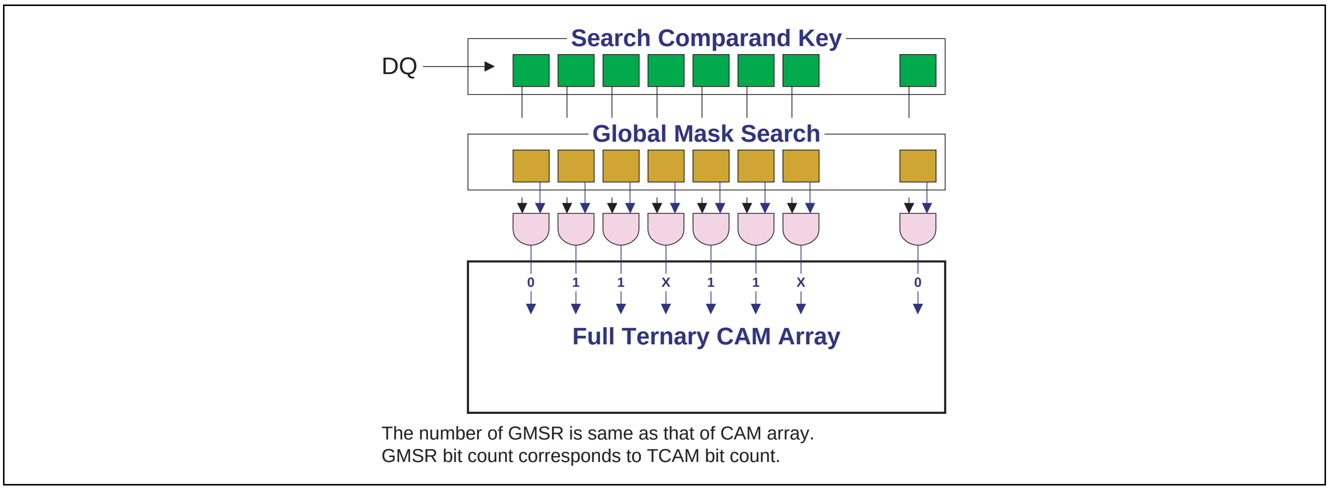


Figure 1 Global Mask Search (conventional)

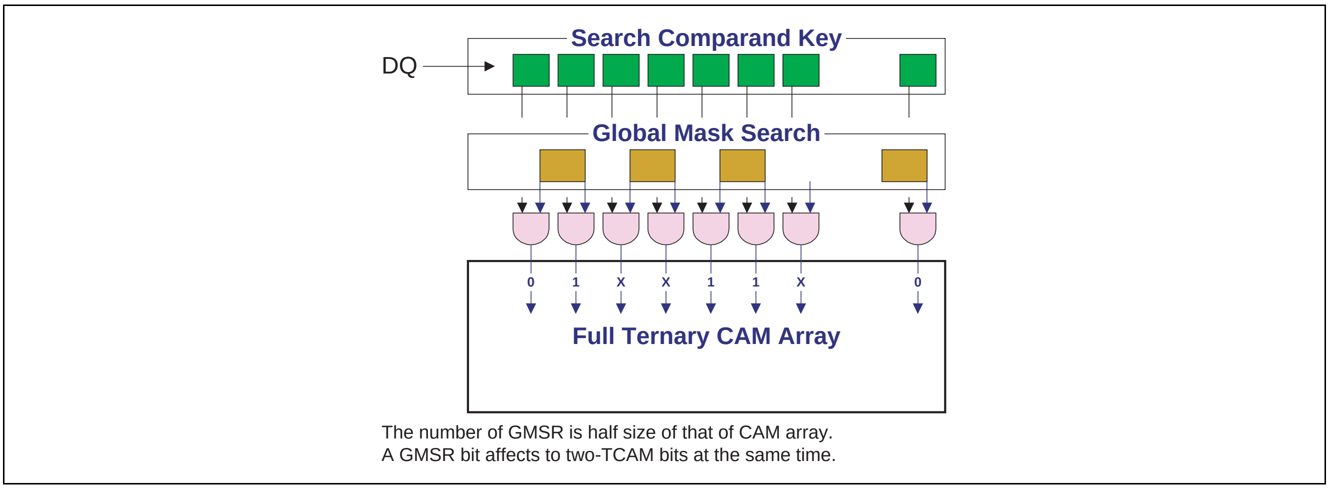


Figure 2 Global Mask Search (MARIE)

3. Special Flag Bits at MSB
   Bit [143:142] in the 144-bit lookup size or bit [287:286] in the 288-bit lookup size can have a special purpose for each entry. These bits are used to indicate whether the entry is empty or full, bit "00" = empty or bit "11" = full. Same data are always written to these bits depending on "empty" or "full".
   When the user wants to search for the first "empty" location, a search key of 2'b00 for bit [143:142] (or [287:286] in 288 configuration) is applied. In other words, the GMSR should set to "0" for [141:0] or [285:0].
   MARIE does not implement special hardware to know the next free address. This is known by using a special flag bit and a normal search command.
   After power on, the TCAM memory data is in the unknown state of empty/full. All the data entries have to be initialized with the Write Delete Entry command so that these special flag bits are all set to "empty" MSB (bit "00").

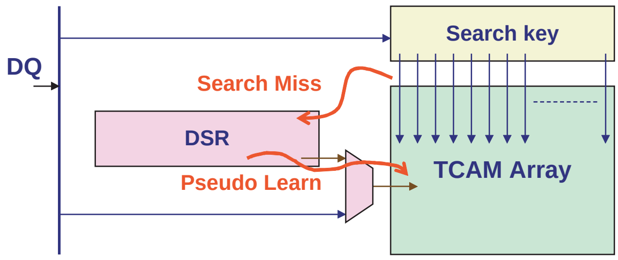
4. Address Source and Data Source
   A couple of different sources can be selected to write data or mask into MARIE's TCAM Array. There are two possible sources for the address; the DQ input pin and the Address Source Register (ASR). Similarly there are two sources for the data input: the DQ input pin and the Data Source Register (DSR).

   — Address Source Register (ASR)
   When Write TCAM is issued DQ-pin input or ASR can be selected as internal Address source.
   When the Search result is a hit, the corresponding #entry address is transferred to ASR. The user can trace the search successful history by reading the data from the ASR to the DQ pin. Searching for a "00XXXXX" would return the first empty location.

   — Data Source Register (DSR)
   The DQ-pin or DSR can be selected as a data source.
   When the Search result is a miss, the corresponding compared key is transferred to DSR. The missed compared data can later be used for pseudo learning or writing to the TCAM.

5. Pre-programmed Configuration
   MARIE's internal configuration should be pre-programmed before operation starts.
   8 K entry times 144-bit lookup
   4 K entry times 288-bit lookup

6. Pseudo Learn
   MARIE does not implement special hardware to support the Learn command. However, Pseudo Learn can be done by a combination of DSR and other common commands. First, when Search miss occurs, the search compared key is memorized into the DSR. By using the Write command and the data source of DSR Learning can be achieved. It is also possible to combine the pseudo learn with the location of the next free address search described in section 4.



What is Pseudo Learn?

Normal search → Search Miss → Stack to DSR → Write from DSR

If the next free address is not known, the additional sequence described in sect. 1-4 should be done before Pseudo Learn.

Figure 3 Pseudo Learn

7. Turbo Mode with Shifting Payload
   When performing unanchored searches on the payload data the turbo mode can be useful. In this mode an internal shifting algorithm helps increase the bandwidth at the IO and also eases the host processing.
   Once the Turbo Data Shift Register (TDSR) is full MARIE performs a search and automatically shifts the key 1-byte per clock, executing one search per clock until a match is found or the register empties. The user would update the Turbo Data Register (TDR) (usually every 36 cycles). No redundant payload data is inputted from the host MARIE allowing for a bandwidth increase (in 36-bit mode) and easing the host processing.
   Additionally the user can provide a header. The header is a register that is kept constant over the search operation. These registers are HDR0 (2B) and HDR1 (16B). In the 144-bit lookup size mode HDR0 or no header can be useful. In the 288-bit lookup size mode HDR0, HDR1, or no header could be selected. The header user mode is selected in the ST register.
   The search result occurs on every clock. The user receives the return data via the IND pin
   The performance limit of that Turbo Search Mode is
   100 Msps in 144-bit lookup
   100 Msps in 288-bit lookup

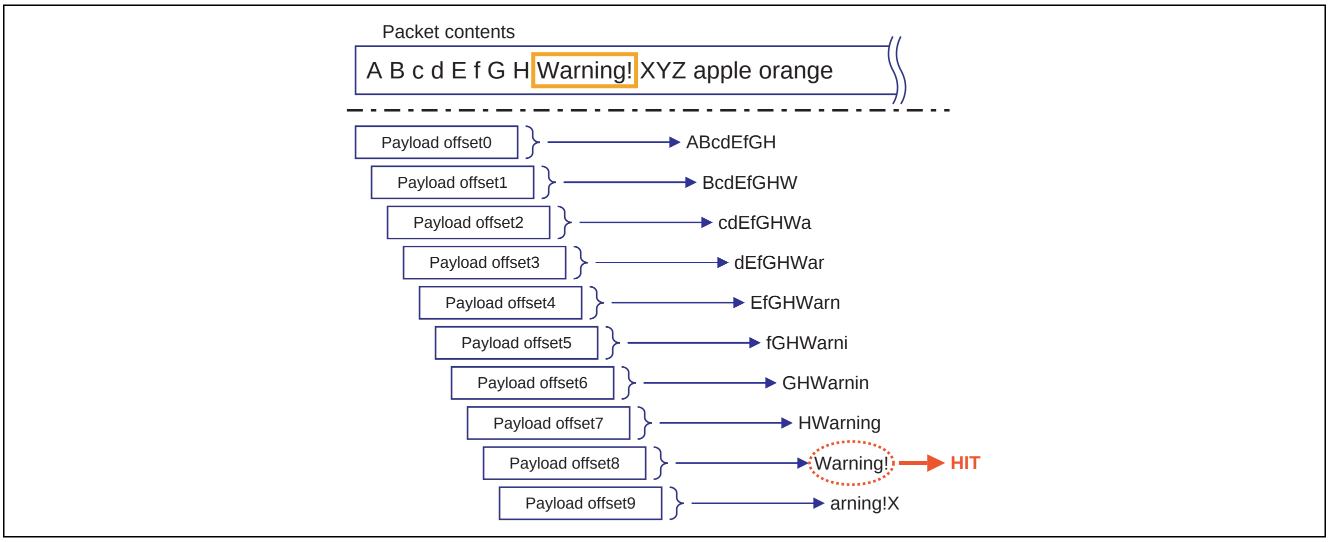


Figure 4 Shifted Payload Search

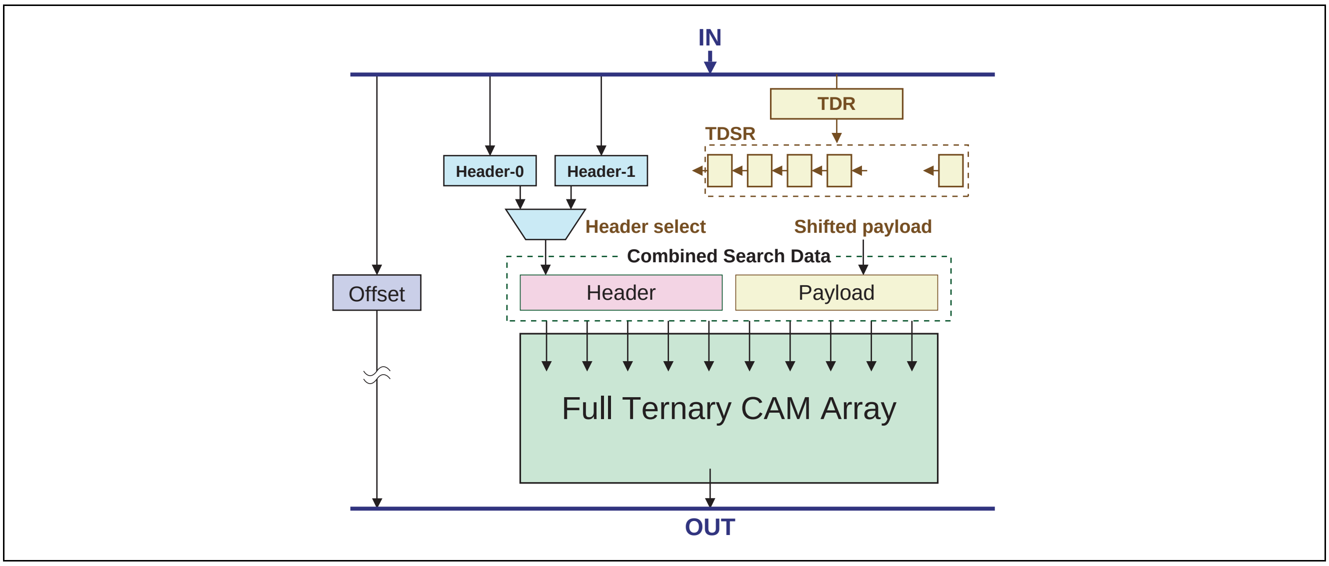


Figure 5 Turbo Search Mode

Pin Description

- Common

Pin Name	Symbol	I/O	Interface	Description
Master clock	CLK	I	SSTL-2	All input pins are referenced to the rising edge of CLK.
/Master clock	ZCLK	I	SSTL-2	Some input pins are referenced to the rising edge of ZCLK.
Reset L	RSTL	I	2.5V LVTTL	This signal is hardware reset of MARIE device.
Tuning enable	TUE	I	2.5V LVTTL	This signal is used only in Power Up Sequence for internal tuning. Keep always GND after Power Up Sequence.

- Network Processor/ASIC Interface

Pin Name	Symbol	I/O	Interface	Description
Operation enable	OP_ENA	I	SSTL-2	OP_ENA enables all functions, which is defined during two cycles, cycle-A and cycle-B.
Operation code [5:0]	OP	I	SSTL-2	OP [5:0] specifies the instruction and other commands, which is defined within two cycles, cycle-A and cycle-B.
DQ [35:0]	DQ	I/O-Tri	SSTL-2	Multiplexed Address/Data bus during Read, Write and Search command. These pins are used for Address field, and for Data field, which specifies Data and Mask.
DQS	DQS	O-Tri	SSTL-2	This signal is buffering the CLK.
Rule index [6:0]	IND	O-Tri	SSTL-2	The IND signal is used to address-input of externally located SRAM. That is to lookup Rule corresponding to MARIE search address.
Offset ID in [2:0]	OID_I	I	SSTL-2	This signal specifies Search results. It sets in Search command.
Offset ID out [2:0]	OID_O	O-Tri	SSTL-2	This signal is directly transferred from OID_I [2:0]. OID_O [2] is used as TRF (TDR Register write enable Flag) in Turbo Search Mode.
Search result flag	SR_F	O	SSTL-2	Search Result Flag is as Local Winner Flag in cycle-A and Multiple Match Flag in cycle-B. Local Winner Flag goes high when Search result is “HIT”. Multiple Match Flag goes high when the multiple matched entries are found.

- JTAG Interface

Pin Name	Symbol	I/O	Interface	Description
Test mode select	TMS	I	2.5V LVTTL	This signal selects the JTAG instruction and the state.
Test data input	TDI	I	2.5V LVTTL	JTAG data input pin
Test data output	TDO	O	2.5V LVTTL	JTAG data output pin
Test clock	TCK	I	2.5V LVTTL	JTAG clock
JTAG reset	TRST	I	2.5V LVTTL	JTAG scan reset

Note: JTAG specification is referenced to IEEE 1149.1.

- Power and Ground

Pin Name	Symbol	I/O	Interface	Description
Vectored	V_CORE	—	—	1.5 V for core and peripheral circuitry
Voltage for search	V_MAT	—	—	1.5 V for search circuitry. Must be same as V_CORE
I/O buffer supply voltage	VCCQ	—	—	2.5 V for DRAM and I/O
Input reference voltage	V_REF	—	—	50% of VCCQ
Ground	GND	—	—	0 V Ground level

Pin Arrangement

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	VCCQ	DQ[0]	GND	OP_ENA	VCCQ	OP[0]	OP[1]	VCCQ	VCCQ	OID_I[0]	OID_I[1]	VCCQ	NC	GND	DQ[1]	VCCQ	A
B	DQ[2]	GND	DQ[4]	V_CORE	DQ[6]	V_REF	OP[2]	OP[3]	OP[4]	OP[5]	VCCQ	OID_I[2]	V_CORE	DQ[5]	GND	DQ[3]	B
C	DQ[8]	VCCQ	V_CORE	DQ[10]	GND	DQ[12]	VCCQ	DQ[14]	NC	VCCQ	NC	GND	DQ[9]	V_CORE	VCCQ	DQ[7]	C
D	DQ[16]	GND	DQ[18]	V_CORE	DQ[20]	V_MAT	DQ[22]	GND	NC	NC	V_MAT	DQ[15]	V_CORE	DQ[13]	GND	DQ[11]	D
E	DQ[24]	V_CORE	DQ[26]	DQ[28]	DQ[30]	V_MAT	GND	V_MAT	V_MAT	TUE	V_MAT	DQ[21]	GND	DQ[19]	V_CORE	DQ[17]	E
F	VCCQ	DQ[32]	GND	GND	V_MAT	V_MAT	GND	GND	GND	GND	V_MAT	V_MAT	DQ[25]	GND	DQ[23]	VCCQ	F
G	DQ[34]	GND	ZCLK	GND	V_MAT	V_MAT	GND	GND	GND	GND	V_MAT	V_MAT	DQ[31]	DQ[29]	GND	DQ[27]	G
H	NC	GND	GND	GND	V_MAT	V_MAT	GND	GND	GND	GND	V_MAT	V_MAT	NC	GND	DQ[35]	DQ[33]	H
J	NC	GND	CLK	GND	V_MAT	V_MAT	GND	GND	GND	GND	V_MAT	V_MAT	NC	GND	NC	NC	J
K	NC	GND	GND	GND	V_MAT	V_MAT	GND	GND	GND	GND	V_MAT	V_MAT	NC	NC	GND	NC	K
L	VCCQ	NC	NC	GND	V_MAT	V_MAT	GND	GND	GND	GND	V_MAT	V_MAT	NC	NC	NC	VCCQ	L
M	NC	V_CORE	NC	NC	NC	V_MAT	GND	V_MAT	V_MAT	GND	V_MAT	NC	GND	NC	V_CORE	NC	M
N	NC	GND	NC	V_CORE	NC	V_MAT	NC	GND	TMS	TRST	V_MAT	NC	V_CORE	NC	GND	NC	N
P	NC	VCCQ	V_CORE	NC	GND	NC	VCCQ	TCK	TDI	VCCQ	TDO	GND	RSTL	V_CORE	VCCQ	NC	P
R	NC	GND	NC	V_CORE	IND[1]	VCCQ	IND[4]	IND[5]	IND[6]	NC	VCCQ	OID_O[1]	V_CORE	GND	GND	NC	R
T	VCCQ	DQS	GND	IND[0]	VCCQ	IND[2]	IND[3]	VCCQ	V_REF	NC	OID_O[0]	VCCQ	OID_O[2]	GND	SR_F	VCCQ	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

(Top view)

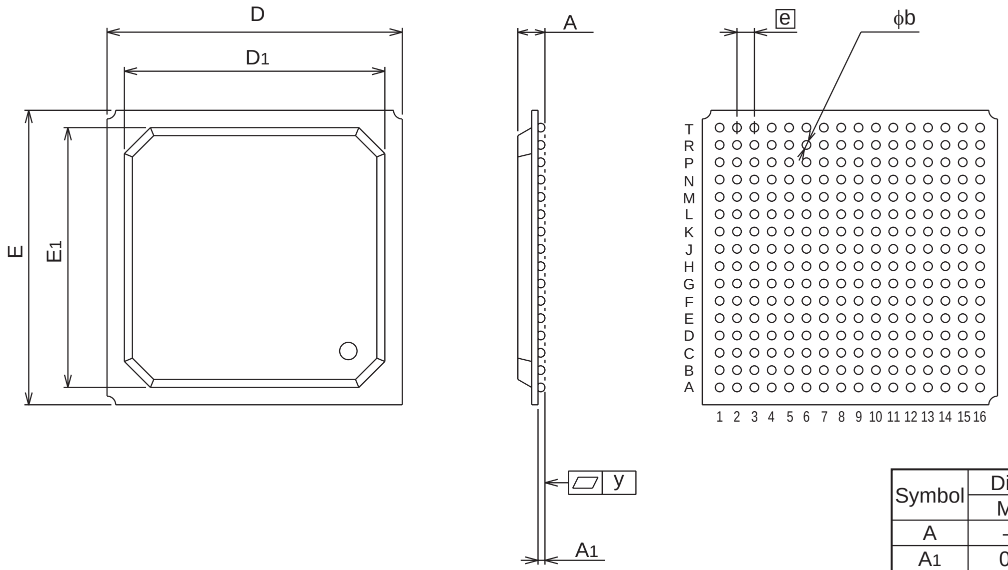
Note: V_CORE and V_MAT can be combined.

Package Dimensions

256F7X-D — **256pin 17 × 17mm body BGA**

EIAJ Package Code	JEDEC Code	Weight(g)
—	—	

Under Development



Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	2.0
A_1	0.3	0.4	0.5
b	0.4	0.5	0.6
D	—	17.0	—
D_1	—	15.0	—
E	—	17.0	—
E_1	—	15.0	—
e	—	1.0	—
y	—	—	0.15

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