NTHS5402T1

Power MOSFET N-Channel ChipFET™

4.9 Amps, 30 Volts

Features

- Low $R_{DS(on)}$ for Higher Efficiency
- Miniature ChipFET Surface Mount Package

Applications

- Power Management in Portable and Battery−Powered Products; i.e., Cellular and Cordless Telephones and PCMCIA Cards

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

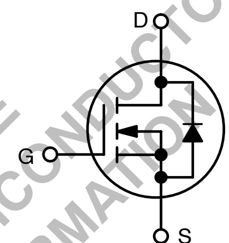
Rating	Symbol	5 secs	Steady State	Unit
Drain−Source Voltage	V_{DS}	30		V
Gate−Source Voltage	V_{GS}	±20		V
Continuous Drain Current (T_J = 150°C) (Note 1.) T_A = 25°C T_A = 85°C	I_D	±6.7 ±4.8	±4.9 ±3.5	A
Pulsed Drain Current	I_{DM}	±20		A
Continuous Source Current (Diode Conduction) (Note 1.)	I_S	2.1	1.1	A
Maximum Power Dissipation (Note 1.) T_A = 25°C T_A = 85°C	P_D	2.5 1.3	1.3 0.7	W
Operating Junction and Storage Temperature Range	T_J, T_{stg}	−55 to +150		°C

1. Surface Mounted on 1″ x 1″ FR4 Board.

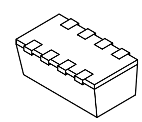
ON Semiconductor™

http://onsemi.com

4.9 AMPS
30 VOLTS
$R_{DS(on)}$ = 35 mΩ

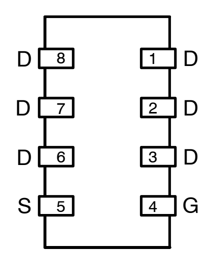


N−Channel MOSFET

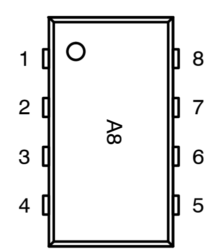


ChipFET
CASE 1206A
STYLE 1

PIN CONNECTIONS



MARKING DIAGRAM



A8 = Specific Device Code

ORDERING INFORMATION

Device	Package	Shipping
NTHS5402T1	ChipFET	3000/Tape & Reel

THERMAL CHARACTERISTICS

Characteristic	Symbol	Typ	Max	Unit
Maximum Junction−to−Ambient (Note 2.) t ≤ 5 sec Steady State	R_{thJA}	 40 80	 50 95	°C/W
Maximum Junction−to−Foot (Drain) Steady State	R_{thJF}	15	20	°C/W

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 250 μA	1.0	–	–	V
Gate−Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V	–	–	±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 24 V, V_{GS} = 0 V	–	–	1.0	μA
		V_{DS} = 24 V, V_{GS} = 0 V, T_J = 85°C	–	–	5.0	
On−State Drain Current (Note 3.)	$I_{D(on)}$	V_{DS} ≥ 5.0 V, V_{GS} = 10 V	20	–	–	A
Drain−Source On−State Resistance (Note 3.)	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 4.9 A	–	0.030	0.035	Ω
		V_{GS} = 4.5 V, I_D = 3.9 A	–	0.045	0.055	
Forward Transconductance (Note 3.)	g_{fs}	V_{DS} = 10 V, I_D = 4.9 A	–	15	–	S
Diode Forward Voltage (Note 3.)	V_{SD}	I_S = 1.1 A, V_{GS} = 0 V	–	0.8	1.2	V
Dynamic (Note 4.)						
Total Gate Charge	Q_g	V_{DS} = 15 V, V_{GS} = 10 V, I_D = 4.9 A	–	13	20	nC
Gate−Source Charge	Q_{gs}		–	1.3	–	
Gate−Drain Charge	Q_{gd}		–	3.1	–	
Turn−On Delay Time	$t_{d(on)}$	V_{DD} = 15 V, R_L = 15 Ω, I_D ≅ 1.0 A, V_{GEN} = 10 V, R_G = 6 Ω	–	10	15	ns
Rise Time	t_r		–	10	15	
Turn−Off Delay Time	$t_{d(off)}$		–	25	40	
Fall Time	t_f		–	10	15	
Source−Drain Reverse Recovery Time	t_{rr}	I_F = 1.1 A, di/dt = 100 A/μs	–	30	60	

2. Surface Mounted on 1″ x 1″ FR4 Board.
3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTICS

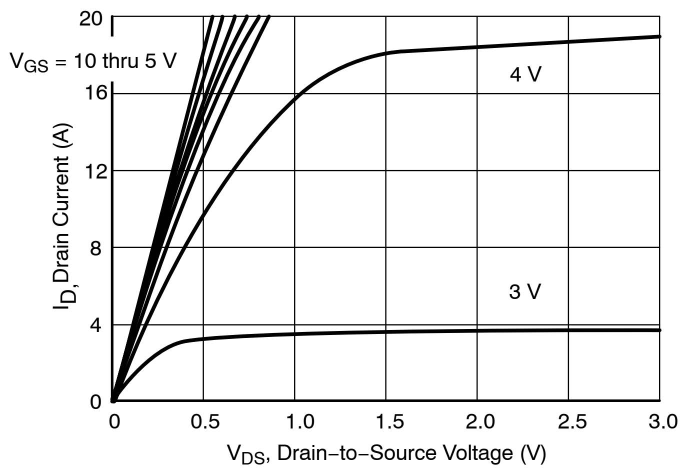


Figure 1. Output Characteristics

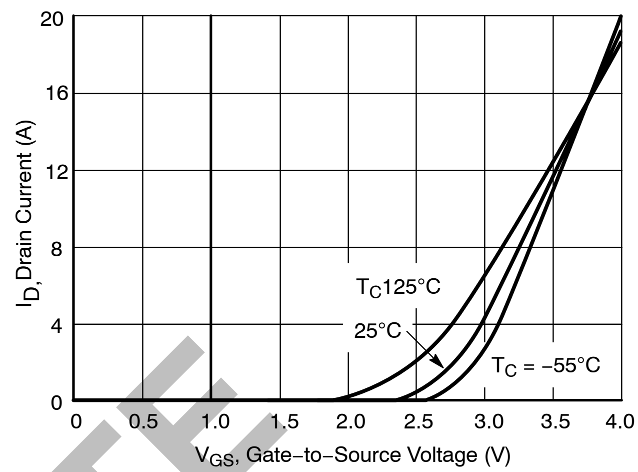


Figure 2. Transfer Characteristics

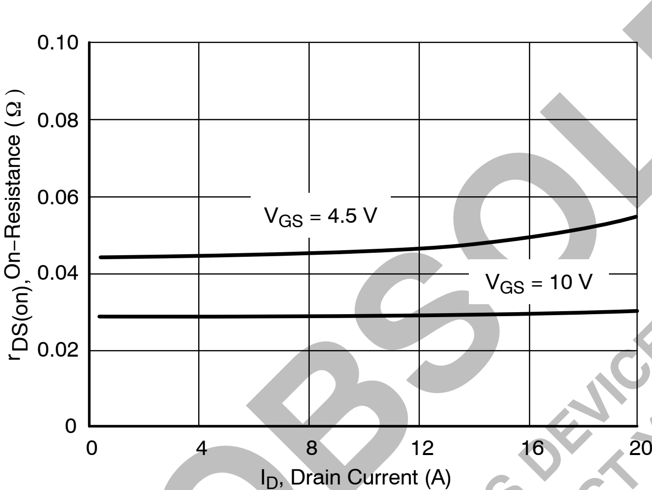


Figure 3. On−Resistance vs. Drain Current

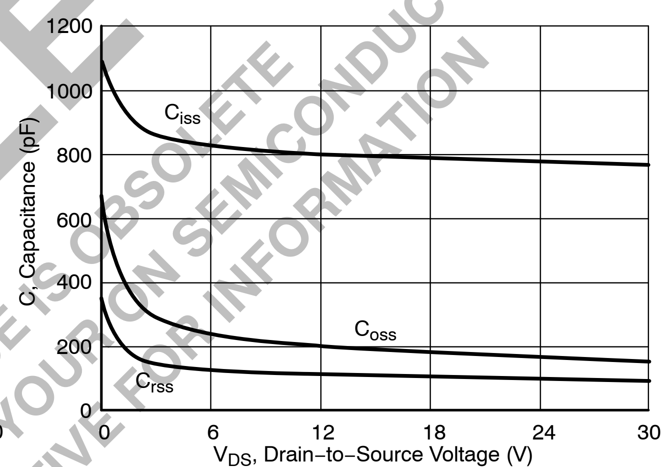


Figure 4. Capacitance

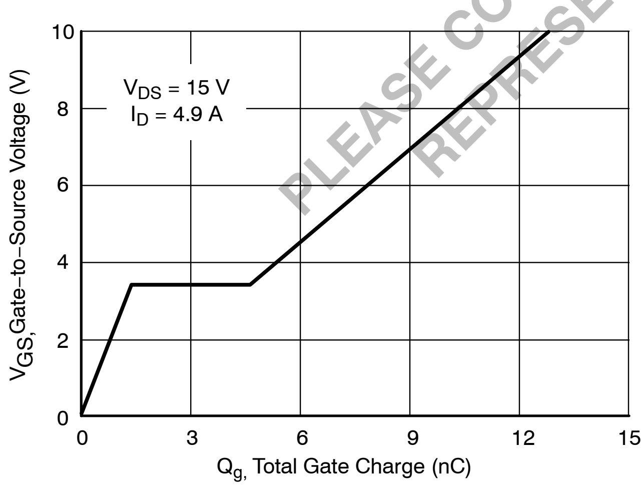


Figure 5. Gate Charge

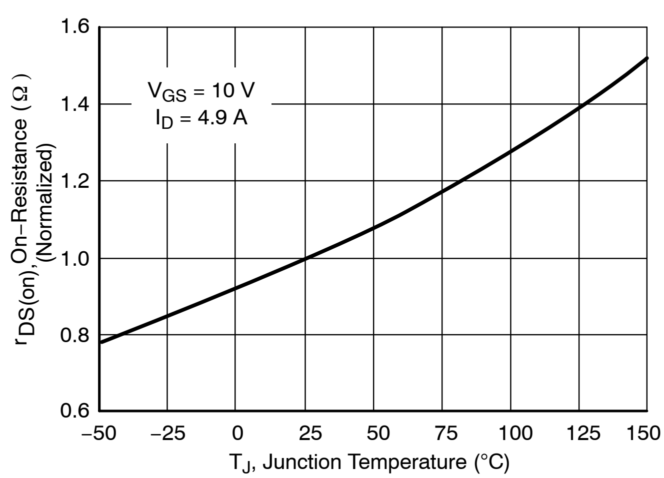


Figure 6. On−Resistance vs. Junction Temperature

TYPICAL CHARACTERISTICS

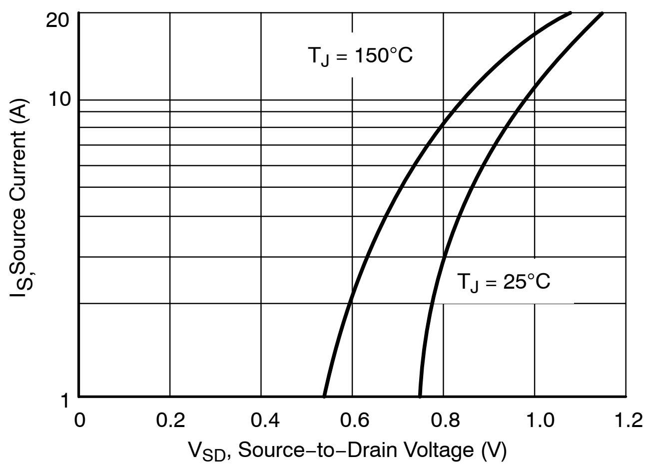


Figure 7. Source−Drain Diode Forward Voltage

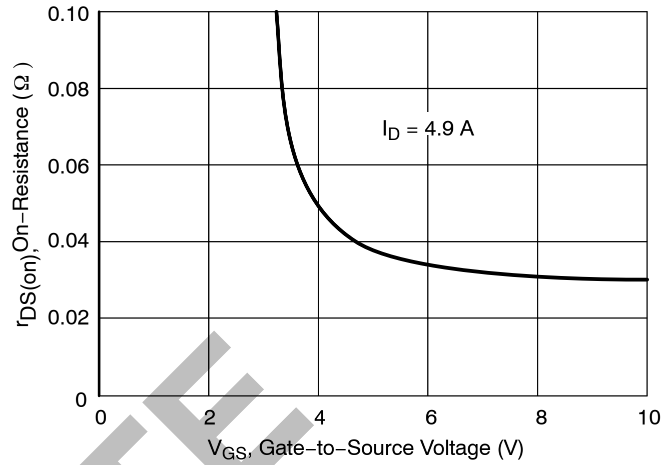


Figure 8. On−Resistance vs. Gate−to−Source Voltage

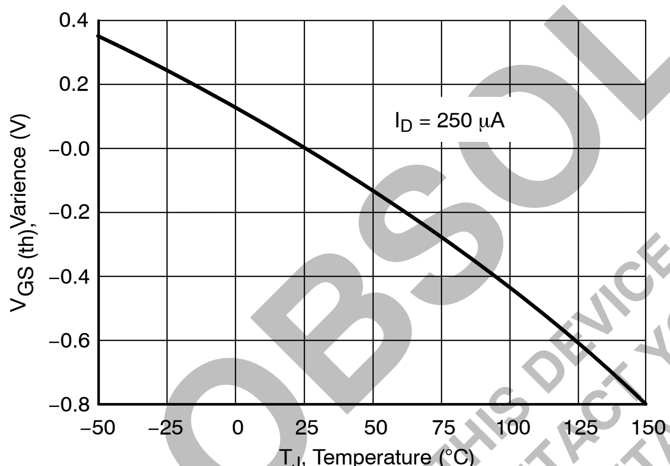


Figure 9. Threshold Voltage

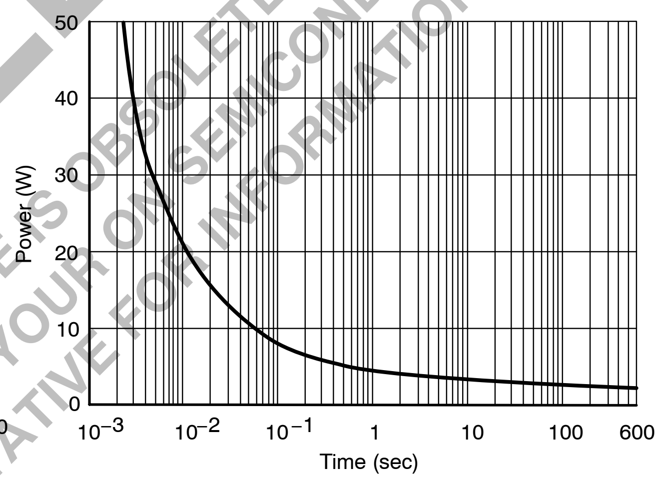


Figure 10. Single Pulse Power

TYPICAL CHARACTERISTICS

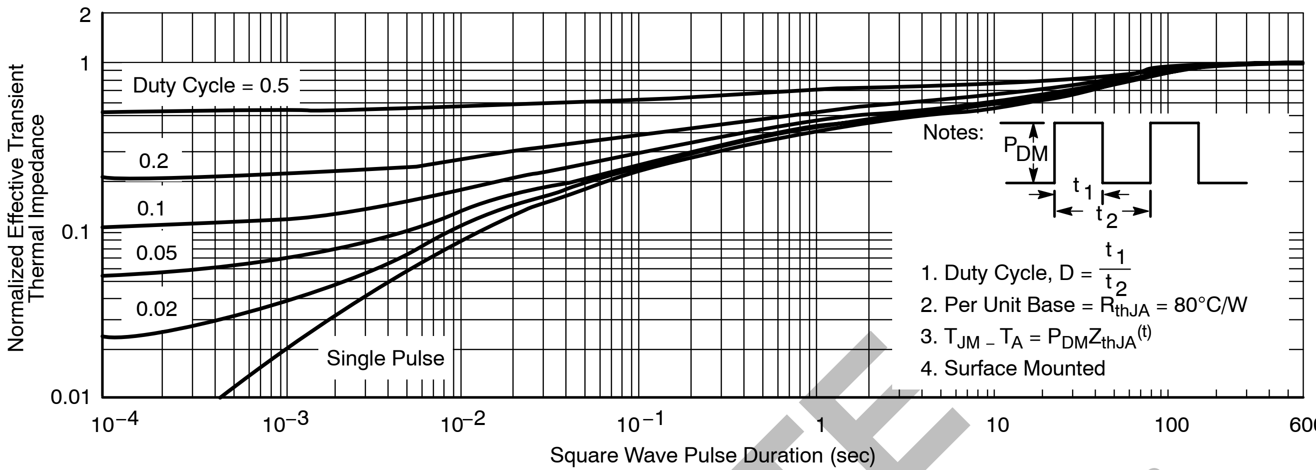


Figure 11. Normalized Thermal Transient Impedance, Junction−to−Ambient

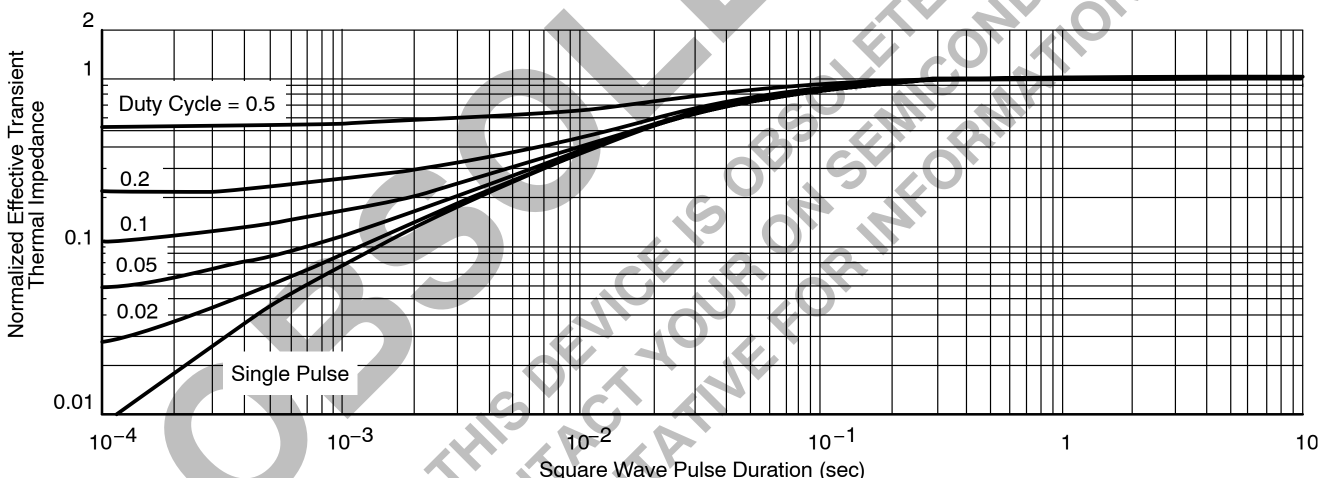


Figure 12. Normalized Thermal Transient Impedance, Junction−to−Foot

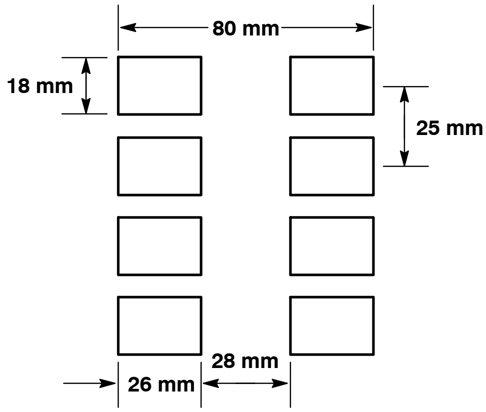


Figure 13.

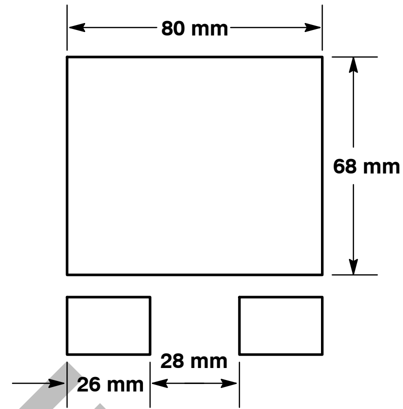


Figure 14.

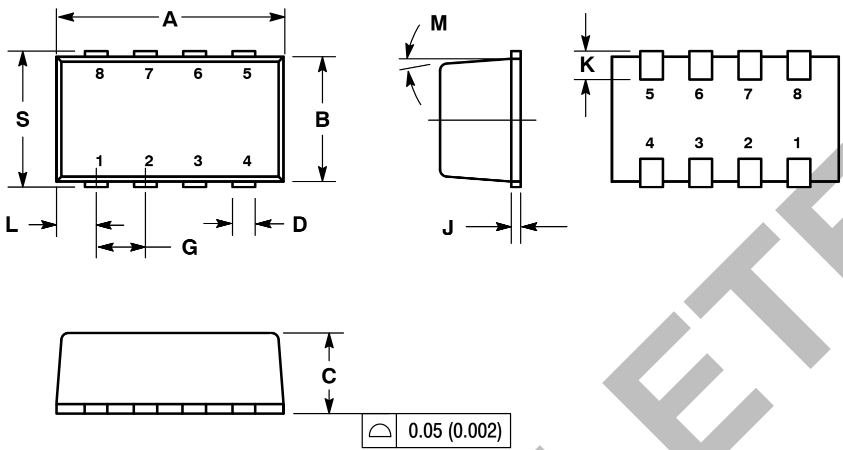
BASIC PAD PATTERNS

The basic pad layout with dimensions is shown in Figure 13. This is sufficient for low power dissipation MOSFET applications, but power semiconductor performance requires a greater copper pad area, particularly for the drain leads.

The minimum recommended pad pattern shown in Figure 14 improves the thermal area of the drain connections (pins 1, 2, 3, 6, 7, 8) while remaining within the confines of the basic footprint. The drain copper area is 0.0054 sq. in. (or 3.51 sq. mm). This will assist the power dissipation path away from the device (through the copper leadframe) and into the board and exterior chassis (if applicable) for the single device. The addition of a further copper area and/or the addition of vias to other board layers will enhance the performance still further.

PACKAGE DIMENSIONS

ChipFET
CASE 1206A−03
ISSUE C



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MOLD GATE BURRS SHALL NOT EXCEED 0.13 MM PER SIDE.
4. LEADFRAME TO MOLDED BODY OFFSET IN HORIZONTAL AND VERTICAL SHALL NOT EXCEED 0.08 MM.
5. DIMENSIONS A AND B EXCLUSIVE OF MOLD GATE BURRS.
6. NO MOLD FLASH ALLOWED ON THE TOP AND BOTTOM LEAD SURFACE.
7. 1206A−01 AND 1206A−02 OBSOLETE. NEW STANDARD IS 1206A−03.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.95	3.10	0.116	0.122
B	1.55	1.70	0.061	0.067
C	1.00	1.10	0.039	0.043
D	0.25	0.35	0.010	0.014
G	0.65 BSC		0.025 BSC	
J	0.10	0.20	0.004	0.008
K	0.28	0.42	0.011	0.017
L	0.55 BSC		0.022 BSC	
M	5 ° NOM		5 ° NOM	
S	1.80	2.00	0.072	0.080

STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. GATE
5. SOURCE
6. DRAIN
7. DRAIN
8. DRAIN

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