SPECTRUM DIGITAL INCORPORATED

TMS320C6455 DSK

Technical Reference

2006 DSP Development Systems

TMS320C6455 DSK
Technical Reference

508555-0001 Rev. C
September 2006

SPECTRUM DIGITAL, INC.
12502 Exchange Drive, Suite 440 Stafford, TX. 77477
Tel: 281.494.4505 Fax: 281.494.5310
sales@spectrumdigital.com www.spectrumdigital.com

IMPORTANT NOTICE

Spectrum Digital, Inc. reserves the right to make changes to its products or to discontinue any product or service without notice. Customers are advised to obtain the latest version of relevant information to verify that the data being relied on is current before placing orders.

Spectrum Digital, Inc. warrants performance of its products and related software to current specifications in accordance with Spectrum Digital's standard warranty. Testing and other quality control techniques are utilized to the extent deemed necessary to support this warranty.

Please be aware that the products described herein are not intended for use in life-support appliances, devices, or systems. Spectrum Digital does not warrant nor is Spectrum Digital liable for the product described herein to be used in other than a development environment.

Spectrum Digital, Inc. assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does Spectrum Digital warrant or represent any license, either express or implied, is granted under any patent right, copyright, or other intellectual property right of Spectrum Digital, Inc. covering or relating to any combination, machine, or process in which such Digital Signal Processing development products or services might be or are used.

WARNING

This equipment is intended for use in a laboratory test environment only. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to subpart J of part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures necessary to correct this interference.

Copyright © 2006 Spectrum Digital, Inc.

Contents

1 Introduction to the TMS320C6455 DSK Module 1-1

Provides you with a description of the TMS320C6455 DSK Module, key features, and block diagram.

1.1 Key Features 1-2
1.2 Functional Overview 1-3
1.3 Basic Operation 1-4
1.4 Memory Map 1-5
1.5 Configuration Switch Settings 1-6
1.6 Bootmode Configurations 1-7
1.7 Power Supply 1-8

2 Board Components 2-1

Describes the operation of the major board components on the TMS320C6455 DSK.

2.1 CPLD (programmable Logic) 2-2
2.1.1 CPLD Overview 2-2
2.1.2 CPLD Registers 2-3
2.1.3 USER_REG Register 2-3
2.1.4 DC_REG Register 2-4
2.1.5 Version Register 2-4
2.1.6 MISC Register 2-5
2.1.7 MISC2 Register 2-5
2.2 Codec Interface 2-6
2.3 DDR2 Memory 2-7
2.4 Flash Memory 2-7
2.5 LEDs and DIP Switches 2-7
2.6 Ethernet Interface 2-7
2.7 I^2C ROM 2-8
2.8 Daughter Card Interface 2-8
2.9 DSP and EMIFA Clock Generation 2-8
2.10 JTAG Interface 2-10

3 Physical Specifications 3-1

Describes the physical layout of the TMS320C6455 DSK and its connectors.

3.1 Board Layout 3-2
3.2 Connector Index 3-3
3.3 Expansion Connectors 3-3
3.3.1 J4, Memory Expansion 3-4
3.3.2 J3, Peripheral Expansion 3-5
3.3.3 J1, HPI Expansion Connector 3-6
3.4 Audio Connectors 3-8
3.4.1 J1301, Microphone Connector 3-8
3.4.2 J1303, Audio Line In Connector 3-8

3.4.3 J1304, Audio Line Out Connector 3-9
3.4.4 J1302, Headphone Connector 3-9
3.5 Power Connectors 3-10
3.5.1 J5, +5V Main Power Connector 3-10
3.5.2 J6, Optional Power Connector 3-10
3.6. Miscellaneous Connectors 3-11
3.6.1 J1201, USB Port 3-11
3.6.2 J8, 14 Pin External JTAG Connector 3-12
3.6.3 J7, 60 Pin Advanced Emulation Connector 3-13
3.6.4 JP3, PLD Programming Connector 3-13
3.6.5 J9, AMCC Connector 3-13
3.6.6 P1102, Ethernet Connector 3-14
3.7 System LEDs 3-14
3.8 SW2, Reset Switch 3-14
A Schematics A-1
Contains the schematics for the TMS320C6455 DSK
B Mechanical Information B-1
Contains the mechanical information about the TMS320C6455 DSK

About This Manual

This document describes the board level operations of the TMS320C6455 DSP Starter Kit (DSK) module. The DSK is based on the Texas Instruments TMS320C6455 Digital Signal Processor.

The TMS320C6455 DSK is a table top card to allow engineers and software developers to evaluate certain characteristics of the TMS320C6455 DSP to determine if the processor meets the designers application requirements. Evaluators can create software to execute onboard or expand the system in a variety of ways.

Notational Conventions

This document uses the following conventions.

The TMS320C6455 DSK will sometimes be referred to as the DSK, C6455 DSK, or TMS320C6455 DSK.

Program listings, program examples, and interactive displays are shown is a special italic typeface. Here is a sample program listing.

equations
!rd = !strobe&rw;

Information About Cautions

This book may contain cautions.
This is an example of a caution statement.
A caution statement describes a situation that could potentially damage your software, or hardware, or other equipment. The information in a caution is provided for your protection. Please read each caution carefully.

Related Documents

Texas Instruments TMS320C64xx DSP CPU Reference Guide
Texas Instruments TMS320C64xx DSP Peripherals Reference Guide

Table 1: Manual History

Revision	History
A	Initial Release
B	Changed CLKIN to 50 Mhz. Fixed swizzle on daughter card interrupts
C	Corrected connector documentation Replaced sheets 4,5 of schematics

Chapter 1

Introduction to the TMS320C6455 DSK

Chapter One provides a description of the TMS320C6455 DSK along with the key features and a block diagram of the circuit board.

Topic		Page
1.1	Key Features	1-2
1.2	Functional Overview	1-3
1.3	Basic Operation	1-4
1.4	Memory Map	1-5
1.5	Configuration Switch Settings	1-6
1.6	Bootmode Configurations	1-7
1.7	Power Supply	1-8

1.1 Key Features

The C6455 DSK is a high performance standalone development platform that enables users to evaluate and develop applications for the TI C64xx DSP family. The DSK also serves as a hardware reference design for the TMS320C6455 DSP. Schematics, logic equations and application notes are available to ease hardware development and reduce time to market.

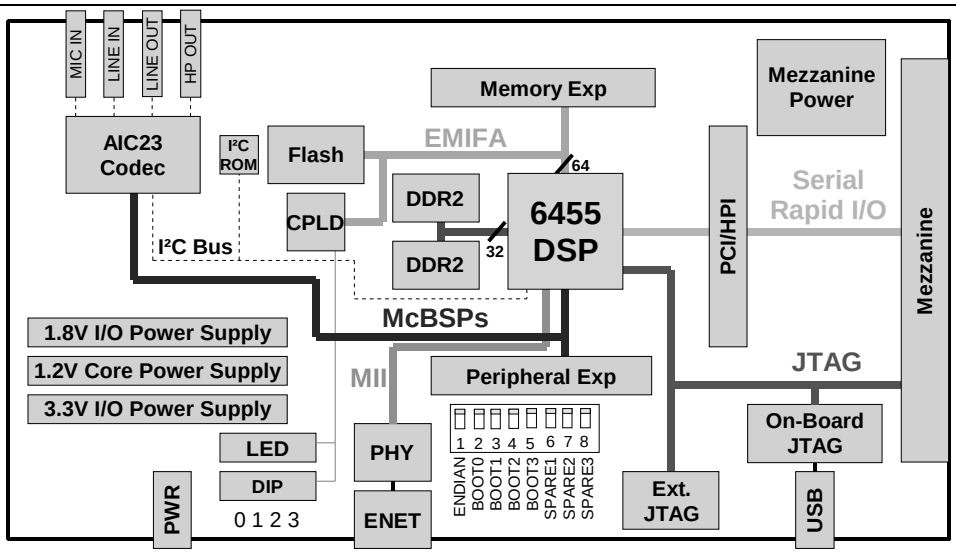


Figure 1-1, Block Diagram C6455 DSK

The DSK comes with a full compliment of on-board devices that suit a wide variety of application environments. Key features include:

- A Texas Instruments TMS320C6455 DSP operating at 1 Gigahertz.
- An AIC23 stereo codec
- 128 Mbytes of DDR2 memory
- 4M bytes of non-volatile Flash memory
- 10/100 MBPs ethernet interface
- I^2C Serial ROM
- 4 user accessible LEDs and DIP switches
- Software board configuration through registers implemented in CPLD
- Configured boot options and clock input selection
- Standard expansion connectors for daughter card use

- JTAG emulation through on-board JTAG emulator with USB host interface or external emulator
- Single voltage power supply (+5V)

1.2 Functional Overview of the TMS320C6455 DSK

The DSP on the C6455 DSK interfaces to on-board peripherals through the 64-bit wide EMIFA configured for 32 bit accesses. The CPLD and daughter card expansion connectors are connected to EMIFA. The DDR2 memory is on its own dedicated EMIF.

An on-board AIC23 codec allows the DSP to transmit and receive analog signals. I^2C is used for the codec control interface and McBSP1 is used for data. Analog I/O is done through four 3.5mm audio jacks that correspond to microphone input, line input, line output and headphone output. The codec can select the microphone or the line input as the active input. The analog output is driven to both the line out (fixed gain) and headphone (adjustable gain) connectors. McBSP0 and McBSP1 can be re-routed to the expansion connectors in software.

A programmable logic device called a CPLD is used to implement glue logic that ties the board components together. The CPLD also has a register based user interface that lets the user configure the board by reading and writing to the CPLD registers.

A Flash memory is mapped into CE3 space. The Flash contains power on self test as shipped, or can be programmed for user programs.

The DSK has a 10/100 mbit Phy which is connected to the DSP's on board EMAC.

The DSK includes 4 LEDs and 4 position DIP switch as a simple way to provide the user with interactive feedback. Both are accessed by reading and writing to the CPLD registers.

An included 5V external power supply is used to power the board. On-board switching voltage regulators provide the 1.2V DSP core voltage, 1.8V for DDR, and 3.3V I/O supplies. The board is held in reset until these supplies are within operating specifications.

Code Composer communicates with the DSK through an embedded JTAG emulator with a USB host interface. The DSK can also be used with an external emulator through the external 60 pin and 14 pin JTAG connectors.

1.3 Basic Operation

The DSK is designed to work with TI's Code Composer Studio development environment and ships with a version specifically tailored to work with the board. Code Composer communicates with the board through the on-board JTAG emulator. To start, follow the instructions in the Quick Start Guide to install Code Composer. This process will install all of the necessary development tools, documentation and drivers.

After the install is complete, follow these steps to run Code Composer. The DSK must be fully connected to launch the DSK version of Code Composer.

1) Connect the included power supply to the DSK.

2) Connect the DSK to your PC with a standard USB cable (also included).

3) Launch Code Composer from its icon on your desktop.

Detailed information about the DSK including a tutorial, examples and reference material is available in the DSK's help file.

1.4 Memory Map

The C64xx family of DSPs has a large byte addressable address space. Program code and data can be placed anywhere in the unified address space. Addresses are always 32-bits wide.

The memory map shows the address space of a generic 6455 processor on the left with specific details of how each region is used on the right. By default, the internal memory sits at the beginning of the address space. Portions of memory can be remapped in software as L2 cache rather than fixed RAM.

EMIFA (External Memory Interface A) has 4 separate addressable regions called chip enable spaces (CE2-CE5). The DDR2 occupies CE0 of DDR2 Memory bus. The CPLD and Flash are mapped to CE2 and CE3 of EMIFA respectively. Daughter cards use CE4 and CE5 of EMIFA.

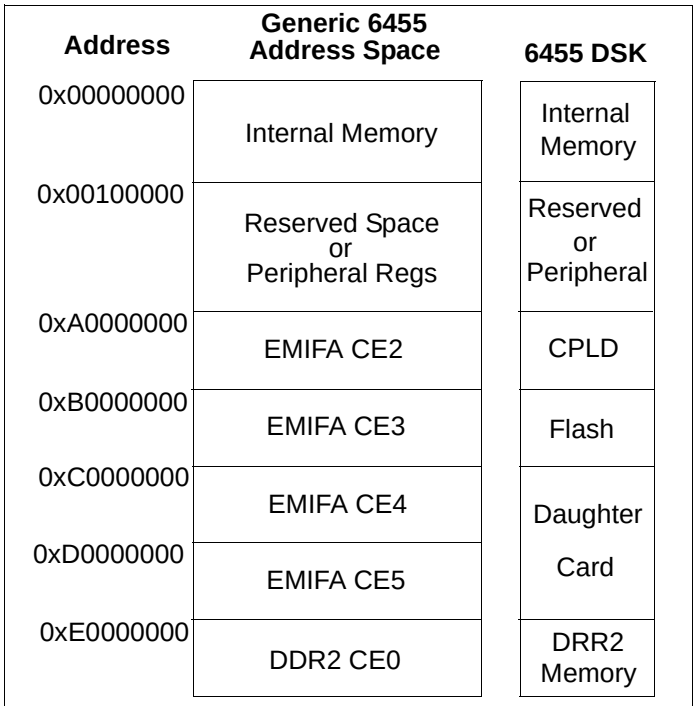


Figure 1-2, Memory Map, C6455 DSK

1.5 Configuration Switch Settings

The DSK has 8 configuration switches that allows users to control the operational state of the DSP when it is released from reset. The configuration switch block is labeled SW3 on the DSK board, next to the reset switch.

Configuration switch 1 controls the endianness of the DSP. The factory default is little endian.The settings of switch 1 are shown in the table below.

Table 1: Endian Configuration Switch Settings

SW3-1	Configuration Description
Off	Little endian *
On	Big endian

***** Default

Switches 2-5 configure the boot mode that will be used when the DSP starts executing. These boot modes are shown in the table below. The default boot mode is EMIFA 8 bit ROM Boot.

Table 2: Boot Load Configuration Switch Settings

SW3-5 AE19	SW3-4 * AE18	SW3-3 AE17	SW3-2 AE16	Configuration Description
Off	Off	Off	Off	No Boot
Off	Off	Off	On	Host Boot HPI
Off	Off	On	Off	Reserved
Off	Off	On	On	Reserved
Off	On	Off	Off	EMIFA 8 bit ROM Boot *****
Off	On	Off	On	I^2C Boot Master
Off	On	On	Off	I^2C slave
Off	On	On	On	Host Boot PCI
On	x	x	x	Serial Rapid I/O Boot see DSP data sheet for more details

** Default

On revision “C” and newer boards the switch positions 6-8 are spare switches. The CLKIN frequency is now set to a fixed 50 Mhz. oscillator.

1.6 Bootmode Configurations

The C6455 uses the address lines to configure the device configuration at RESET. Although many of these configurations can be changed in software via internal DSP configuration registers, the defaults for the DSK are shown in the table below.

Table 3: Bootmode Configurations

Config Pin Name	Function	Controlled By
AE19	Boot Mode 3	SW3-5
AE18	Boot Mode 2	SW3-4
AE17	Boot Mode 1	SW3-3
AE16	Boot Mode 0	SW3-2
AE15	AECLKIN Selected	Resistor Strap
AE14	HPI 32 bit Mode Selected	Resistor Strap
AE13	Endian Mode	SW3-1
AE12	Ethernet MAC Enabled	Resistor Strap
AE11	Reserved	Resistor Strap
AE10	EMAC MDIO/MII Mode	Resistor Strap
AE9	EMAC MDIO/MII Mode	Resistor Strap
AE8	PCI I^2C ROM Enable	Resistor Strap
AE7	Reserved	Resistor Strap
AE6	PCI 33 Mhz.	Resistor Strap
AE5	McBSP1 Enabled	Resistor Strap
AE4	SYSCLK4 Output	Resistor Strap
AE3	Reserved	Resistor Strap
AE2	CFGGP2	Resistor Strap
AE1	CFGGP1	Resistor Strap
AE0	CFGGP0	Resistor Strap
ABA1	EMIFA Enabled	Resistor Strap
ABA0	DDR Enabled	Resistor Strap

1.7 Power Supply

The DSK operates from a single +5V external power supply connected to the main power input (J5). Internally, the +5V input is converted into +1.5, +1.8V and +3.3V using multiple voltage regulators. The +1.2V supply is used for the DSP core while the +3.3V supply is used for the DSP's I/O buffers and all other chips on the board. The +1.8 volt supply is used to support DDR2 memories. The power connector is a 2.5mm barrel-type plug.

The DSK provides +3.3V, up to 1A for the daughter card. The +3.3V supply is derived from the +5V power source via the main +3.3 volt regulator. It is also possible to provide the daughter card with +12V and -12V when the external power connector (J6) is used.

Chapter 2

Board Components

This chapter describes the operation of the major board components on the TMS320C6455 DSK.

Topic **Page**

2.1	CPLD (Programmable Logic)	2-2
2.1.1	CPLD Overview	2-2
2.1.2	CPLD Registers	2-3
2.1.3	USER_REG Register	2-3
2.1.4	DC_REG Register	2-4
2.1.5	Version Register	2-4
2.1.6	MISC Register	2-5
2.1.7	MISC2 Register	2-5
2.2	AIC23 Codec	2-6
2.3	DDR2 Memory	2-7
2.4	Flash Memory	2-7
2.5	LEDs and DIP Switches	2-7
2.6	Ethernet Interface	2-7
2.7	I^2C ROM	2-8
2.8	Daughter Card Interface	2-8
2.9	DSP and EMIFA Clock Generation	2-8
2.10	JTAG Interfaces	2-10

2.1 CPLD (Programmable Logic)

The C6455 DSK uses an Altera EPM3128TC100-10 Complex Programmable Logic Device (CPLD) device to implement:

- 5 Memory-mapped control/status registers that allow software control of various board features.
- Address decode and memory access logic.
- Control of the daughter card interface and signals.
- Assorted "glue" logic that ties the board components together.

2.1.1 CPLD Overview

The CPLD logic is used to implement functionality specific to the DSK. Your own hardware designs will likely implement a completely different set of functions or take advantage of the DSPs high level of integration for system design and avoid the use of external logic completely.

The CPLD implements simple random logic functions that eliminate the need for additional discrete devices. In particular, the CPLD aggregates the various reset signals coming from the reset button and power supervisors and generates a global reset.

The EPM3128TC100-10 is a 3.3V (5V tolerant), 100-pin QFP device that provides 128 macrocells, 80 I/O pins, and a 10 ns pin-to-pin delay. The device is EEPROM-based and is in-system programmable via a dedicated JTAG interface (a 10-pin header on the DSK). The CPLD source files are written in the industry standard VHDL (Hardware Design Language) and included with the DSK.

2.1.2 CPLD Registers

The 5 CPLD memory-mapped registers allows users to control CPLD functions in software. On the C6455 DSK the registers are primarily used to access the LEDs and DIP switches and control the daughter card interface. The registers are mapped into CE2 data space at address 0xA0000000. They appear as 8-bit registers with a simple asynchronous memory interface. The following table gives a high level overview of the CPLD registers and their bit fields:

The table below shows the bit definitions for the 5 registers in CPLD.

Table 1: CPLD Register Definitions

Offset	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	USER_REG	USR_SW3 R	USR_SW2 R	USR_SW1 R	USR_SW0 R	USR_LED3 R/W 0(Off)	USR_LED2 R/W 0(Off)	USR_LED1 R/W 0(Off)	USR_LED0 R/W 0(Off)
1	DC_REG	DC_DET R	0	DC_STAT1 R	DC_STAT0 R	DC_RST R 0(No reset)	0	DC_CNTL1 R/W 0(low)	DC_CNTL0 R/W 0(low)
4	VERSION	CPLD_VER[3.0] R				0	BOARD VERSION[2.0] R		
6	MISC	McBSP2_EN R (MCBSP2 enabled)	Spare3	Spare2	Spare1	Spare0	Resv 0	Resv 0	McBSP1 ON/OFF Board R/W 0 (Onboard)
7	MISC2	DSPA RSTST (Reset Status)	Resv 0	Resv 0	Resv 0	HUR RST EN	Ethernet PHY RST	CPUB Enable	CPUB PRSNT

2.1.3 USER_REG Register

USER_REG is used to read the state of the 4 DIP switches and turn the 4 LEDs on or off to allow the user to interact with the DSK. The DIP switches are read by reading the top 4 bits of the register and the LEDs are set by writing to the low 4 bits.

Table 2: CPLD USER_REG Register

Bit	Name	R/W	Description
7	USER_SW3	R	User DIP Switch 3(1 = Off, 0 = On)
6	USER_SW2	R	User DIP Switch 2(1 = Off, 0 = On)
5	USER_SW1	R	User DIP Switch 1(1 = Off, 0 = On)
4	USER_SW0	R	User DIP Switch 0(1 = Off, 0 = On)
3	USER_LED3	R/W	User-defined LED 3 Control (0 = Off, 1 = On)
2	USER_LED2	R/W	User-defined LED 2 Control (0 = Off, 1 = On)
1	USER_LED1	R/W	User-defined LED 1 Control (0 = Off, 1 = On)
0	USER_LED0	R/W	User-defined LED 0 Control (0 = Off, 1 = On)

2.1.4 DC_REG Register

DC_REG is used to monitor and control the daughter card interface. DC_DET detects the presence of a daughter card. DC_STAT and DC_CNTL provide simple communications with the daughter card through readable status lines and writable control lines.

The daughter card is released from reset when the DSP is released from reset. DC_RST can be used to put the card back in reset.

Table 3: DC_REG Register

Bit	Name	R/W	Description
7	DC_DET	R	Daughter Card Detect (1= Board detected)
6	0	R	Always 0
5	DC_STAT1	R	Daughter Card Status 1 (0=Low, 1 = High)
4	DC_STAT0	R	Daughter Card Status 0 (0=Low, 1 = High)
3	DC_RST	R/W	Daughter Card Reset (0=No Reset, 1 = Reset)
2	0	R	Always zero
1	DC_CNTL1	R/W	Daughter Card Control 1(0 = Low, 1 = High)
0	DC_CNTL0	R/W	Daughter Card Control 0(0 = Low, 1 = High)

2.1.5 VERSION Register

The VERSION register contains two read only fields that indicate the BOARD and CPLD versions. This register will allow your software to differentiate between production releases of the DSK and account for any variances. This register is not expected to change often, if at all.

Table 4: Version Register Bit Definitions

Bit #	Name	R/W	Description
7	CPLD_VER3	R	Most Significant CPLD Version Bit
6	CPLD_VER2	R	CPLD Version Bit
5	CPLD_VER1	R	CPLD Version Bit
4	CPLD_VER0	R	Least Significant CPLD Version Bit
3	0	R	Always 0
2	DSK_VER2	R	Most Significant DSK Board Version Bit
1	DSK_VER1	R	DSK Board Version Bit
0	DSK_VER0	R	Least Significant DSK Board Version Bit

2.1.6 MISC Register

The MISC register is used to provide software control for miscellaneous board functions. On the C6455 DSK, the MISC register controls how auxiliary signals are brought out to the daughter-card connectors.

McBSP1 is usually used as the control and data port of the on-board AIC23 codec. The power-on state of this bit (0) represents that configuration. Set MCBSP0SEL to route the McBSP1 to the daughter card connectors rather than the codec.

The scratch bits are unused. They can be set to any value.

Table 5: MISC Register

Bit	Name	R/W	Description
7	Reserved	R	
6	Spare3	R	Spare switch
5	Spare2	R	Spare switch
4	Spare1	R	Spare switch
3	Spare0	R	Spare switch
2	Reserved	R	
1	Reserved	R	
0	MCBSP1SEL	R/W	McBSP1 on/off board (0 = on-board, 1 = off-board)

2.1.7 MISC2 Register

MISC2 register is used for factory test and EVM functions when a C64xx AMCC mezzanine card is used.

This register also contains a bit for resetting the on board PHY.

Bits 0 and 1 are used for EVM configurations. Bit 0 is used to detect that a mezzanine card is plugged into the AMCC slot which is not populated on a DSK. Bit 1 enables the AMCC mezzanine card. When driven to a zero the AMCC card is enabled.

Bit 3 provides a mechanism to reset the ethernet PHY. Writing as 1 resets the on board ethernet PHY.

Bits 4 and 7 are used for factory tests, and the remaining bits are reserved for future use.

Table 6: MISC2 Register

Bit	Name	R/W	Description
7	DSPA RSTST	W	DSP A Reset Status (0 = Not in reset, 1 = In Reset), Factory Test
6	Reserved	R	Not Used
5	Reserved	R	Not Used
4	Reserved	R	Not Used
3	Reserved	R	User-defined LED 3 Control (0 = Off, 1 = On)
2	Ethernet PHY RST	R/W	Ethernet PHY reset Enable (0 = Not Reset, 1 = Reset)
1	CPUB Enable	W	CPU B Reset (0 = Not Reset, 1 = Reset)
0	CPUB PRSNT	R	CPU B Present (0 = Not present, 1 = Present)

2.2 AIC23 Codec

The DSK uses a Texas Instruments AIC23 (part #TLV320AIC23) stereo codec for input and output of audio signals. The codec samples analog signals on the microphone or line inputs and converts them into digital data so it can be processed by the DSP. When the DSP is finished with the data it uses the codec to convert the samples back into analog signals on the line and headphone outputs so the user can hear the output.

The codec communicates using two serial channels, one to control the codec's internal configuration registers and one to send and receive digital audio samples. The C6455's I^2C interface is used as the unidirectional control channel. The control channel is only used when configuring the codec, it is generally idle when audio data is being transmitted,

McBSP1 is used as the bi-directional data channel. All audio data flows through the data channel. Many data formats are supported based on the three variables of sample width, clock signal source and serial data format. The DSK examples generally use a 55-bit sample width with the codec in master mode so it generates the frame sync and bit clocks at the correct sample rate without effort on the DSP side. The preferred serial format is DSP mode which is designed specifically to operate with the McBSP ports on TI DSPs.

The codec has a 12MHz system clock. The 12MHz system clock corresponds to USB sample rate mode, named because many USB systems use a 12MHz clock and can use the same clock for both the codec and USB controller. The internal sample rate generate subdivides the 12MHz clock to generate common frequencies such as 48KHz, 44.1KHz and 8KHz. The sample rate is set by the codec's SAMPLERATE register. The figure below shows the codec interface on the C6455 DSK.

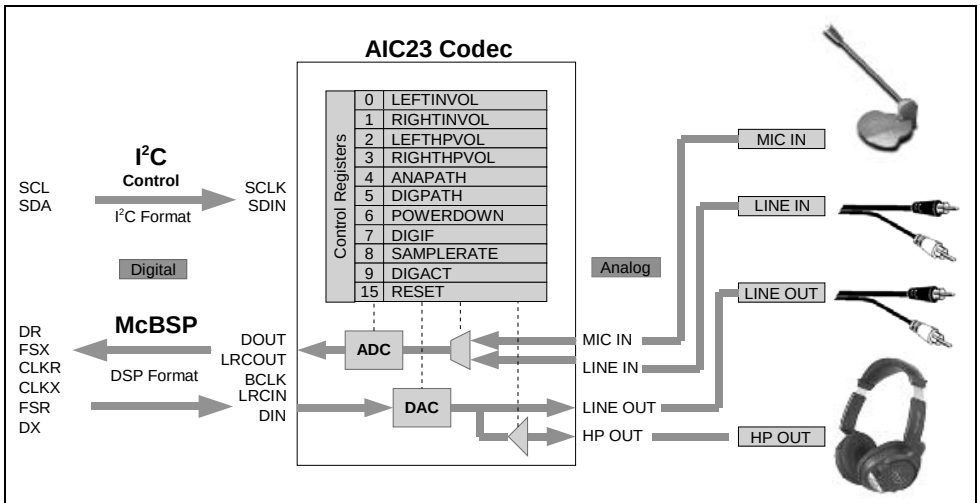


Figure 2-1, TMS320C6455 DSK CODEC INTERFACE

2.3 DDR2 Memory

The DSK uses a pair of industry standard 512 megabit DDR2 in CE0. The two devices are used in parallel to create a 32-bit wide interface. Total available memory is 128 megabytes, and is accessible from addresses 0xE0000 0000 to 0xE800 0000.

The DSK uses a factory setting DDR2 clock at 250 MHz. The integrated DDR2 controller is started by configuring the EMIF in software. Timings can be found in the DDR2 data sheet and the DSK help file.

2.4 Flash Memory

The DSK uses a 4 Mbyte external Flash as a boot option. It is connected to CE3 of EMIFA with an 8-bit interface, and is accessible from addresses 0xB0000 0000 to 0xB01F FFFF. Flash is a type of memory which does not lose its contents when the power is turned off. When read it looks like a simple asynchronous read-only memory (ROM). Flash can be erased in large blocks commonly referred to as sectors or pages. Once a block has been erased each word can be programmed once through a special command sequence. After that the entire block must be erased again to change the contents.

2.5 LEDs and DIP Switches

The DSK includes 4 software accessible LEDs (D7-D10) and DIP switches (SW1) that provide the user a simple form of input/output. Both are accessed through the CPLD USER_REG register.

2.6 Ethernet Interface

An Intel LTX971ACE 10/100 Mbps PHY is connected to the DSP's internal EMAC controller. There are 2 status LEDs which detail the status of the ethernet link.

2.7 I^2C ROM

The DSK incorporates a 1 Mbit I^2C ROM. The ROM can be used for general storage or configured as a boot device for the DSP.

2.8 Daughter Card Interface

The DSK provides three expansion connectors that can be used to accept plug-in daughter cards. The daughter card allows users to build on their DSK platform to extend its capabilities and provide customer and application specific I/O. The expansion connectors are for memory, peripherals, and the Host Port Interface (HPI)

The memory connector provides access to the DSP's asynchronous EMIF signals to interface with memories and memory mapped devices. It supports byte addressing on 32 bit boundaries. The peripheral connector brings out the DSP's peripheral signals like McBSPs, timers, and clocks. Both connectors provide power and ground to the daughter card.

The HPI is a high speed interface that can be used to allow multiple DSPs to communicate and cooperate on a given task. The HPI connector brings out the HPI specific control signals as well as a PCI multiplexed interface.

Most of the expansion connector signals are buffered so that the daughter card cannot directly influence the operation of the DSK board. The use of TI low voltage, 5V tolerant buffers, and CBT interface devices allows the use of either +5V or +3.3V devices to be used on the daughter card.

Other than the buffering, most daughter card signals are not modified on the board. However, a few daughter card specific control signals like DC_RESET and DC_DET exist and are accessible through the CPLD DC_REG register. The DSK also multiplexes the McBSP1 for on board or external use. This function is controlled through the CPLD MISC register.

2.9 DSP and EMIFA Clock Generation

The C6455 DSK uses the internal DSP divides to select the user PLL frequency, and multiple oscillators. This allows the DSK to support 600, 725, 850, 1000, and 1200 megahertz CPU clocks. However, the default configuration is 1 gigahertz and the software shipped with the DSK assumes the default configuration.

2.10 JTAG Interfaces

The DSK supports embedded emulation controller as its primary debug channel. However it has an option to support 14 pin and 60 pin TI style JTAG connections for external emulators. When either the 14 pin or 60 pin interface is plugged into the DSK the on board embedded emulator is disabled. The 60 pin interface also supports trace functions when used with the appropriate trace emulation platform.

Chapter 3

Physical Description

This chapter describes the physical layout of the TMS320C6455 DSK and its connectors.

Topic **Page**

3.1	Board Layout	3-2
3.2	Connector Index	3-3
3.3	Expansion Connectors	3-3
3.3.1	J4, Memory Expansion Connector	3-4
3.3.2	J3, Peripheral Expansion Connector	3-5
3.3.3	J1, PCI Expansion Connector	3-6
3.3.4	J1, Used as HPI Expansion Connector	3-6
3.4	Audio Connectors	3-8
3.4.1	J1301, Microphone Connector	3-8
3.4.2	J1303, Audio Line In Connector	3-8
3.4.3	J1304, Audio Line Out Connector	3-9
3.4.4	J1302, Headphone Connector	3-9
3.5	Power Connectors	3-10
3.5.1	J5, +5 Volt Connector	3-10
3.5.2	J6, Optional Power Connector	3-10
3.6	Miscellaneous Connectors	3-11
3.6.1	J1201, USB Connector	3-11
3.6.2	J8, 14 Pin External JTAG Connector	3-12
3.6.3	J7, 60 Pin Advanced Emulation Connector	3-13
3.6.4	JP3, PLD Programming Connector	3-13
3.6.5	J9, AMCC Connector	3-13
3.6.6	P1102, Ethernet Connector	3-14
3.7	System LEDs	3-14
3.8	SW2, Reset Switch	3-14

3.1 Board Layout

The C6455 DSK is a 10.0 x 4.5 inch (254 x 115 mm.) multi-layer board which is powered by an external +5 volt only power supply. Figure 3-1 shows the layout of the C6455 DSK.

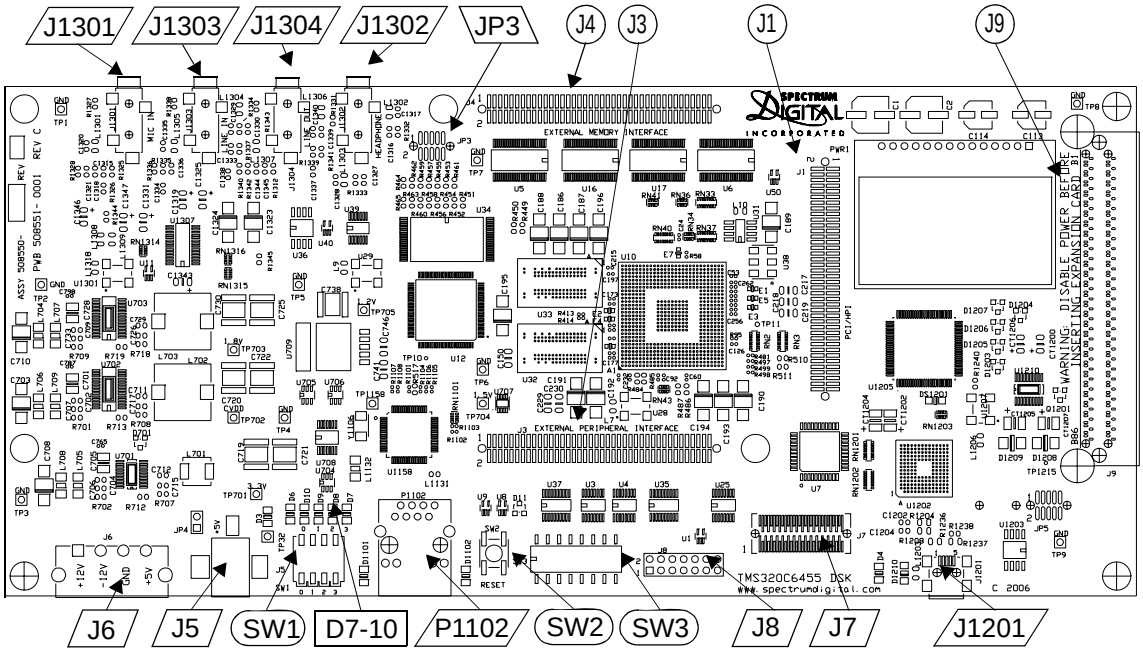


Figure 3-1, TMS320C6455 DSK

3.2 Connector Index

The TMS320C6455 DSK has many connectors which provide the user access to the various signals on the DSK.

Table 1: TMS320C6455 DSK Connectors

Connector	# Pins	Function
J4	80	Memory
J3	80	Peripheral
J1	80	HPI
J1301	3	Microphone
J1303	3	Line In
J1304	3	Line Out
J1302	3	Headphone
J5	2	+5 Volt
J6 *	4	Optional Power Connector
J7	80	Enhanced JTAG Connector
J8	14	External JTAG
J1201	5	USB Port
JP3	4	CPLD Programming
P1102	8	Ethernet
SW3	8	DSP Configuration Switch

Note: "*****" Not populated

3.3 Expansion Connectors

The TMS320C6455 DSK supports three expansion connectors that follow the Texas Instruments interconnection guidelines. The expansion connector pinouts are described in the following three sections.

The three expansion connectors are all 80 pin 0.050 x 0.050 inches low profile connectors from Samtec or AMP. The Samtec SFM Series (surface mount) connectors are designed for high speed interconnections because they have low propagation delay, capacitance, and cross talk. The connectors present a small foot print on the DSK. Each connector includes multiple ground, +5V, and +3.3V power signals so that the daughter card can obtain power directly from the DSK. The peripheral expansion connector additionally provides both +12V and -12V to the daughter card. The recommended mating connector, whose part number is TFM-140-32-S-D-LC, is a surface mount connector that provides a 0.465" mated height.

Note: I is on an Input pin
O is on an Output pin
Z is on a High Impedance pin

3.3.1 J4, Memory Expansion Connector

Table 2: J4, Memory Expansion Connector

Pin	Signal	I/O	Description	Pin	Signal	I/O	Description
1	5V	Vcc	5V voltage supply pin	2	5V	Vcc	5V voltage supply pin
3	AEA19	O	EMIF address pin 21	4	AEA18	O	EMIF address pin 20
5	AEA17	O	EMIF address pin 19	6	AEA16	O	EMIF address pin 18
7	AEA15	O	EMIF address pin 17	8	AEA14	O	EMIF address pin 16
9	AEA13	O	EMIF address pin 15	10	AEA12	O	EMIF address pin 14
11	GND	Vss	System ground	12	GND	Vss	System ground
13	AEA11	O	EMIF address pin 13	14	AEA10	O	EMIF address pin 12
15	AEA9	O	EMIF address pin 11	16	AEA8	O	EMIF address pin 10
17	AEA7	O	EMIF address pin 9	18	AEA6	O	EMIF address pin 8
19	AEA5	O	EMIF address pin 7	20	AEA4	O	EMIF address pin 6
21	5V	Vcc	5V voltage supply pin	22	5V	Vcc	5V voltage supply pin
23	AEA3	O	EMIF address pin 5	24	AEA2	O	EMIF address pin 4
25	AEA1	O	EMIF address pin 3	26	AEA0	O	EMIF address pin 2
27	ABE3#	O	EMIF byte enable 3	28	ABE2#	O	EMIF byte enable 2
29	ABE1#	O	EMIF byte enable 1	30	ABE0#	O	EMIF byte enable 0
31	GND	Vss	System ground	32	GND	Vss	System ground
33	AED31	I/O	EMIF data pin 31	34	AED30	I/O	EMIF data pin 30
35	AED29	I/O	EMIF data pin 29	36	AED28	I/O	EMIF data pin 28
37	AED27	I/O	EMIF data pin 27	38	AED26	I/O	EMIF data pin 26
39	AED25	I/O	EMIF data pin 25	40	AED24	I/O	EMIF data pin 24
41	3.3V	Vcc	3.3V voltage supply pin	42	3.3V	Vcc	3.3V voltage supply pin
43	AED23	I/O	EMIF data pin 23	44	AED22	I/O	EMIF data pin 22
45	AED21	I/O	EMIF data pin 21	46	AED20	I/O	EMIF data pin 20
47	AED19	I/O	EMIF data pin 19	48	AED18	I/O	EMIF data pin 18
49	AED17	I/O	EMIF data pin 17	50	AED16	I/O	EMIF data pin 16
51	GND	Vss	System ground	52	GND	Vss	System ground
53	AED15	I/O	EMIF data pin 15	54	AED14	I/O	EMIF data pin 14
55	AED13	I/O	EMIF data pin 13	56	AED12	I/O	EMIF data pin 12
57	AED11	I/O	EMIF data pin 11	58	AED10	I/O	EMIF data pin 10
59	AED9	I/O	EMIF data pin 9	60	AED8	I/O	EMIF data pin 8
61	GND	Vss	System ground	62	GND	Vss	System ground
63	AED7	I/O	EMIF data pin 7	64	AED6	I/O	EMIF data pin 6
65	AED5	I/O	EMIF data pin 5	66	AED4	I/O	EMIF data pin 4
67	AED3	I/O	EMIF data pin 3	68	AED2	I/O	EMIF data pin 2
69	AED1	I/O	EMIF data pin 1	70	AED0	I/O	EMIF data pin 0
71	GND	Vss	System ground	72	GND	Vss	System ground
73	AARE#	O	EMIF async read enable	74	AAWE#	O	EMIF async write enable
75	AAOE#	O	EMIF async output enable	76	AARDY	I	EMIF asynchronous ready
77	ACE3#	O	Chip enable 3	78	ACE2#	O	Chip enable 2
79	GND	Vss	System ground	80	GND	Vss	System ground

3.3.2 J3, Peripheral Expansion Connector

Table 3: J3, Peripheral Expansion Connector

Pin	Signal	I/O	Description	Pin	Signal	I/O	Description
1	12V	Vcc	12V voltage supply pin	2	-12V	Vcc	-12V voltage supply pin
3	GND	Vss	System ground	4	GND	Vss	System ground
5	5V	Vcc	5V voltage supply pin	6	5V	Vcc	5V voltage supply pin
7	GND	Vss	System ground	8	GND	Vss	System ground
9	5V	Vcc	5V voltage supply pin	10	5V	Vcc	5V voltage supply pin
11	N/C	-	No connect	12	N/C	-	No connect
13	N/C	-	No connect	14	N/C	-	No connect
15	N/C	-	No connect	16	N/C	-	No connect
17	N/C	-	No connect	18	N/C	-	No connect
19	3.3V	Vcc	3.3V voltage supply pin	20	3.3V	Vcc	3.3V voltage supply pin
21	CLKX0	I/O	McBSP0 transmit clock	22	CLKS0	I	McBSP0 clock source
23	FSX0	I/O	McBSP0 transmit frame sync	24	DX0	O	McBSP0 transmit data
25	GND	Vss	System ground	26	GND	Vss	System ground
27	CLKR0	I/O	McBSP0 receive clock	28	N/C	-	No connect
29	FSR0	I/O	McBSP0 receive frame sync	30	DR0	I	McBSP0 receive data
31	GND	Vss	System ground	32	GND	Vss	System ground
33	CLKX2	I/O	McBSP2 transmit clock	34	CLKS2	I	McBSP2 clock source
35	FSX2	I/O	McBSP2 transmit frame sync	36	DX2	O	McBSP2 transmit data
37	GND	Vss	System ground	38	GND	Vss	System ground
39	CLKR2	I/O	McBSP2 receive clock	40	N/C	-	No connect
41	FSR2	I/O	McBSP2 receive frame sync	42	DR2	I	McBSP2 receive data
43	GND	Vss	System ground	44	GND	Vss	System ground
45	TOUT0	O	Timer 0 output	46	TINP0	I	Timer 0 input
47	N/C	-	No connect	48	EXT_INT5	I	External interrupt 5
49	TOUT1	O	Timer 1 output	50	TINP1	I	Timer 1 input
51	GND	Vss	System ground	52	GND	Vss	System ground
53	EXT_INT4	I	External interrupt 4	54	N/C	-	No connect
55	N/C	-	No connect	56	N/C	-	No connect
57	N/C	-	No connect	58	N/C	-	No connect
59	RESET	O	System reset	60	N/C	-	No connect
61	GND	Vss	System ground	62	GND	Vss	System ground
63	CNTL1	O	Daughtercard control 1	64	CNTL0	O	Daughtercard control
65	STAT1	I	Daughtercard status 1	66	STAT0	I	Daughtercard status
67	EXT_INT6	I	External interrupt 6	68	EXT_INT7	I	External interrupt 7
69	ACE3#	O	Chip enable 3	70	N/C	-	No connect
71	N/C	-	No connect	72	N/C	-	No connect
73	N/C	-	No connect	74	N/C	-	No connect
75	DC_DET#	Vss	System ground	76	GND	Vss	System ground
77	GND	Vss	System ground	78	ECL KOUT	O	EMIF Clock
79	GND	Vss	System ground	80	GND	Vss	System ground

3.3.3 J1, PCI Expansion Connector

Table 4: J1, PCI Expansion Connector

Pin	Signal	I/O	Description	Pin	Signal	I/O	Description
1	PCI_EN	I	PCI enable	2	Resv	N/C	Resv
3	GND	Vss	System ground	4	HPI_RS#	I	HPI reset
5	Resv	N/C	Resv	6	Resv	N/C	Resv
7	GND	Vss	System ground	8	GND	Vss	System ground
9	AD1	I/O	PCI address/data 1	10	GP[2]	I/O	General purpose I/O
11	AD3	I/O	PCI address/data 3	12	AD0	I/O	PCI address/data 0
13	AD5	I/O	PCI address/data 5	14	AD2	I/O	PCI address/data 2
15	AD7	I/O	PCI address/data 7	16	AD4	I/O	PCI address/data 4
17	GND		System ground	18	AD6	I/O	PCI address/data 6
19	AD8	I/O	PCI address/data 8	20	GND	Vss	System ground
21	AD10	I/O	PCI address/data 10	22	AD9	I/O	PCI address/data 9
23	AD12	I/O	PCI address/data 12	24	AD11	I/O	PCI address/data 11
25	AD14	I/O	PCI address/data 14	26	AD13	I/O	PCI address/data 13
27	GND	Vss	System ground	28	AD15	I/O	PCI address/data 15
29	PCBE1#	I/O	PCI command/byte ena 1	30	GND	Vss	System ground
31	GND	Vss	System ground	32	PPAR	I/O	PCI parity
33	PSERR#	I/O	PCI system error	34	GND	Vss	System ground
35	GND	Vss	System ground	36	PSTOP#	I/O	PCI stop
37	PPERR#	I/O	PCI parity error	38	GND	Vss	System ground
39	GND	Vss	System ground	40	Resv		None
41	PDEVSEL#	I/O	PCI device select	42	GND	Vss	System ground
43	GND	Vss	System ground	44	PFRAME#	I/O	PCI Frame
45	PIRDY#	I/O	PCI initiator ready	46	GND	Vss	System ground
47	GND	Vss	System ground	48	AD16	I/O	PCI address/data 16
49	PCBE2#	I/O	PCI command/byte ena 2	50	AD18	I/O	PCI address/data 18
51	AD17	I/O	PCI address/data 17	52	AD20	I/O	PCI address/data 20
53	AD19	I/O	PCI address/data 19	54	AD22	I/O	PCI address/data 22
55	AD21	I/O	PCI address/data 21	56	GND	Vss	System ground
57	AD23	I/O	PCI address/data 23	58	Resv		None
59	Resv		None	60	AD24	I/O	PCI address/data 24
61	GND	Vss	System ground	62	AD26	I/O	PCI address/data 26
63	AD25	I/O	PCI address/data 25	64	AD28	I/O	PCI address/data 28
65	AD27	I/O	PCI address/data 27	66	AD30	I/O	PCI address/data 30
67	AD29	I/O	PCI address/data 29	68	GP[12]	I/O	General purpose I/O
69	AD31	I/O	PCI address/data 31	70	GND	Vss	System ground
71	GND	Vss	System ground	72	GP[13]	I/O	General purpose I/O
73	GP[15]	I/O	General purpose I/O	74	GND	Vss	System ground
75	GND	Vss	System ground	76	GP[14]	I/O	General purpose I/O
77	PCLK	I	PCI Clock	78	GND	Vss	System ground
79	GND	Vss	System ground	80	N/C	-	No connect

3.3.4 J1, Used As HPI Expansion Connector

Table 5: J1, Used as HPI Expansion Connector

Pin	Signal	I/O	Description	Pin	Signal	I/O	Description
1	PCI_EN	I	PCI enable	2	Resv	N/C	Resv
3	GND	Vss	System ground	4	HPI_RS#	I	HPI reset
5	Resv	N/C	Resv	6	Resv	N/C	Resv
7	GND	Vss	System ground	8	GND	Vss	System ground
9	HD1	I/O	Host data 1	10	PCBE0#	I/O	PCI command/byte ena 0
11	HD3	I/O	Host data 3	12	HD0	I/O	Host data 0
13	HD5	I/O	Host data 5	14	HD2	I/O	Host data 2
15	HD7	I/O	Host data 7	16	HD4	I/O	Host data 4
17	GND		System ground	18	HD6	I/O	Host data 6
19	HD8	I/O	Host data 8	20	GND	Vss	System ground
21	HD10	I/O	Host data 10	22	HD9	I/O	Host data 9
23	HD12	I/O	Host data 12	24	HD11	I/O	Host data 11
25	HD14	I/O	Host data 14	26	HD13	I/O	Host data 13
27	GND	Vss	System ground	28	HD15	I/O	Host data 15
29	HDS2#	I/O	Host data strobe 2	30	GND	Vss	System ground
31	GND	Vss	System ground	32	HAS#	I/O	Host address strobe
33	HDS1#	I/O	Host data strobe 1	34	GND	Vss	System ground
35	GND	Vss	System ground	36	HCNTL0	I/O	Host Control 0
37	HCS#	I/O	Host chip select	38	GND	Vss	System ground
39	GND	Vss	System ground	40	PTRDY#	I/O	PCI target ready
41	HCNTL1	I/O	Host Control 1	42	GND	Vss	System ground
43	GND	Vss	System ground	44	HINT#	I/O	Host Interrupt
45	HRDY#	I/O	Host ready	46	GND	Vss	System ground
47	GND	Vss	System ground	48	HD16	I/O	Host data 16
49	HR/W#	I/O	Host Read/Write	50	HD18	I/O	Host data 18
51	HD17	I/O	Host data 17	52	HD20	I/O	Host data 20
53	HD19	I/O	Host data 19	54	HD22	I/O	Host data 22
55	HD21	I/O	Host data 21	56	GND	Vss	System ground
57	HD23	I/O	Host data 23	58	Resv		Resv
59	Resv		Resv	60	HD24	I/O	Host data 24
61	GND	Vss	System ground	62	HD26	I/O	Host data 26
63	HD25	I/O	Host data 25	64	HD28	I/O	Host data 28
65	HD27	I/O	Host data 27	66	HD30	I/O	Host data 30
67	HD29	I/O	Host data 29	68	PGNT#	I	PCI bus grant
69	HD31	I/O	Host data 31	70	GND	Vss	System ground
71	GND	Vss	System ground	72	Resv		Resv
73	Resv		Resv	74	GND	Vss	System ground
75	GND	Vss	System ground	76	Resv		Resv
77	Resv		Resv	78	GND	Vss	System ground
79	GND	Vss	System ground	80	N/C	-	No connect

3.4 Audio Connectors

The C6455 DSK has 4 audio connectors. They are described in the following sections.

3.4.1 J1301, Microphone Connector

The input is a 3.5 mm. stereo jack. Both inputs are connected to the microphone so it is monaural. The signals on the plug are shown in the figure below.

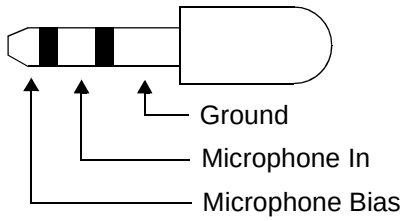


Figure 3-2, Microphone Stereo Jack

3.4.2 J1303, Audio Line In Connector

The audio line in is a stereo input. The input connector is a 3.5 mm stereo jack. The signals on the mating plug are shown in the figure below.

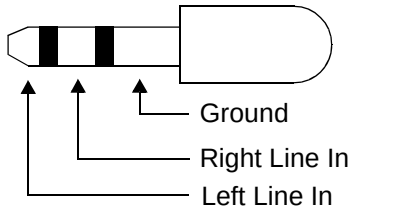


Figure 3-3, Audio Line In Stereo Jack

3.4.3 J1304, Audio Line Out Connector

The audio line out is a stereo output. The output connector is a 3.5 mm stereo jack. The signals on the mating plug are shown in the figure below.

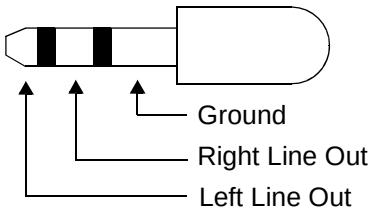


Figure 3-4, Audio Line Out Stereo Jack

3.4.4 J1302, Headphone Connector

Connector J1302 is a headphone/speaker jack. It can drive standard headphones or a high impedance speaker directly. The standard 3.5 mm jack is shown in the figure below.

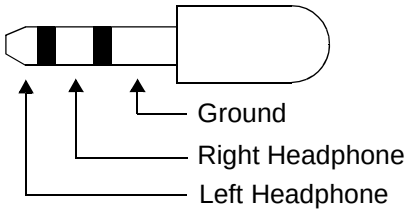


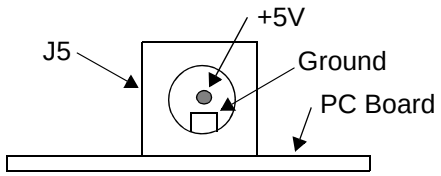
Figure 3-5, Headphone Jack

3.5 Power Connectors

The C6455 DSK has 2 power connectors. They are described in the following sections.

3.5.1 J5, +5 Volt Connector

Power (+5 volts) is brought onto the TMS320C6455 DSK via connector J5. The connector has an outside diameter of 5.5 mm. and an inside diameter of 2.5 mm. The A diagram of J5 is shown below.



Front View

Figure 3-6, TMS320C6455 DSK Power Connector

3.5.2 J6, Optional Power Connector

Connector J6 is an optional power connector. It will operate with the standard personal computer power supply. To populate this connector use a Molex #15109-0410 or Tyco #174552-1. The table below shows the voltages on the respective pins.

Table 6: J6, Optional Power Connector

Pin #	Voltage Level
1	+12 Volts
2	-12 Volts
3	Ground
4	+5 Volts

WARNING !
Do not plug into J5 and J6 at the same time.

3.6 Miscellaneous Connectors

The C6455 DSK has 6 additional connectors to aid the user in developing with this product. They are described in the following sections.

3.6.1 J1201, USB Connector

Connector J1201 provides a Universal Serial Bus (USB) Interface to the embedded JTAG emulation logic on the DSK. This allows for code development and debug without the use of an external emulator. The signals on this connector are shown in the below.

Table 7: J1201, USB Connector

Pin #	USB Signal Name
1	USBVdd
2	D+
3	D-
4	USB Vss
5	Shield
6	Shield

3.6.2 J8, 14 Pin External JTAG Connector

The TMS320C6455 DSK is supplied with a 14 pin header interface, J8. This is the standard interface used by JTAG emulators to interface to Texas Instruments DSPs. The pinout for the connector is shown figure 3-6 below.

TMS	1	2	TRST-	
TDI	3	4	GND	Header Dimensions
PD (+3.3V)	5	6	**no pin (key)**	Pin-to-Pin spacing, 0.100 in. (X,Y)
TDO	7	8	GND	Pin width, 0.025-in. square post
TCK-RET	9	10	GND	Pin length, 0.235-in. nominal
TCK	11	12	GND	
EMU0	13	14	EMU1	

Figure 3-7, JTAG INTERFACE

The signal names for each pin are shown in the table below.

Table 8: J8, JTAG Interface

Pin #	Signal Name
1	TMS
2	TRST-
3	TDI
4	GND
5	PD
6	no pin
7	TDO
8	GND
9	TCK-RET
10	GND
11	TCK
12	GND
13	EMU0
14	EMU1

3.6.3 J7, 60 Pin Advanced Emulation Connector

The 60 pin emulation connector is mounted on the side of the board near the 14 pin JTAG connector. This connector is for advanced emulation capability. The signals on this connector are 4 columns by 15 rows as shown in the table below

Table 9: J7, 60 Pin Emulation Connector

Row #	Column A Signal Name	Column B Signal Name	Column C Signal Name	Column D Signal Name
1	Ground	IDO	ID2	Ground
2	Ground	TMS	EMU18	Ground
3	Ground	EMU17	TRSTn	Ground
4	Ground	TDI	EMU16	Ground
5	Ground	EMU14	EMU15	Ground
6	Ground	EMU12	EMU13	Ground
7	Ground	TDO	EMU11	Ground
8	TYPE0	TVD	TCLKRTN	TYPE1
9	Ground	EMU9	EMU10	Ground
10	Ground	EMU7	EMU8	Ground
11	Ground	EMU5	EMU6	Ground
12	Ground	TCLK	EMU4	Ground
13	Ground	EMU2	EMU3	Ground
14	Ground	EMU0	EMU1	Ground
15	Ground	ID1	ID3	Ground

3.6.4 JP3, PLD Programming Connector

This connector interfaces to the Altera CPLD, U12. It is used in the in the factory for the programming of the CPLD. This connector is not intended to be used outside the factory.

3.6.5 J9, AMCC Connector

This connector provides a high speed Serial Rapid I/O to other platforms. This connector has 170 pins. This connector is not populated on DSK platforms.

3.6.6 P1102, Ethernet Connector

Connector P1102 is a standard RJ-45 ethernet connector. The connector pin out is shown below.

Table 10: P1102 Connector Pin Out

Pin #	Signal Name
1	TXD+
2	TXD-
3	RXD+
4	TXD-CT
5	Not Used
6	RXD-
7	NC
8	Ground

3.7 System LEDs

TheTMS320C6455 DSK has six system light emitting diodes (LEDs). These LEDs indicate various conditions on the DSK. These function of each LED is shown in the table below.

Table 11: System LEDs

Reference Designator	Color	Function	On Signal State
D4	Green	USB Emulation in use. When External JTAG Emulator is used this LED is off.	1
D3	Green	+5 Volt present	1
D6	Orange	RESET Active	1
DS201	Green	USB Active, Blinks during USB data transfer	1
DS1101	Yellow	Ethernet status	0
DS1102	Green	Ethernet Status	0

3.8 SW2, Reset Switch

There are three resets on the TMS320C6455 DSK. The first reset is the power on reset. This circuit waits until power is within the specified range before releasing the power on reset pin to the TMS320C6455.

External sources which control the reset are push button SW2, and the on board embedded USB JTAG emulator.

Appendix A

Schematics

This appendix contains the schematics for the TMS320C6455 DSK.

SCHEMATIC CONTENTS:

1 COVER SHEET
2 USER OPTIONS
3 Clock Inputs
4 645X DDR2 Interface
5 DDR2 Memories
6 645X EMIF A
7 BOOT Options
8 CPLD
9 FLASH MEMORY
10 645X MII INTERFACE

11 MCBSP INTERFACE
12 645X HOST PORT INTERFACE
13 645X SRIO INTERFACE
14 DSK DAUGHTERCARD BUFFERS
15 DSK DAUGHTERCARD INTERFACE
16 645X POWER PINS I
17 645X POWER PINS II
18 645X EMULATION
19 645X EMULATION INTERFACE

20 EMULATION INTERFACE
21 HIERARCHICAL BLOCKS
22 645X RGMII INTERFACE
23 645X DECOUPLING CAPS I
24 645X DECOUPLING CAPS II
25 POWER INPUT
26 AIC23 CODEC
27 ETHERNET PHY
28 DSK POWER SUPPLIES I
29 DSK POWER SUPPLIES II

30-34 Embedded Emulation Not Included

REVISION STATUS OF SHEETS

REV	A	A	A	A	A	A	A	A	A	
SH	21	22	23	24	25	26	27	28	29	
REV	A	A	A	A	A	A	A	A	A	A
SH	11	12	13	14	15	16	17	18	19	20
REV	C	C	A	A	A	A	A	A	A	A
SH	1	2	3	4	5	6	7	8	9	10

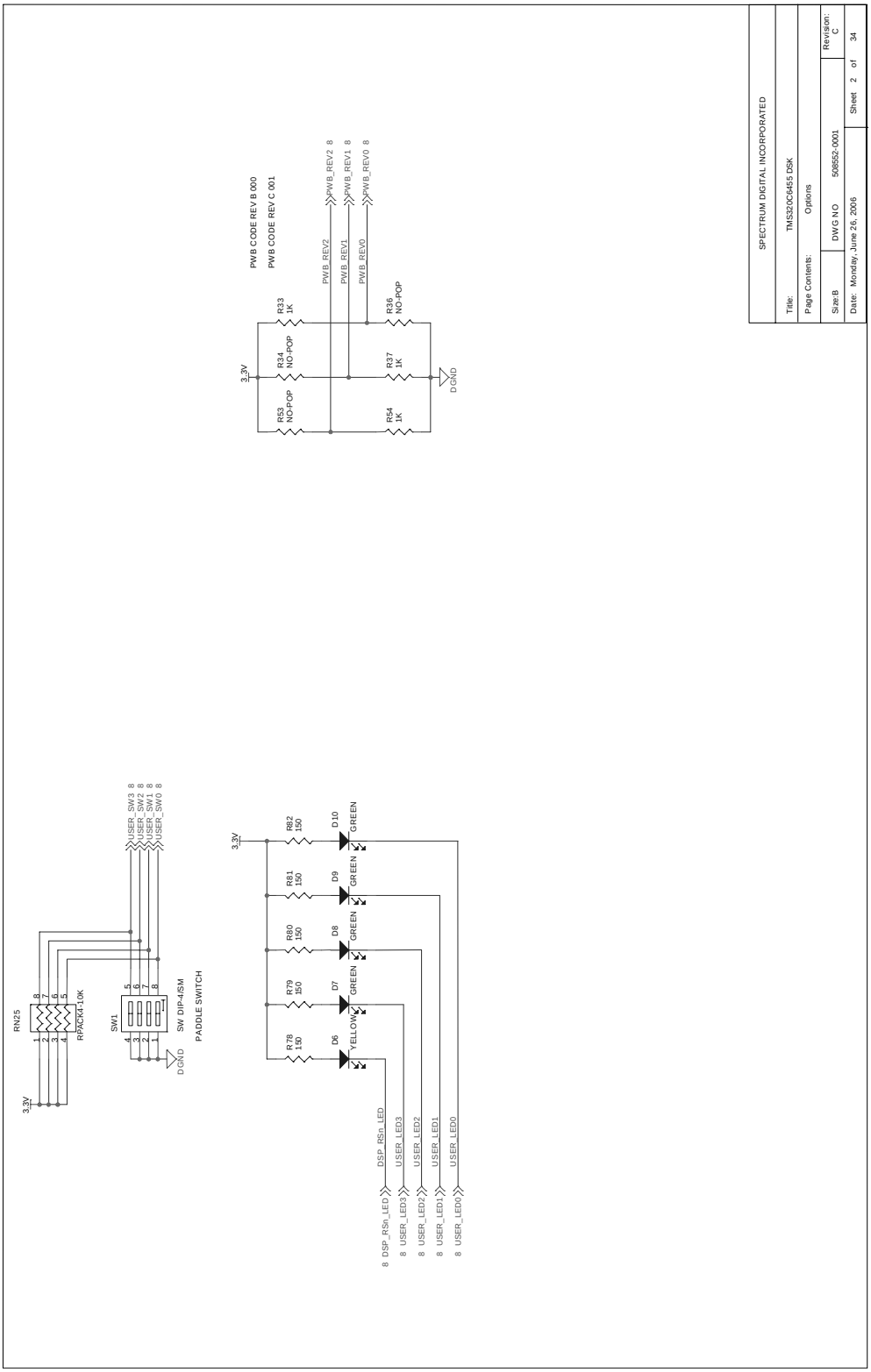
NEXT ASSY | USED ON

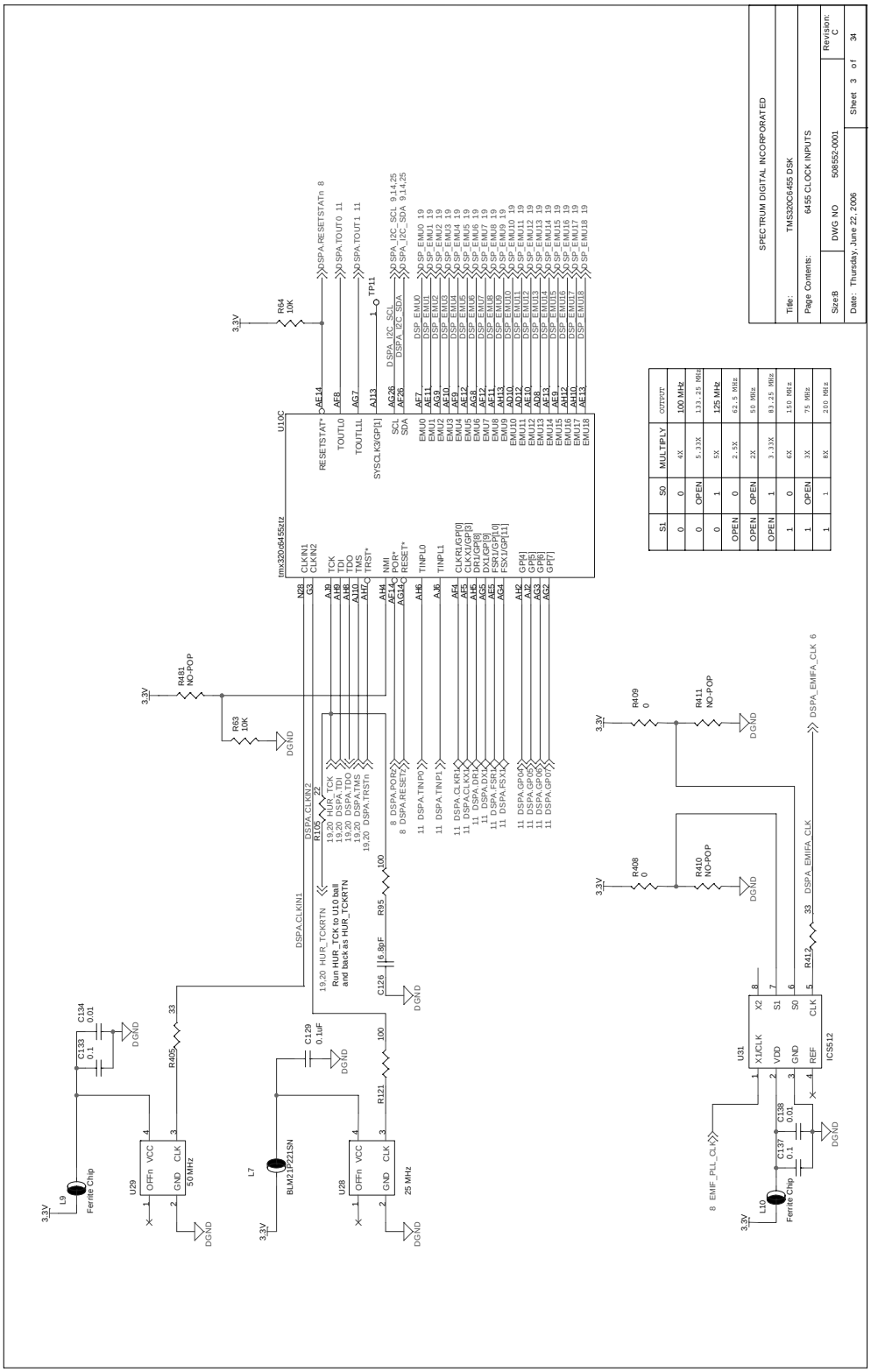
APPLICATION

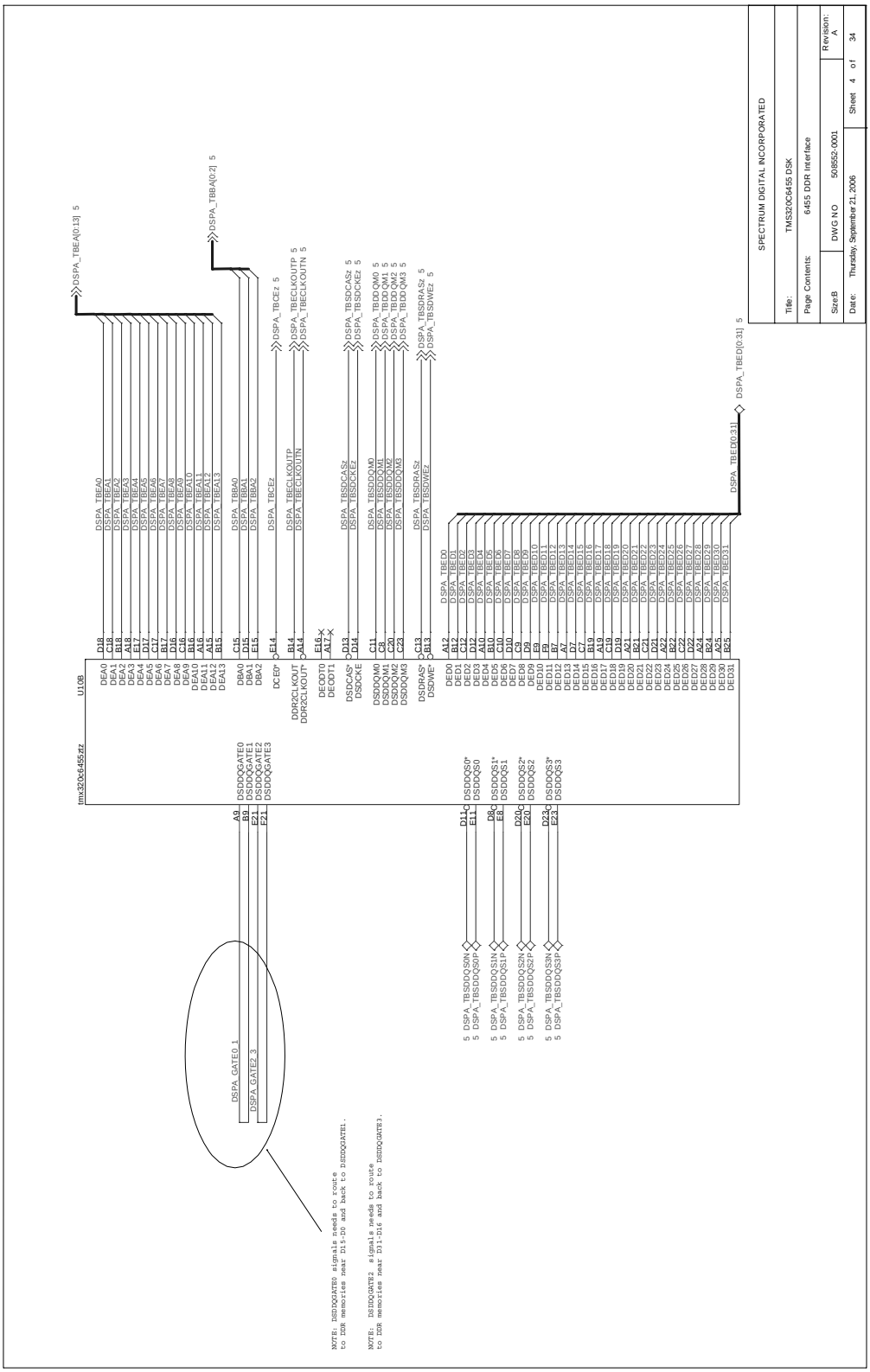
		DATE
DWN	R.R.P.	AUG 01,2005
CHK	R.R.P.	AUG 01,2005
ENGR	J.T.C.	AUG 01,2005
ENGR-MGR	R.R.P.	AUG 01,2005
QA	C.M.D.	AUG 01,2005
MFG	C.M.D.	AUG 01,2005
RLSE	T.M.K.	AUG 01,2005

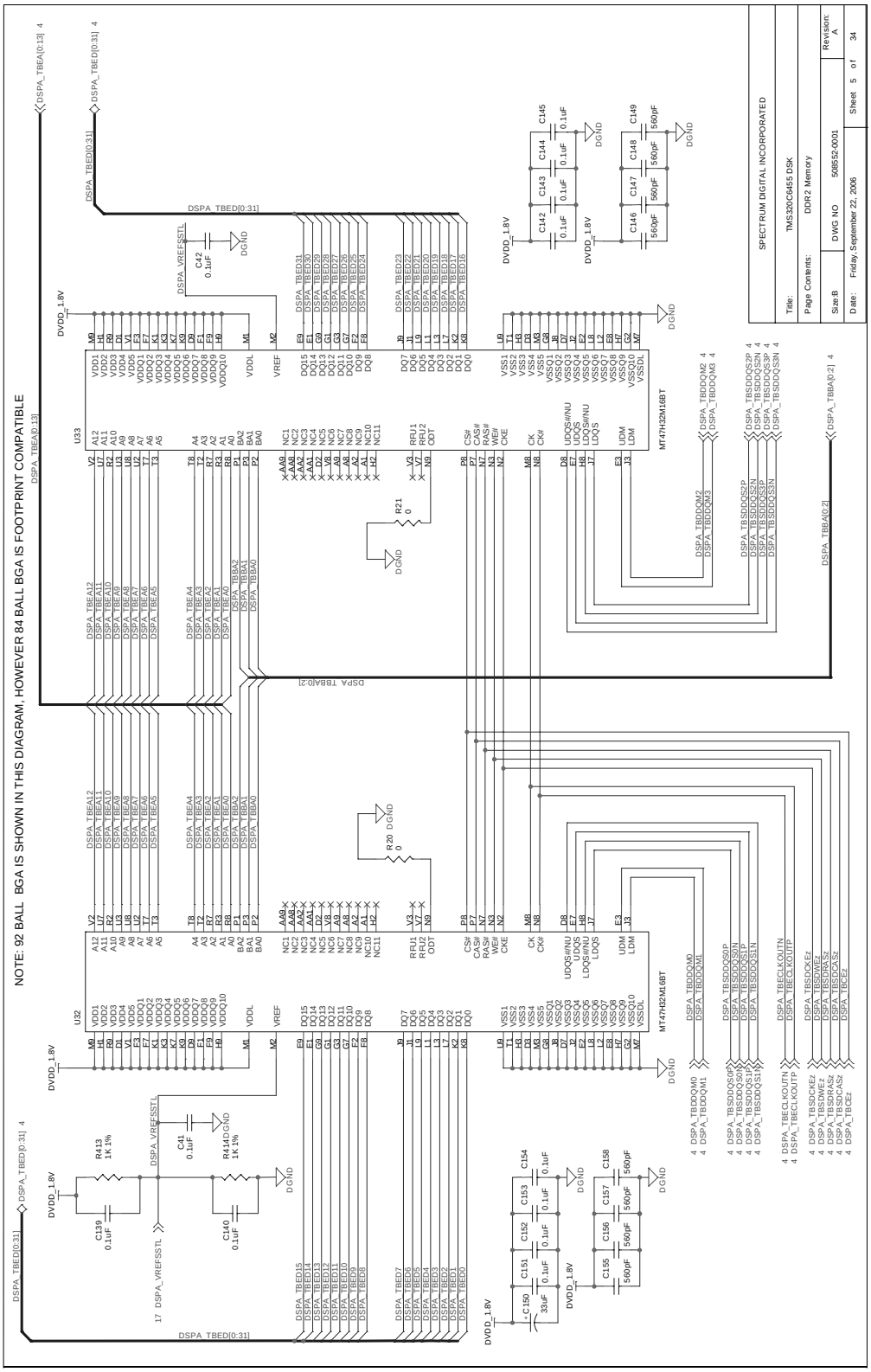
SPECTRUM DIGITAL INCORPORATED

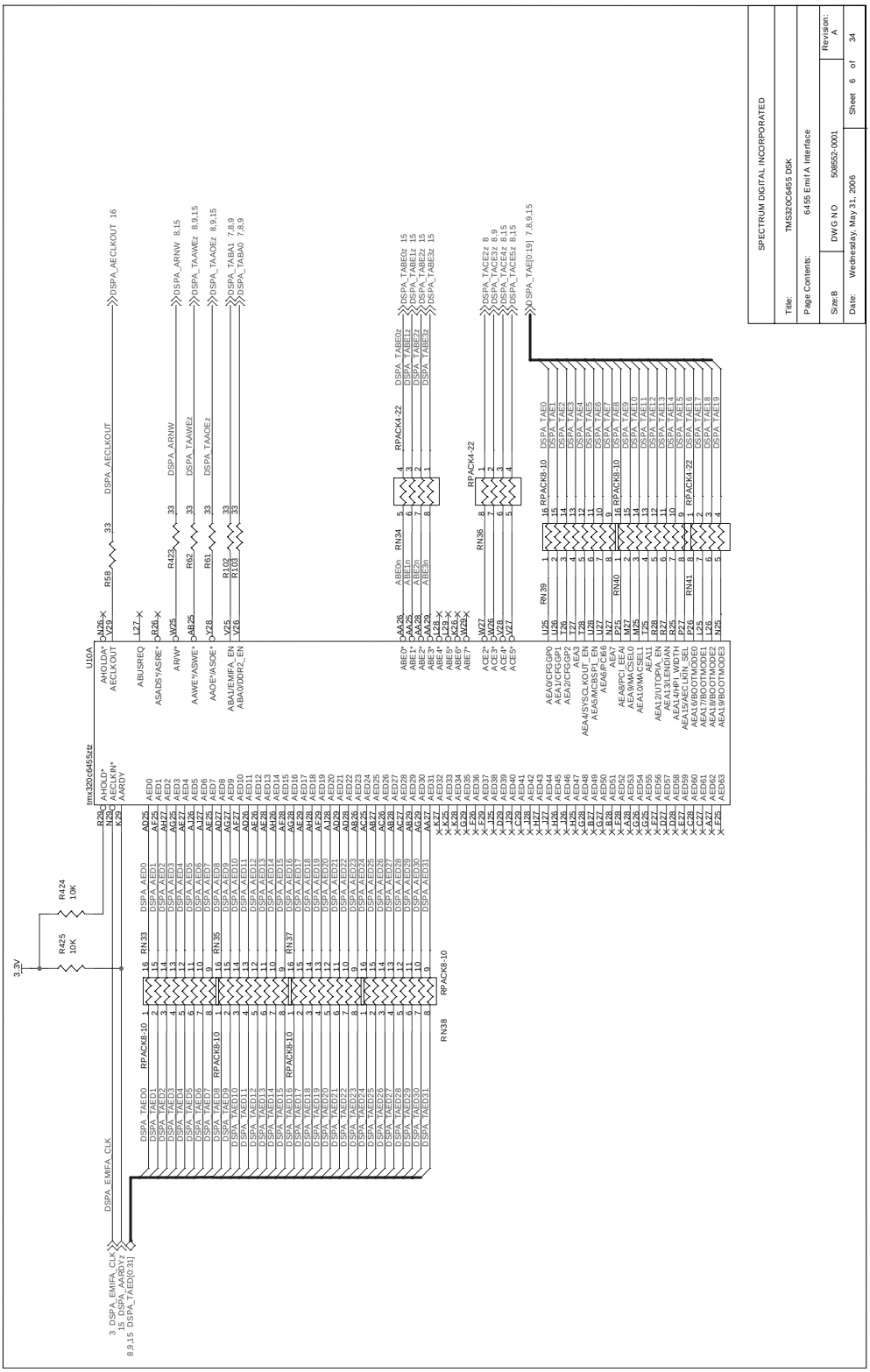
Title:	TMS320C6455 DSK	
Page Contents:	Title Block	
Size:B	DWG NO 508552-0001	Revision: C
Date: Monday, June 26, 2006	Sheet 1 of 34	

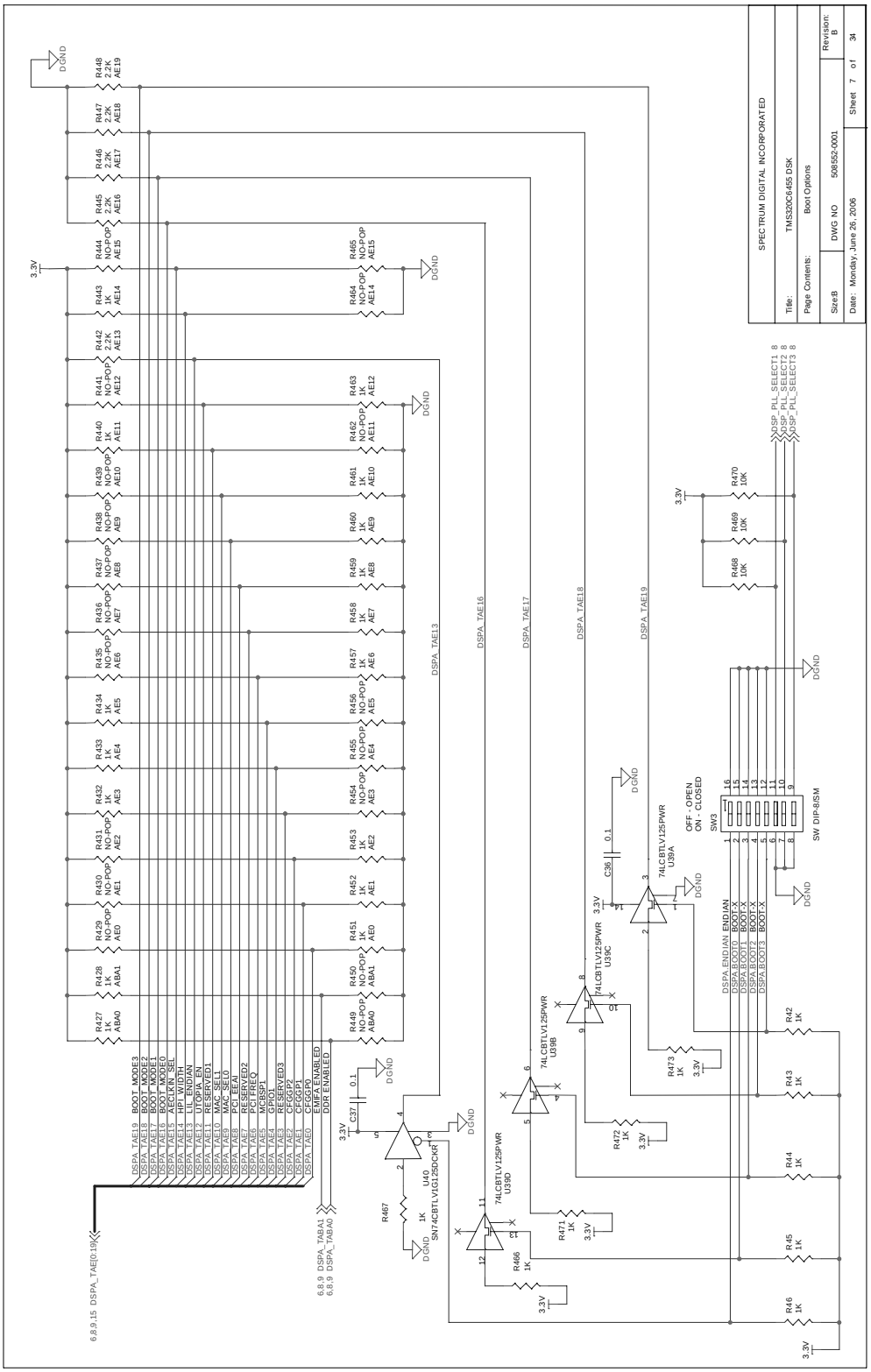

PWB CODE REV B 000
PWB CODE REV C 001
3.3V
R53 NO-POP
R34 NO-POP
R33 1K
R54 1K
R37 1K
R36 NO-POP
DGND
PWB_REV2
PWB_REV1
PWB_REV0
PWB_REV2 8
PWB_REV1 8
PWB_REV0 8
RN25
RPACK4-10K
SW1
SW DIP-4/SM
PADDLE SWITCH
USER_SW3 8
USER_SW2 8
USER_SW1 8
USER_SW0 8
R78 150
R79 150
R80 150
R81 150
R82 150
D6 YELLOW
D7 GREEN
D8 GREEN
D9 GREEN
D10 GREEN
DSP_RSn_LED
USER_LED3
USER_LED2
USER_LED1
USER_LED0
8 DSP_RSn_LED
8 USER_LED3
8 USER_LED2
8 USER_LED1
8 USER_LED0
SPECTRUM DIGITAL INCORPORATED
Title: TMS320C6455 DSK
Page Contents: Options
Size:B DWG NO 508552-0001 Revision: C
Date: Monday, June 26, 2006 Sheet 2 of 34

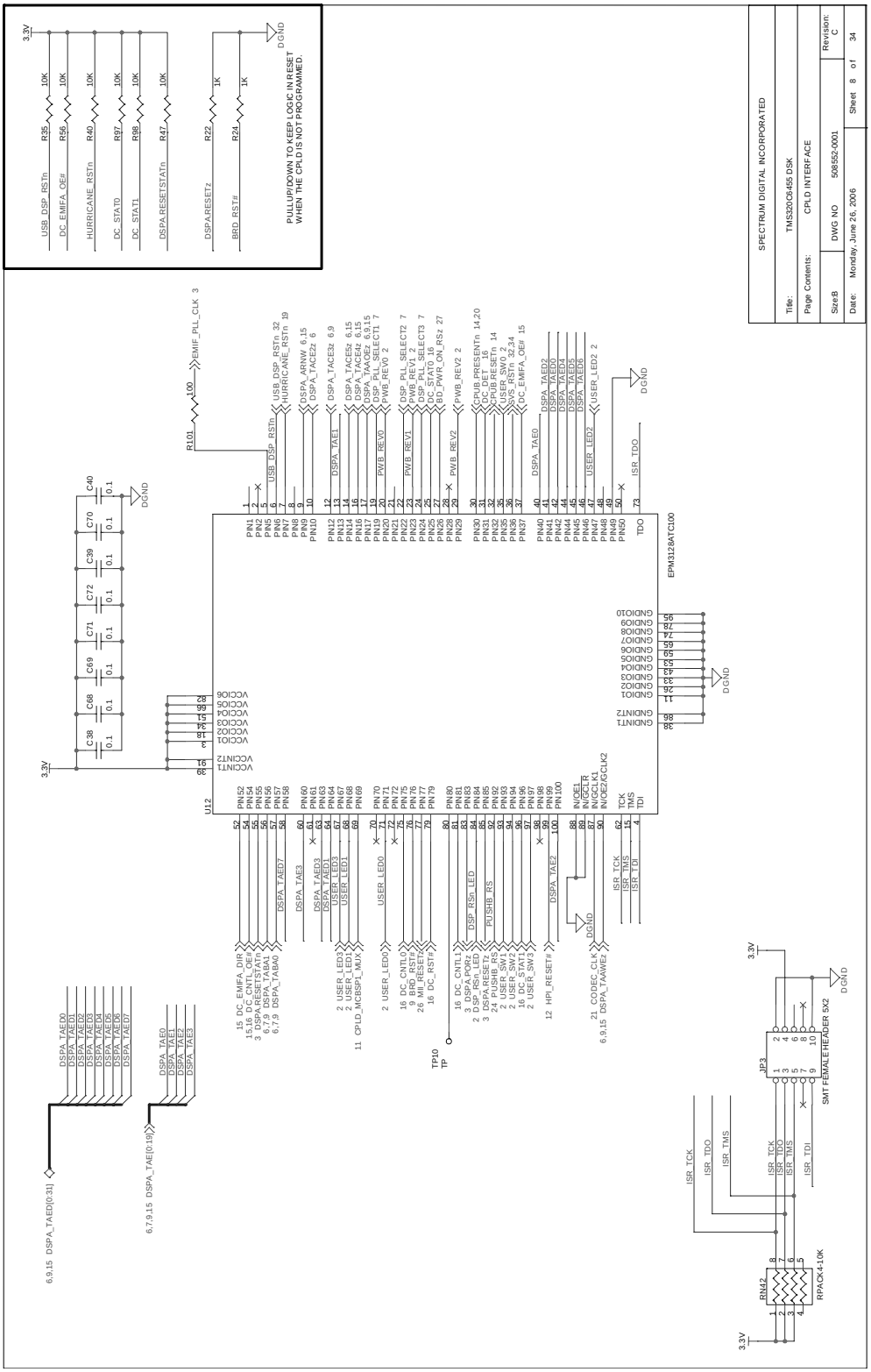

SPECTRUM DIGITAL INCORPORATED
Title: TMS320C6455 DSK
Page Contents: 6455 CLOCK INPUTS
Size:B DWG NO 508552-0001 Revision: C
Date: Thursday, June 22, 2006 Sheet 3 of 34
S1 S0 MULTIPLY OUTPUT
0 0 4X 100 MHz
0 OPEN 5.33X 133.25 MHz
0 1 5X 125 MHz
OPEN 0 2.5X 62.5 MHz
OPEN OPEN 2X 50 MHz
OPEN 1 3.33X 83.25 MHz
1 0 6X 150 MHz
1 OPEN 3X 75 MHz
1 1 8X 200 MHz
Run HUR_TCK to U10 ball and back as HUR_TCKRTN
U10C
tms320c6455ctz
U29
U28
U31
ICS512
L9
L7
L10
Ferrite Chip
BLM21PG221SN
50 MHz
25 MHz
DGND
3.3V

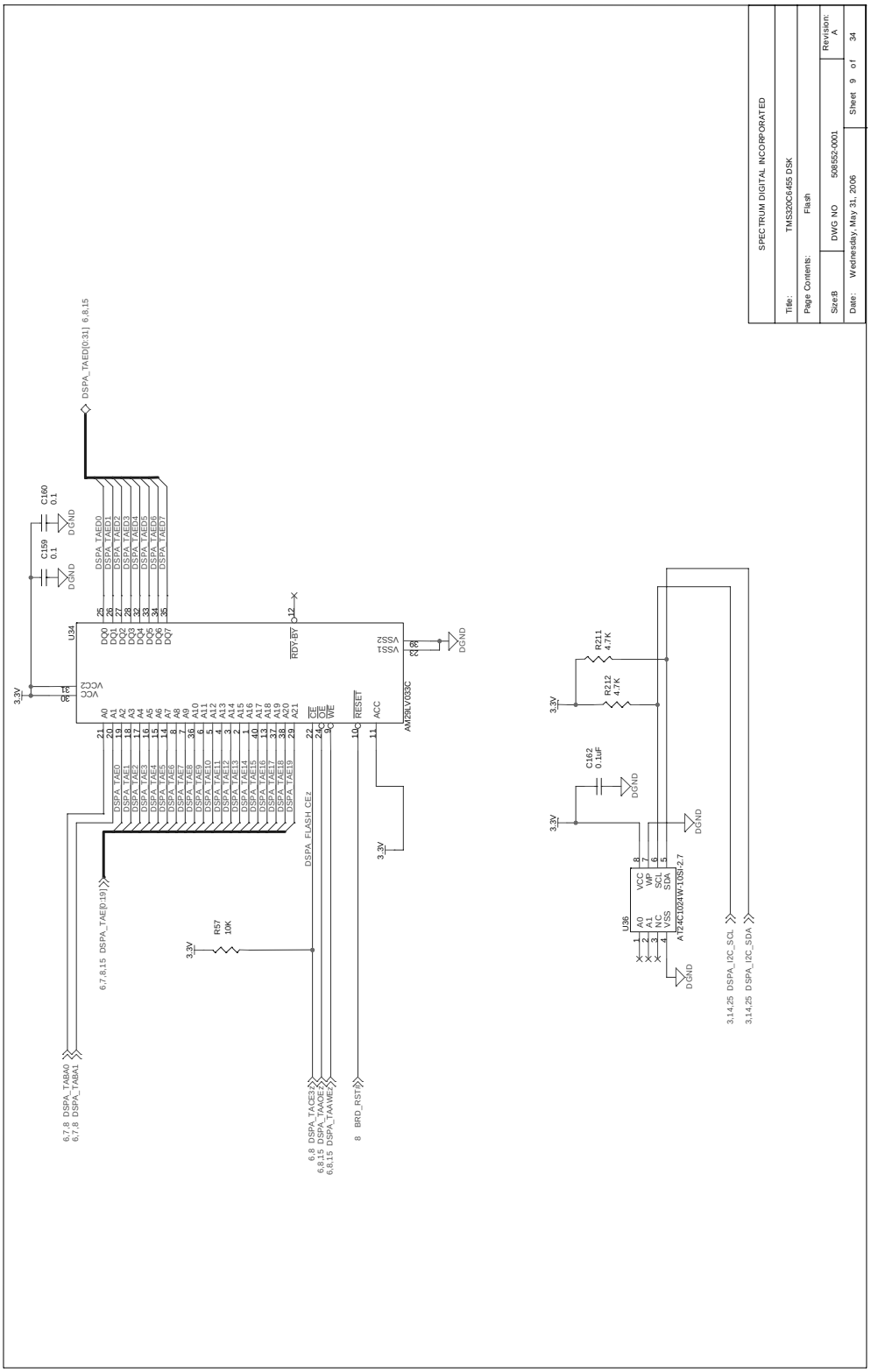

SPECTRUM DIGITAL INCORPORATED
Title: TMS320C6455 DSK
Page Contents: 6455 DDR Interface
Size:B
DWG NO 508552-0001
Revision: A
Date: Thursday, September 21, 2006
Sheet 4 of 34
tms320c6455zez
U1:08
DSPA_TBEA[0:13] 5
DSPA_TBBA[0:2] 5
DSPA_TBCEz 5
DSPA_TBECLKOUTP 5
DSPA_TBECLKOUTN 5
DSPA_TBSDCASz 5
DSPA_TBSDCKEz 5
DSPA_TBDDQM0 5
DSPA_TBDDQM1 5
DSPA_TBDDQM2 5
DSPA_TBDDQM3 5
DSPA_TBSDRASz 5
DSPA_TBSDWEz 5
DSPA_TBED[0:31] 5
DSPA_GATE0_1
DSPA_GATE2_3
NOTE: DSDDQGATE0 signals needs to route to DDR memories near D15-D0 and back to DSDDQGATE1.
NOTE: DSDDQGATE2 signals needs to route to DDR memories near D31-D16 and back to DSDDQGATE3.

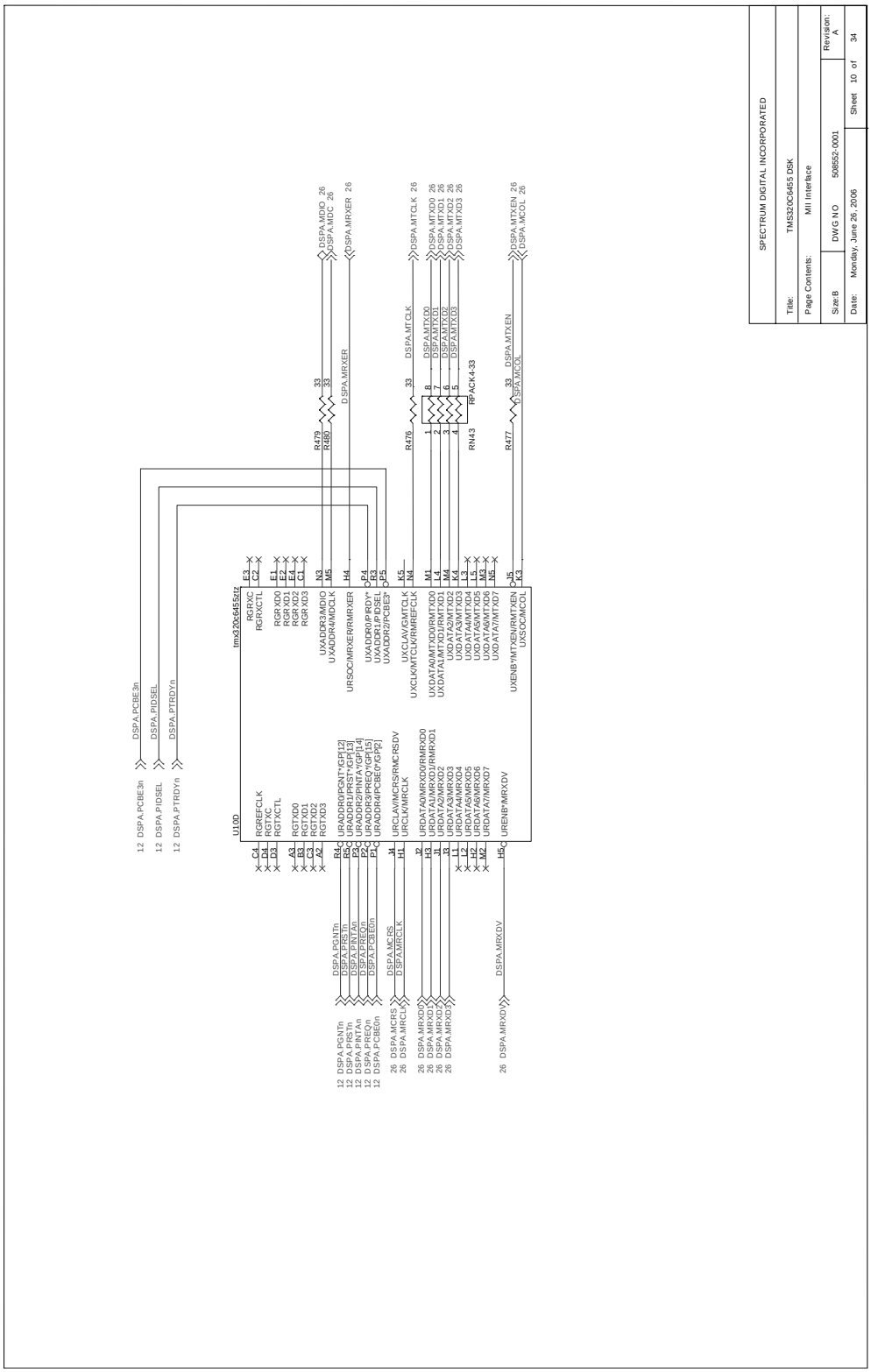

NOTE: 92 BALL BGA IS SHOWN IN THIS DIAGRAM, HOWEVER 84 BALL BGA IS FOOTPRINT COMPATIBLE
SPECTRUM DIGITAL INCORPORATED
Title: TMS320C6455 DSK
Page Contents: DDR2 Memory
Size:B
DWG NO 508552-0001
Revision: A
Date: Friday, September 22, 2006
Sheet 5 of 34
U32
U33
MT47H32M16BT
DSPA_TBED[0:31]
DSPA_TBEA[0:13]
DSPA_TBBA[0:2]
DSPA_VREFSSTL
DVDD_1.8V
DGND

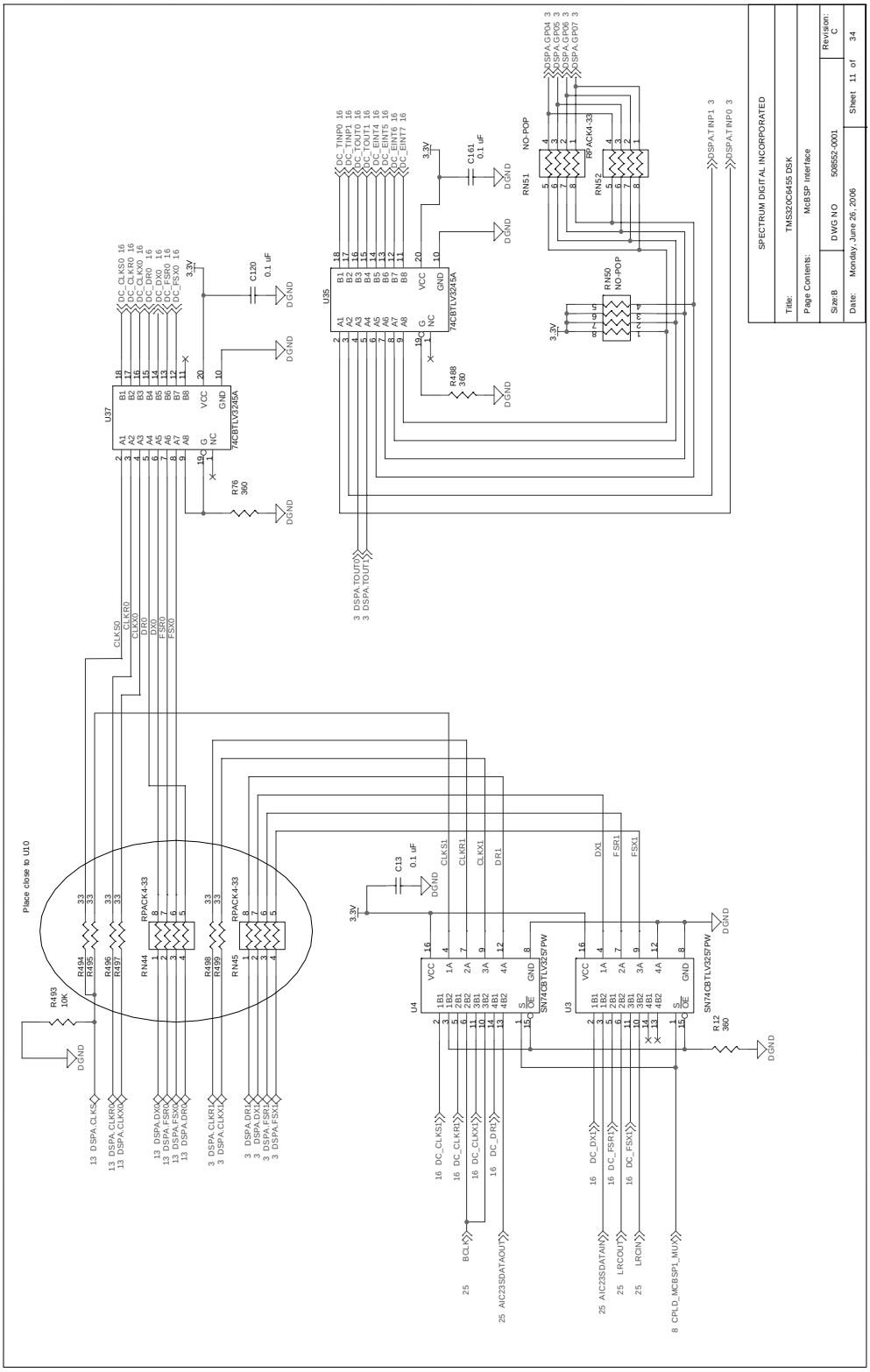

SPECTRUM DIGITAL INCORPORATED
Title: TMS320C6455 DSK
Page Contents: 6455 Emif A Interface
Size:B
DWG NO 508552-0001
Revision: A
Date: Wednesday, May 31, 2006
Sheet 6 of 34

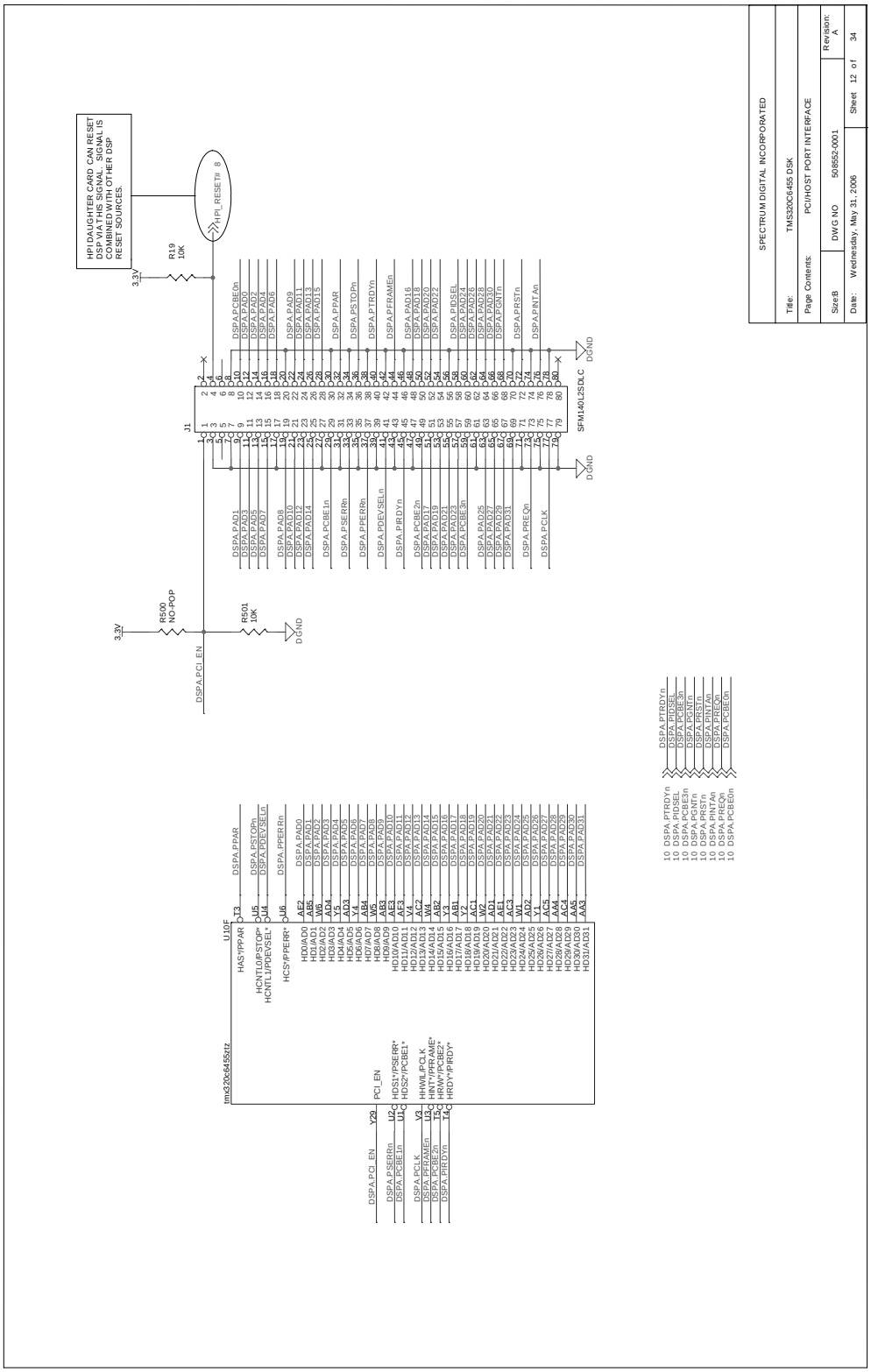

SPECTRUM DIGITAL INCORPORATED
Title: TMS320C6455 DSK
Page Contents: Boot Options
Size:B
DWG NO 508552-0001
Revision: B
Date: Monday, June 26, 2006
Sheet 7 of 34
DSPA_TAE[0:19]
BOOT_MODE3
BOOT_MODE2
BOOT_MODE1
BOOT_MODE0
AECLKIN_SEL
HPI_WIDTH
LIL_ENDIAN
UTOPA_EN
RESERVED1
MAC_SEL1
MAC_SEL0
PCI_EEAI
RESERVED2
PCI_EEPROM
MCBSP1
GPIO1
RESERVED3
RESERVED2
CFGGP2
CFGGP1
CFGGP0
EMIF_ENABLED
DDR ENABLED
DSPA_TABA[1:0]
SN74CBTLV1G125DCKR
74LCBTLV125PWR
SW DIP-8/SM
OFF - OPEN
ON - CLOSED
DSPA_ENDIAN ENDIAN
DSPA_BOOT0 BOOT_X
DSPA_BOOT1 BOOT_X
DSPA_BOOT2 BOOT_X
DSPA_BOOT3 BOOT_X
DSP_PLL_SELECT1
DSP_PLL_SELECT2
DSP_PLL_SELECT3
DSPA_TAE13
DSPA_TAE16
DSPA_TAE17
DSPA_TAE18
DSPA_TAE19
DGND
3.3V

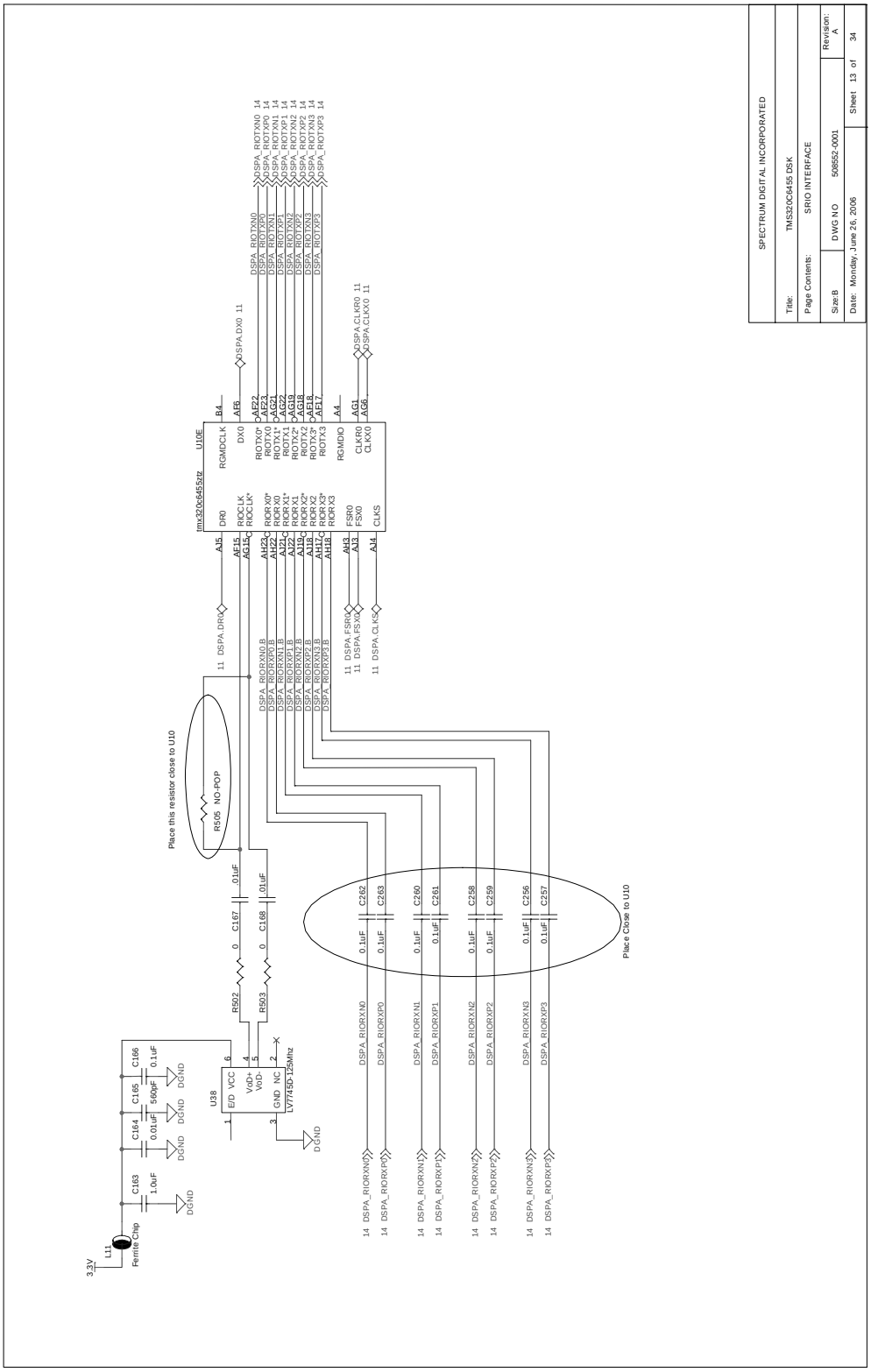

USB_DSP_RSTn R35 10K
DC_EMIFA_OE# R56 10K
HURRICANE_RSTn R40 10K
DC_STAT0 R97 10K
DC_STAT1 R98 10K
DSPA_RESETSTATn R47 10K
DSPA_RESET2 R22 1K
BRD_RST# R24 1K
PULLUP/DOWN TO KEEP LOGIC IN RESET WHEN THE CPLD IS NOT PROGRAMMED.
SPECTRUM DIGITAL INCORPORATED
Title: TMS320C6455 DSK
Page Contents: CPLD INTERFACE
Size:B DWG NO 508552-0001 Revision: C
Date: Monday, June 26, 2006 Sheet 8 of 34
U12
EPM3128ATC100
R101 100
EMIF_PLL_CLK 3
USB_DSP_RSTn 32
HURRICANE_RSTn 19
DSPA_ARNW 6,15
DSPA_TACE2z 6
DSPA_TACE2z 6,9
DSPA_TAE1
DSPA_TACE1z 6,15
DSPA_TACE4z 6,15
DSPA_TACE5z 6,9,15
DSP_PLL_SELECT1 7
PWB_REV0 2
DSP_PLL_SELECT2 7
PWB_REV1 2
DSP_PLL_SELECT3 7
DC_STAT0 16
BD_PWR_ON_RSz 27
PWB_REV2 2
CPUB PRESENTn 14,20
DC_DET 16
CPUB RESETn 14
USER_SW0 2
USER_SW1 2
DC_RSTn 34
DC_EMIFA_OE# 15
DSPA_TAED2
DSPA_TAED0
DSPA_TAED1
DSPA_TAED5
DSPA_TAED6
USER_LED2 2
ISR_TDO
DGND
3.3V
C38 0.1
C68 0.1
C69 0.1
C71 0.1
C72 0.1
C39 0.1
C70 0.1
C40 0.1
VCCINT2
VCCINT1
VCCIO6
VCCIO5
VCCIO4
VCCIO3
VCCIO2
VCCIO1
GND INT2
GND INT1
GND IO1
GND IO2
GND IO3
GND IO4
GND IO5
GND IO6
GND IO7
GND IO8
GND IO9
GND IO10
TDO
TCK
TMS
TDI
IN/OE1
IN/OE2/CLK
IN/GCLK1
IN/OE3/GCLK2
DSPA_TAED0
DSPA_TAED1
DSPA_TAED2
DSPA_TAED3
DSPA_TAED4
DSPA_TAED5
DSPA_TAED6
DSPA_TAED7
6,9,15 DSPA_TAED[0:31]
DSPA_TAE0
DSPA_TAE1
DSPA_TAE2
DSPA_TAE3
6,7,9,15 DSPA_TAE[0:19]
15 DC_EMIFA_DIR
15,16 DC_CNTL_OE#
3 DSPA_RESETSTATn
6,7,9,15 DSPA_TAB[1:0]
6,7,9 DSPA_TAB0
DSPA_TAE7
DSPA_TAE3
DSPA_TAED3
DSPA_TAED1
USER_LED3
USER_LED1
2 USER_LED3
2 USER_LED1
11 CPLD_MCBSP1_MUX
2 USER_LED0
16 DC_CNTL0
9 BRD_RST#
26 MII_RESETz
16 DC_RST#
TP10
TP
16 DC_CNTL1
3 DSPA_PORz
2 DSPA_RSn_LED
3 DSPA_RESET2
24 PUSHB_RS
2 USER_SW1
2 USER_SW2
16 DC_STAT1
2 USER_SW3
12 HPI_RESET#
21 CODEC_CLK
6,9,15 DSPA_TAAWEz
DSP_RSn_LED
PUSHB_RS
DSPA_TAE2
ISR_TCK
ISR_TMS
ISR_TDI
JP3
SMT FEMALE HEADER 5X2
RN42
RPACK-10K

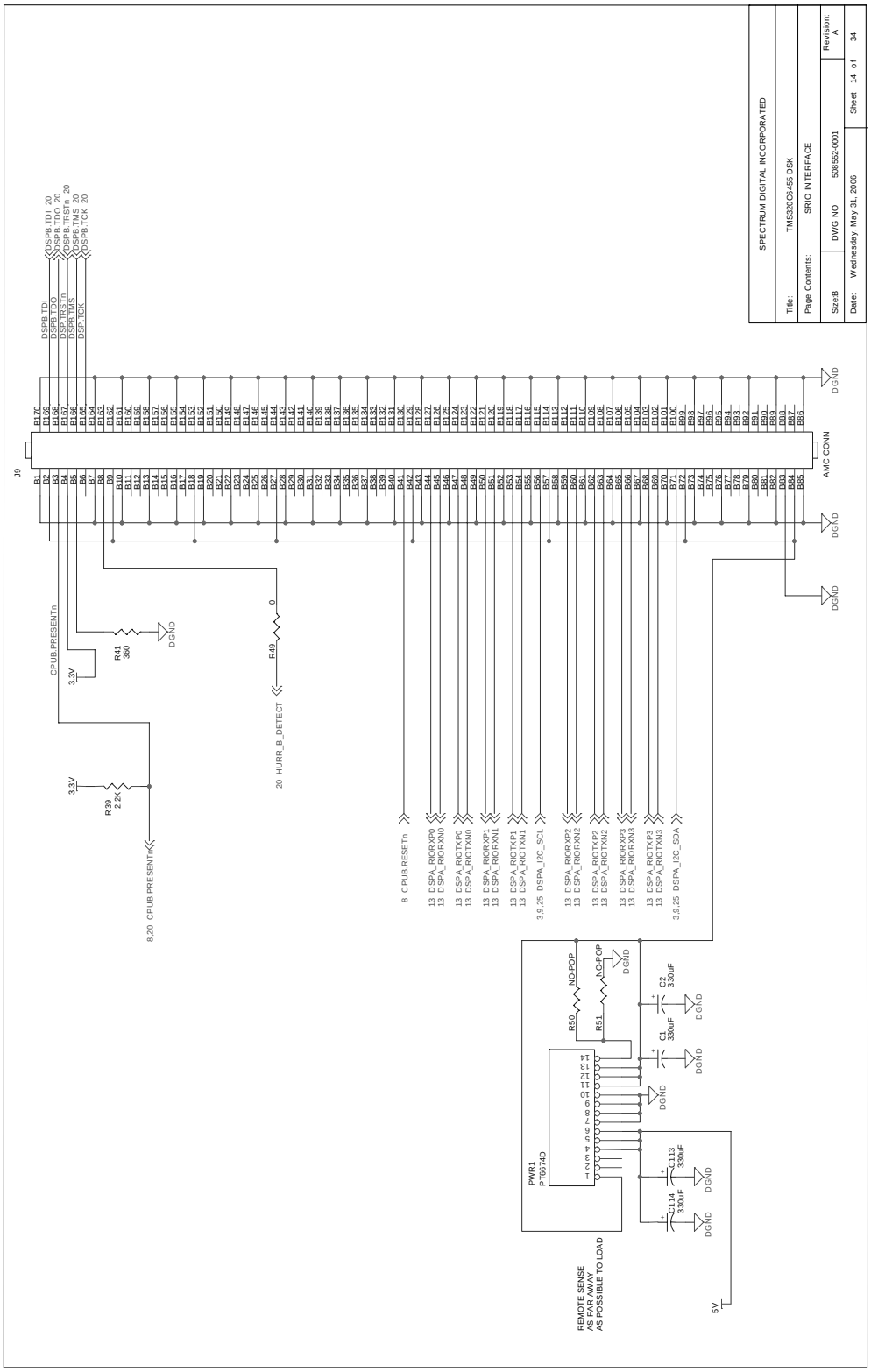

SPECTRUM DIGITAL INCORPORATED
Title: TMS320C6455 DSK
Page Contents: Flash
Size:B DWG NO 508552-0001 Revision: A
Date: Wednesday, May 31, 2006 Sheet 9 of 34
U34
AM29LV033C
U36
AT24C1024W-10SI-2.7
DSPA_TAED[0:31] 6,8,15
DSPA_TAE[0:19] 6,7,8,15
DSPA_FLASH_CE2
6,7,8 DSPA_TABA0
6,7,8 DSPA_TABA1
6,8 DSPA_TACE3
6,8,15 DSPA_TAOE
6,8,15 DSPA_TAAWE
8 BRD_RST
3,14,25 DSPA_I2C_SCL
3,14,25 DSPA_I2C_SDA
3.3V
DGND
C159 0.1
C160 0.1
C162 0.1uF
R57 10K
R211 4.7K
R212 4.7K

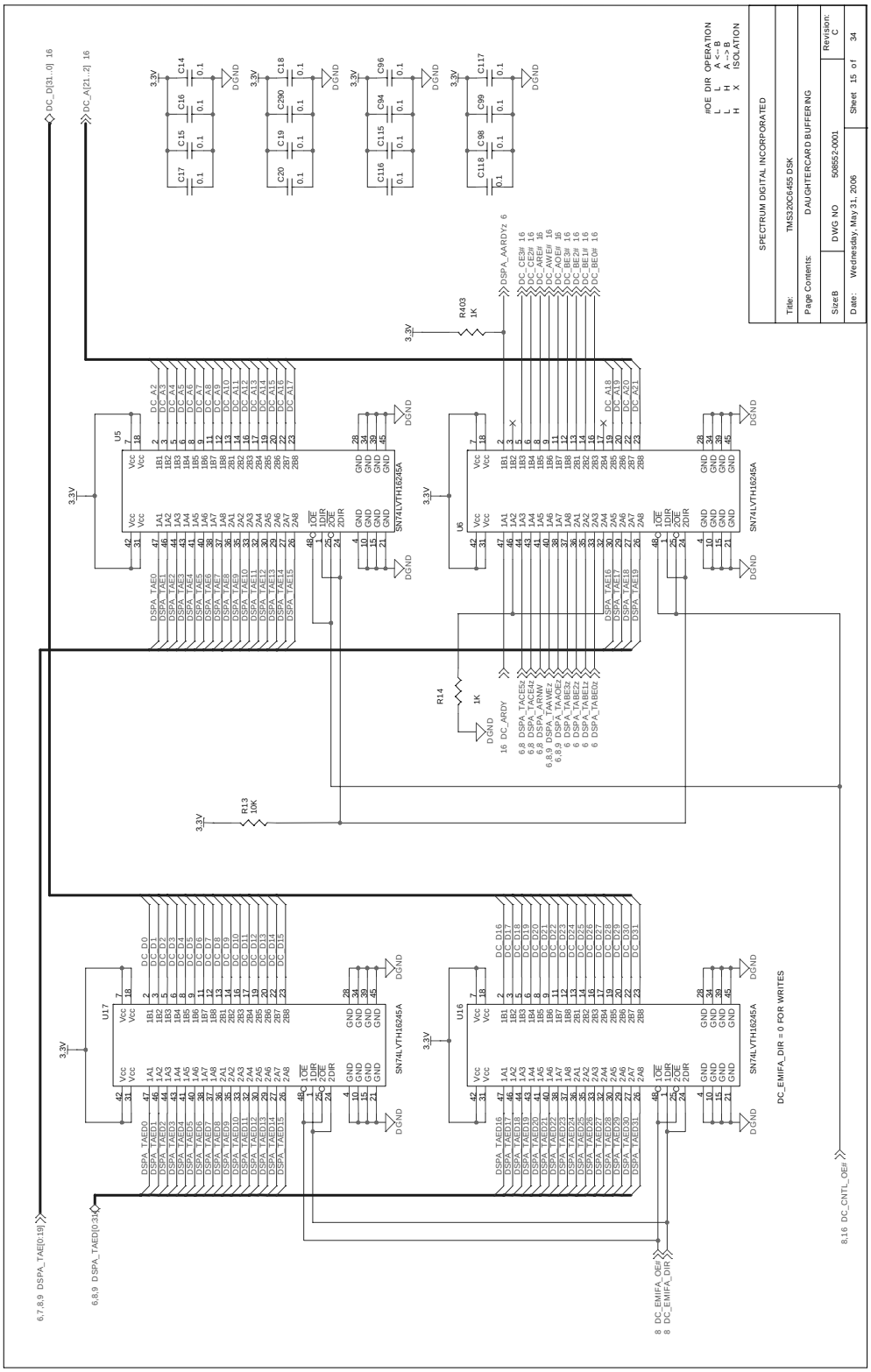

SPECTRUM DIGITAL INCORPORATED
Title: TMS320C6455 DSK
Page Contents: MII Interface
Size:B
DWG N O 508552-0001
Revision: A
Date: Monday, June 26, 2006
Sheet 10 of 34
U10D
tms320c6455zrz
DSPA.PCBE3n
DSPA.PIDSEL
DSPA.PTRDYn
DSPA.MDIO
DSPA.MDC
DSPA.MRXER
DSPA.MTCLK
DSPA.MTXD0
DSPA.MTXD1
DSPA.MTXD2
DSPA.MTXD3
DSPA.MTXEN
DSPA.MCOL
DSPA.MRXD0
DSPA.MRXD1
DSPA.MRXD2
DSPA.MRXD3
DSPA.MRXDV
DSPA.MCRS
DSPA.MRCLK
DSPA.PGNTn
DSPA.PRSTn
DSPA.PINTAn
DSPA.PREQn
DSPA.PCBEOn
R479
R480
R476
R477
RN43
RP ACK4-33

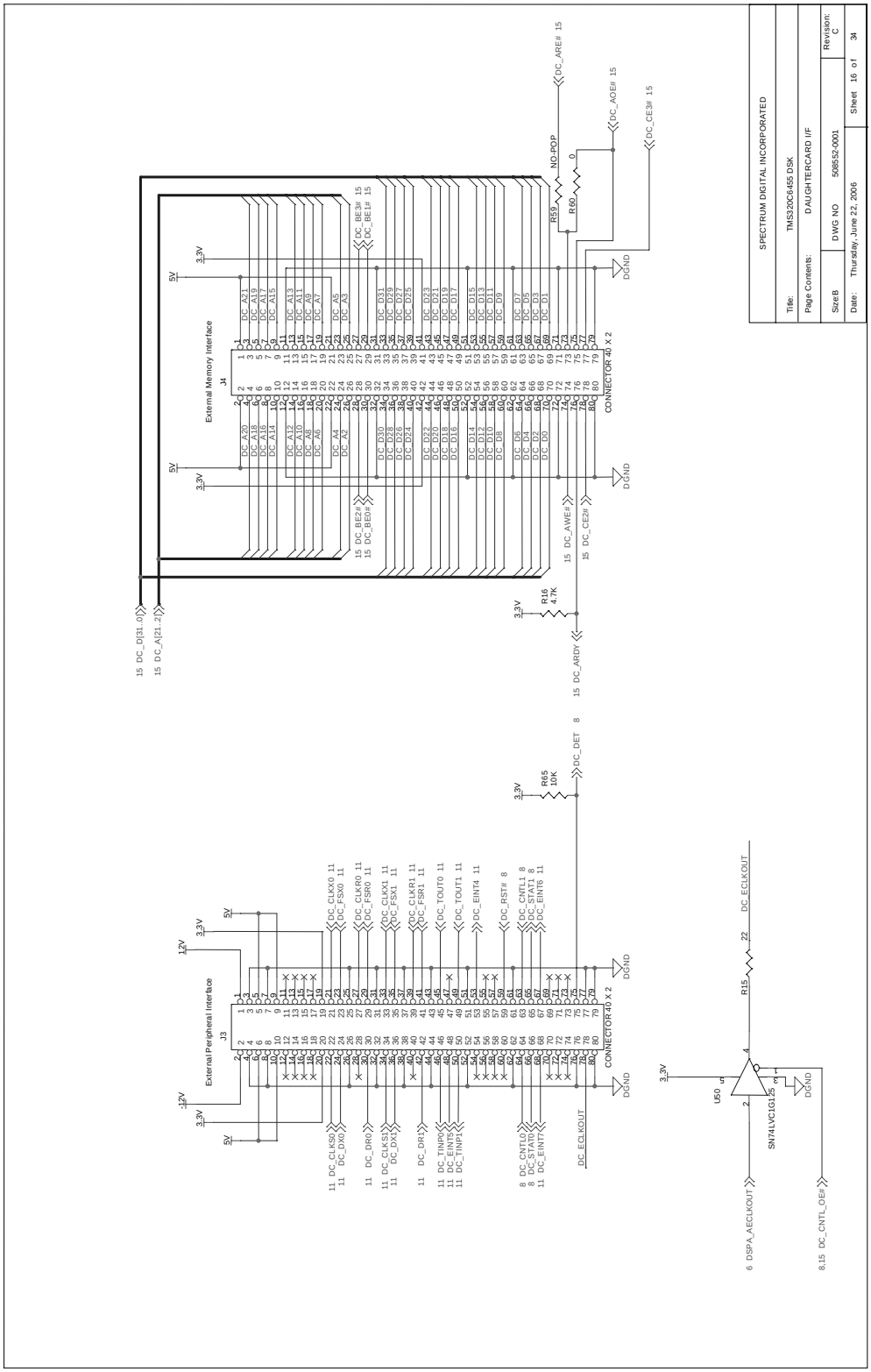

SPECTRUM DIGITAL INCORPORATED
Title: TMS320C6455 DSK
Page Contents: McBSP Interface
Size: B
DWG NO 508552-0001
Revision: C
Date: Monday, June 26, 2006
Sheet 11 of 34
Place close to U10
U37
74CBTLV3245A
U35
74CBTLV3245A
U4
SN74CBTLV3257PW
U3
SN74CBTLV3257PW
RN44
RPACK4-33
RN45
RPACK4-33
RN51
RPACK4-33
RN52
RPACK4-33
RN50
NO-POP
RN51
NO-POP
R493
10K
R494
33
R495
33
R496
33
R497
33
R498
33
R499
33
R76
360
R488
360
R12
360
C120
0.1 uF
C161
0.1 uF
C13
0.1 uF
3.3V
DGND
CLKS0
CLKR0
CLKX0
DR0
DX0
FSR0
FSX0
CLKS1
CLKR1
CLKX1
DR1
DX1
FSR1
FSX1
DC_CLKS0 16
DC_CLKR0 16
DC_CLKX0 16
DC_DR0 16
DC_DX0 16
DC_FSR0 16
DC_FSX0 16
DC_TINP0 16
DC_TINP1 16
DC_TOUT0 16
DC_TOUT1 16
DC_CLKS1 16
DC_CLKR1 16
DC_CLKX1 16
DC_DR1 16
DC_DX1 16
DC_FSR1 16
DC_FSX1 16
DC_EINT4 16
DC_EINT5 16
DC_EINT6 16
DC_EINT7 16
DSPA.GP04 3
DSPA.GP05 3
DSPA.GP06 3
DSPA.GP07 3
DSPA.TINP1 3
DSPA.TINP0 3
3 DSPA.TOUT0
3 DSPA.TOUT1
13 DSPA.CLKS
13 DSPA.CLKR0
13 DSPA.CLKX0
13 DSPA.DX0
13 DSPA.FSR0
13 DSPA.FSX0
13 DSPA.DR0
3 DSPA.CLKR1
3 DSPA.CLKX1
3 DSPA.DR1
3 DSPA.DX1
3 DSPA.FSR1
3 DSPA.FSX1
16 DC_CLKS1
16 DC_CLKR1
16 DC_CLKX1
16 DC_DR1
16 DC_DX1
16 DC_FSR1
16 DC_FSX1
25 BCLK
25 AIC23SDATAOUT
25 AIC23SDATAIN
25 LRCOUT
25 LRCIN
8 CPLD_MCBSP1_MUX

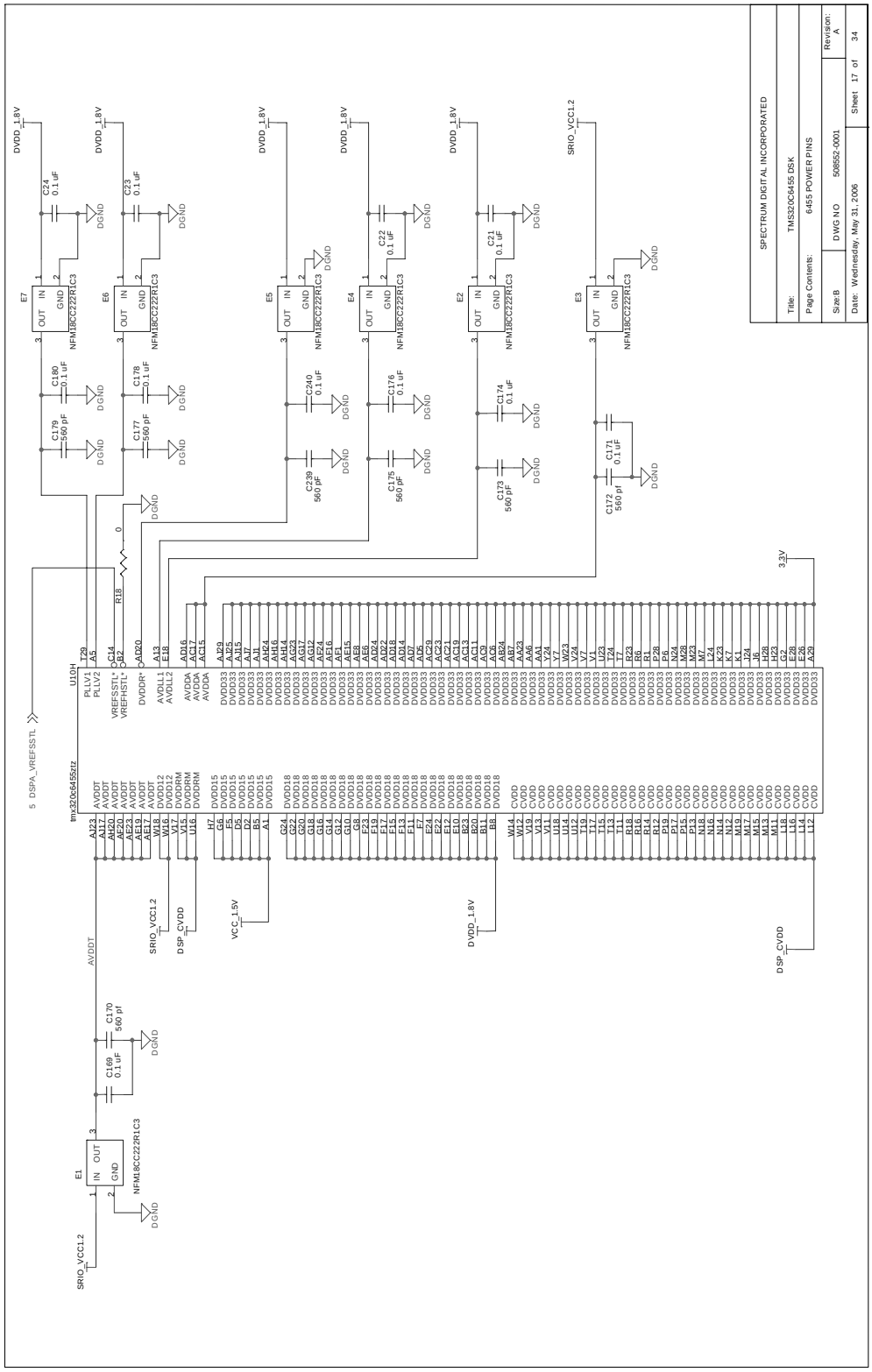

HPI DAUGHTER CARD CAN RESET DSP VIA THIS SIGNAL. SIGNAL IS COMBINED WITH OTHER DSP RESET SOURCES.
HPI_RESETn# 8
R19 10K
3.3V
R500 NO-POP
R501 10K
DGND
DSPA.PCI_EN
J1
SFM140-L2-S-D-L-C
U10F
tmx320c6455ztz
SPECTRUM DIGITAL INCORPORATED
Title: TMS320C6455 DSK
Page Contents: PCI/HOST PORT INTERFACE
Size:B
DWG NO 508552-0001
Revision: A
Date: Wednesday, May 31, 2006
Sheet 12 of 34

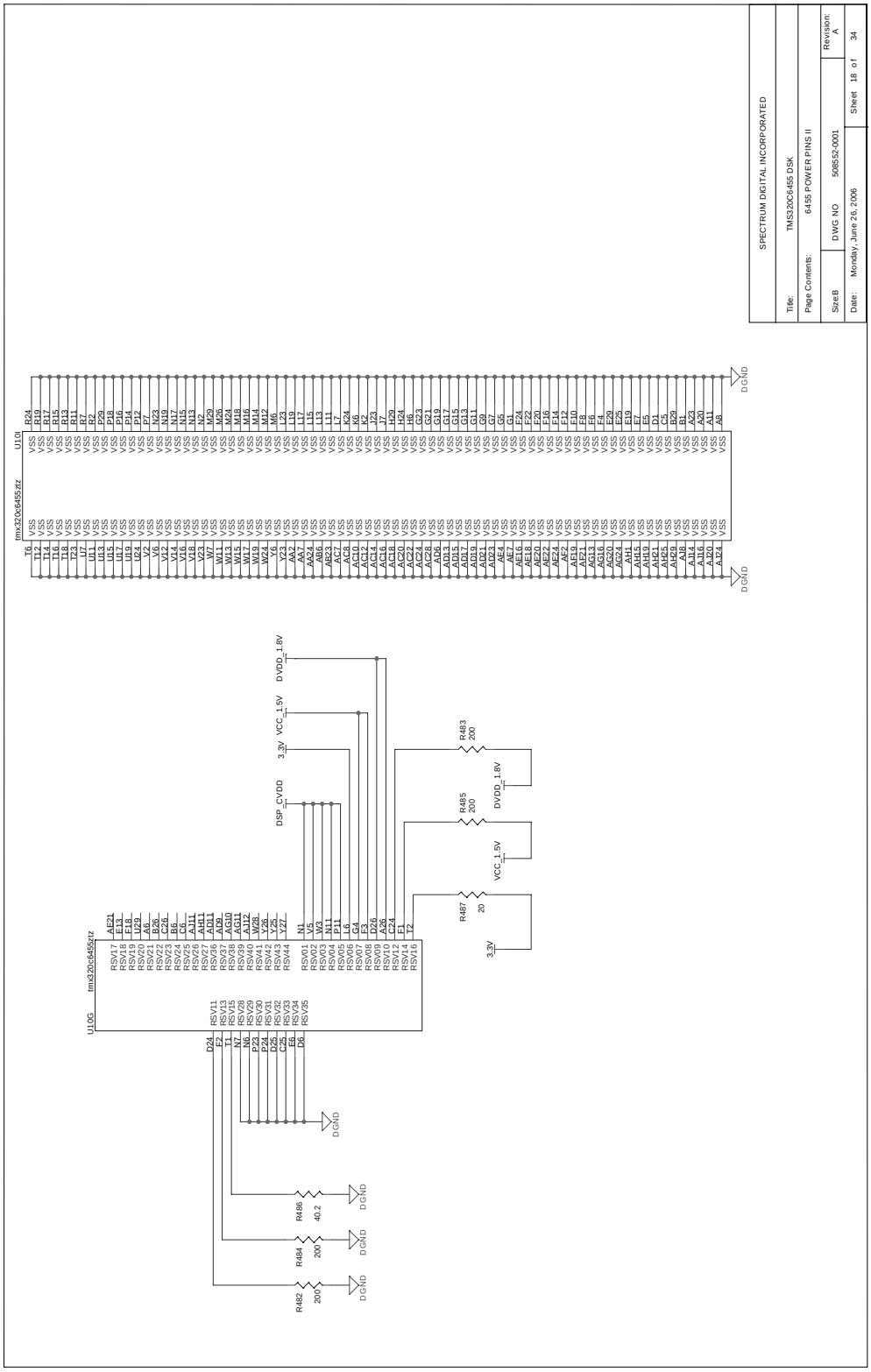

SPECTRUM DIGITAL INCORPORATED
Title: TMS320C6455 DSK
Page Contents: SRIO INTERFACE
Size:B
DWG NO 508552-0001
Revision: A
Date: Monday, June 26, 2006
Sheet 13 of 34
U10E
tms320c6455ztz
U38
LV7745D-125Mhz
R505 NO-POP
Place this resistor close to U10
Place Close to U10
3.3V
L11
Ferrite Chip
DGND

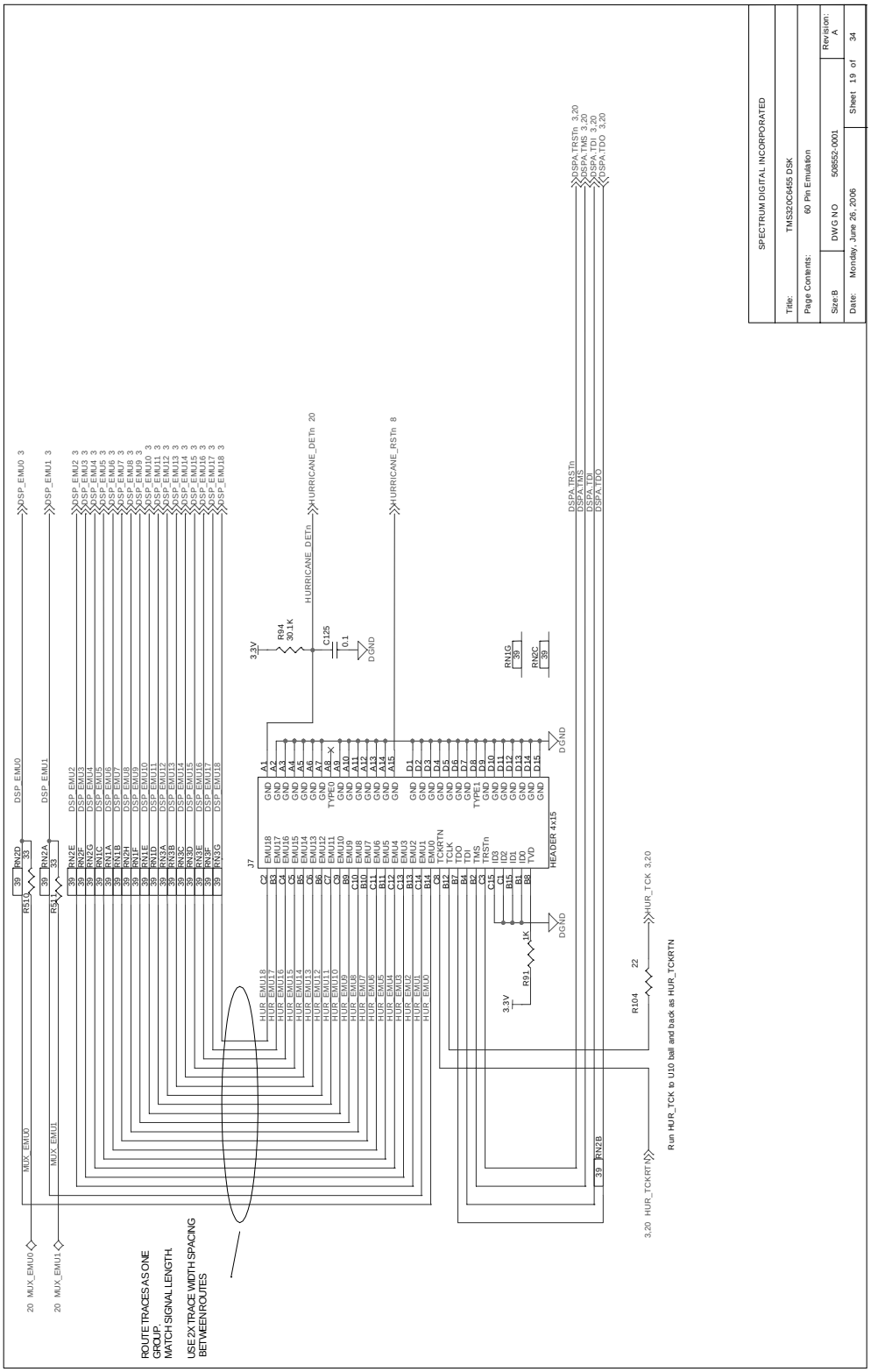

SPECTRUM DIGITAL INCORPORATED
Title: TMS320C6455 DSK
Page Contents: SRIO INTERFACE
Size:B DWG NO 508552-0001 Revision: A
Date: Wednesday, May 31, 2006 Sheet 14 of 34
J9
AMC CONN
DSPB.TDI 20
DSPB.TDO 20
DSPB.TRSTn 20
DSPB.TMS 20
DSPB.TCK 20
DSP.TDI
DSP.TDO
DSP.TRSTn
DSP.TMS
DSP.TCK
DGND
CPUB.PRESENTn
3.3V
R41 360
R39 2.2K
R49 0
20 HURR_B_DETECT
8,20 CPUB.PRESENTn
8 CPUB.RESETn
13 DSPA_RIOR.XP0
13 DSPA_RIOR.XN0
13 DSPA_RIOTX.P0
13 DSPA_RIOTX.N0
13 DSPA_RIOR.XP1
13 DSPA_RIOR.XN1
13 DSPA_RIOTX.P1
13 DSPA_RIOTX.N1
3,9,25 DSPA_I2C_SCL
13 DSPA_RIOR.XP2
13 DSPA_RIOR.XN2
13 DSPA_RIOTX.P2
13 DSPA_RIOTX.N2
13 DSPA_RIOR.XP3
13 DSPA_RIOR.XN3
13 DSPA_RIOTX.P3
13 DSPA_RIOTX.N3
3,9,25 DSPA_I2C_SDA
PWR1 PT6674D
NO-POP
R50
R51
C2 330uF
C1 330uF
C113 330uF
C114 330uF
5V
REMOTE SENSE
AS STRAIGHT AWAY
AS POSSIBLE TO LOAD

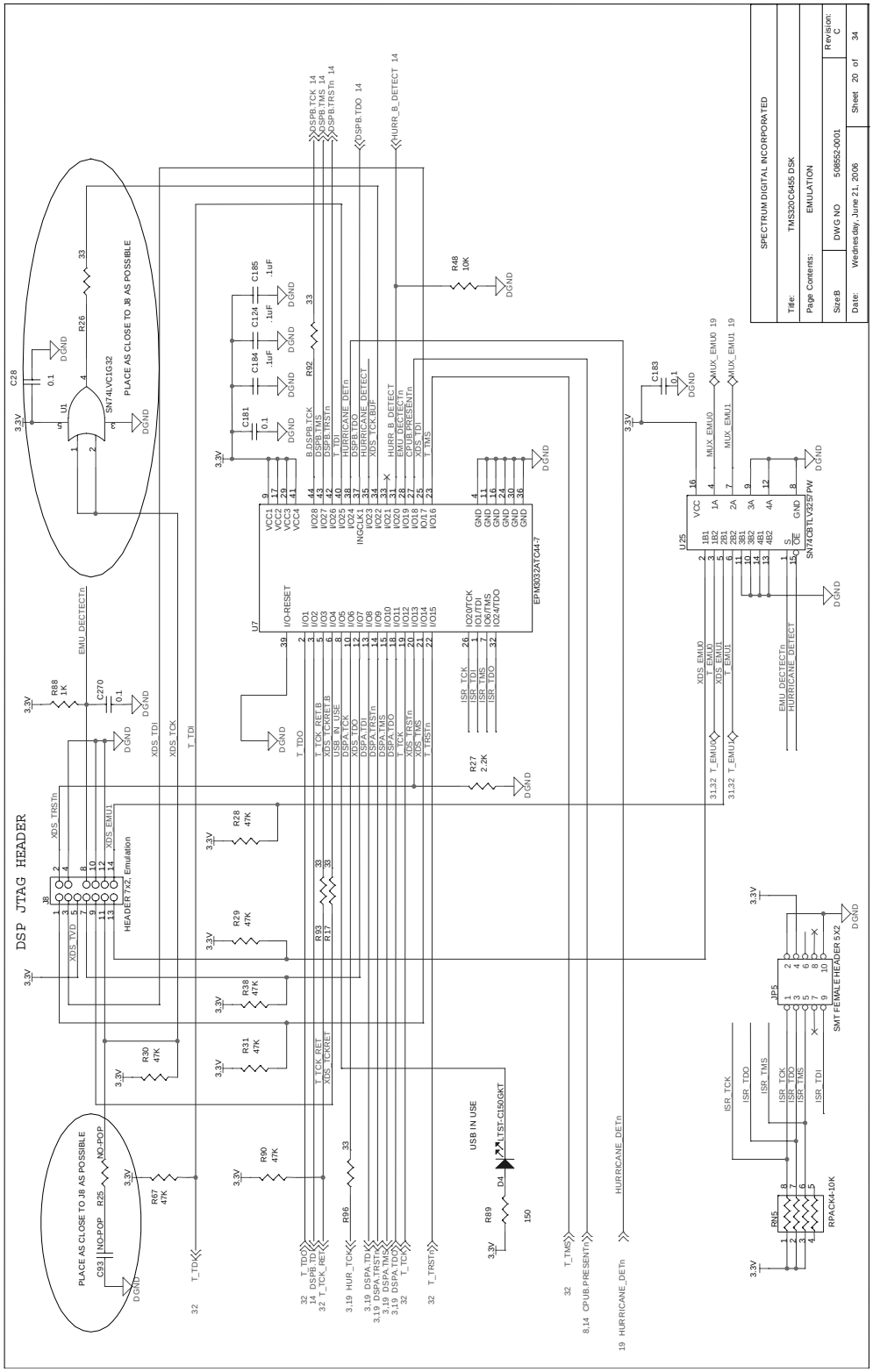

SPECTRUM DIGITAL INCORPORATED
Title: TMS320C6455 DSK
Page Contents: DAUGHTERCARD BUFFERING
Size:B
DWG NO 508552-0001
Revision: C
Date: Wednesday, May 31, 2006
Sheet 15 of 34
#OE DIR OPERATION
L L A <-- B
L H A --> B
H X ISOLATION
DC_D[31..0] 16
DC_A[21..2] 16
DSPA_AARDY2 6
DC_CE2# 16
DC_CE2# 16
DC_ARE# 16
DC_TAAE# 16
DC_AOE# 16
DC_BE3# 16
DC_BE2# 16
DC_BE1# 16
DC_BE0# 16
R403 1K
R14 1K
R13 10K
16 DC_ARDY
6,7,8,9 DSPA_TAE[0:19]
6,8,9 DSPA_TAED[0:31]
8,16 DC_CNTL_OE#
8 DC_EMIFA_OE#
8 DC_EMIFA_DIR
DC_EMIFA_DIR = 0 FOR WRITES
SN74LVTH16245A
U5
U6
U16
U17

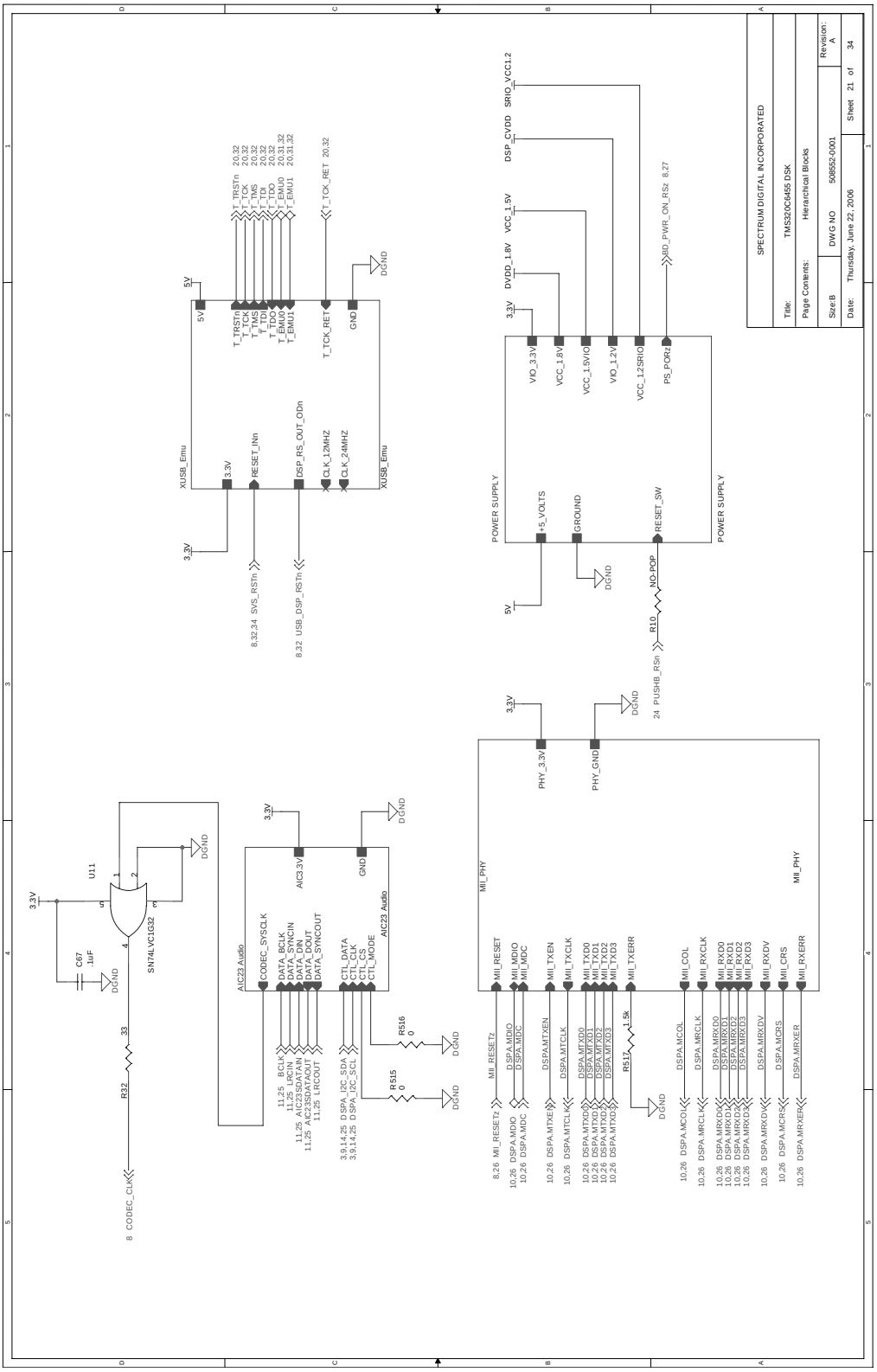

External Memory Interface
J4
CONNECTOR 40 X 2
External Peripheral Interface
J3
CONNECTOR 40 X 2
SPECTRUM DIGITAL INCORPORATED
Title:
TMS320C6455 DSK
Page Contents:
DAUGHTERCARD I/F
Size:B
DWG NO
508552-0001
Revision: C
Date: Thursday, June 22, 2006
Sheet 16 of 34

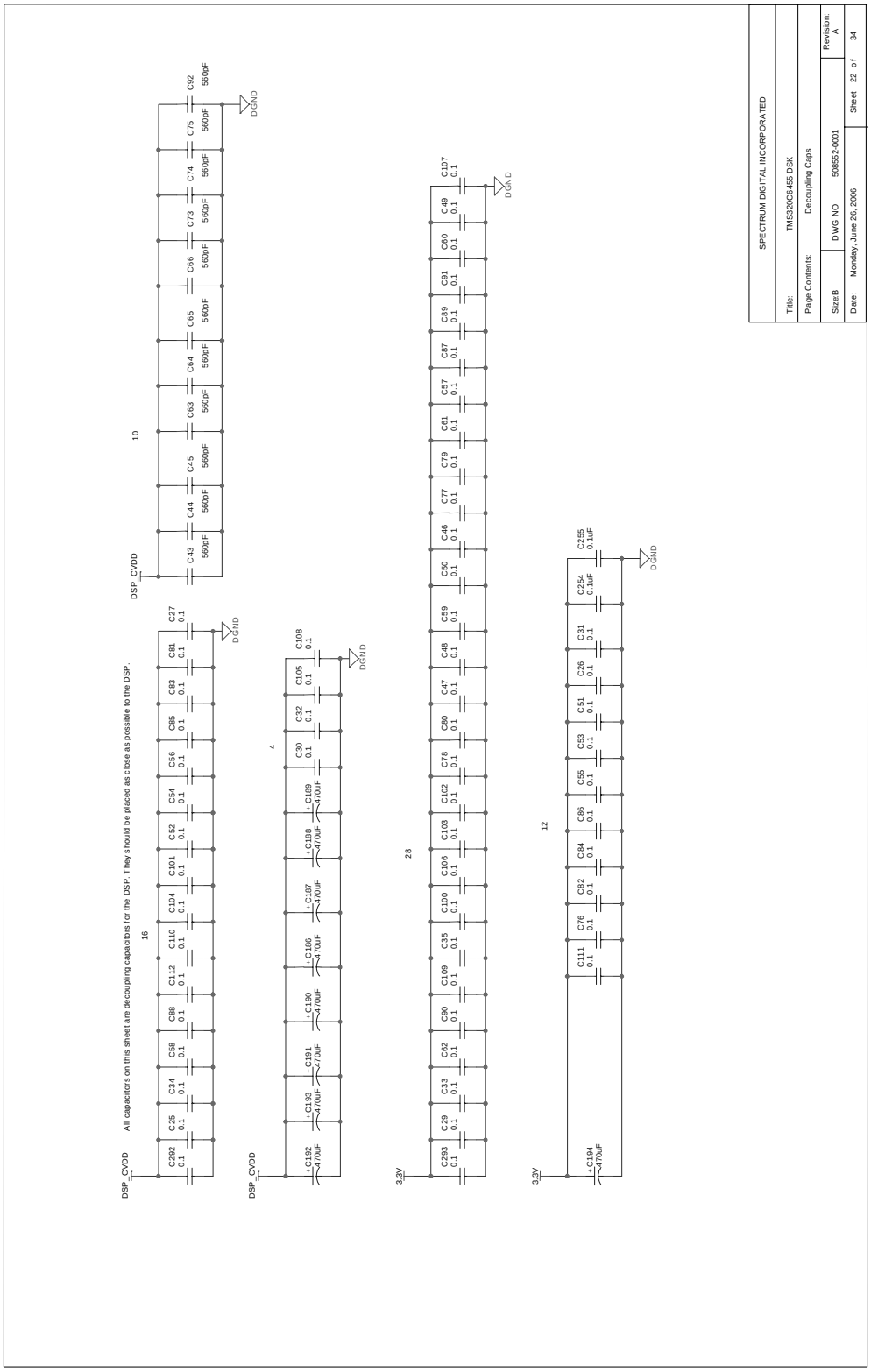

SPECTRUM DIGITAL INCORPORATED
Title: TMS320C6455 DSK
Page Contents: 6455 POWER PINS
Size:B
DWG NO 508552-0001
Revision: A
Date: Wednesday, May 31, 2006
Sheet 17 of 34
DVDD_1.8V
SRIO_VCC1.2
DSP_CVDD
VCC_1.5V
3.3V
AVDDT
DGND
NFM18CC222R1C3
tms320c6455ztz
U104
5 DSPA_VREFSSTL

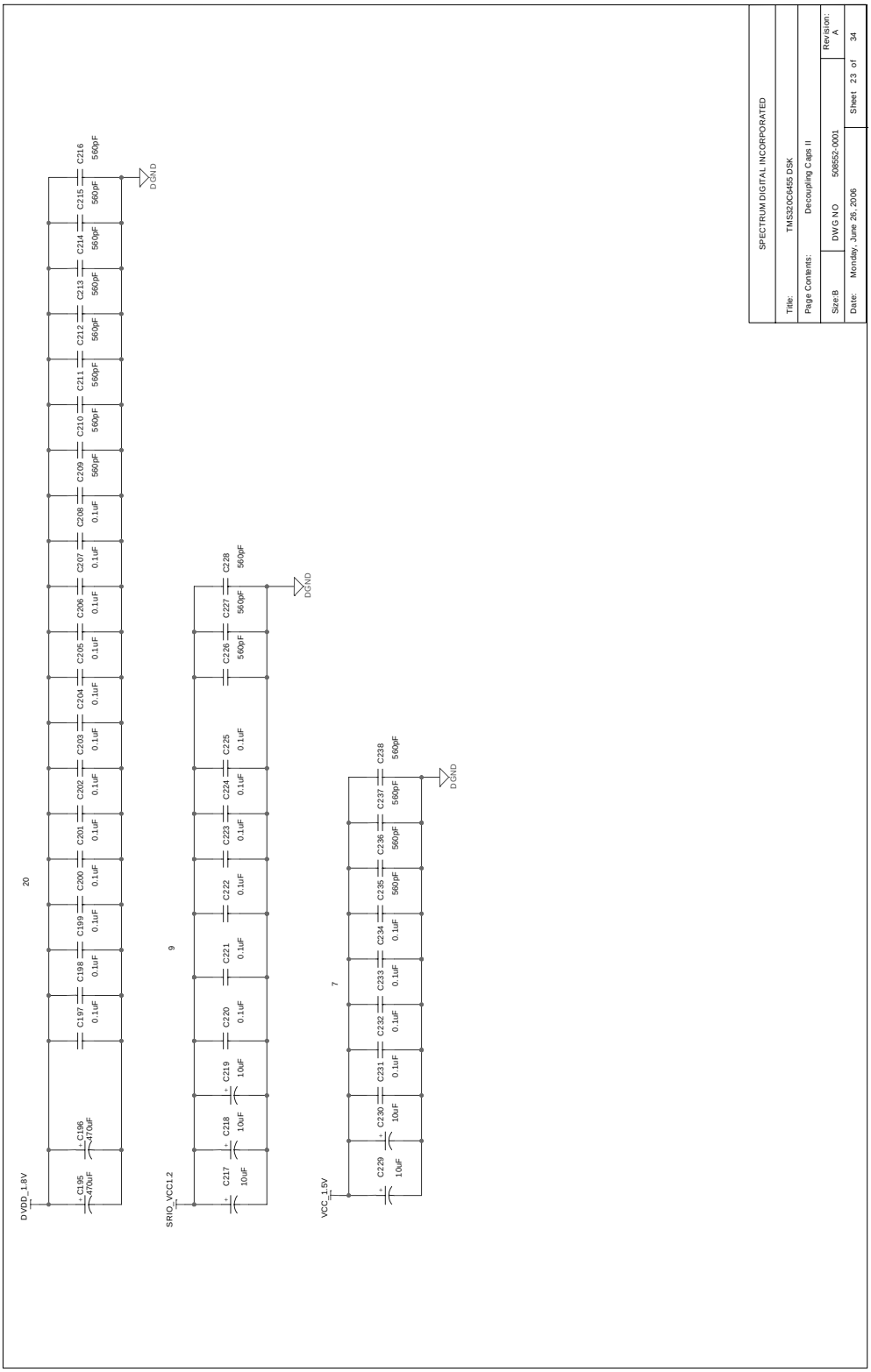

SPECTRUM DIGITAL INCORPORATED
Title: TMS320C6455 DSK
Page Contents: 6455 POWER PINS II
Size:B DWG NO 508552-0001 Revision: A
Date: Monday, June 26, 2006 Sheet 18 of 34
tmx320c6455ztz
U10G
U10I
DGND
DSP_CVDD
3.3V
VCC_1.5V
DVDD_1.8V
R482 200
R484 200
R486 40.2
R487 20
R485 200
R483 200

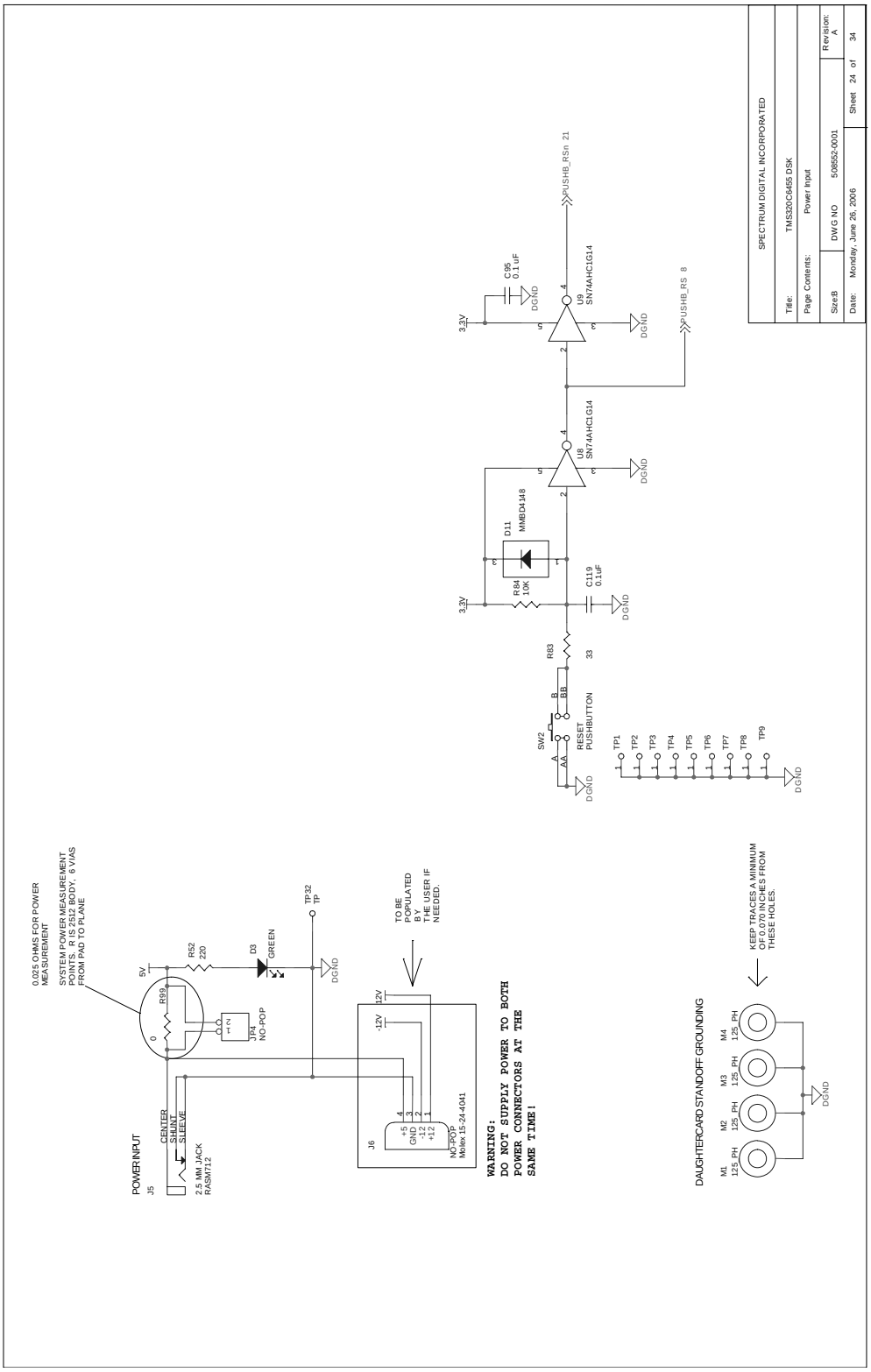

SPECTRUM DIGITAL INCORPORATED
Title: TMS320C6455 DSK
Page Contents: 60 Pin Emulation
Size:B DWG NO 508552-0001 Revision: A
Date: Monday, June 26, 2006 Sheet 19 of 34
ROUTE TRACES AS ONE GROUP. MATCH SIGNAL LENGTH.
USE 2X TRACE WIDTH+SPACING BETWEEN ROUTES
Run HUR_TCK to U10 ball and back as HUR_TCKRTN
HEADER 4x15
J7
R94 30.1K
C125 0.1
R91 1K
R104 22
R51 33
R510 33
HURRICANE_DETn
HURRICANE_RSTn
DSP_EMU0
DSP_EMU1
MUX_EMU0
MUX_EMU1
HUR_TCK
HUR_TCKRTN
DSPA.TRSTn
DSPA.TMS
DSPA.TDI
DSPA.TDO
3.3V
DGND

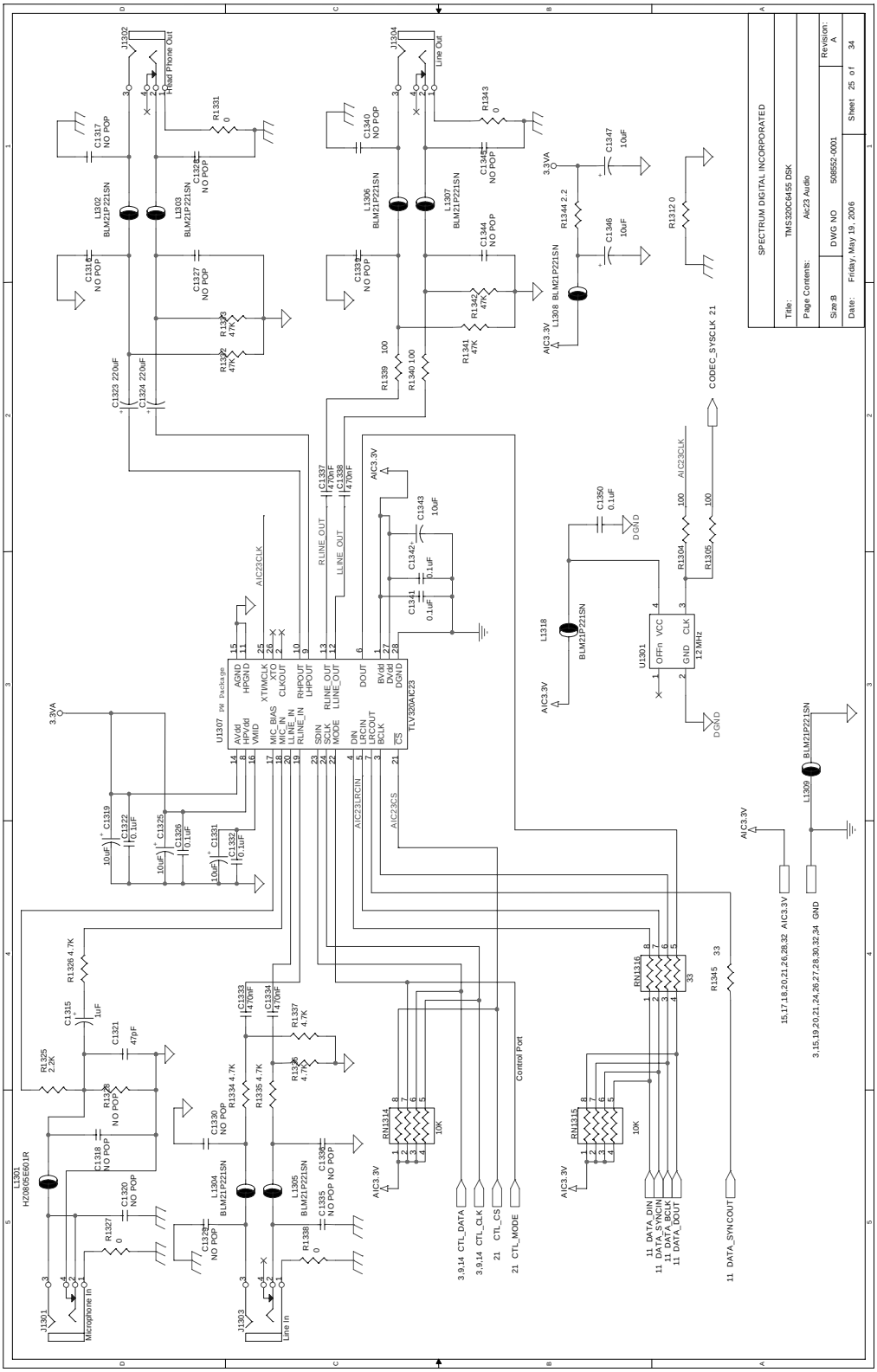

SPECTRUM DIGITAL INCORPORATED
Title: TMS320C6455 DSK
Page Contents: EMULATION
Size B
DWG NO 508552-0001
Revision: C
Date: Wednesday, June 21, 2006
Sheet 20 of 34
DSP JTAG HEADER
HEADER 7X2, Emulation
PLACE AS CLOSE TO J8 AS POSSIBLE
SN74LVC1G32
EPM3032ATC44-7
SN74CBTLV3257PW
USB IN USE
SMT FEMALE HEADER 5X2
RPACK4-10K

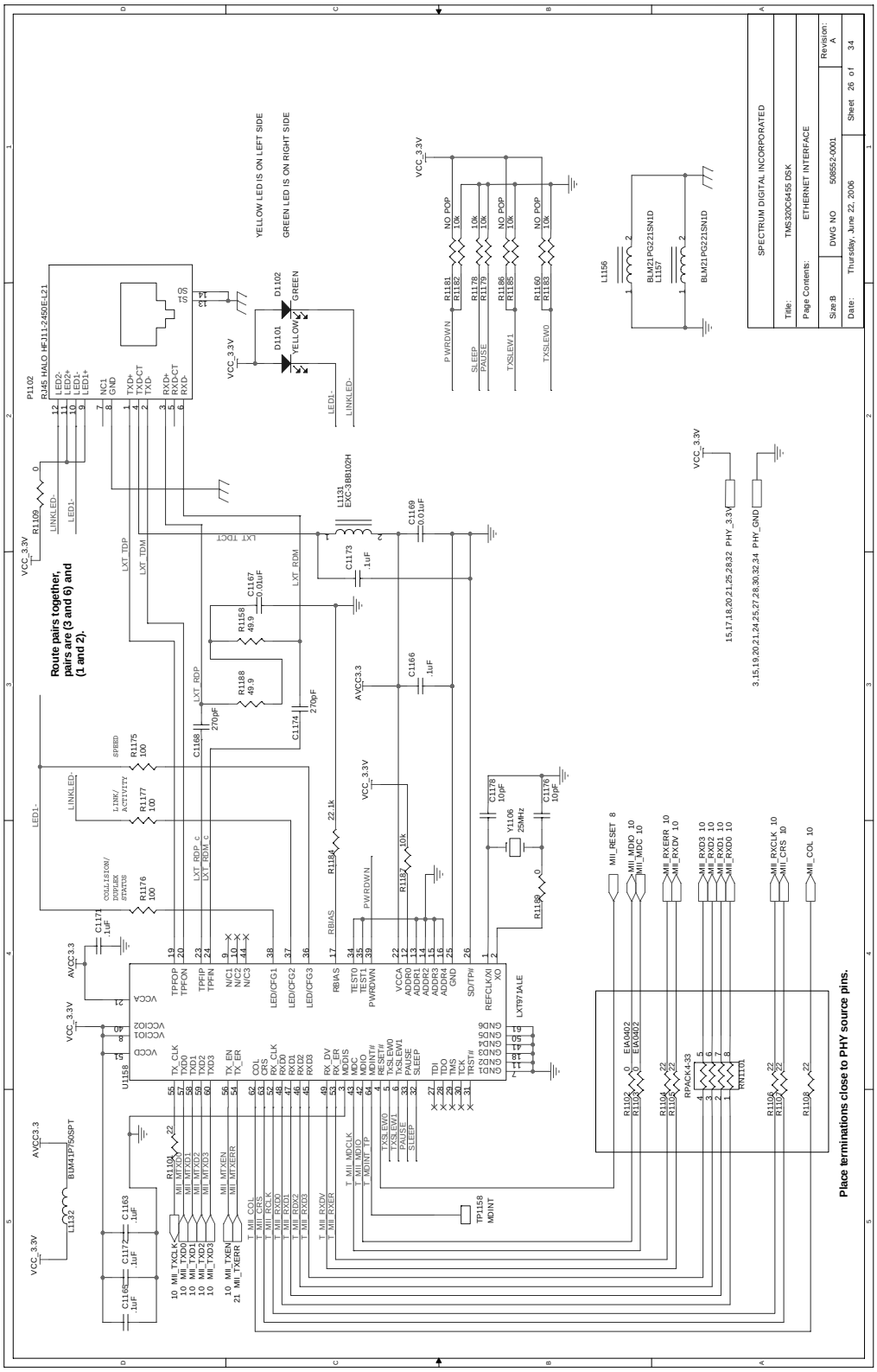

SPECTRUM DIGITAL INCORPORATED
Title: TMS320C6455 DSK
Page Contents: Hierarchial Blocks
Size:B DWG NO 508552-0001 Revision: A
Date: Thursday, June 22, 2006 Sheet 21 of 34
XUSB_Emu
T_TRSTn
T_TCK
T_TMS
T_TDI
T_TDO
T_EMU0
T_EMU1
T_TCK_RET
RESET_INn
DSP_RS_OUT_ODn
CLK_12MHZ
CLK_24MHZ
POWER SUPPLY
+5_VOLTS
GROUND
RESET_SW
VIO_3.3V
VCC_1.8V
VCC_1.5VIO
VIO_1.2V
VCC_1.2SRIO
PS_PORz
DVDD_1.8V
VCC_1.5V
DSP_CVDD
SRIO_VCC1.2
RD_PWR_ON_RSz
NO-POP
R10
PUSHB_RSn
SVS_RSTn
USB_DSP_RSTn
U11
SN74LVC1G32
C67
.1uF
R32
33
CODEC_CLK
AIC23 Audio
CODEC_SYSCLK
DATA_BCLK
DATA_SYNCIN
DATA_DIN
DATA_DOUT
DATA_SYNCOUT
CTL_DATA
CTL_CLK
CTL_CS
CTL_MODE
AIC23.3V
R516
0
R515
0
DSPA_I2C_SDA
DSPA_I2C_SCL
MII_PHY
PHY_3.3V
PHY_GND
MII_RESET
MII_MDIO
MII_MDC
MII_TXEN
MII_TXCLK
MII_TXD0
MII_TXD1
MII_TXD2
MII_TXD3
MII_TXERR
MII_COL
MII_RXCLK
MII_RXD0
MII_RXD1
MII_RXD2
MII_RXD3
MII_RXDV
MII_CRS
MII_RXERR
R517
1.5k
MII_RESETz
DSPA.MDIO
DSPA.MDC
DSPA.MTXEN
DSPA.MTCLK
DSPA.MTXD0
DSPA.MTXD1
DSPA.MTXD2
DSPA.MTXD3
DSPA.MCOL
DSPA.MRCLK
DSPA.MRXD0
DSPA.MRXD1
DSPA.MRXD2
DSPA.MRXD3
DSPA.MRXDV
DSPA.MCRS
DSPA.MRXER

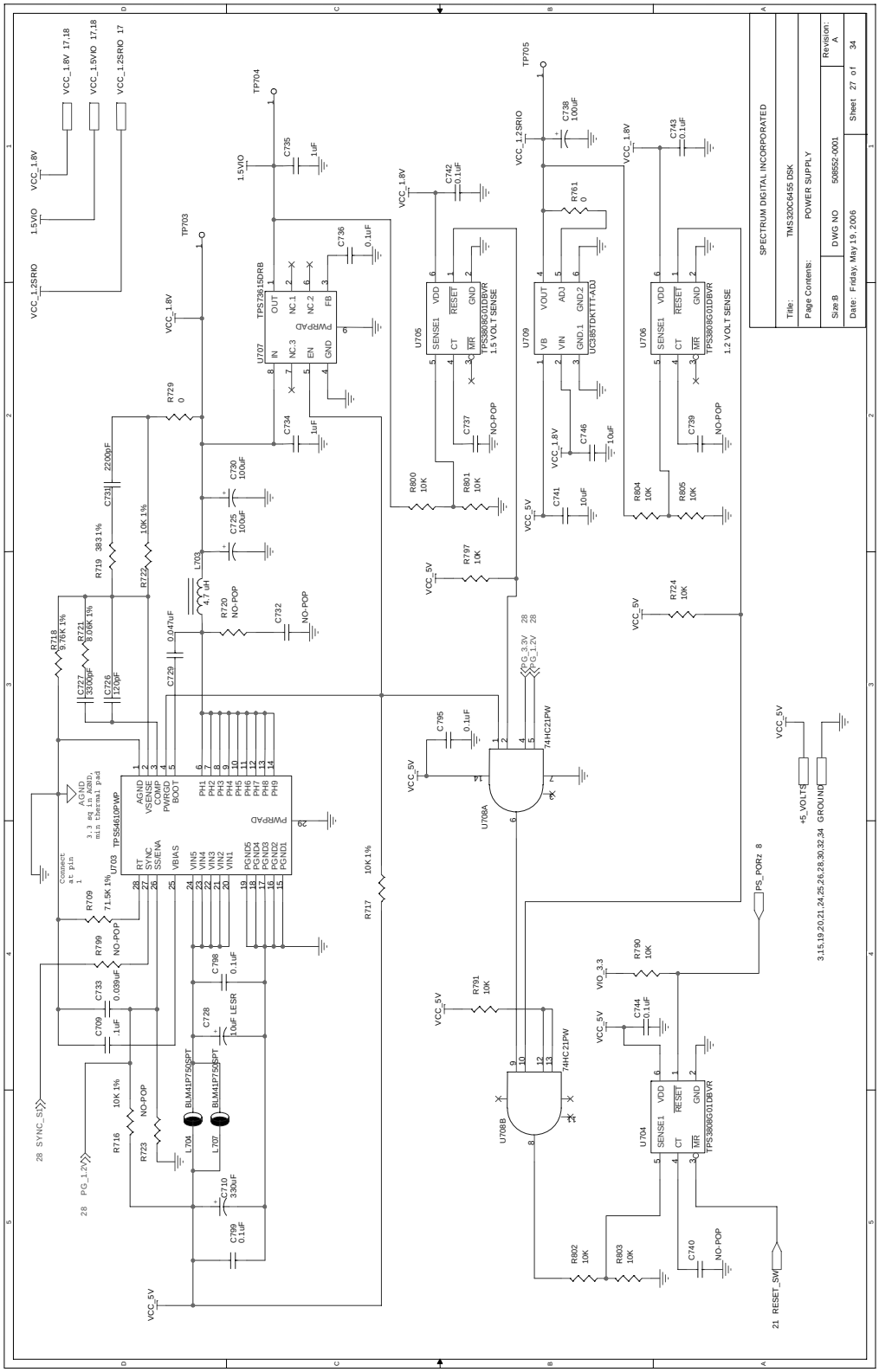

All capacitors on this sheet are decoupling capacitors for the DSP. They should be placed as close as possible to the DSP.
DSP_CVDD
DGND
3.3V
SPECTRUM DIGITAL INCORPORATED
Title: TMS320C6-455 DSK
Page Contents: Decoupling Caps
Size:B
DWG NO 508552-0001
Revision: A
Date: Monday, June 26, 2006
Sheet 22 of 34

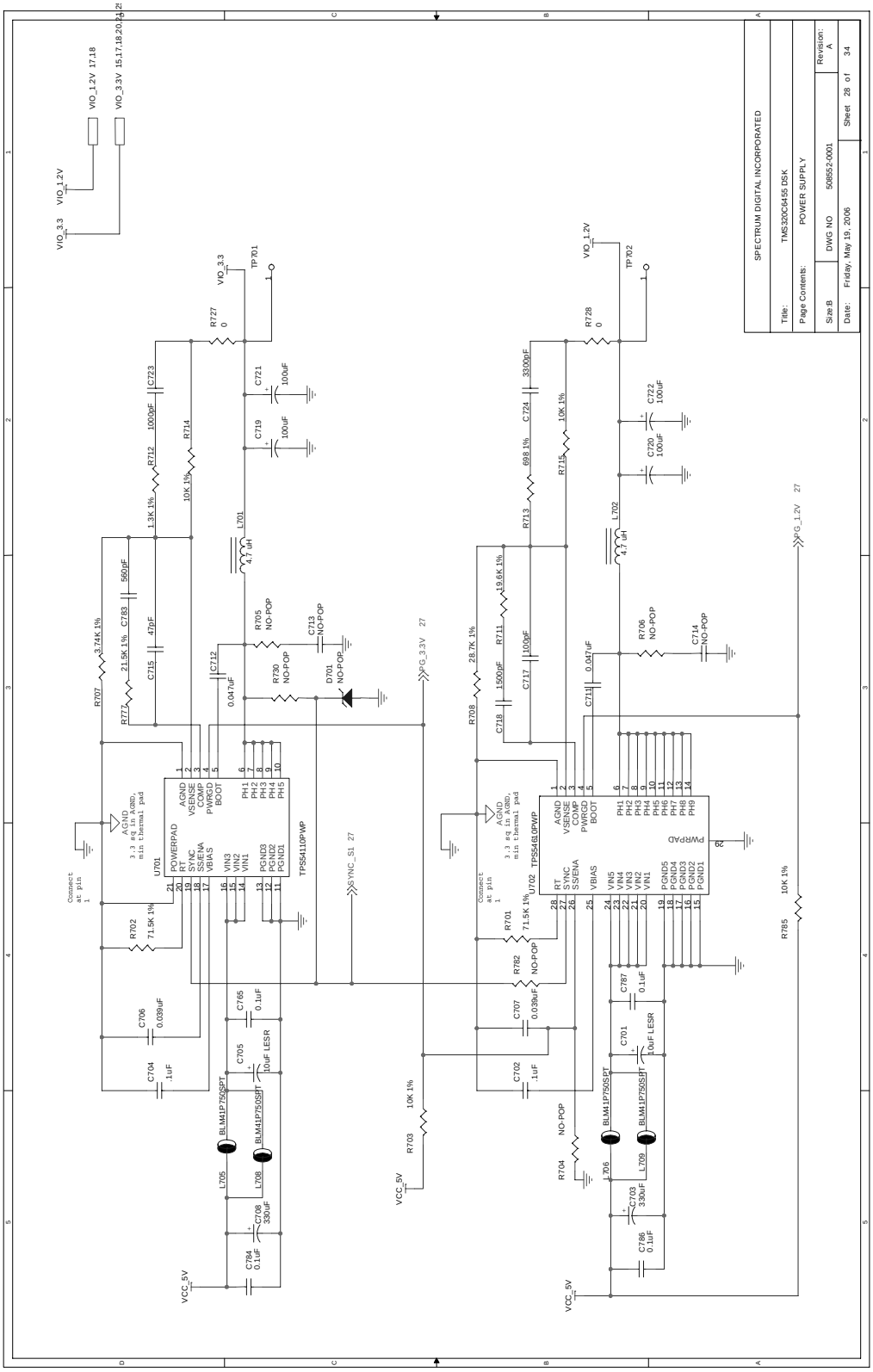

DVDD_1.8V
C195 470uF
C196 470uF
20
C197 0.1uF
C198 0.1uF
C199 0.1uF
C200 0.1uF
C201 0.1uF
C202 0.1uF
C203 0.1uF
C204 0.1uF
C205 0.1uF
C206 0.1uF
C207 0.1uF
C208 0.1uF
C209 560pF
C210 560pF
C211 560pF
C212 560pF
C213 560pF
C214 560pF
C215 560pF
C216 560pF
DGND
SRIO_VCC1.2
C217 10uF
C218 10uF
C219 10uF
9
C220 0.1uF
C221 0.1uF
C222 0.1uF
C223 0.1uF
C224 0.1uF
C225 0.1uF
C226 560pF
C227 560pF
C228 560pF
DGND
VCC_1.5V
C229 10uF
C230 10uF
C231 0.1uF
7
C232 0.1uF
C233 0.1uF
C234 0.1uF
C235 560pF
C236 560pF
C237 560pF
C238 560pF
DGND
SPECTRUM DIGITAL INCORPORATED
Title: TMS320C6455 DSK
Page Contents: Decoupling Caps II
Size:B DWG NO 508552-0001 Revision: A
Date: Monday, June 26, 2006 Sheet 23 of 34


SPECTRUM DIGITAL INCORPORATED
Title: TMS320C6455 DSK
Page Contents: Power Input
Size:B DWG NO 508552-0001 Revision: A
Date: Monday, June 26, 2006 Sheet 24 of 34
PUSHB_RS 8
PUSHB_RSn 21
U9 SN74AHC1G14
U8 SN74AHC1G14
C 95 0.1 uF
C119 0.1uF
R 94 10K
D11 MMBD4148
R83 33
SW2
RESET PUSHBUTTON
3.3V
DGND
TP1
TP2
TP3
TP4
TP5
TP6
TP7
TP8
TP9
0.025 OHMS FOR POWER MEASUREMENT
SYSTEM POWER MEASUREMENT POINTS. R IS 25/2 BODY, 6 VIAS FROM PAD TO PLANE
R99
5V
R52 220
D3 GREEN
TP32 TP
JP4 NO-POP
POWER INPUT
J5
CENTER
SHAFT
SLEEVE
2.5 MM JACK PJ-SM-712
TO BE POPULATED BY YOU IF THE USER IF NEEDED.
12V
-12V
J6
+5
GND
-12
+12
NO-POP Molex 15-24-4041
WARNING:
DO NOT SUPPLY POWER TO BOTH POWER CONNECTORS AT THE SAME TIME!
KEEP TRACES A MINIMUM OF 0.070 IN CHES FROM THESE HOLES.
DAUGHTERCARD STANDOFF GROUNDING
M1 125 PH
M2 125 PH
M3 125 PH
M4 125 PH


SPECTRUM DIGITAL INCORPORATED
Title: TMS320C6455 DSK
Page Contents: Aic23 Audio
Size:B DWG NO 508552-0001 Revision: A
Date: Friday, May 19, 2006 Sheet 25 of 34
U1307 TLV320AIC23
U1301 12MHz
J1301 Microphone In
J1303 Line In
J1302 Head Phone Out
J1304 Line Out
L1301 HZ0805E601R
L1302 BLM21P221SN
L1303 BLM21P221SN
L1304 BLM21P221SN
L1305 BLM21P221SN
L1306 BLM21P221SN
L1307 BLM21P221SN
L1308 BLM21P221SN
L1309 BLM21P221SN
L1318 BLM21P221SN
RN1314 10K
RN1315 10K
RN1316 33
CODEC_SYSCLK 21
AIC23CLK
Control Port
3,9,14 CTL_DATA
3,9,14 CTL_CLK
21 CTL_CS
21 CTL_MODE
11 DATA_DIN
11 DATA_SYNCIN
11 DATA_BCLK
11 DATA_DOUT
11 DATA_SYNCOUT
15,17,18,20,21,26,28,32 AIC3.3V
3,15,19,20,21,24,26,27,28,30,32,34 GND


SPECTRUM DIGITAL INCORPORATED
Title: TMS320C6455 DSK
Page Contents: ETHERNET INTERFACE
Size:B DWG NO 50855-2-0001 Revision: A
Date: Thursday, June 22, 2006 Sheet 26 of 34
Route pairs together, pairs are (3 and 6) and (1 and 2).
Place terminations close to PHY source pins.
YELLOW LED IS ON LEFT SIDE
GREEN LED IS ON RIGHT SIDE
P1102
RJ45 HALO HFJ11-2450E-L21
U1158
LXT971ALE
Y1106
25MHz
L1131
EXC-3BB102H
L1132
BLM41PG50SPT
L1156
BLM21PG221SN1D
L1157
BLM21PG221SN1D
D1101
YELLOW
D1102
GREEN
VCC_3.3V
AVCC3.3
PHY_3.3V
PHY_GND
MII_RESET 8
MII_MDIO 10
MII_MDC 10
MII_RXERR 10
MII_RXDV 10
MII_RXD3 10
MII_RXD2 10
MII_RXD1 10
MII_RXD0 10
MII_RXCLK 10
MII_CRS 10
MII_COL 10
10 MII_TXCLK
10 MII_TXD0
10 MII_TXD1
10 MII_TXD2
10 MII_TXD3
10 MII_TXEN
21 MII_TXERR
TP1158
MDINT
RPACK4-33
RN1101
EA0402
LXT_TDP
LXT_TDM
LXT_TDCT
LXT_RDM
LXT_RDP
LXT_RDP_c
LXT_RDM_c
LINKLED-
LED1-
SPEED
LINK/ACTIVITY
COLLISION/FULLDUPLEX STATUS
PWRDWN
RBIAS
AVCC3.3
15,17,18,20,21,25,28,32 PHY_3.3V
3,15,19,20,21,24,25,27,28,30,32,34 PHY_GND

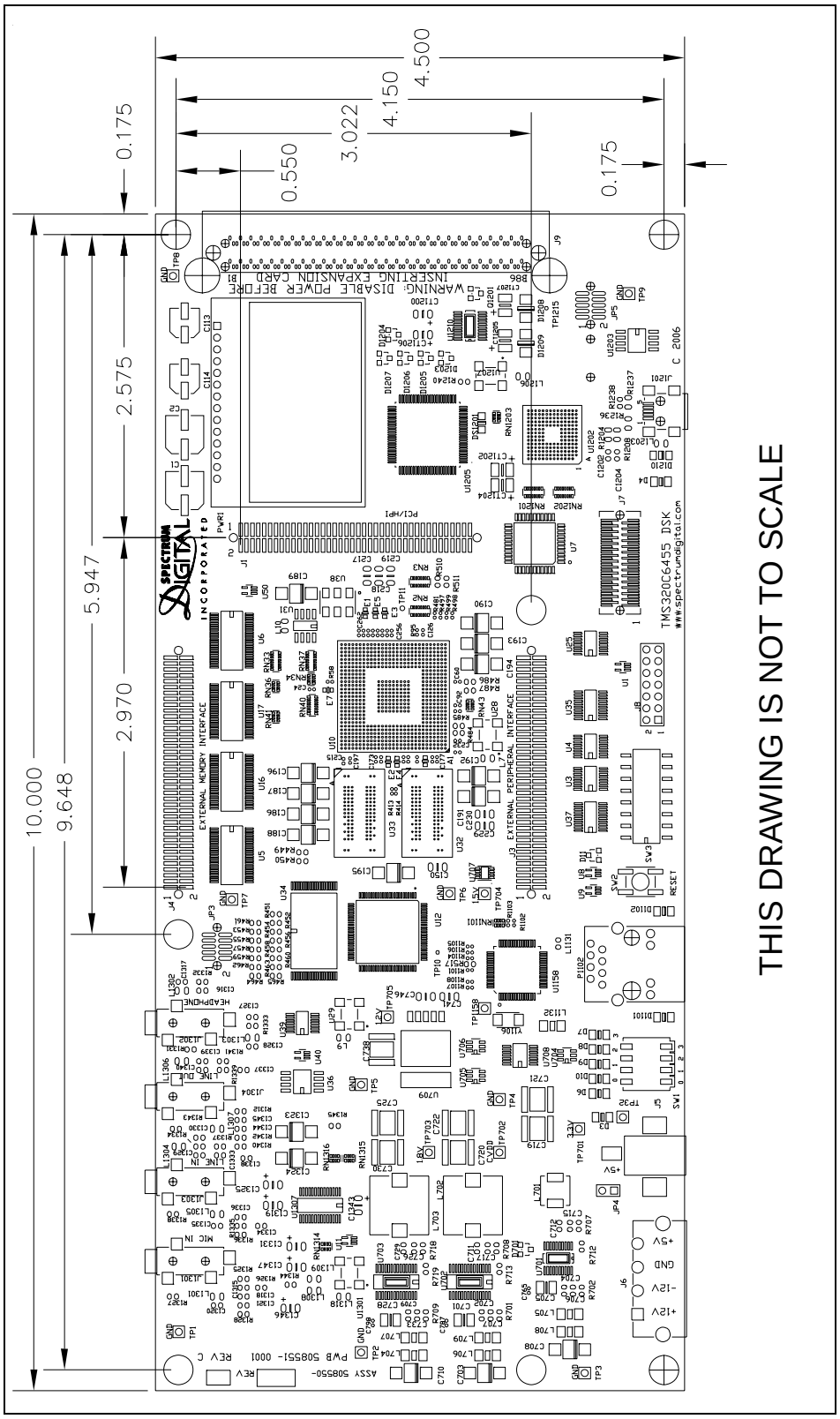

SPECTRUM DIGITAL INCORPORATED
Title: TMS320C6455 DSK
Page Contents: POWER SUPPLY
Size:B
DWG NO 506552-0001
Revision: A
Date: Friday, May 19, 2006
Sheet 27 of 34
VCC_1.8V 17,18
VCC_1.5VIO 17,18
VCC_1.25RIO 17
1.5VIO
TP704
TP703
TP705
C735 1uF
C736 0.1uF
TPS73615DRB
PWRPAD
U707
C734 1uF
R729 0
C730 100uF
C725 100uF
L703 4.7 uH
R720 NO-POP
C732 NO-POP
C729 0.047uF
C731 2200pF
R719 383 1%
R732 10K 1%
R718 9.76K 1%
R721 8.06K 1%
C727 3300pF
C726 1270pF
TPS54610PWP
U703
AGND
VSENSE
COMP
PWRPAD
BOOT
RT
SYNC
SS/ENA
VBIAS
VIN5
VIN4
VIN3
VIN2
VIN1
PGND5
PGND4
PGND3
PGND2
PGND1
PH1
PH2
PH3
PH4
PH5
PH6
PH7
PH8
PH9
Connect at pin 1
AGND 3.3 eq in AGND, min thermal pad
R709 71.5K 1%
R799 NO-POP
C733 0.039uF
C709 1uF
C798 0.1uF
C728 10uF LESR
BLM41P750SPT
L704
L707
C710 330uF
C799 0.1uF
R716 10K 1%
R723 NO-POP
28 SYNC_S
28 PG_1.2V
VCC_5V
R717 10K 1%
U705
SENSE1
CT
RESET
MR
VDD
GND
TPS3808G01DBVR
1.5 VOLT SENSE
C742 0.1uF
C737 NO-POP
R800 10K
R801 10K
R797 10K
U709
VB
VIN
VOUT
ADJ
GND.1
GND.2
UC3857DKTTT-ADJ
R761 0
C738 100uF
C746 10uF
C741 10uF
U706
1.2 VOLT SENSE
C743 0.1uF
C739 NO-POP
R804 10K
R805 10K
R724 10K
PG_3.3V 28
PG_1.2V 28
C795 0.1uF
74HC21PW
U708A
U708B
R791 10K
R790 10K
VIO_3.3
C744 0.1uF
U704
C740 NO-POP
R802 10K
R803 10K
PS_PORz 8
21 RESET_SW
+5_VOLTS
GROUND
3,15,19,20,21,24,25,26,28,30,32,34


SPECTRUM DIGITAL INCORPORATED
Title: TMS320C6455 DSK
Page Contents: POWER SUPPLY
Size:B DWG NO 508552-0001 Revision: A
Date: Friday, May 19, 2006 Sheet 28 of 34
VIO_1.2V 17,18
VIO_3.3V 15,17,18,20,21
VIO_1.2V
VIO_3.3
TP701
TP702
U701
TPS54110PWP
U702
TPS54610PWP
L701
L702
L705
L706
L708
L709
D701
VCC_5V
PG_3.3V 27
PG_1.2V 27
SYNC_S1 27

Appendix B

Mechanical Information

This appendix contains the mechanical information about the TMS320C6455 DSK produced by Spectrum Digital.


4.500
4.150
3.022
0.550
0.175
0.175
2.575
5.947
2.970
10.000
9.648
THIS DRAWING IS NOT TO SCALE

Printed in U.S.A., September 2006
508555-0001 Rev. C