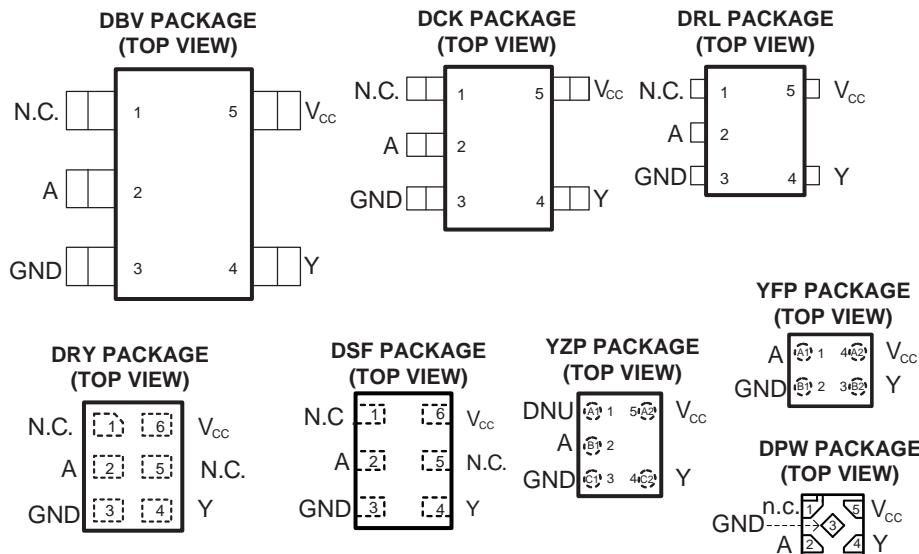


## LOW-POWER SINGLE BUFFER GATE

Check for Samples: [SN74AUP1G34](#)

### FEATURES

- Available in the Texas Instruments NanoStar™ Package
- Low Static-Power Consumption;  $I_{cc} = 0.9 \mu A$  Max
- Low Dynamic-Power Consumption;  $C_{pd} = 4.1 \text{ pF}$  Typ at 3.3 V
- Low Input Capacitance;  $C_i = 1.5 \text{ pF}$  Typ
- Low Noise - Overshoot and Undershoot <10% of  $V_{cc}$
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Input Hysteresis Allows Slow Input Transition and Better Switching Noise Immunity at the Input ( $V_{hys} = 250 \text{ mV}$  Typ at 3.3 V)
- Wide Operating  $V_{cc}$  Range of 0.8 V to 3.6 V
- Optimized for 3.3-V Operation
- 3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation
- $t_{pd} = 4.1 \text{ ns}$  Max at 3.3 V
- Suitable for Point-to-Point Applications
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)



N.C. – No internal connection

See mechanical drawings for dimensions.

### DESCRIPTION/ORDERING INFORMATION

The AUP family is TI's premier solution to the industry's low-power needs in battery-powered portable applications. This family ensures a very low static and dynamic power consumption across the entire  $V_{cc}$  range of 0.8 V to 3.6 V resulting in an increased battery life. This product also maintains excellent signal integrity (see [Figure 1](#) and [Figure 2](#)).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NanoStar is a trademark of Texas Instruments.

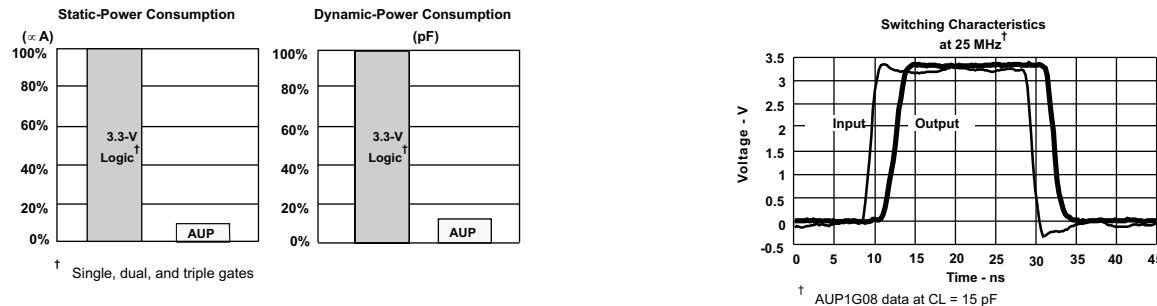


Figure 1. AUP – The Lowest-Power Family

Figure 2. Excellent Signal Integrity

This single buffer gate performs the Boolean function  $Y = A$  in positive logic.

NanoStar™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

#### ORDERING INFORMATION<sup>(1)</sup>

$T_A$	PACKAGE <sup>(2)</sup>	ORDERABLE PART NUMBER	TOP-SIDE MARKING <sup>(3)</sup>
-40°C to 85°C	NanoStar – WCSP (DSBGA) 0.23-mm Large Bump – YFP	Reel of 3000	SN74AUP1G34YFPR
	NanoStar – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)	Reel of 3000	SN74AUP1G34YZPR
	QFN – DRY	Reel of 5000	SN74AUP1G34DRYR
	uQFN – DSF	Reel of 5000	SN74AUP1G34DSFR
	uQFN – DPW	Reel of 5000	SN74AUP1G34DPWR
	SOT (SOT-23) – DBV	Reel of 3000	SN74AUP1G34DBVR
	SOT (SC-70) – DCK	Reel of 3000	SN74AUP1G34DCKR
	SOT (SOT-553) – DRL	Reel of 4000	SN74AUP1G34DRLR

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).

(2) Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).

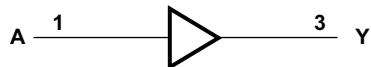
(3) DBV/DCK/DRL: The actual top-side marking has one additional character that designates the wafer fab/assembly site.

YFP/YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the wafer fab/assembly site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).

#### FUNCTION TABLE

INPUT A	OUTPUT Y
H	H
L	L

Figure 3. LOGIC DIAGRAM (POSITIVE LOGIC)  
(DBV, DCK, DRL, DRY, and YZP PACKAGES)

**Figure 4. LOGIC DIAGRAM (POSITIVE LOGIC)  
(YFP PACKAGE)**

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage range	-0.5	4.6	V
$V_I$	Input voltage range <sup>(2)</sup>	-0.5	4.6	V
$V_O$	Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup>	-0.5	4.6	V
$V_O$	Output voltage range in the high or low state <sup>(2)</sup>	-0.5	$V_{CC} + 0.5$	V
$I_{IK}$	Input clamp current	$V_I < 0$	-50	mA
$I_{OK}$	Output clamp current	$V_O < 0$	-50	mA
$I_O$	Continuous output current		$\pm 20$	mA
	Continuous current through $V_{CC}$ or GND		$\pm 50$	mA
$\theta_{JA}$	Package thermal impedance <sup>(3)</sup>	DBV package	206	°C/W
		DCK package	252	
		DRL package	142	
		DSF package	300	
		DRY package	234	
		YFP/YZP package	132	
$T_{stg}$	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS<sup>(1)</sup>

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	0.8	3.6	V
$V_{IH}$	High-level input voltage	$V_{CC} = 0.8 \text{ V}$	$V_{CC}$	V
		$V_{CC} = 1.1 \text{ V to } 1.95 \text{ V}$	$0.65 \times V_{CC}$	
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.6	
		$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$	2	
$V_{IL}$	Low-level input voltage	$V_{CC} = 0.8 \text{ V}$	0	V
		$V_{CC} = 1.1 \text{ V to } 1.95 \text{ V}$	$0.35 \times V_{CC}$	
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	0.7	
		$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$	0.9	
$V_I$	Input voltage	0	3.6	V
$V_O$	Output voltage	0	$V_{CC}$	V
$I_{OH}$ <sup>(2)</sup>	High-level output current	$V_{CC} = 0.8 \text{ V}$	-20	μA
		$V_{CC} = 1.1 \text{ V}$	-1.1	
		$V_{CC} = 1.4 \text{ V}$	-1.7	
		$V_{CC} = 1.65 \text{ V}$	-1.9	
		$V_{CC} = 2.3 \text{ V}$	-3.1	
		$V_{CC} = 3 \text{ V}$	-4	
$I_{OL}$ <sup>(2)</sup>	Low-level output current	$V_{CC} = 0.8 \text{ V}$	20	μA
		$V_{CC} = 1.1 \text{ V}$	1.1	
		$V_{CC} = 1.4 \text{ V}$	1.7	
		$V_{CC} = 1.65 \text{ V}$	1.9	
		$V_{CC} = 2.3 \text{ V}$	3.1	
		$V_{CC} = 3 \text{ V}$	4	
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 0.8 \text{ V to } 3.6 \text{ V}$	200	ns/V
$T_A$	Operating free-air temperature		-40	85 °C

(1) All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

(2) Defined by the signal integrity requirements and design goal priorities

## ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			T <sub>A</sub> = -40°C to 85°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = -20 µA	0.8 V to 3.6 V	V <sub>CC</sub> – 0.1			V <sub>CC</sub> – 0.1		V
	I <sub>OH</sub> = -1.1 mA	1.1 V	0.75 × V <sub>CC</sub>			0.7 × V <sub>CC</sub>		
	I <sub>OH</sub> = -1.7 mA	1.4 V		1.11			1.03	
	I <sub>OH</sub> = -1.9 mA	1.65 V		1.32			1.3	
	I <sub>OH</sub> = -2.3 mA	2.3 V		2.05			1.97	
	I <sub>OH</sub> = -3.1 mA			1.9			1.85	
	I <sub>OH</sub> = -2.7 mA	3 V		2.72			2.67	
	I <sub>OH</sub> = -4 mA			2.6			2.55	
V <sub>OL</sub>	I <sub>OL</sub> = 20 µA	0.8 V to 3.6 V			0.1		0.1	V
	I <sub>OL</sub> = 1.1 mA	1.1 V			0.3 × V <sub>CC</sub>		0.3 × V <sub>CC</sub>	
	I <sub>OL</sub> = 1.7 mA	1.4 V			0.31		0.37	
	I <sub>OL</sub> = 1.9 mA	1.65 V			0.31		0.35	
	I <sub>OL</sub> = 2.3 mA				0.31		0.33	
	I <sub>OL</sub> = 3.1 mA	2.3 V			0.44		0.45	
	I <sub>OL</sub> = 2.7 mA				0.31		0.33	
	I <sub>OL</sub> = 4 mA	3 V			0.44		0.45	
I <sub>I</sub>	A input	V <sub>I</sub> = GND to 3.6 V	0 V to 3.6 V			0.1		0.5 µA
I <sub>off</sub>		V <sub>I</sub> or V <sub>O</sub> = 0 V to 3.6 V	0 V			0.2		0.6 µA
ΔI <sub>off</sub>		V <sub>I</sub> or V <sub>O</sub> = 0 V to 3.6 V	0 V to 0.2 V			0.2		0.6 µA
I <sub>CC</sub>	V <sub>I</sub> = GND or (V <sub>CC</sub> to 3.6 V)	I <sub>O</sub> = 0	0.8 V to 3.6 V			0.5		0.9 µA
ΔI <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> – 0.6 V	I <sub>O</sub> = 0	3.3 V			40		50 µA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	0 V		1.5				pF
		3.6 V		1.5				
C <sub>o</sub>	V <sub>O</sub> = GND	0 V		2.5				pF

## SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, C<sub>L</sub> = 5 pF (unless otherwise noted) (see [Figure 5](#) and [Figure 6](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub>	T <sub>A</sub> = 25°C			T <sub>A</sub> = -40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t <sub>pd</sub>	A	Y	0.8 V	1.8	14.5	27.4			ns
			1.2 V ± 0.1 V	3	5.6	11.2	0.4	13.9	
			1.5 V ± 0.1 V	2.5	4	7.2	0.7	9.2	
			1.8 V ± 0.15 V	2.2	3.2	6	0.8	7.3	
			2.5 V ± 0.2 V	1.8	2.4	3.9	0.6	5.1	
			3.3 V ± 0.3 V	1.4	2	3.2	0.6	4.1	

## SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range,  $C_L = 10 \text{ pF}$  (unless otherwise noted) (see [Figure 5](#) and [Figure 6](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC}$	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C to } 85^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	
$t_{pd}$	A	Y	0.8 V	2.7	16.6	28.2			ns
			$1.2 \text{ V} \pm 0.1 \text{ V}$	3.6	6.6	12.7	0.3	15.4	
			$1.5 \text{ V} \pm 0.1 \text{ V}$	3	4.8	8.3	1.2	10.3	
			$1.8 \text{ V} \pm 0.15 \text{ V}$	2.7	3.9	6.9	1.3	8.3	
			$2.5 \text{ V} \pm 0.2 \text{ V}$	2.3	2.9	4.5	1.2	5.8	
			$3.3 \text{ V} \pm 0.3 \text{ V}$	2	2.4	3.8	1.1	4.8	

## SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range,  $C_L = 15 \text{ pF}$  (unless otherwise noted) (see [Figure 5](#) and [Figure 6](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC}$	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C to } 85^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	
$t_{pd}$	A	Y	0.8 V	5.1	18.6	30.2			ns
			$1.2 \text{ V} \pm 0.1 \text{ V}$	4.3	7.5	13.6	1.3	16.5	
			$1.5 \text{ V} \pm 0.1 \text{ V}$	3.6	5.5	9	1.9	11.2	
			$1.8 \text{ V} \pm 0.15 \text{ V}$	3.2	4.5	7.5	1.9	8.9	
			$2.5 \text{ V} \pm 0.2 \text{ V}$	2.6	3.4	5.2	1.7	6.5	
			$3.3 \text{ V} \pm 0.3 \text{ V}$	2.3	2.9	4.2	1.5	5	

## SWITCHING CHARACTERISTICS

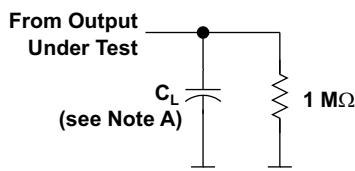
over recommended operating free-air temperature range,  $C_L = 30 \text{ pF}$  (unless otherwise noted) (see [Figure 5](#) and [Figure 6](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC}$	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C to } 85^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	
$t_{pd}$	A	Y	0.8 V	9.9	24.2	36.3			ns
			$1.2 \text{ V} \pm 0.1 \text{ V}$	6.3	10.1	16.3	3.6	18.9	
			$1.5 \text{ V} \pm 0.1 \text{ V}$	5.1	7.4	11	3.4	13	
			$1.8 \text{ V} \pm 0.15 \text{ V}$	4.5	6.1	9.3	3.2	10.6	
			$2.5 \text{ V} \pm 0.2 \text{ V}$	3.7	4.7	6.4	2.7	7.8	
			$3.3 \text{ V} \pm 0.3 \text{ V}$	3.3	4	5.3	2.5	6.5	

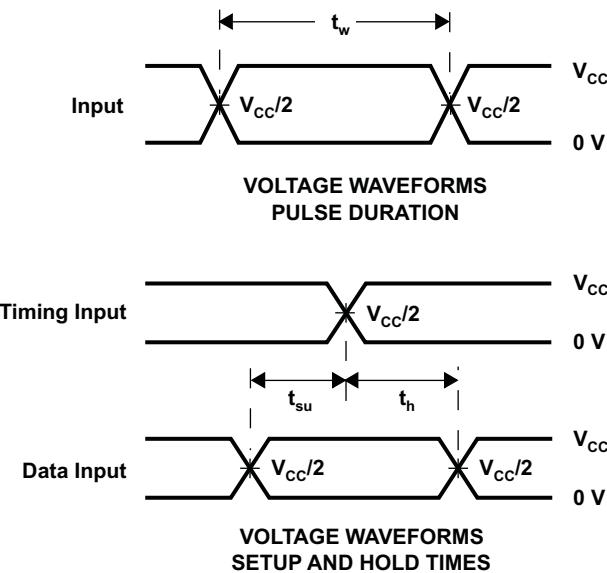
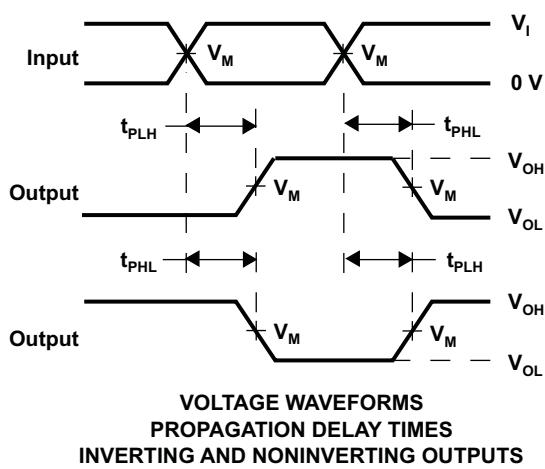
## OPERATING CHARACTERISTICS

$T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	$V_{CC}$	TYP	UNIT
$C_{pd}$ Power dissipation capacitance	$f = 10 \text{ MHz}$	0.8 V	3.8	pF
		$1.2 \text{ V} \pm 0.1 \text{ V}$	3.8	
		$1.5 \text{ V} \pm 0.1 \text{ V}$	3.8	
		$1.8 \text{ V} \pm 0.15 \text{ V}$	3.8	
		$2.5 \text{ V} \pm 0.2 \text{ V}$	3.9	
		$3.3 \text{ V} \pm 0.3 \text{ V}$	4.1	

**PARAMETER MEASUREMENT INFORMATION  
(Propagation Delays, Setup and Hold Times, and Pulse Width)**

**LOAD CIRCUIT**

	$V_{CC} = 0.8 \text{ V}$	$V_{CC} = 1.2 \text{ V} \pm 0.1 \text{ V}$	$V_{CC} = 1.5 \text{ V} \pm 0.1 \text{ V}$	$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$	$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$
$C_L$ $V_M$ $V_I$	5, 10, 15, 30 pF $V_{CC}/2$ $V_{CC}$	5, 10, 15, 30 pF $V_{CC}/2$ $V_{CC}$	5, 10, 15, 30 pF $V_{CC}/2$ $V_{CC}$			

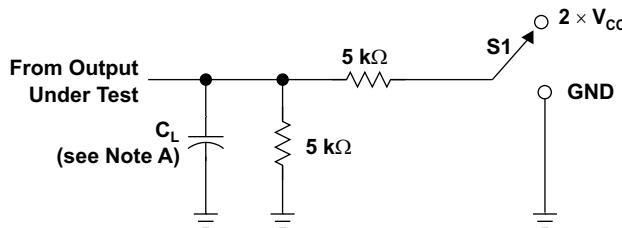


NOTES:

- A.  $C_L$  includes probe and jig capacitance.
- B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r/t_f = 3 \text{ ns}$ .
- C. The outputs are measured one at a time, with one transition per measurement.
- D.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
- E. All parameters and waveforms are not applicable to all devices.

**Figure 5. Load Circuit and Voltage Waveforms**

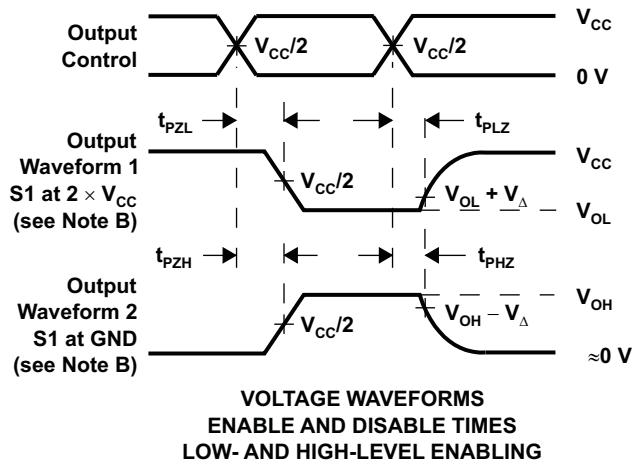
## PARAMETER MEASUREMENT INFORMATION (Enable and Disable Times)



TEST	S1
$t_{PLZ}/t_{PZL}$	$2 \times V_{CC}$
$t_{PHZ}/t_{PZH}$	GND

LOAD CIRCUIT

	$V_{CC} = 0.8 \text{ V}$	$V_{CC} = 1.2 \text{ V} \pm 0.1 \text{ V}$	$V_{CC} = 1.5 \text{ V} \pm 0.1 \text{ V}$	$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$	$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$
$C_L$	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
$V_M$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
$V_I$	$V_{CC}$	$V_{CC}$	$V_{CC}$	$V_{CC}$	$V_{CC}$	$V_{CC}$
$V_{\Delta}$	0.1 V	0.1 V	0.1 V	0.15 V	0.15 V	0.3 V



NOTES:

- A. CL includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ ,  $t_r/t_f = 3 \text{ ns}$ .
- D. The outputs are measured one at a time, with one transition per measurement.
- E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
- G. All parameters and waveforms are not applicable to all devices.

Figure 6. Load Circuit and Voltage Waveforms

## REVISION HISTORY

<b>Changes from Revision G (March 2010) to Revision H</b>	<b>Page</b>
• Added uQFN – DPW package option to the ORDERING INFORMATION table.	<a href="#">2</a>

<b>Changes from Revision H (October 2012) to Revision I</b>	<b>Page</b>
• Changed DPW package pinout	<a href="#">1</a>

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
SN74AUP1G34DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	H34R	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74AUP1G34DBVRE4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	H34R	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74AUP1G34DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	H34R	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74AUP1G34DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	H34R	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74AUP1G34DBVTE4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	H34R	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74AUP1G34DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	H34R	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74AUP1G34DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(H95 ~ H9F ~ H9K ~ H9R)	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74AUP1G34DCKRE4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(H95 ~ H9F ~ H9K ~ H9R)	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74AUP1G34DCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(H95 ~ H9F ~ H9K ~ H9R)	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74AUP1G34DCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(H95 ~ H9R)	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74AUP1G34DCKTE4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(H95 ~ H9R)	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74AUP1G34DCKTG4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(H95 ~ H9R)	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74AUP1G34DRLR	ACTIVE	SOT	DRL	5	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(H97 ~ H9R)	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74AUP1G34DRLRG4	ACTIVE	SOT	DRL	5	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(H97 ~ H9R)	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74AUP1G34DRYR	ACTIVE	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	H9	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74AUP1G34DSFR	ACTIVE	SON	DSF	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		H9	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74AUP1G34YFPR	ACTIVE	DSBGA	YFP	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM		H9 N	<span style="background-color: red; color: white; padding: 2px;">Samples</span>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
SN74AUP1G34YZPR	ACTIVE	DSBGA	YZP	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(H97 ~ H9N)	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

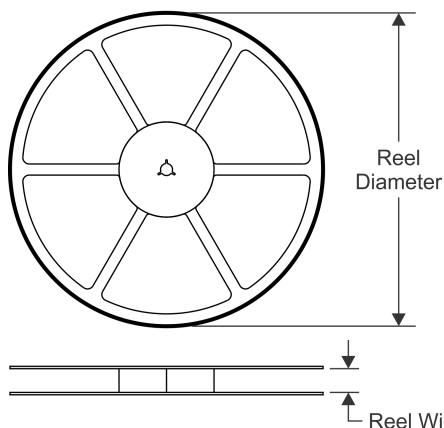
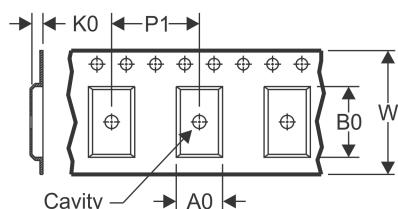
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

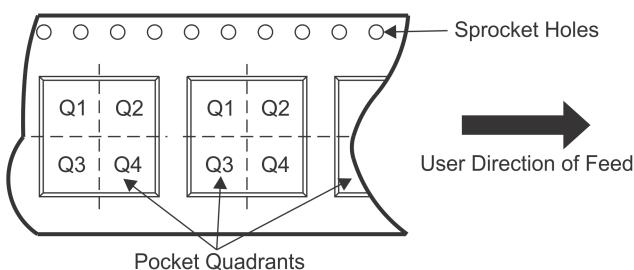
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUP1G34DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74AUP1G34DBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74AUP1G34DCKR	SC70	DCK	5	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74AUP1G34DCKR	SC70	DCK	5	3000	180.0	9.2	2.3	2.55	1.2	4.0	8.0	Q3
SN74AUP1G34DCKT	SC70	DCK	5	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74AUP1G34DRLR	SOT	DRL	5	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
SN74AUP1G34DRLR	SOT	DRL	5	4000	180.0	9.5	1.78	1.78	0.69	4.0	8.0	Q3
SN74AUP1G34DRYR	SON	DRY	6	5000	180.0	9.5	1.15	1.6	0.75	4.0	8.0	Q1
SN74AUP1G34DSFR	SON	DSF	6	5000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
SN74AUP1G34YFPR	DSBGA	YFP	4	3000	178.0	9.2	0.89	0.89	0.58	4.0	8.0	Q1
SN74AUP1G34YZPR	DSBGA	YZP	5	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1

**TAPE AND REEL BOX DIMENSIONS**

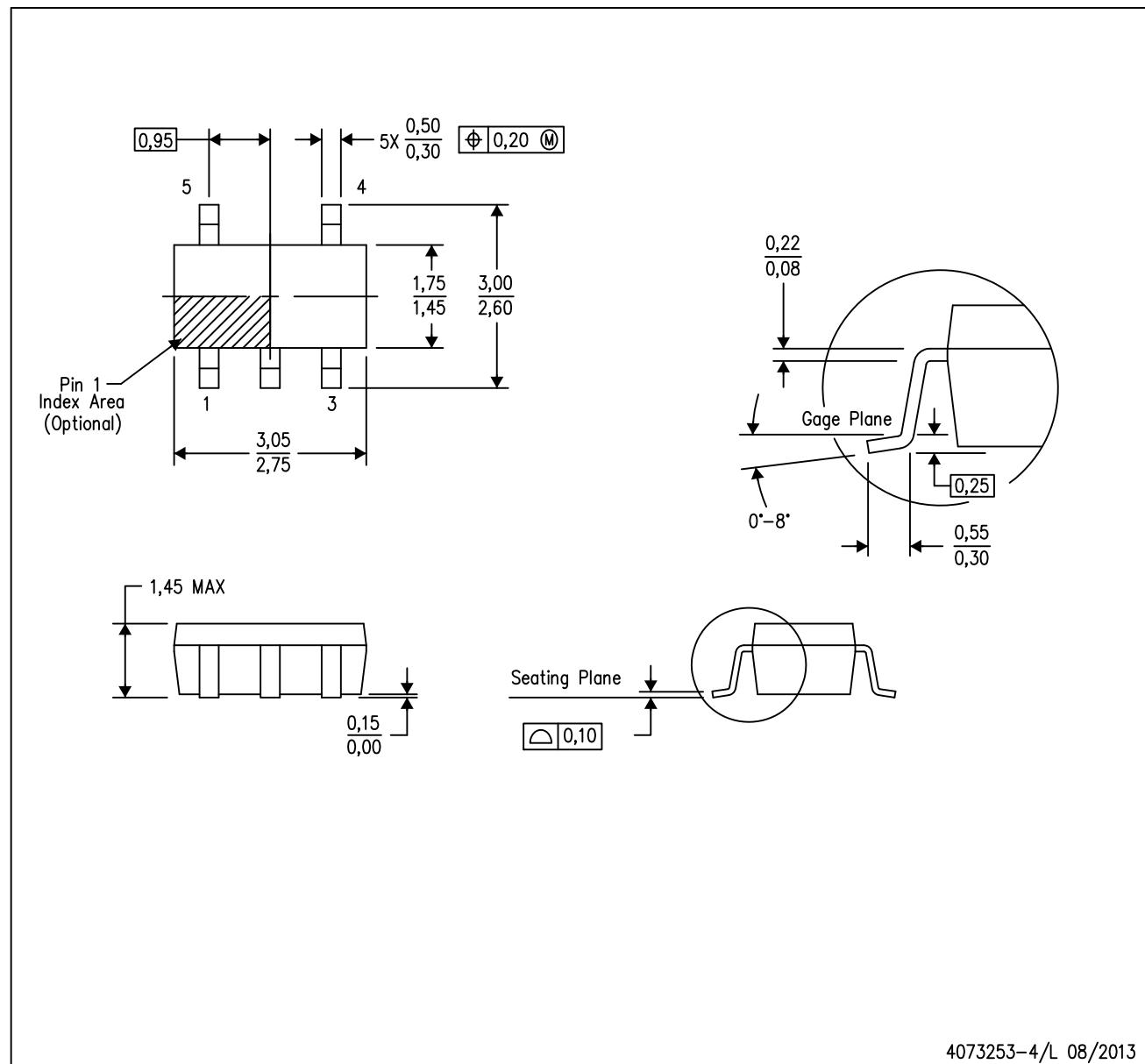

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUP1G34DBVR	SOT-23	DBV	5	3000	202.0	201.0	28.0
SN74AUP1G34DBVT	SOT-23	DBV	5	250	202.0	201.0	28.0
SN74AUP1G34DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74AUP1G34DCKR	SC70	DCK	5	3000	205.0	200.0	33.0
SN74AUP1G34DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74AUP1G34DRLR	SOT	DRL	5	4000	202.0	201.0	28.0
SN74AUP1G34DRLR	SOT	DRL	5	4000	180.0	180.0	30.0
SN74AUP1G34DRYR	SON	DRY	6	5000	180.0	180.0	30.0
SN74AUP1G34DSFR	SON	DSF	6	5000	180.0	180.0	30.0
SN74AUP1G34YFPR	DSBGA	YFP	4	3000	220.0	220.0	35.0
SN74AUP1G34YZPR	DSBGA	YZP	5	3000	220.0	220.0	35.0

## MECHANICAL DATA

DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



4073253-4/L 08/2013

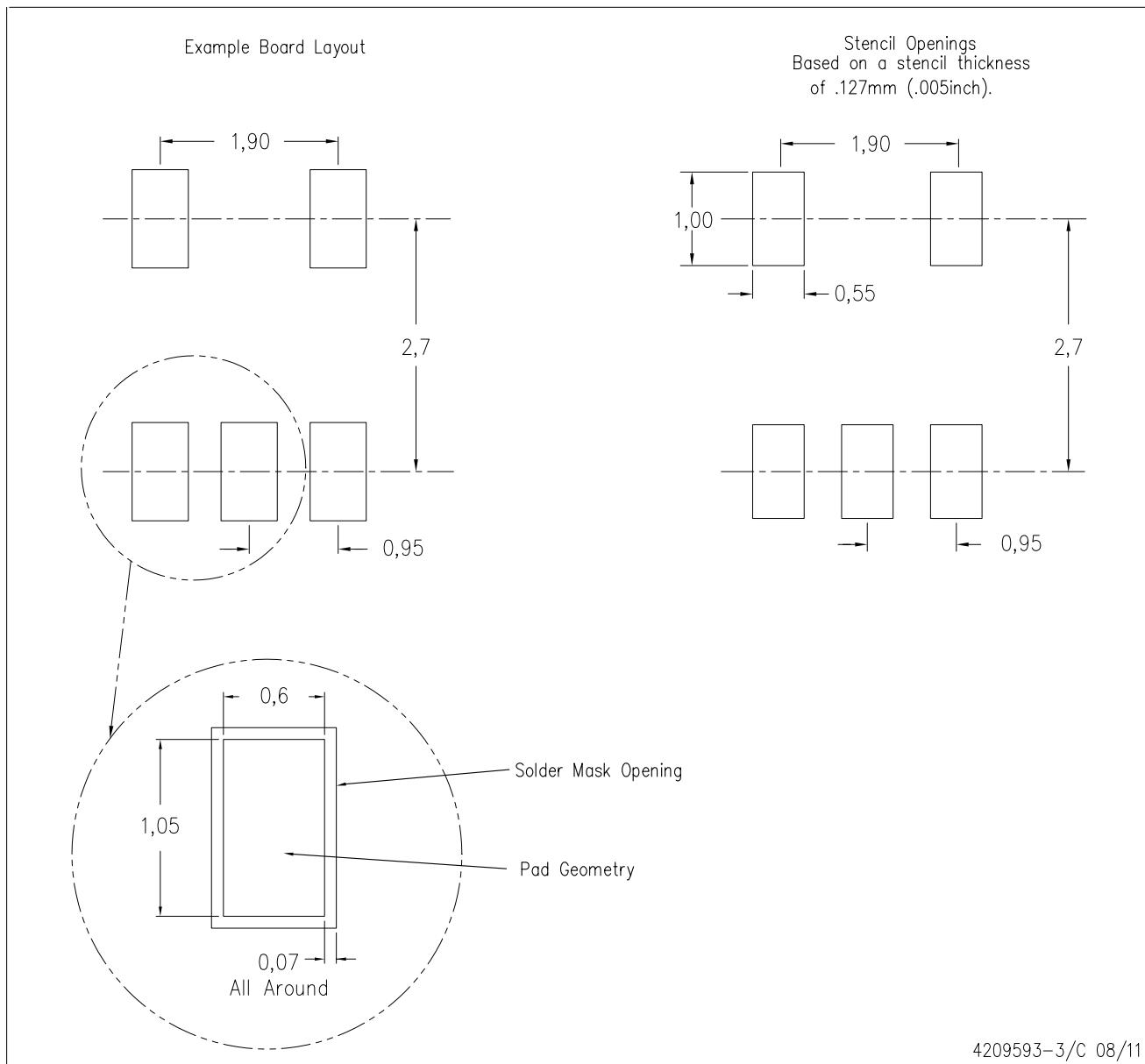
NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Falls within JEDEC MO-178 Variation AA.

# LAND PATTERN DATA

DBV (R-PDSO-G5)

PLASTIC SMALL OUTLINE

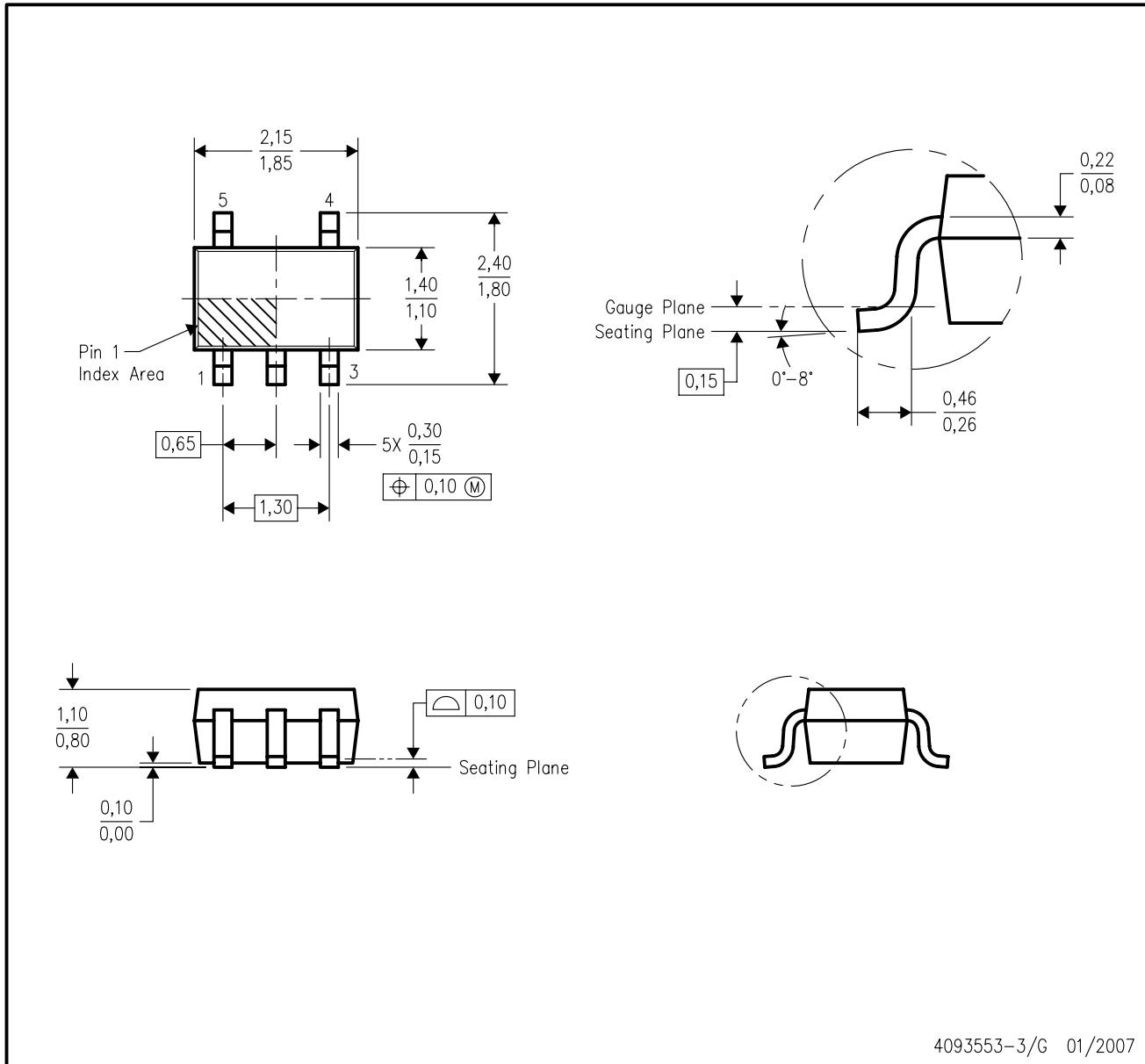


NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

## DCK (R-PDSO-G5)

## PLASTIC SMALL-OUTLINE PACKAGE



4093553-3/G 01/2007

NOTES:

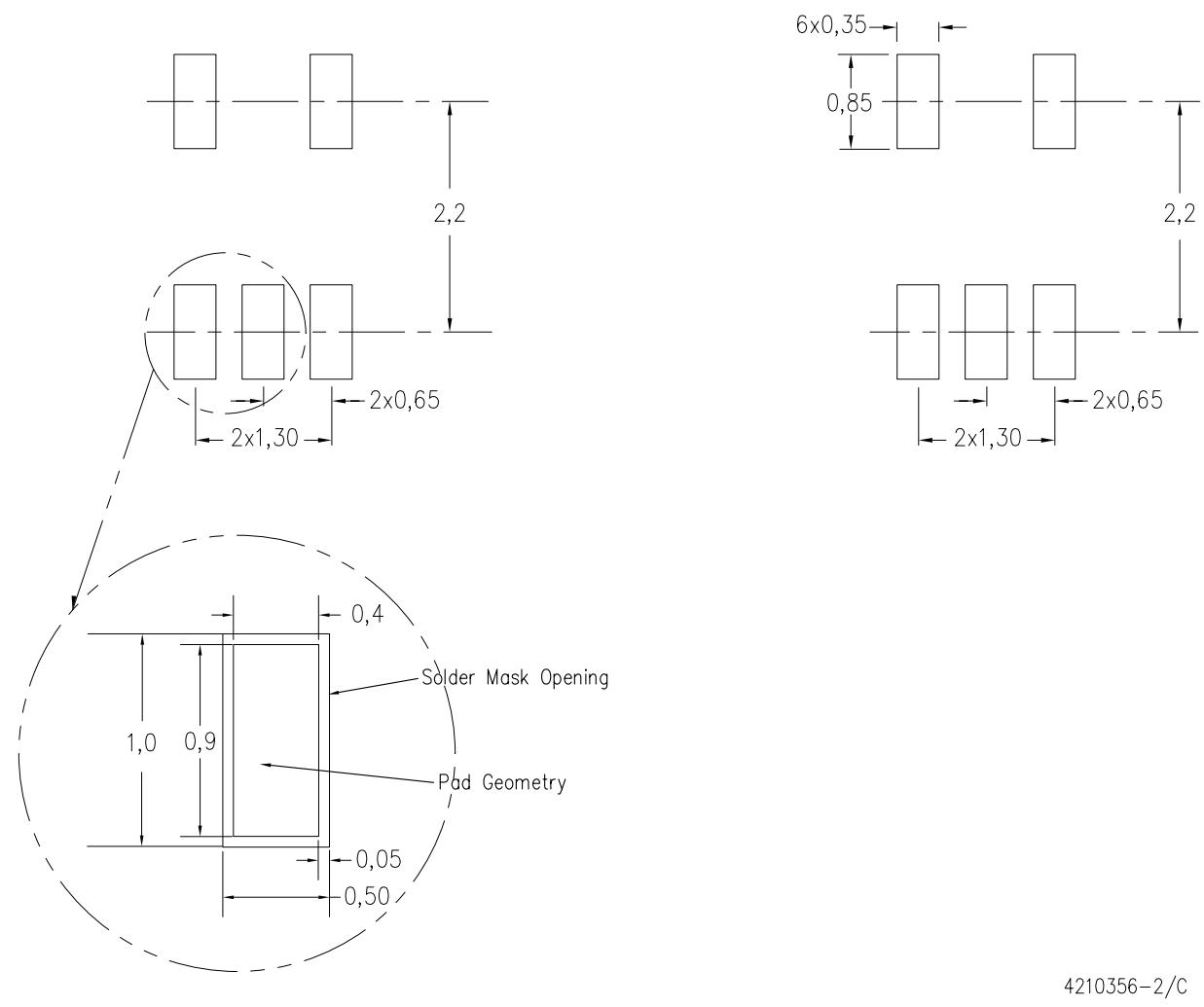
- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- Falls within JEDEC MO-203 variation AA.

DCK (R-PDSO-G5)

PLASTIC SMALL OUTLINE

Example Board Layout

Stencil Openings  
Based on a stencil thickness  
of .127mm (.005inch).

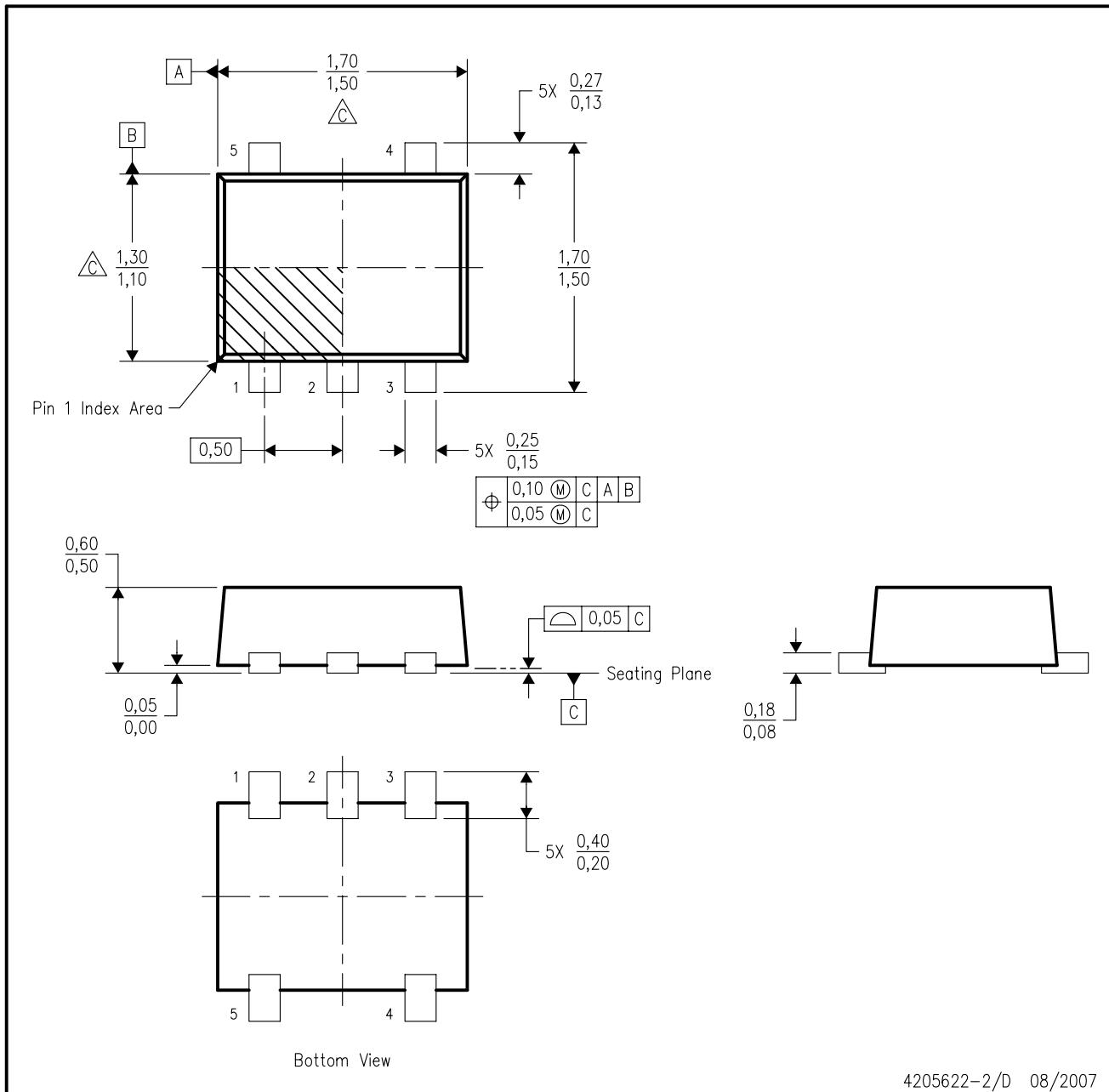


NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- Publication IPC-7351 is recommended for alternate designs.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

## DRL (R-PDSO-N5)

## PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.  
B. This drawing is subject to change without notice.

 THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.

 Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0,15 per end or side.

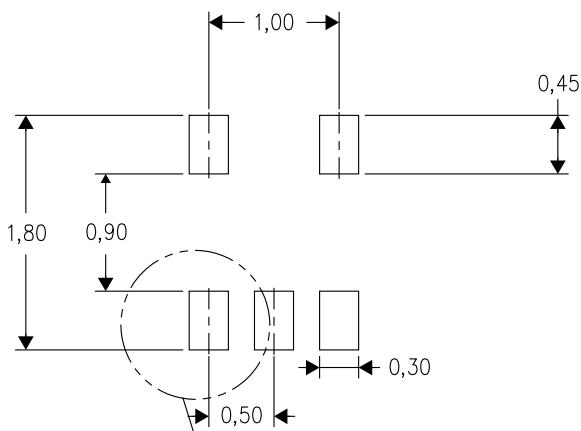
D. JEDEC package registration is pending.

D. JEDEC package registration is pending.

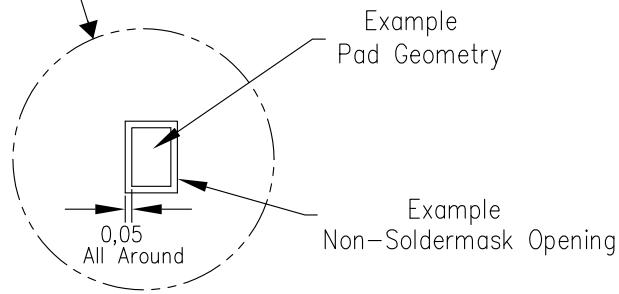
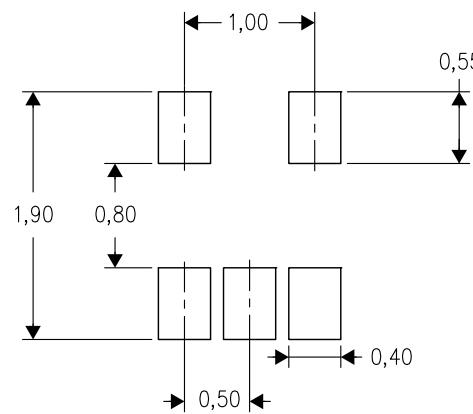
DRL (R-PDSO-N5)

PLASTIC SMALL OUTLINE

Example Board Layout



Example Non-Soldermask Defined Pad

Example Stencil Design  
(Note E)

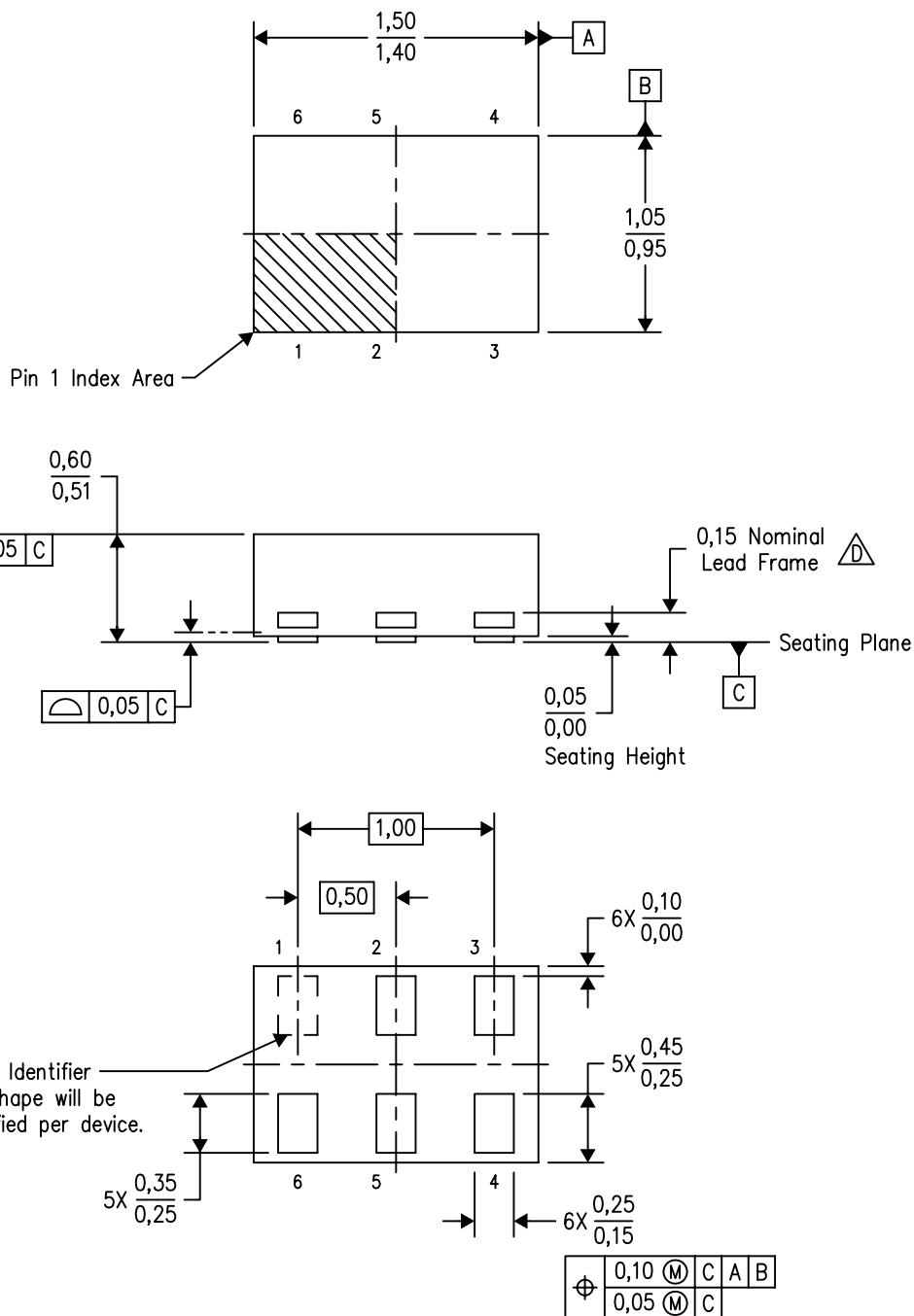
4208207-2/E 06/12

NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Publication IPC-7351 is recommended for alternate designs.
- Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
- Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- Side aperture dimensions over-print land for acceptable area ratio  $> 0.66$ . Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

DRY (R-PUSON-N6)

PLASTIC SMALL OUTLINE NO-LEAD



Bottom View

4207181/F 12/11

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

C. SON (Small Outline No-Lead) package configuration.

D. The exposed lead frame feature on side of package may or may not be present due to alternative lead frame designs.

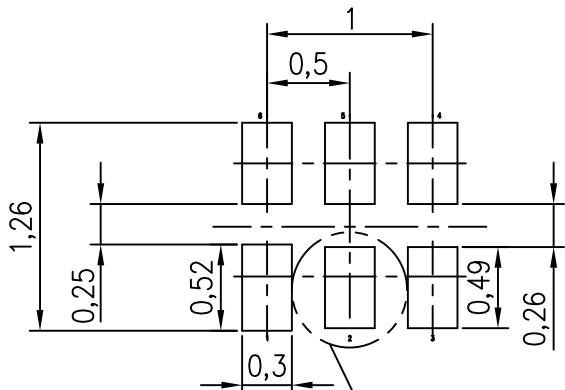
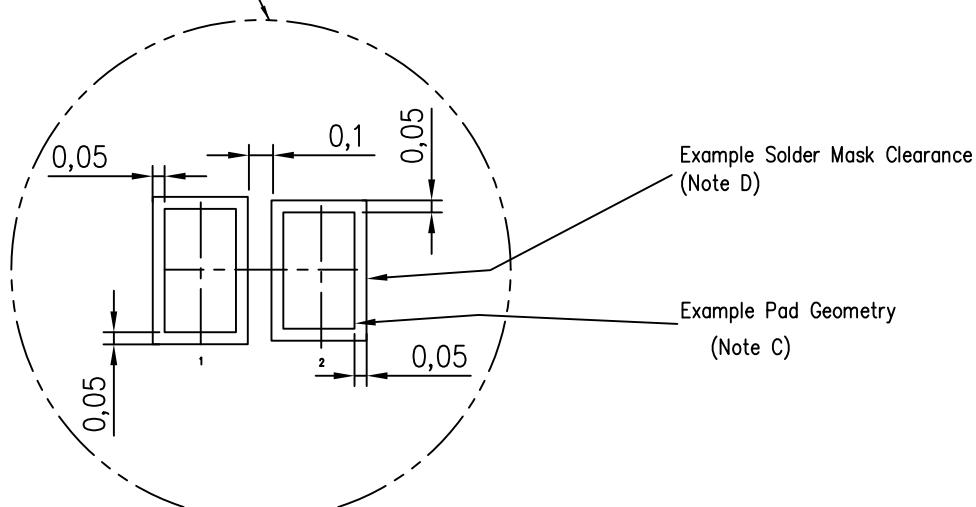
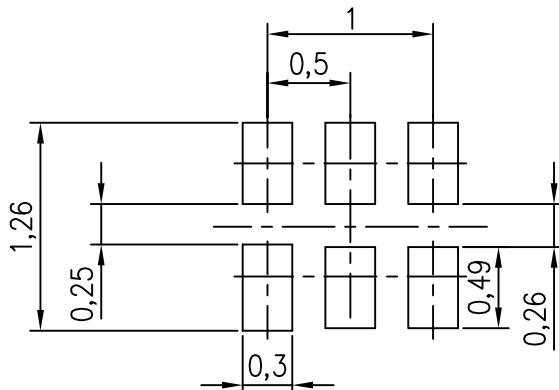
E. This package complies to JEDEC MO-287 variation UFAD.

F. See the additional figure in the Product Data Sheet for details regarding the pin 1 identifier shape.

DRY (R-PUSON-N6)

PLASTIC SMALL OUTLINE NO-LEAD

Example Board Layout

Example Stencil Design  
(Note E, F, G)

4208310/E 02/13

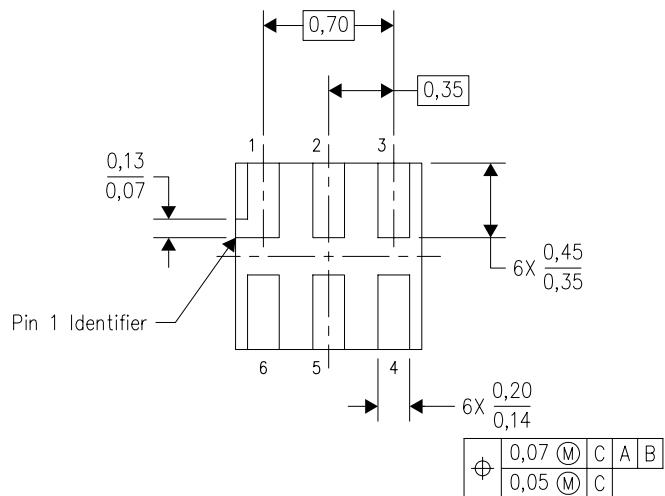
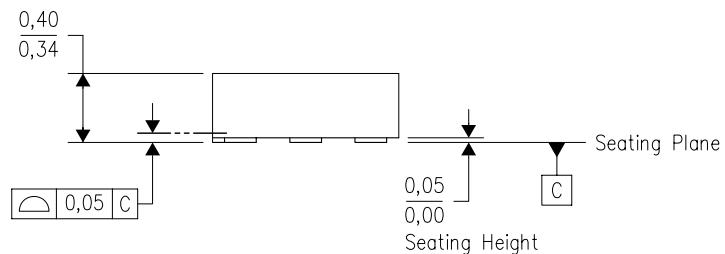
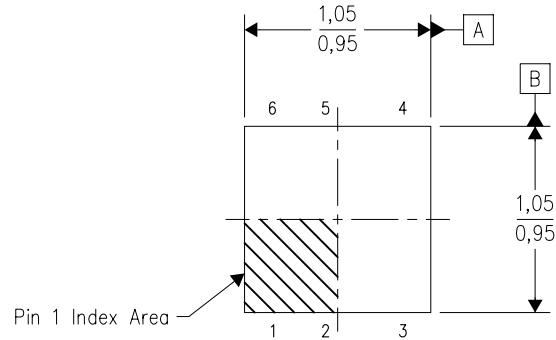
NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Publication IPC-7351 is recommended for alternate designs.
- Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
- Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- Side aperture dimensions over-print land for acceptable area ratio  $> 0.66$ . Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

## MECHANICAL DATA

DSF (S-PX2SON-N6)

PLASTIC SMALL OUTLINE NO-LEAD



Bottom View

4208186/E 03/11

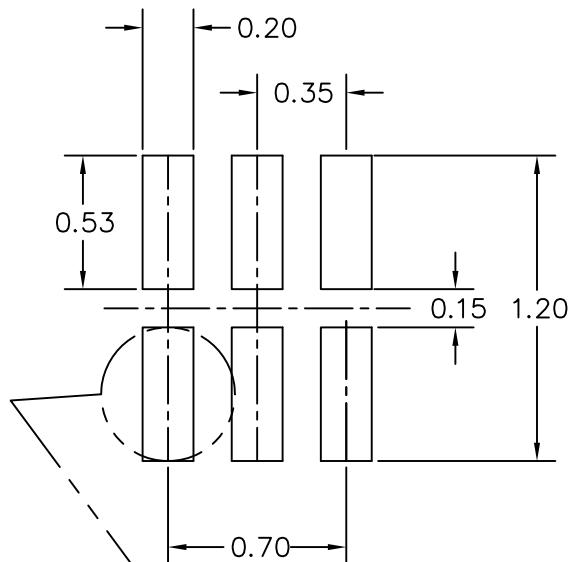
NOTES:

- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
- B. This drawing is subject to change without notice.
- C. SON (Small Outline No-Lead) package configuration.
- D. This package complies to JEDEC MO-287 variation X2AAF.

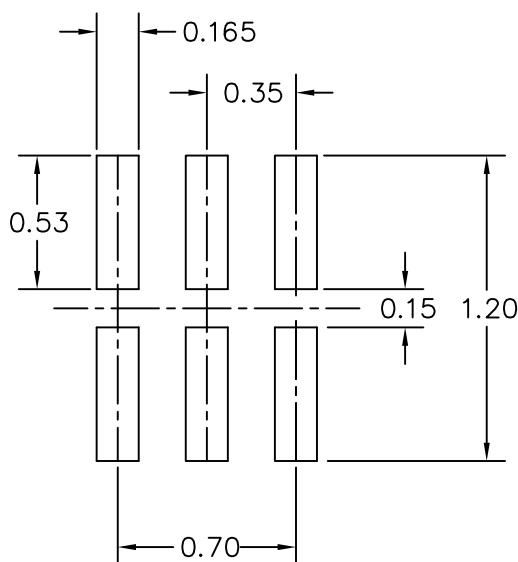
DSF (S-PX2SON-N6)

PLASTIC SMALL OUTLINE NO-LEAD

Land Pattern



Stencil Pattern



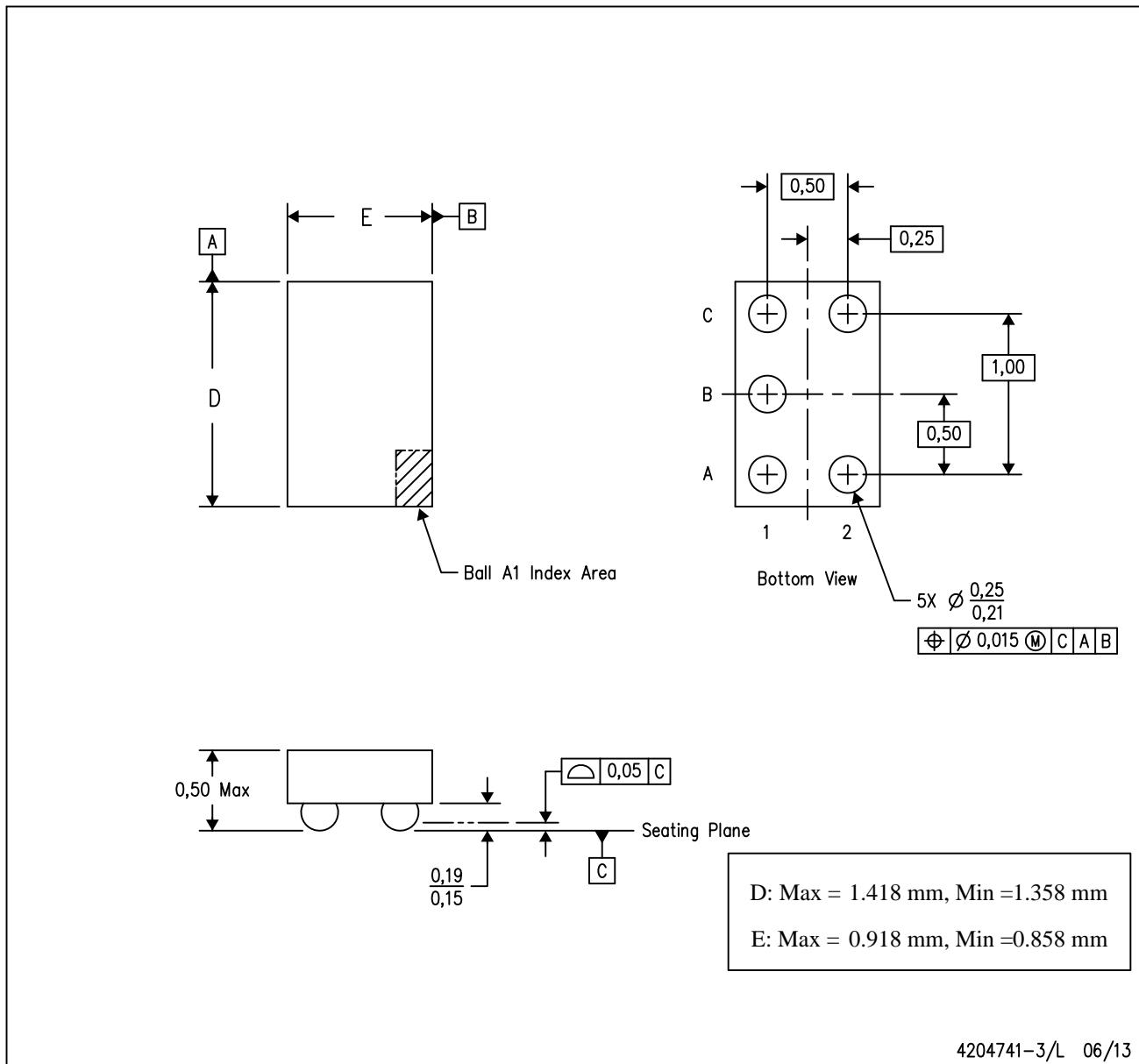
Contact your PCB vendor for  
allowable Solder Mask clearance (Notes C, D.)

4210277/D 05/12

NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Publication IPC-7351 is recommended for alternate designs.  
 D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.  
     If 2 mil solder mask is outside PCB vendor capability, it is advised to omit solder mask.  
 E. Maximum stencil thickness 0,1016 mm (4 mils). All linear dimensions are in millimeters.  
 F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.  
 G. Suggest stencils cut with lasers such as Fiber Laser that produce the greatest positional accuracy.  
 H. Component placement force should be minimized to prevent excessive paste block deformation.

YZP (R-XBGA-N5)

DIE-SIZE BALL GRID ARRAY



NOTES:

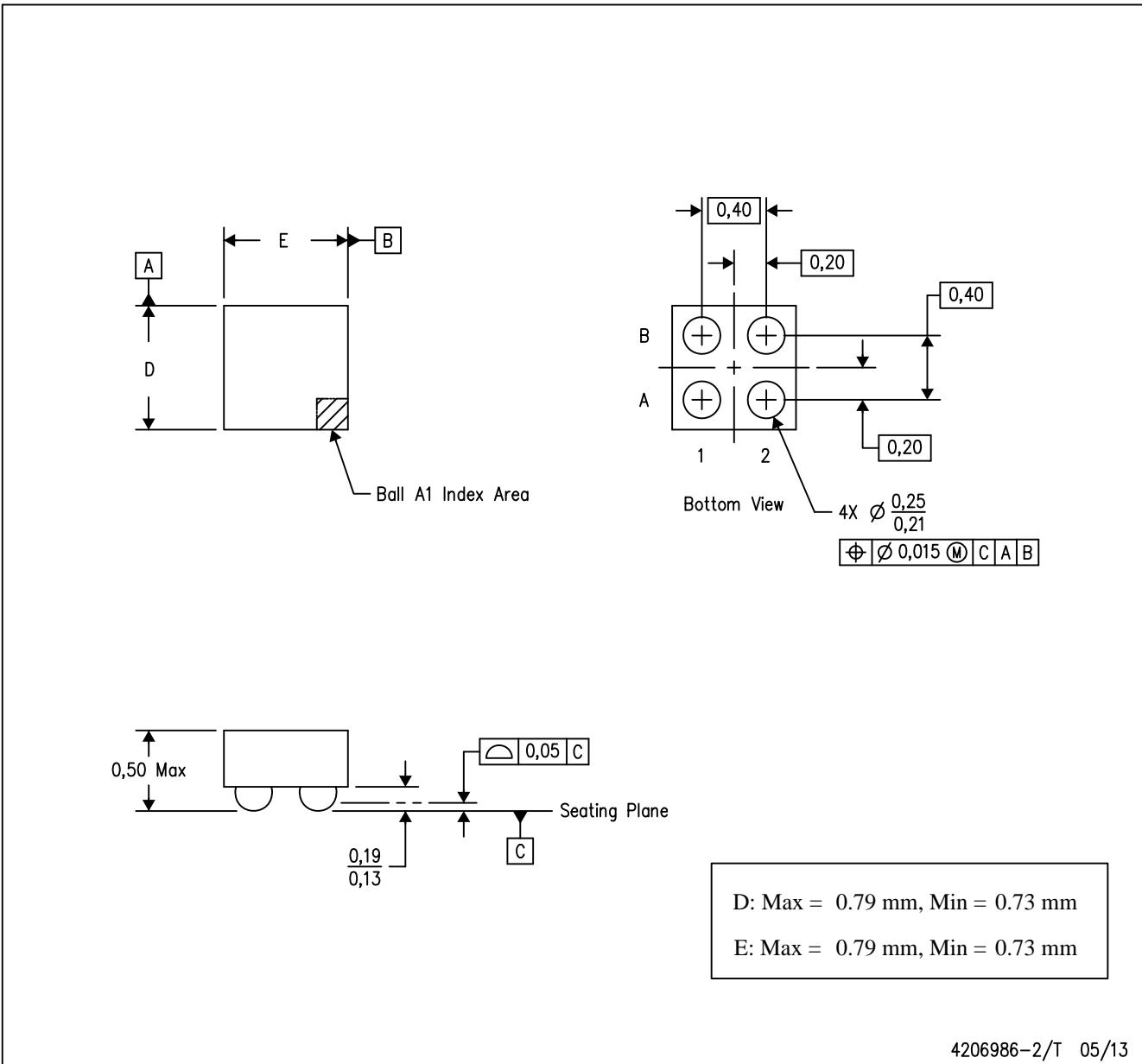
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
- This drawing is subject to change without notice.
- NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments.

## MECHANICAL DATA

YFP (S-XBGA-N4)

DIE-SIZE BALL GRID ARRAY



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Products	Applications
Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>
DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>
RFID	<a href="http://www.ti-rfid.com">www.ti-rfid.com</a>
OMAP Applications Processors	<a href="http://www.ti.com/omap">www.ti.com/omap</a>
Wireless Connectivity	<a href="http://www.ti.com/wirelessconnectivity">www.ti.com/wirelessconnectivity</a>
	<b>TI E2E Community</b>
	<a href="http://e2e.ti.com">e2e.ti.com</a>