

TrenchMOS™ transistor

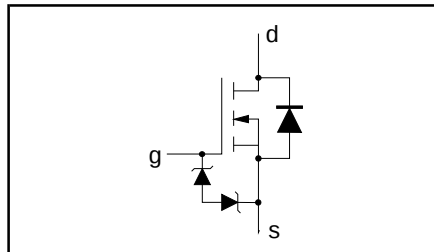
Logic level FET

PHP50N06LT, PHB50N06LT, PHD50N06LT

FEATURES

- 'Trench' technology
- Very low on-state resistance
- Fast switching
- Stable off-state characteristics
- High thermal cycling performance
- Low thermal resistance

SYMBOL



QUICK REFERENCE DATA

$V_{DSS} = 55 \text{ V}$
$I_D = 50 \text{ A}$
$R_{DS(ON)} \leq 24 \text{ m}\Omega \text{ (} V_{GS} = 5 \text{ V)}$
$R_{DS(ON)} \leq 22 \text{ m}\Omega \text{ (} V_{GS} = 10 \text{ V)}$

GENERAL DESCRIPTION

N-channel enhancement mode, logic level, field-effect power transistor in a plastic envelope using 'trench' technology. The device has very low on-state resistance. It is intended for use in dc to dc converters and general purpose switching applications.

The PHP50N06LT is supplied in the SOT78 (TO220AB) conventional lead package.

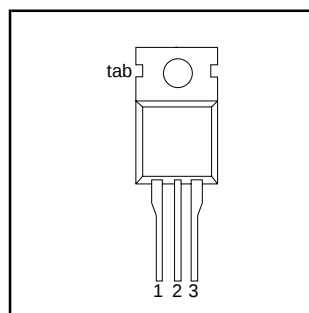
The PHB50N06LT is supplied in the SOT404 surface mounting package.

The PHD50N06LT is supplied in the SOT428 surface mounting package.

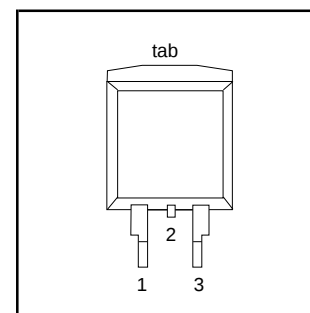
PINNING

PIN	DESCRIPTION
1	gate
2	drain ¹
3	source
tab	drain

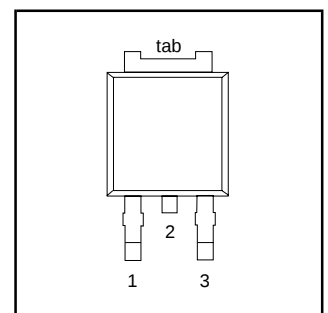
SOT78 (TO220AB)



SOT404



SOT428



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	$T_j = 25^\circ\text{C}$ to 175°C	-	55	V
V_{DGR}	Drain-gate voltage	$T_j = 25^\circ\text{C}$ to 175°C ; $R_{GS} = 20 \text{ k}\Omega$	-	55	V
V_{GS}	Gate-source voltage		-	± 13	V
I_D	Continuous drain current	$T_{mb} = 25^\circ\text{C}$	-	50	A
		$T_{mb} = 100^\circ\text{C}$	-	35	A
I_{DM}	Pulsed drain current	$T_{mb} = 25^\circ\text{C}$	-	200	A
P_D	Total power dissipation	$T_{mb} = 25^\circ\text{C}$	-	125	W
T_j, T_{stg}	Operating junction and storage temperature		- 55	175	$^\circ\text{C}$

¹ It is not possible to make connection to pin 2 of the SOT428 or SOT404 packages.

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THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j-mb}$	Thermal resistance junction to mounting base		-	1.2	K/W
$R_{th\ j-a}$	Thermal resistance junction to ambient	SOT78 package, in free air SOT404 and SOT428 package, pcb mounted, minimum footprint	60 50	- -	K/W K/W

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage, all pins	Human body model (100 pF, 1.5 kΩ)	-	2	kV

ELECTRICAL CHARACTERISTICS

 $T_j = 25^\circ\text{C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$; $I_D = 0.25\text{ mA}$; $T_j = -55^\circ\text{C}$	55 50	- -	- -	V V
$V_{(BR)GSS}$	Gate-source breakdown voltage	$I_G = \pm 1\text{ mA}$;	10	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	$V_{DS} = V_{GS}$; $I_D = 1\text{ mA}$ $T_j = 175^\circ\text{C}$ $T_j = -55^\circ\text{C}$	1.0 0.5 -	1.5 - -	2.0 - 2.3	V V V
$R_{DS(ON)}$	Drain-source on-state resistance	$V_{GS} = 5\text{ V}$; $I_D = 12.5\text{ A}$ $V_{GS} = 10\text{ V}$; $I_D = 12.5\text{ A}$ $T_j = 175^\circ\text{C}$	- - -	19 17 -	24 22 50	mΩ mΩ mΩ
g_{fs}	Forward transconductance	$V_{DS} = 25\text{ V}$; $I_D = 25\text{ A}$	15	40	-	S
I_{GSS}	Gate source leakage current	$V_{GS} = \pm 5\text{ V}$; $V_{DS} = 0\text{ V}$ $T_j = 175^\circ\text{C}$	- -	0.02 -	1 20	μA μA
I_{DSS}	Zero gate voltage drain current	$V_{DS} = 55\text{ V}$; $V_{GS} = 0\text{ V}$; $T_j = 175^\circ\text{C}$	- -	0.05 -	10 500	μA μA
$Q_{g(tot)}$	Total gate charge	$I_D = 50\text{ A}$; $V_{DD} = 44\text{ V}$; $V_{GS} = 5\text{ V}$	-	27	-	nC
Q_{gs}	Gate-source charge		-	4	-	nC
Q_{gd}	Gate-drain (Miller) charge		-	14	-	nC
t_{don}	Turn-on delay time	$V_{DD} = 30\text{ V}$; $I_D = 25\text{ A}$;	-	30	45	ns
t_r	Turn-on rise time	$V_{GS} = 5\text{ V}$; $R_G = 10\ \Omega$	-	80	130	ns
t_{doff}	Turn-off delay time	Resistive load	-	95	135	ns
t_f	Turn-off fall time		-	40	55	ns
L_d	Internal drain inductance	Measured from tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead to centre of die (SOT78 package only)	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	$V_{GS} = 0\text{ V}$; $V_{DS} = 25\text{ V}$; $f = 1\text{ MHz}$	-	1500	2000	pF
C_{oss}	Output capacitance		-	300	360	pF
C_{rss}	Feedback capacitance		-	150	200	pF

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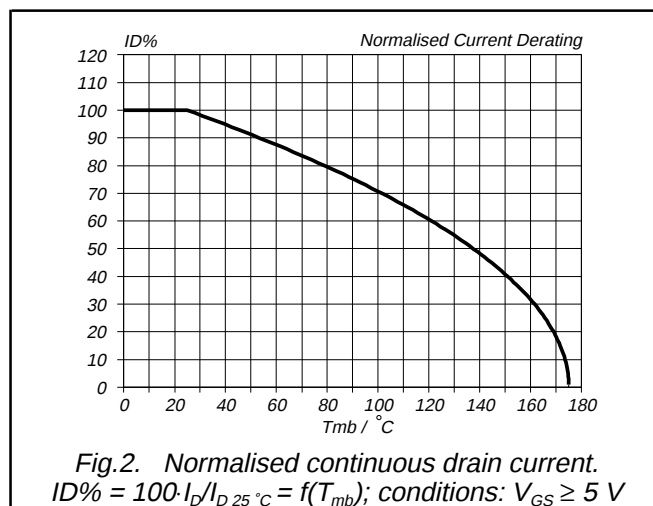
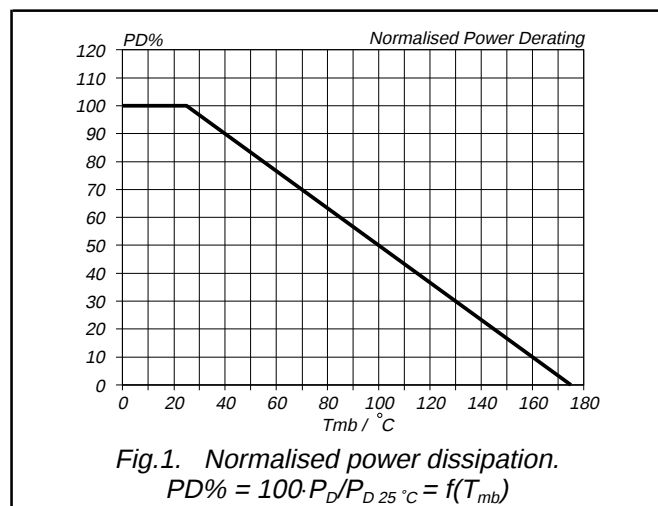
REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I _S	Continuous source current (body diode)		-	-	50	A
I _{SM}	Pulsed source current (body diode)		-	-	200	A
V _{SD}	Diode forward voltage	I _F = 25 A; V _{GS} = 0 V	-	0.95	1.2	V
		I _F = 40 A; V _{GS} = 0 V	-	1.0	-	V
t _{rr}	Reverse recovery time	I _F = 40 A; -dI _F /dt = 100 A/μs;	-	40	-	ns
Q _{rr}	Reverse recovery charge	V _{GS} = -10 V; V _R = 30 V	-	0.07	-	μC

AVALANCHE LIMITING VALUE

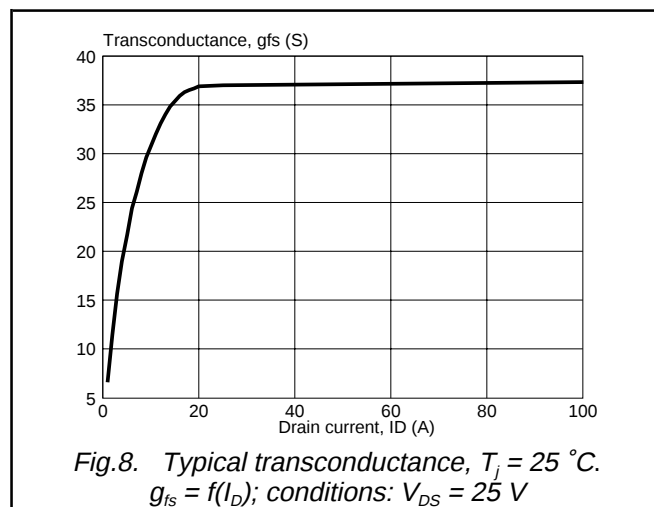
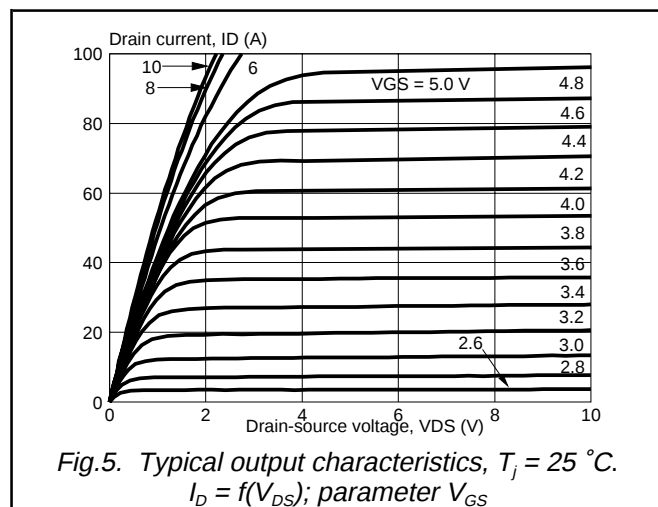
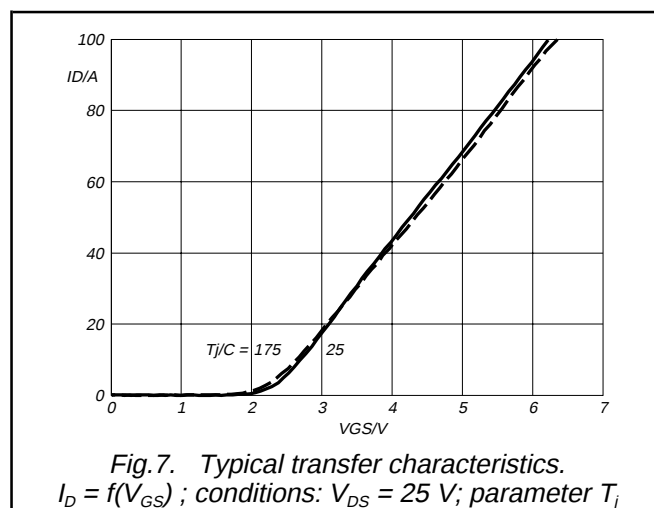
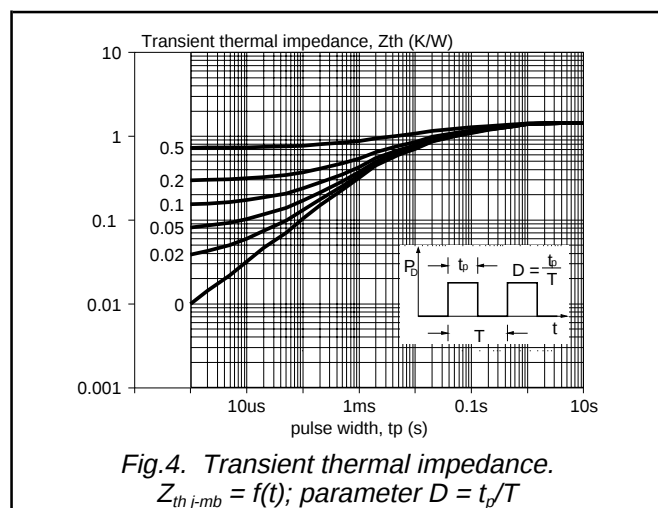
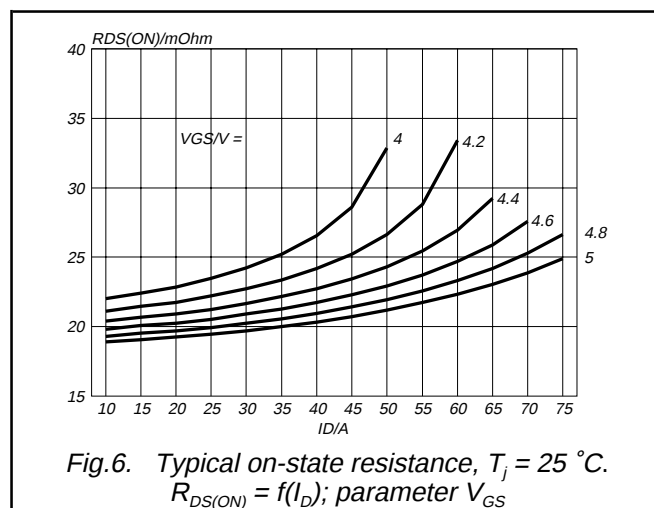
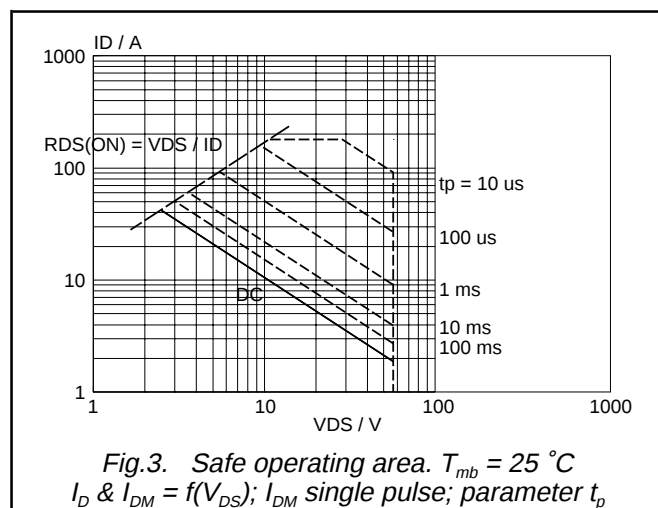
SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
W _{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I _D = 40 A; V _{DD} ≤ 25 V; V _{GS} = 5 V; R _{GS} = 50 Ω; T _{mb} = 25 °C	-	80	mJ



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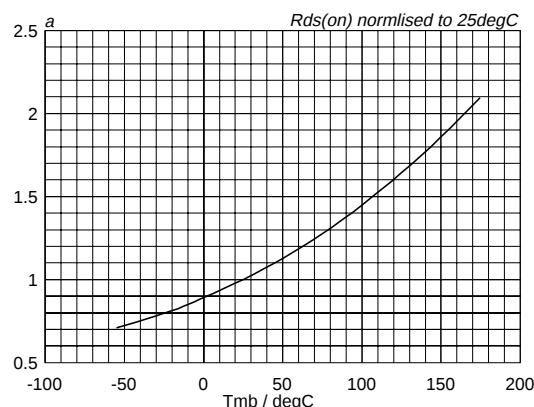


Fig.9. Normalised drain-source on-state resistance.
 $a = R_{DS(ON)}/R_{DS(ON)25^\circ C} = f(T_j)$; $I_D = 25\text{ A}$; $V_{GS} = 5\text{ V}$

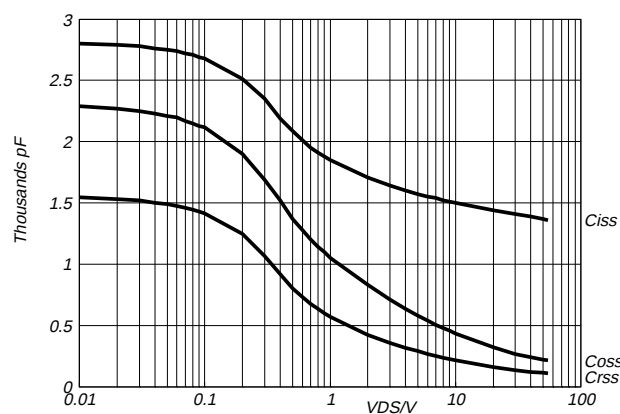


Fig.12. Typical capacitances, C_{iss} , C_{oss} , C_{rss} .
 $C = f(V_{DS})$; conditions: $V_{GS} = 0\text{ V}$; $f = 1\text{ MHz}$

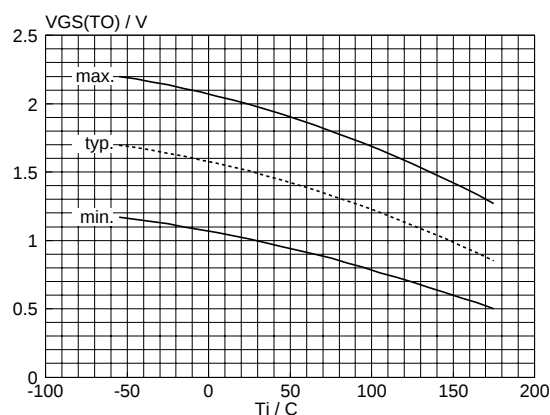


Fig.10. Gate threshold voltage.
 $V_{GS(T0)} = f(T_j)$; conditions: $I_D = 1\text{ mA}$; $V_{DS} = V_{GS}$

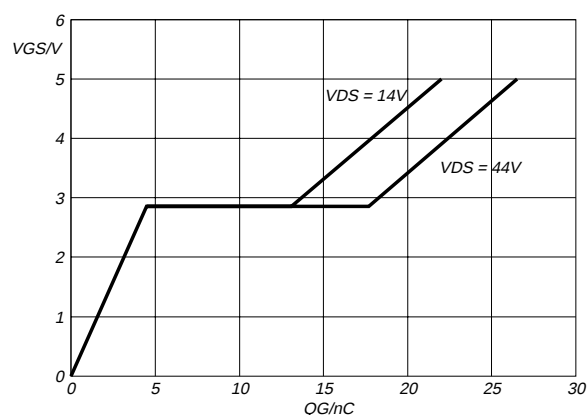


Fig.13. Typical turn-on gate-charge characteristics.
 $V_{GS} = f(Q_G)$; conditions: $I_D = 50\text{ A}$; parameter V_{DS}

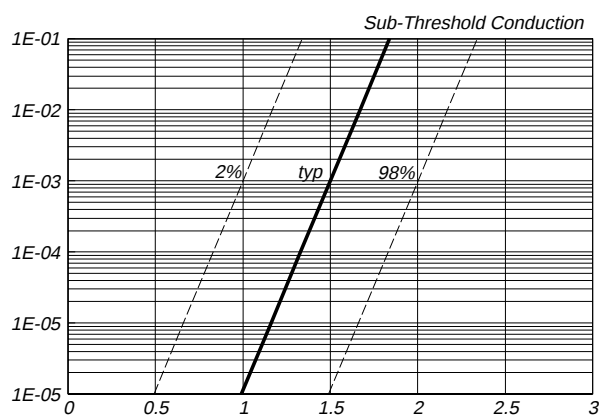


Fig.11. Sub-threshold drain current.
 $I_D = f(V_{GS})$; conditions: $T_j = 25^\circ\text{C}$; $V_{DS} = V_{GS}$

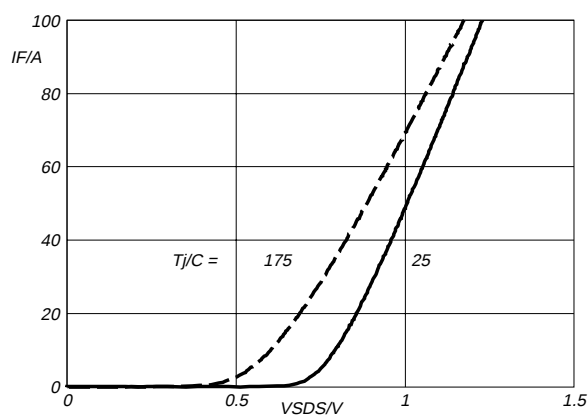


Fig.14. Typical reverse diode current.
 $I_F = f(V_{SDS})$; conditions: $V_{GS} = 0\text{ V}$; parameter T_j

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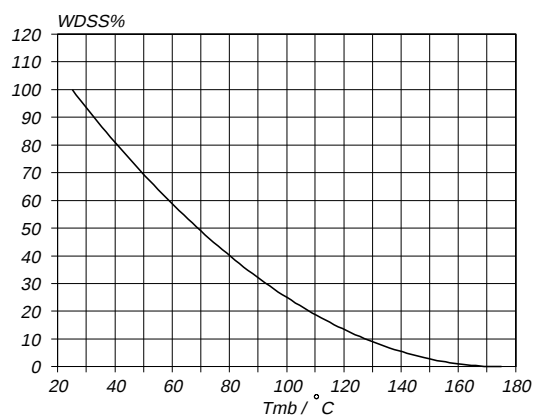


Fig.15. Normalised avalanche energy rating.
 $W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 40\text{ A}$

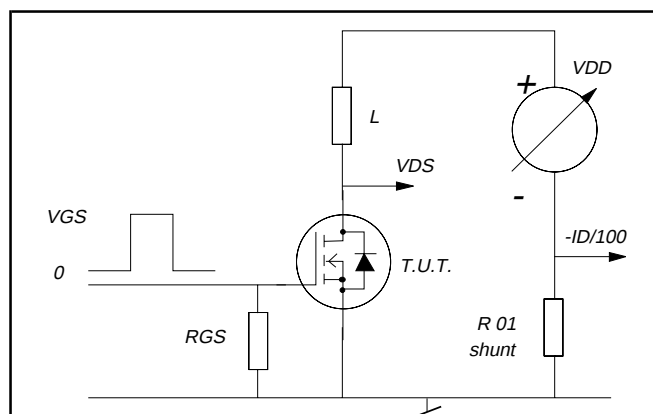


Fig.16. Avalanche energy test circuit.

$$W_{DSS} = 0.5 \cdot L I_D^2 \cdot BV_{DSS} / (BV_{DSS} - V_{DD})$$

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MECHANICAL DATA

Dimensions in mm

Net Mass: 1.4 g

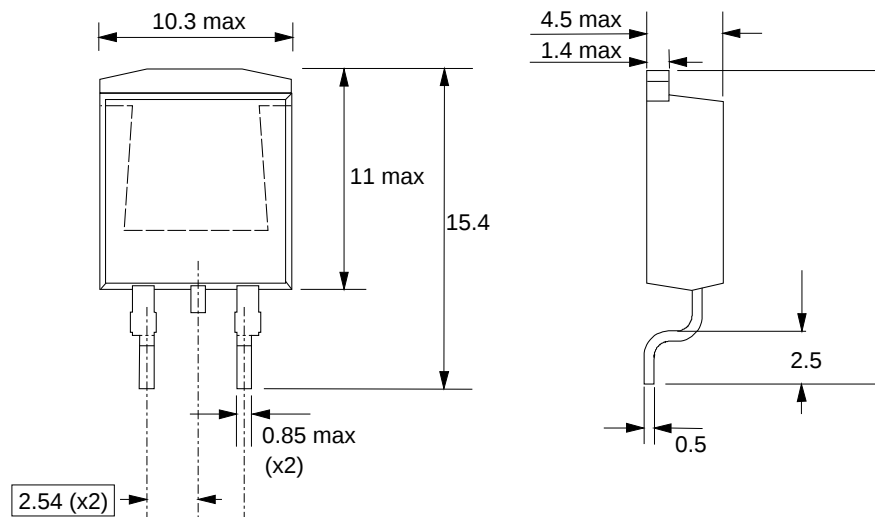


Fig.18. SOT404 : centre pin connected to mounting base.

MOUNTING INSTRUCTIONS

Dimensions in mm

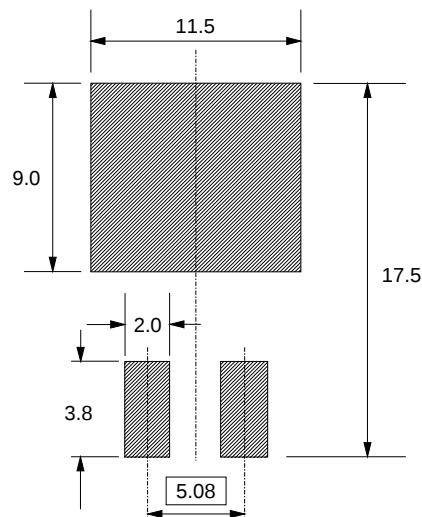


Fig.19. SOT404 : soldering pattern for surface mounting.

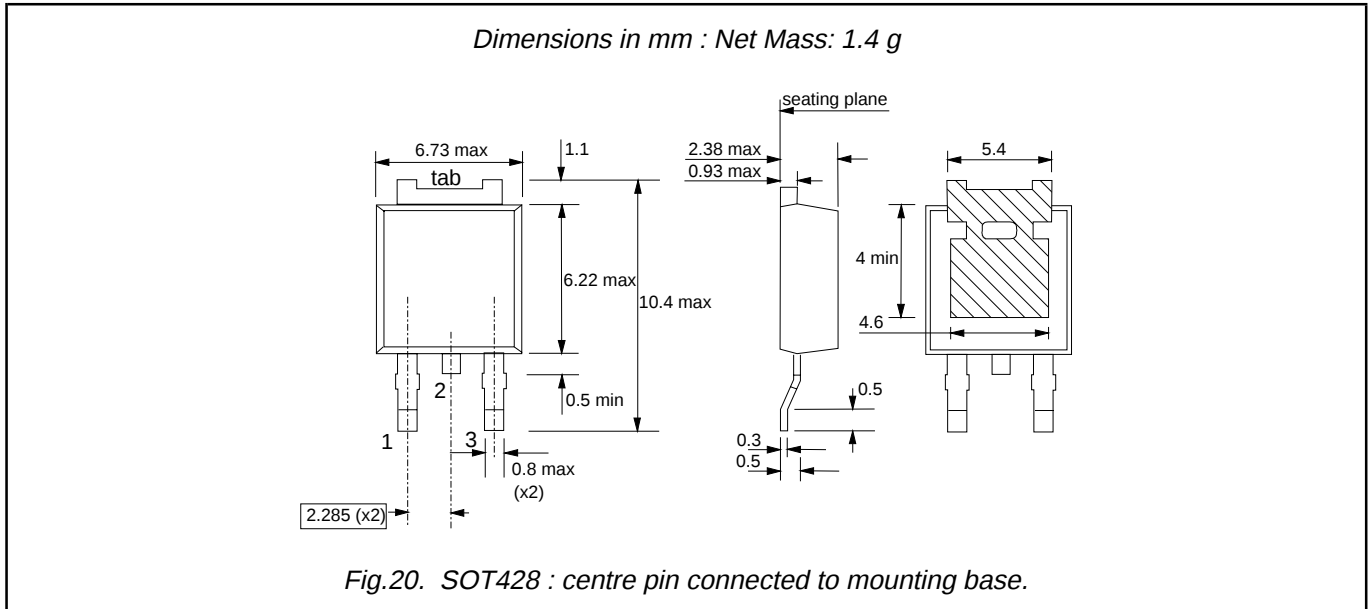
Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Epoxy meets UL94 V0 at 1/8".

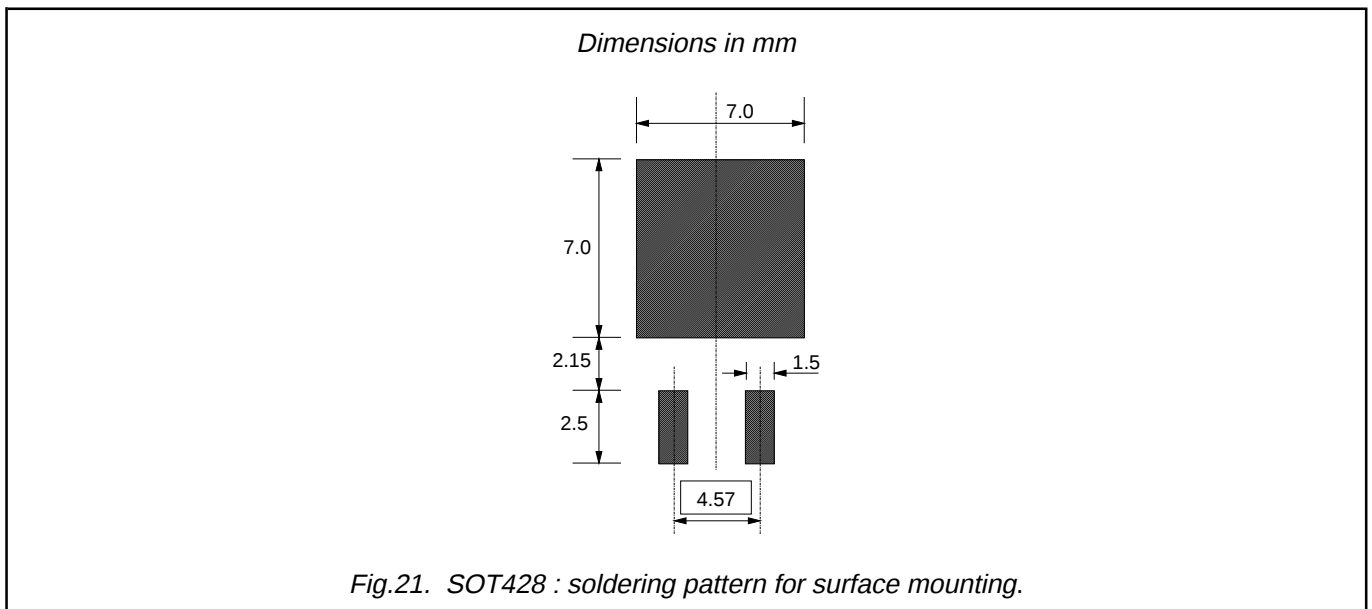
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DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	
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