

MN3644D

2048-Bit High-Responsivity CCD Linear Image Sensor with Internal Clock Driver

Overview

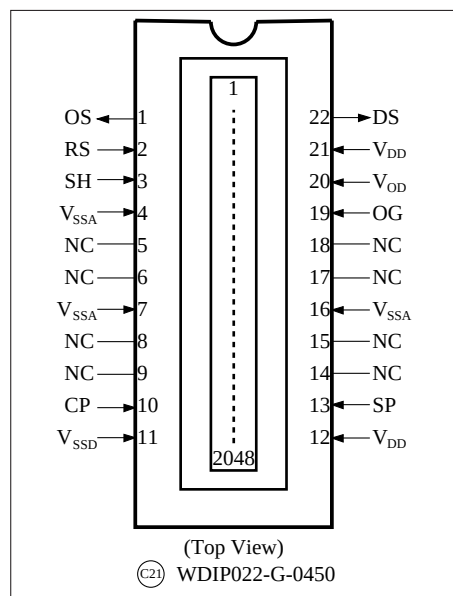
The MN3644D is a high responsivity CCD linear image sensor having floating photodiodes in the photodetector region, CCD analog shift registers for read out, and a built-in clock driver.

It provides large output at a high S/N ratio for visible light inputs over a wide range of wavelength.

Features

- 2048 floating photodiodes and n-channel buried type CCD shift registers for read out are integrated in a single chip.
- Since a clock driver circuit is built in, it is possible to drive this device using CMOS or TTL 5V logic.
- Large signal output of typically 1500mV at saturation can be obtained.
- Because a sample hold circuit is built in, the output waveform makes signal processing easy.
- Since a compensation output pin (DS) is provided in addition to the signal output pin (OS), it is possible to obtain a signal with a high S/N ratio by carrying out differential amplification of the OS and DS outputs.
- Operation with a single +12V positive power supply.

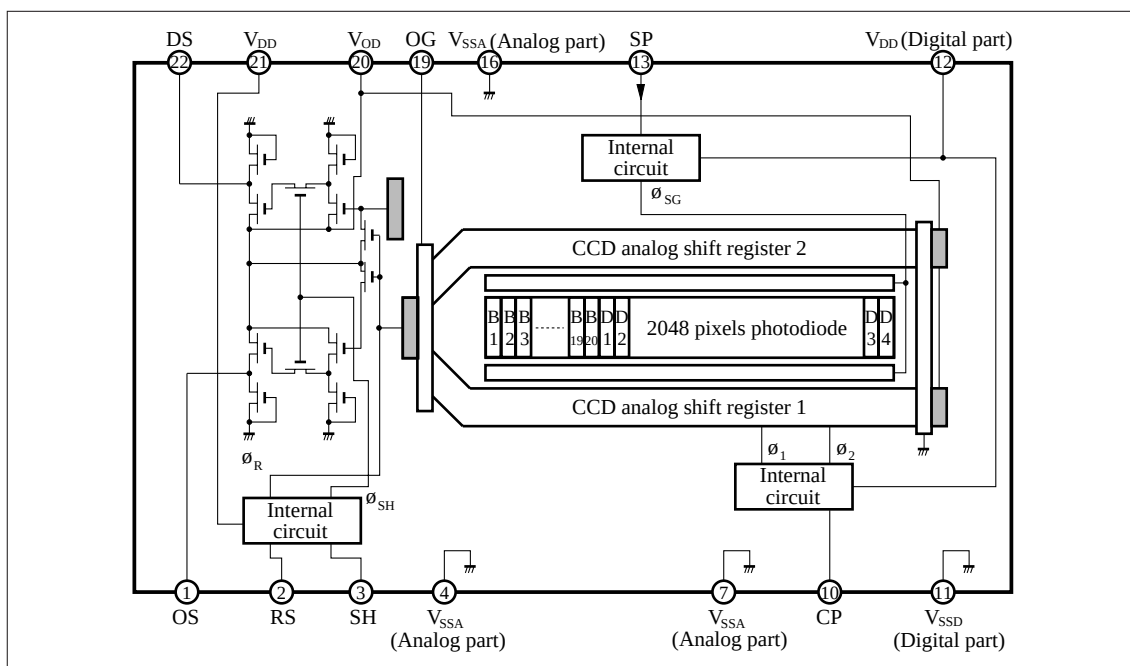
Pin Assignments



Application

- Barcode readers
- Measurement of position and dimensions of objects.

Block Diagram



■ Absolute Maximum Ratings (Ta=25°C, V_{SSA}=V_{SSD}=0V)

Parameter	Symbol	Rating	Unit
Power supply voltage	V _{DD}	− 0.3 to +17	V
	V _{OD}	− 0.3 to +17	V
Input pin voltage	V _i	− 0.3 to +17	V
Output pin voltage	V _O	− 0.3 to +17	V
Operating temperature range	T _{opr}	−20 to + 60	°C
Storage temperature range	T _{stg}	−40 to +100	°C

■ Operating Conditions

- Voltage conditions (Ta=−20 to +60°C, V_{SSA}=0V)

Parameter	Symbol	Condition	min	typ	max	Unit
Internal clock driver power supply voltage	V _{DD}	V _{OD} =V _{DD}	11.4	12.0	13.6	V
CCD output circuit power supply voltage	V _{OD}		11.4	12.0	13.6	V
Output gate voltage	V _{OG}		4.2	4.5	5.1	V
Shift register clock High level	V _{CPH}		4.5	5.0	5.5	V
Shift register clock Low level	V _{CPL}		0	—	0.5	V
Shift clock High level	V _{SPH}		4.5	5.0	5.5	V
Shift clock Low level	V _{SPL}		0	—	0.5	V
Reset clock High level	V _{RSH}		4.5	5.0	5.5	V
Reset clock Low level	V _{RSL}		0	—	0.5	V
Rimple hold clock High level	V _{SHH}		4.5	5.0	5.5	V
Rimple hold clock Low level	V _{SHL}		0	—	0.5	V

- Timing conditions

Parameter	Symbol	Condition	min	typ	max	Unit
Shift register clock frequency	f _C	f _C = 1/2T, f _R = 1/T = data rate	40	—	750	kHz
Reset clock frequency	f _R		80	—	1500	kHz
Shift register clock rise time	t _{Cr}		0	15	50	ns
Shift regisster clock fall time	t _{Cf}		0	15	50	ns
Shift clock rise time	t _{Sr}		0	15	50	ns
Shift clock fall time	t _{Sf}		0	15	50	ns
Shift clock set up time	t _{Ss}		0	400	1000	ns
Shift clock pulse width	t _{Sw}		10	12	50	ns
Shift clock hold time	t _{Sh}		0	1	10	ns
Reset clock rise time	t _{Rr}		0	15	50	ns
Reset clock fall time	t _{Rf}		0	15	50	ns
Reset clock set up time	t _{Rs}		0.7T	—	—	ns
Reset clock pulse width	t _{Rw}		100	150	—	ns
Reset clock hold time	t _{Rh}		0	10	—	ns
Sample hold clock rise time	t _{Hr}		0	15	50	ns
Sample hold clock fall time	t _{Hf}		0	15	50	ns
Sample hold clock set up time	t _{HS}		350	—	—	ns
Sample hold clock pulse width	t _{HW}		100	150	—	ns
Sample hold clock hold time	t _{Hh}		100	—	—	ns

• Clock input capacitance (Ta=−20 to +60°C)

Parameter	Symbol	Condition	min	typ	max	Unit
Shift register clock input capacitance	C _{CP}	f = 1MHz	—	10	—	pF
Shift clock input capacitance	C _{SP}		—	10	—	pF
Reset clock input capacitance	C _{RS}		—	10	—	pF
Sample hold clock input capacitance	C _{SH}		—	10	—	pF

• DC characteristics

Parameter	Symbol	Condition	min	typ	max	Unit
Power supply current	I _{CC}	V _{DD} =V _{OD} =+12V, f _R =500kHz	—	15	30	mA
Output gate leak current	I _{OG}	V _{OG} =+4.5V	—	—	1	mA

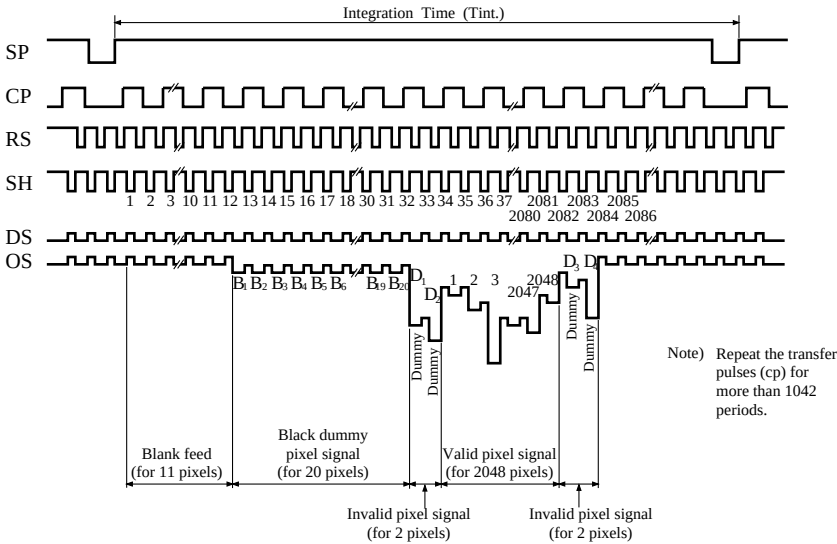
■ Optical Characteristics

Parameter	Symbol	Condition	min	typ	max	Unit
Saturation output voltage	V _{SAT}		1000	1500	—	mV
Saturation exposure	SE		3.0	—	—	mlx·s
Output voltage at constant exposure (Responsivity)	V _{CEmin.}	1.5mlx·s	345	—	495	mV
Photoresponse non-uniformity	PRNU	1.5mlx·s	—	—	20	%
Bit non-uniformity	BNU	1.5mlx·s	—	—	±10	%
Odd/even bit non-uniformity	O/E	1.5mlx·s	—	1	5	%
Dark signal output voltage	V _d	Dark condition	—	10	20	mV
Shift register total transfer efficiency	STTE	1.5mlx·s	92	99	—	%
Modulation transfer function (f _{NVq} =Nyquist spatial frequency)	MTFR	Space frequency	1 × f _{NVq}	—	64	%
			1/2 × f _{NVq}	—	84	%
			1/3 × f _{NVq}	—	97	%

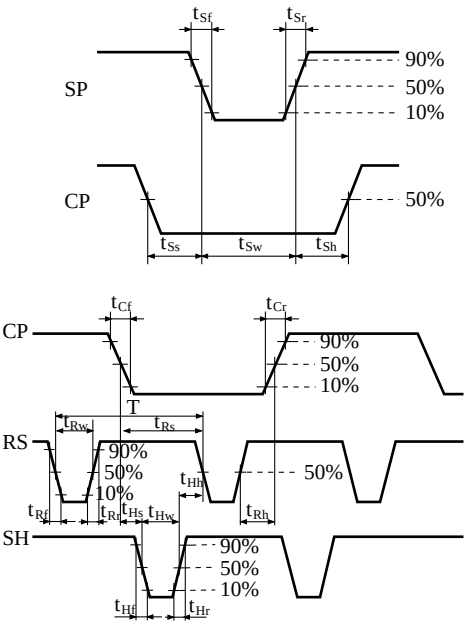
■ Pin Descriptions

Pin No.	Symbol	Pin name	Condition
1	OS	Signal output	Connected to the substrate.
2	RS	Reset clock	
3	SH	Sample hold clock	
4	V _{SSA}	Analog ground	
5	NC	Non connection	
6	NC	Non connection	
7	V _{SSA}	Analog ground	Connected to the substrate.
8	NC	Non connection	
9	NC	Non connection	
10	CP	CCD shift register clock	
11	V _{SSD}	Digital ground	Ground pin for the internal clock driver.
12	V _{DD}	Internal clock driver power supply	
13	SP	Shift clock	
14	NC	Non connection	
15	NC	Non connection	Connected to the substrate.
16	V _{SSA}	Analog ground	
17	NC	Non connection	
18	NC	Non connection	
19	OG	Output gate	
20	V _{OD}	CCD Output part power supply	
21	V _{DD}	Internal clock driver power supply	
22	DS	Compensation output	

■ Timing Diagram
(1) I/O timing



(2) Drive timing



■ Construction of the Image Sensor

The MN3644D can be made up of the three sections of—a) photo detector region, b) CCD transfer region (shift register), and c) output region.

a) Photo detector region

- The photoelectric conversion device consists of an $11\mu\text{m}$ floating photodiode and a $3\mu\text{m}$ channel stopper for each pixel, and 2048 of these devices are linearly arranged side by side at a pitch of $14\mu\text{m}$.
- The photo detector's windows are $14\mu\text{m} \times 200\mu\text{m}$ rectangle and light incident on areas other than these windows is optically shut out.
- The photo detector is provided with 20 optically shielded pixels (black reference pixels) which serve as the black reference.

b) CCD Transfer region (shift register)

- The light output that has been photoelectrically converted is transferred to the CCD transfer for each odd and even pixel

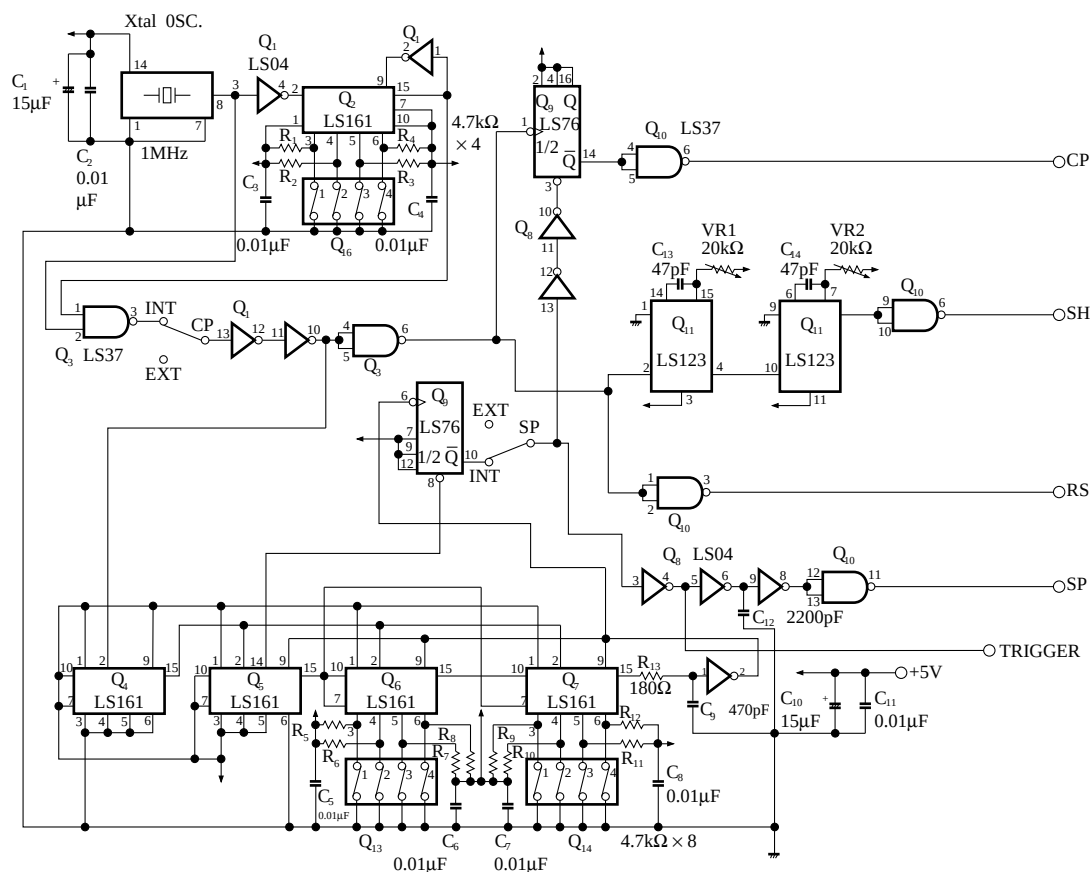
at the timing of the shift clock (SP). The optical signal charge transferred to this analog shift register is successively transferred out and guided to the output region.

- A buried type CCD that can be driven by a two phase clock (ϕ_1, ϕ_2) is used for the analog shift register. The 2-phase clock is being generated based on the CCD shift register clock (CP) by the built-in clock driver circuit.

c) Output region

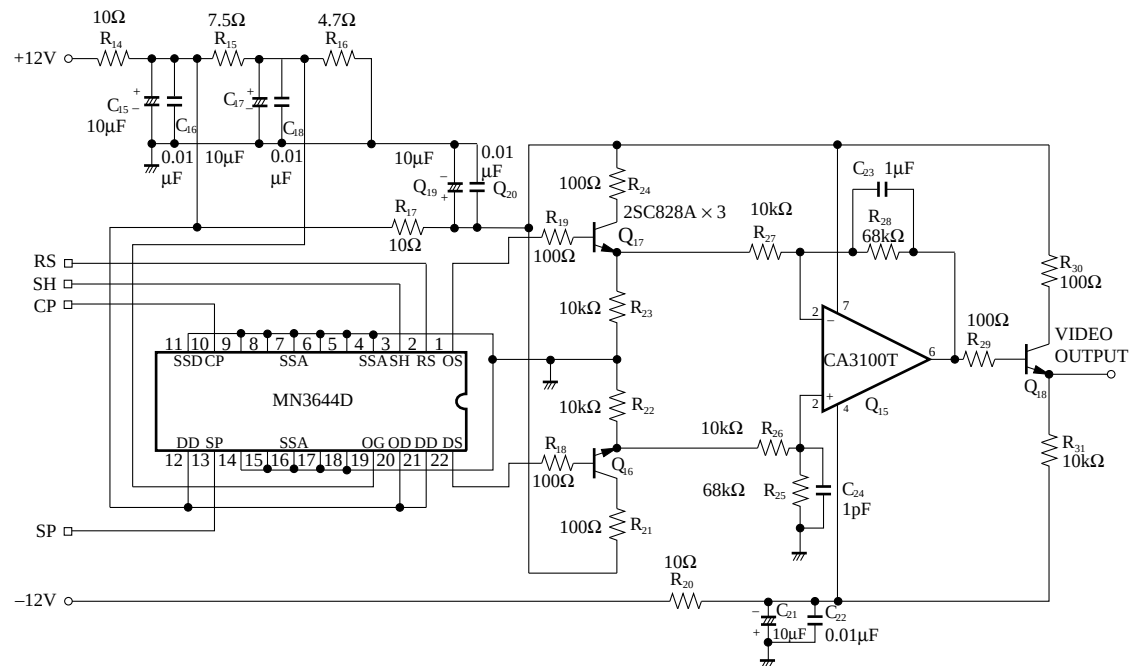
- The signal charge transferred to the output region is sent to the detector region, passed through a sample hold circuit, and is impedance converted by a source follower amplifier.
- The DC level component and the clock noise component not containing optical signals are output from the DS pin.
- By carrying out differential amplification of the two outputs OS and DS externally, it is possible to obtain an output signal with a high S/N ratio by reducing the clock noise, etc.

■ Drive Circuit Diagram (Digital Section)



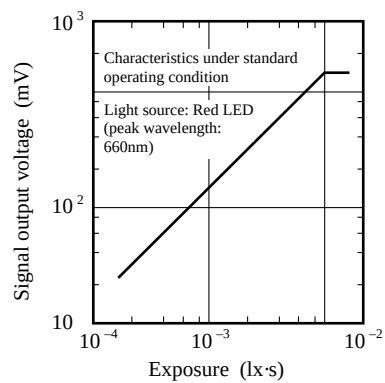
- Connect a $0.01\mu\text{F}$ capacitor between the V_{CC} and GND pins of each TTL.
- Set VR_1 and VR_2 so that an optimum sample hold operation can be performed.

■ Drive Circuit Diagram (Analog Section)



■ Graphs and Characteristics

Photoelectric Conversion Characteristics



Spectral Response Characteristics

