DS1302
Trickle-Charge Timekeeping Chip

www.maxim-ic.com

FEATURES

- Real-Time Clock Counts Seconds, Minutes, Hours, Date of the Month, Month, Day of the Week, and Year with Leap-Year Compensation Valid Up to 2100
- 31 x 8 RAM for Scratchpad Data Storage
- Serial I/O for Minimum Pin Count
- 2.0V to 5.5V Full Operation
- Uses Less than 300nA at 2.0V
- Single-Byte or Multiple-Byte (Burst Mode) Data Transfer for Read or Write of Clock or RAM Data
- 8-Pin DIP or Optional 8-Pin SO for Surface Mount
- Simple 3-Wire Interface
- TTL-Compatible (V_{CC} = 5V)
- Optional Industrial Temperature Range: -40°C to +85°C
- DS1202 Compatible
- Underwriters Laboratory (UL) Recognized

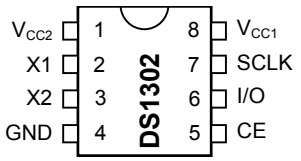
ORDERING INFORMATION

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK*
DS1302	0°C to +70°C	8 PDIP (300 mils)	DS1302
DS1302+	0°C to +70°C	8 PDIP (300 mils)	DS1302
DS1302N	-40°C to +85°C	8 PDIP (300 mils)	DS1302
DS1302N+	-40°C to +85°C	8 PDIP (300 mils)	DS1302
DS1302S	0°C to +70°C	8 SO (208 mils)	DS1302S
DS1302S+	0°C to +70°C	8 SO (208 mils)	DS1302S
DS1302SN	-40°C to +85°C	8 SO (208 mils)	DS1302S
DS1302SN+	-40°C to +85°C	8 SO (208 mils)	DS1302S
DS1302Z	0°C to +70°C	8 SO (150 mils)	DS1302Z
DS1302Z+	0°C to +70°C	8 SO (150 mils)	DS1302Z
DS1302ZN	-40°C to +85°C	8 SO (150 mils)	DS1302ZN
DS1302ZN+	-40°C to +85°C	8 SO (150 mils)	DS1302ZN
DS1302S-16	0°C to +70°C	16 SO (300 mils)	DS1302S16
DS1302SN-16	-40°C to +85°C	16 SO (300 mils)	DS1302SN16

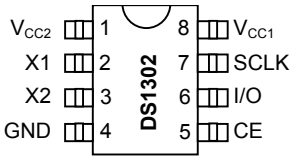
+ Denotes a lead-free/RoHS-compliant device.
**An N anywhere on the top mark indicates an industrial temperature grade device. A + anywhere on the top mark indicates a lead-free device.*

PIN CONFIGURATIONS

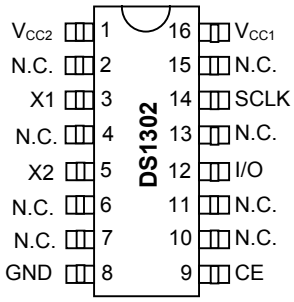
TOP VIEW



DIP (300 mils)



SO (208 mils/150 mils)



SO (300 mils)

Note: *Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, click here: www.maxim-ic.com/errata.*

REV: 110805

DETAILED DESCRIPTION

The DS1302 trickle-charge timekeeping chip contains a real-time clock/calendar and 31 bytes of static RAM. It communicates with a microprocessor via a simple serial interface. The real-time clock/calendar provides seconds, minutes, hours, day, date, month, and year information. The end of the month date is automatically adjusted for months with fewer than 31 days, including corrections for leap year. The clock operates in either the 24-hour or 12-hour format with an AM/PM indicator.

Interfacing the DS1302 with a microprocessor is simplified by using synchronous serial communication. Only three wires are required to communicate with the clock/RAM: CE, I/O (data line), and SCLK (serial clock). Data can be transferred to and from the clock/RAM 1 byte at a time or in a burst of up to 31 bytes. The DS1302 is designed to operate on very low power and retain data and clock information on less than 1μW.

The DS1302 is the successor to the DS1202. In addition to the basic timekeeping functions of the DS1202, the DS1302 has the additional features of dual power pins for primary and backup power supplies, programmable trickle charger for V_{CC1}, and seven additional bytes of scratchpad memory.

OPERATION

Figure 1 shows the main elements of the serial timekeeper: shift register, control logic, oscillator, real-time clock, and RAM.

TYPICAL OPERATING CIRCUIT

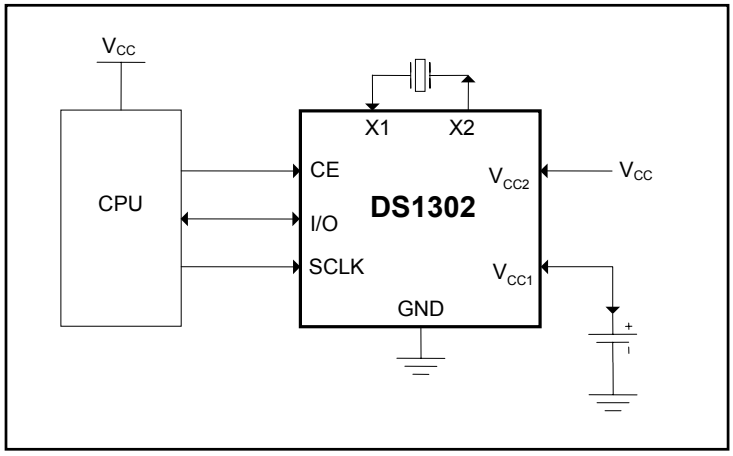
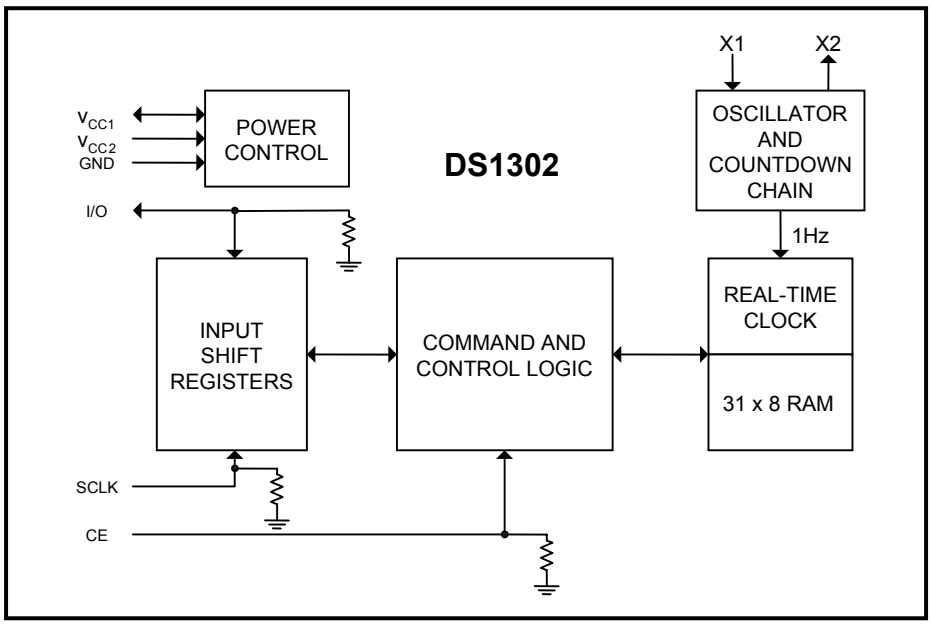
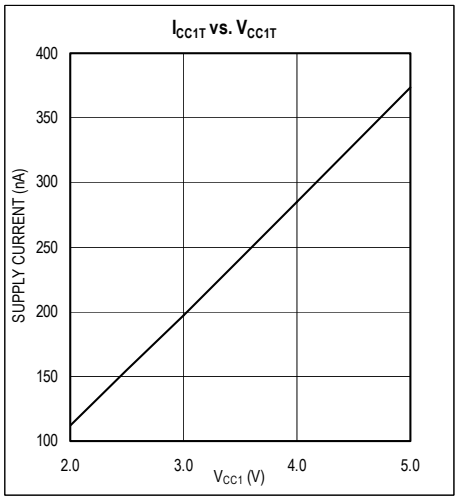


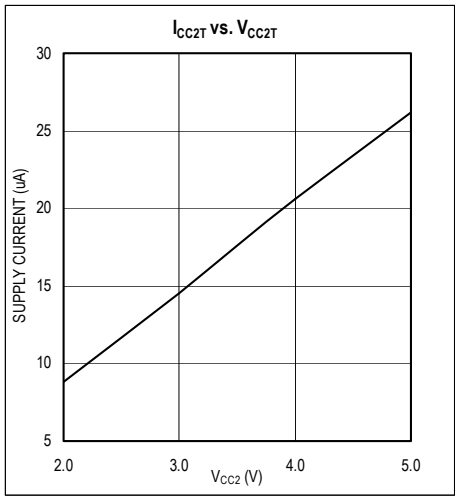
Figure 1. Block Diagram



TYPICAL OPERATING CHARACTERISTICS

(V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.)





PIN DESCRIPTION

PIN		NAME	FUNCTION
8	16		
1	1	V_{CC2}	Primary Power-Supply Pin in Dual Supply Configuration. V_{CC1} is connected to a backup source to maintain the time and date in the absence of primary power. The DS1302 operates from the larger of V_{CC1} or V_{CC2}. When V_{CC2} is greater than V_{CC1} + 0.2V, V_{CC2} powers the DS1302. When V_{CC2} is less than V_{CC1}, V_{CC1} powers the DS1302.
2	3	X1	Connections for Standard 32.768kHz Quartz Crystal. The internal oscillator is designed for operation with a crystal having a specified load capacitance of 6pF. For more information on crystal selection and crystal layout considerations, refer to *Application Note 58: Crystal Considerations for Dallas Real-Time Clocks*. The DS1302 can also be driven by an external 32.768kHz oscillator. In this configuration, the X1 pin is connected to the external oscillator signal and the X2 pin is floated.
3	5	X2	
4	8	GND	Ground
5	9	CE	Input. CE signal must be asserted high during a read or a write. This pin has an internal 40kΩ (typ) pulldown resistor to ground. Note: Previous data sheet revisions referred to CE as $\overline{RST}$. The functionality of the pin has not changed.
6	12	I/O	Input/Push-Pull Output. The I/O pin is the bidirectional data pin for the 3-wire interface. This pin has an internal 40kΩ (typ) pulldown resistor to ground.
7	14	SCLK	Input. SCLK is used to synchronize data movement on the serial interface. This pin has an internal 40kΩ (typ) pulldown resistor to ground.
8	16	V_{CC1}	Low-Power Operation in Single Supply and Battery-Operated Systems and Low-Power Battery Backup. In systems using the trickle charger, the rechargeable energy source is connected to this pin. UL recognized to ensure against reverse charging current when used with a lithium battery.
—	2, 4, 6, 7, 10, 11, 13, 15	N.C.	No Connection

OSCILLATOR CIRCUIT

The DS1302 uses an external 32.768kHz crystal. The oscillator circuit does not require any external resistors or capacitors to operate. Table 1 specifies several crystal parameters for the external crystal. Figure 2 shows a functional schematic of the oscillator circuit. If using a crystal with the specified characteristics, the startup time is usually less than one second.

CLOCK ACCURACY

The accuracy of the clock is dependent upon the accuracy of the crystal and the accuracy of the match between the capacitive load of the oscillator circuit and the capacitive load for which the crystal was trimmed. Additional error will be added by crystal frequency drift caused by temperature shifts. External circuit noise coupled into the oscillator circuit may result in the clock running fast. Figure 3 shows a typical PC board layout for isolating the crystal and oscillator from noise. Refer to *Application Note 58: Crystal Considerations for Dallas Real-Time Clocks* for detailed information.

Table 1. Crystal Specifications*

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Nominal Frequency	f_O		32.768		kHz
Series Resistance	ESR			45	kΩ
Load Capacitance	C_L		6		pF

**The crystal, traces, and crystal input pins should be isolated from RF generating signals. Refer to* Application Note 58: Crystal Considerations for Dallas Real-Time Clocks *for additional specifications.*

Figure 2. Oscillator Circuit Showing Internal Bias Network

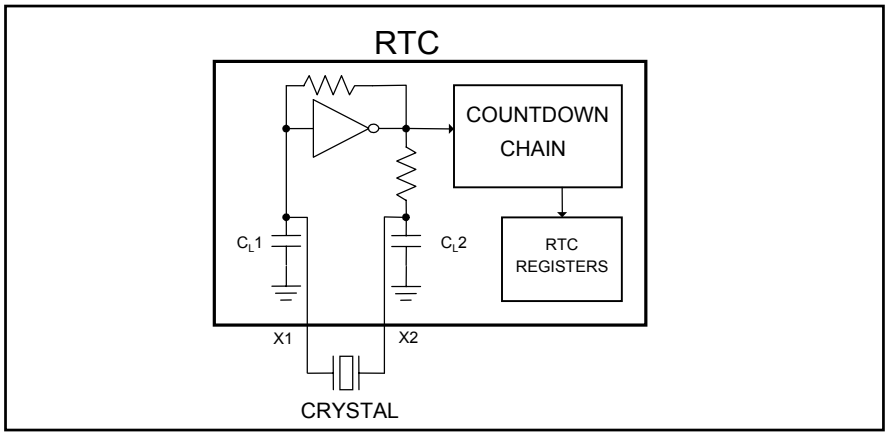
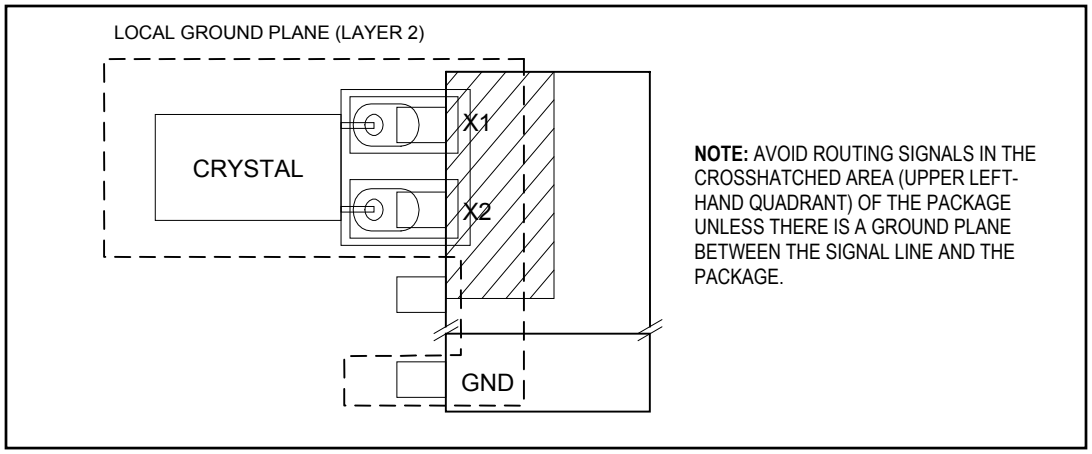


Figure 3. Typical PC Board Layout for Crystal



COMMAND BYTE

Figure 4 shows the command byte. A command byte initiates each data transfer. The MSB (bit 7) must be a logic 1. If it is 0, writes to the DS1302 will be disabled. Bit 6 specifies clock/calendar data if logic 0 or RAM data if logic 1. Bits 1 to 5 specify the designated registers to be input or output, and the LSB (bit 0) specifies a write operation (input) if logic 0 or read operation (output) if logic 1. The command byte is always input starting with the LSB (bit 0).

Figure 4. Address/Command Byte

7	6	5	4	3	2	1	0
1	RAM $\overline{CK}$	A4	A3	A2	A1	A0	RD $\overline{WR}$

CE AND CLOCK CONTROL

Driving the CE input high initiates all data transfers. The CE input serves two functions. First, CE turns on the control logic that allows access to the shift register for the address/command sequence. Second, the CE signal provides a method of terminating either single-byte or multiple-byte CE data transfer.

A clock cycle is a sequence of a rising edge followed by a falling edge. For data inputs, data must be valid during the rising edge of the clock and data bits are output on the falling edge of clock. If the CE input is low, all data transfer terminates and the I/O pin goes to a high-impedance state. Figure 5 shows data transfer. At power-up, CE must be a logic 0 until V_{CC} > 2.0V. Also, SCLK must be at a logic 0 when CE is driven to a logic 1 state.

DATA INPUT

Following the eight SCLK cycles that input a write command byte, a data byte is input on the rising edge of the next eight SCLK cycles. Additional SCLK cycles are ignored should they inadvertently occur. Data is input starting with bit 0.

DATA OUTPUT

Following the eight SCLK cycles that input a read command byte, a data byte is output on the falling edge of the next eight SCLK cycles. Note that the first data bit to be transmitted occurs on the first falling edge after the last bit of the command byte is written. Additional SCLK cycles retransmit the data bytes should they inadvertently occur so long as CE remains high. This operation permits continuous burst mode read capability. Also, the I/O pin is tri-stated upon each rising edge of SCLK. Data is output starting with bit 0.

BURST MODE

Burst mode can be specified for either the clock/calendar or the RAM registers by addressing location 31 decimal (address/command bits 1 through 5 = logic 1). As before, bit 6 specifies clock or RAM and bit 0 specifies read or write. There is no data storage capacity at locations 9 through 31 in the Clock/Calendar Registers or location 31 in the RAM registers. Reads or writes in burst mode start with bit 0 of address 0.

When writing to the clock registers in the burst mode, the first eight registers must be written in order for the data to be transferred. However, when writing to RAM in burst mode it is not necessary to write all 31 bytes for the data to transfer. Each byte that is written to will be transferred to RAM regardless of whether all 31 bytes are written or not.

CLOCK/CALENDAR

The time and calendar information is obtained by reading the appropriate register bytes. Table 2 illustrates the RTC registers. The time and calendar are set or initialized by writing the appropriate register bytes. The contents of the time and calendar registers are in the binary-coded decimal (BCD) format.

The day-of-week register increments at midnight. Values that correspond to the day of week are user-defined but must be sequential (i.e., if 1 equals Sunday, then 2 equals Monday, and so on.). Illogical time and date entries result in undefined operation.

When reading or writing the time and date registers, secondary (user) buffers are used to prevent errors when the internal registers update. When reading the time and date registers, the user buffers are synchronized to the internal registers the rising edge of CE.

The countdown chain is reset whenever the seconds register is written. Write transfers occur on the falling edge of CE. To avoid rollover issues, once the countdown chain is reset, the remaining time and date registers must be written within 1 second.

The DS1302 can be run in either 12-hour or 24-hour mode. Bit 7 of the hours register is defined as the 12- or 24-hour mode-select bit. When high, the 12-hour mode is selected. In the 12-hour mode, bit 5 is the $\overline{AM}$/PM bit with logic high being PM. In the 24-hour mode, bit 5 is the second 10-hour bit (20–23 hours). The hours data must be re-initialized whenever the 12/$\overline{24}$ bit is changed.

CLOCK HALT FLAG

Bit 7 of the seconds register is defined as the clock halt (CH) flag. When this bit is set to logic 1, the clock oscillator is stopped and the DS1302 is placed into a low-power standby mode with a current drain of less than 100nA. When this bit is written to logic 0, the clock will start. The initial power-on state is not defined.

WRITE-PROTECT BIT

Bit 7 of the control register is the write-protect bit. The first seven bits (bits 0 to 6) are forced to 0 and always read 0 when read. Before any write operation to the clock or RAM, bit 7 must be 0. When high, the write-protect bit prevents a write operation to any other register. The initial power-on state is not defined. Therefore, the WP bit should be cleared before attempting to write to the device.

TRICKLE-CHARGE REGISTER

This register controls the trickle-charge characteristics of the DS1302. The simplified schematic of Figure 6 shows the basic components of the trickle charger. The trickle-charge select (TCS) bits (bits 4 to 7) control the selection of the trickle charger. To prevent accidental enabling, only a pattern of 1010 enables the trickle charger. All other patterns will disable the trickle charger. The DS1302 powers up with the trickle charger disabled. The diode select (DS) bits (bits 2 and 3) select whether one diode or two diodes are connected between V_{CC2} and V_{CC1}. If DS is 01, one diode is selected or if DS is 10, two diodes are selected. If DS is 00 or 11, the trickle charger is disabled independently of TCS. The RS bits (bits 0 and 1) select the resistor that is connected between V_{CC2} and V_{CC1}. The resistor selected by the resistor select (RS) bits is as follows:

RS BITS	RESISTOR	TYPICAL VALUE
00	None	None
01	R1	2kΩ
10	R2	4kΩ
11	R3	8kΩ

If RS is 00, the trickle charger is disabled independently of TCS.

Diode and resistor selection is determined by the user according to the maximum current desired for battery or super cap charging. The maximum charging current can be calculated as illustrated in the following example. Assume that a system power supply of 5V is applied to V_{CC2} and a super cap is connected to V_{CC1}. Also assume that the trickle charger has been enabled with one diode and resistor R1 between V_{CC2} and V_{CC1}. The maximum current I_{MAX} would therefore be calculated as follows:

$$I_{MAX} = (5.0V - \text{diode drop}) / R1 \approx (5.0V - 0.7V) / 2k\Omega \approx 2.2mA$$

As the super cap charges, the voltage drop between V_{CC2} and V_{CC1} decreases and therefore the charge current decreases.

CLOCK/CALENDAR BURST MODE

The clock/calendar command byte specifies burst mode operation. In this mode, the first eight clock/calendar registers can be consecutively read or written (see Table 2) starting with bit 0 of address 0.

If the write-protect bit is set high when a write clock/calendar burst mode is specified, no data transfer will occur to any of the eight clock/calendar registers (this includes the control register). The trickle charger is not accessible in burst mode.

At the beginning of a clock burst read, the current time is transferred to a second set of registers. The time information is read from these secondary registers, while the clock may continue to run. This eliminates the need to re-read the registers in case of an update of the main registers during a read.

RAM

The static RAM is 31 x 8 bytes addressed consecutively in the RAM address space.

RAM BURST MODE

The RAM command byte specifies burst mode operation. In this mode, the 31 RAM registers can be consecutively read or written (see Table 2) starting with bit 0 of address 0.

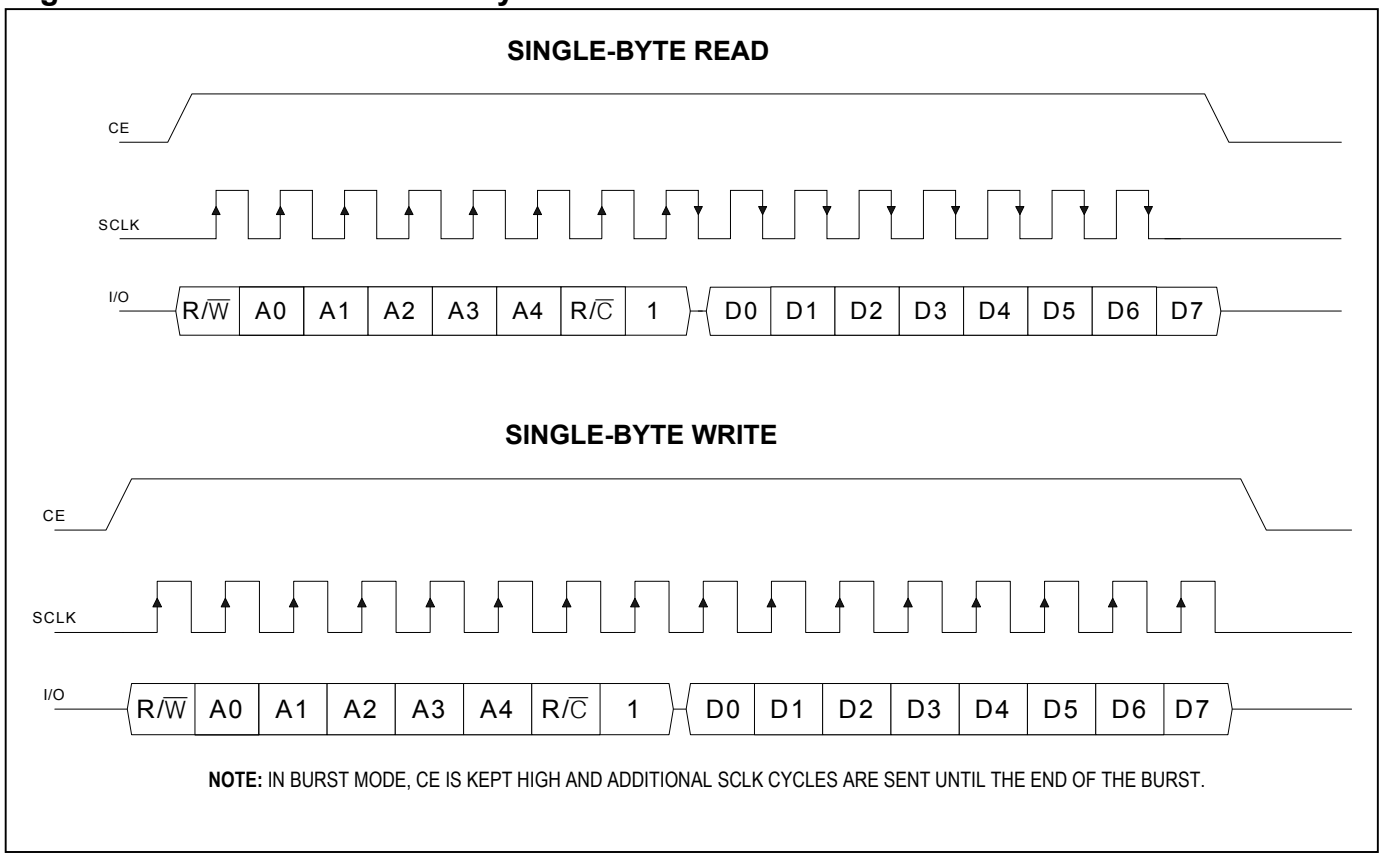
REGISTER SUMMARY

A register data format summary is shown in Table 2.

CRYSTAL SELECTION

A 32.768kHz crystal can be directly connected to the DS1302 via pins 2 and 3 (X1, X2). The crystal selected for use should have a specified load capacitance (C_L) of 6pF. For more information on crystal selection and crystal layout consideration, refer to *Application Note 58: Crystal Considerations for Dallas Real-Time Clocks*.

Figure 5. Data Transfer Summary



NOTE: IN BURST MODE, CE IS KEPT HIGH AND ADDITIONAL SCLK CYCLES ARE SENT UNTIL THE END OF THE BURST.

Table 2. Register Address/Definition

RTC

READ	WRITE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	RANGE
81h	80h	CH	10 Seconds			Seconds				00–59
83h	82h		10 Minutes			Minutes				00–59
85h	84h	12/$\overline{24}$	0	10 $\overline{AM}$/PM	Hour	Hour				1–12/0–23
87h	86h	0	0	10 Date		Date				1–31
89h	88h	0	0	0	10 Month	Month				1–12
8Bh	8Ah	0	0	0	0	0	Day			1–7
8Dh	8Ch	10 Year				Year				00–99
8Fh	8Eh	WP	0	0	0	0	0	0	0	—
91h	90h	TCS	TCS	TCS	TCS	DS	DS	RS	RS	—

CLOCK BURST

BFh	BEh

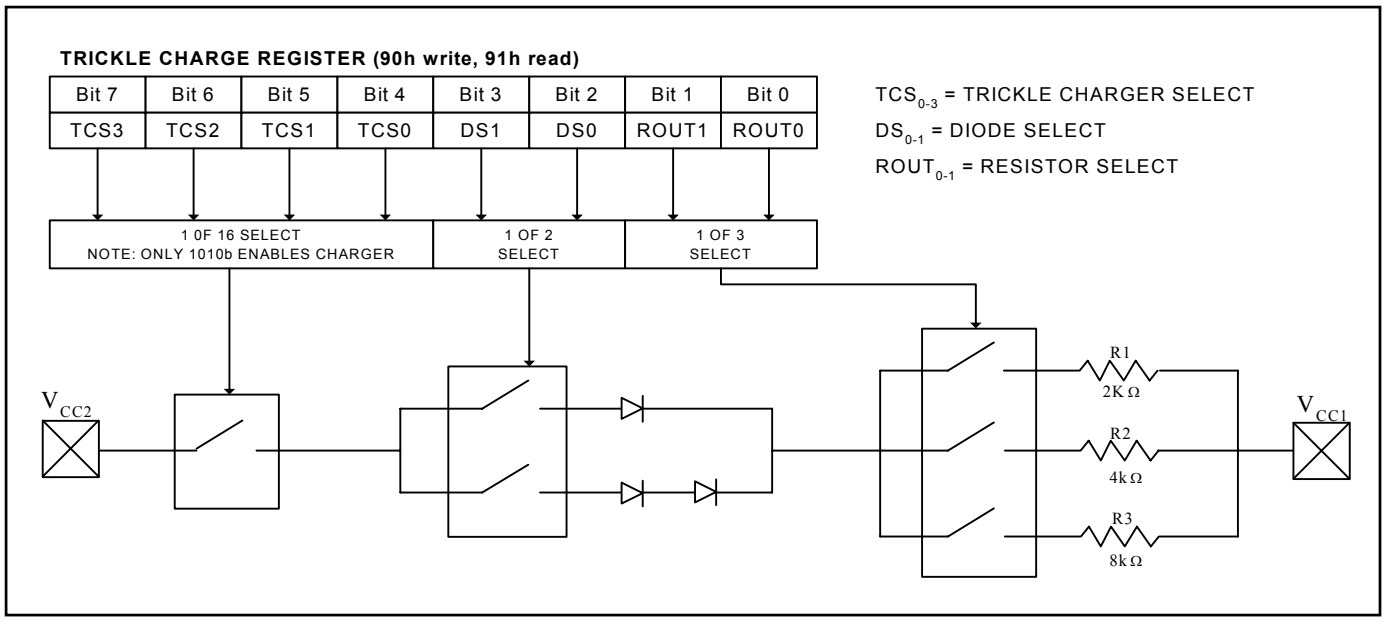
RAM

C1h	C0h		00-FFh
C3h	C2h		00-FFh
C5h	C4h		00-FFh
.	.		.
.	.		.
.	.		.
FDh	FCh		00-FFh

RAM BURST

FFh	FEh

Figure 6. Programmable Trickle Charger



ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin Relative to Ground……-0.5Vto +7.0V
Operating Temperature Range, Commercial……0°C to +70°C
Operating Temperature Range, Industrial (IND)……-40°C to +85°C
Storage Temperature Range……..…-55°C to +125°C
Soldering Temperature (leads, 10 seconds)……..…….260°C
Soldering Temperature (surface mount)……..…….See IPC/JEDEC J-STD-020

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(T_A = 0°C to +70°C or T_A = -40°C to +85°C.) (Note 1)

PARAMETER	SYMBOL		CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage V_{CC1}, V_{CC2}	V_{CC1}, V_{CC2}		(Notes 2, 10)	2.0	3.3	5.5	V
Logic 1 Input	V_{IH}		(Note 2)	2.0		V_{CC} + 0.3	V
Logic 0 Input	V_{IL}	V_{CC} = 2.0V	(Note 2)	-0.3		+0.3	V
		V_{CC} = 5V		-0.3		+0.8	

DC ELECTRICAL CHARACTERISTICS

(T_A = 0°C to +70°C or T_A = -40°C to +85°C.) (Note 1)

PARAMETER	SYMBOL		CONDITIONS	MIN	TYP	MAX	UNITS
Input Leakage	I_{LI}		(Notes 5, 13)		85	500	µA
I/O Leakage	I_{LO}		(Notes 5, 13)		85	500	µA
Logic 1 Output (I_{OH} = -0.4mA)	V_{OH}	V_{CC} = 2.0V	(Note 2)	1.6			V
Logic 1 Output (I_{OH} = -1.0mA)		V_{CC} = 5V		2.4			
Logic 0 Output (I_{OL} = 1.5mA)	V_{OL}	V_{CC} = 2.0V	(Note 2)			0.4	V
Logic 0 Output (I_{OL} = 4.0mA)		V_{CC} = 5V				0.4	
Active Supply Current (Oscillator Enabled)	I_{CC1A}	V_{CC1} = 2.0V	CH = 0 (Notes 4, 11)			0.4	mA
		V_{CC1} = 5V				1.2	
Timekeeping Current (Oscillator Enabled)	I_{CC1T}	V_{CC1} = 2.0V	CH = 0 (Notes 3, 11,13)		0.2	0.3	µA
		V_{CC1} = 5V			0.45	1	
Standby Current (Oscillator Disabled)	I_{CC1S}	V_{CC1} = 2.0V	CH = 1 (Notes 9, 11, 13)		1	100	nA
		V_{CC1} = 5V			1	100	
		IND			5	200	
Active Supply Current (Oscillator Enabled)	I_{CC2A}	V_{CC2} = 2.0V	CH = 0 (Notes 4, 12)			0.425	mA
		V_{CC2} = 5V				1.28	
Timekeeping Current (Oscillator Enabled)	I_{CC2T}	V_{CC2} = 2.0V	CH = 0 (Notes 3, 12)			25.3	µA
		V_{CC2} = 5V				81	
Standby Current (Oscillator Disabled)	I_{CC2S}	V_{CC2} = 2.0V	CH = 1 (Notes 9, 12)			25	µA
		V_{CC2} = 5V				80	
Trickle-Charge Resistors	R1				2		kΩ
	R2				4		
	R3				8		
Trickle-Charge Diode Voltage Drop	V_{TD}				0.7		V

CAPACITANCE

(T_A = +25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Input Capacitance	C_I		10		pF
I/O Capacitance	$C_{I/O}$		15		pF

AC ELECTRICAL CHARACTERISTICS

(T_A = 0°C to +70°C or T_A = -40°C to +85°C.) (Note 1)

PARAMETER	SYMBOL		CONDITIONS	MIN	TYP	MAX	UNITS
Data to CLK Setup	t_{DC}	V_{CC} = 2.0V	(Note 6)	200			ns
		V_{CC} = 5V		50			
CLK to Data Hold	t_{CDH}	V_{CC} = 2.0V	(Note 6)	280			ns
		V_{CC} = 5V		70			
CLK to Data Delay	t_{CDD}	V_{CC} = 2.0V	(Notes 6, 7, 8)			800	ns
		V_{CC} = 5V				200	
CLK Low Time	t_{CL}	V_{CC} = 2.0V	(Note 6)	1000			ns
		V_{CC} = 5V		250			
CLK High Time	t_{CH}	V_{CC} = 2.0V	(Note 6)	1000			ns
		V_{CC} = 5V		250			
CLK Frequency	t_{CLK}	V_{CC} = 2.0V	(Note 6)			0.5	MHz
		V_{CC} = 5V		DC		2.0	
CLK Rise and Fall	t_R, t_F	V_{CC} = 2.0V				2000	ns
		V_{CC} = 5V				500	
CE to CLK Setup	t_{CC}	V_{CC} = 2.0V	(Note 6)	4			µs
		V_{CC} = 5V		1			
CLK to CE Hold	t_{CCH}	V_{CC} = 2.0V	(Note 6)	240			ns
		V_{CC} = 5V		60			
CE Inactive Time	t_{CWH}	V_{CC} = 2.0V	(Note 6)	4			µs
		V_{CC} = 5V		1			
CE to I/O High Impedance	t_{CDZ}	V_{CC} = 2.0V	(Note 6)			280	ns
		V_{CC} = 5V				70	
SCLK to I/O High Impedance	t_{CCZ}	V_{CC} = 2.0V	(Note 6)			280	ns
		V_{CC} = 5V				70	

Note 1: Limits at -40°C are guaranteed by design and are not production tested.
Note 2: All voltages are referenced to ground.
Note 3: I_{CC1T} and I_{CC2T} are specified with I/O open, CE and SCLK set to a logic 0.
Note 4: I_{CC1A} and I_{CC2A} are specified with the I/O pin open, CE high, SCLK = 2MHz at V_{CC} = 5V; SCLK = 500kHz, V_{CC} = 2.0V.
Note 5: CE, SCLK, and I/O all have 40kΩ pulldown resistors to ground.
Note 6: Measured at V_{IH} = 2.0V or V_{IL} = 0.8V and 10ns maximum rise and fall time.
Note 7: Measured at V_{OH} = 2.4V or V_{OL} = 0.4V.
Note 8: Load capacitance = 50pF.
Note 9: I_{CC1S} and I_{CC2S} are specified with CE, I/O, and SCLK open.
Note 10: V_{CC} = V_{CC2}, when V_{CC2} > V_{CC1} + 0.2V; V_{CC} = V_{CC1}, when V_{CC1} > V_{CC2}.
Note 11: V_{CC2} = 0V.
Note 12: V_{CC1} = 0V.
Note 13: Typical values are at +25°C.

Figure 7. Timing Diagram: Read Data Transfer

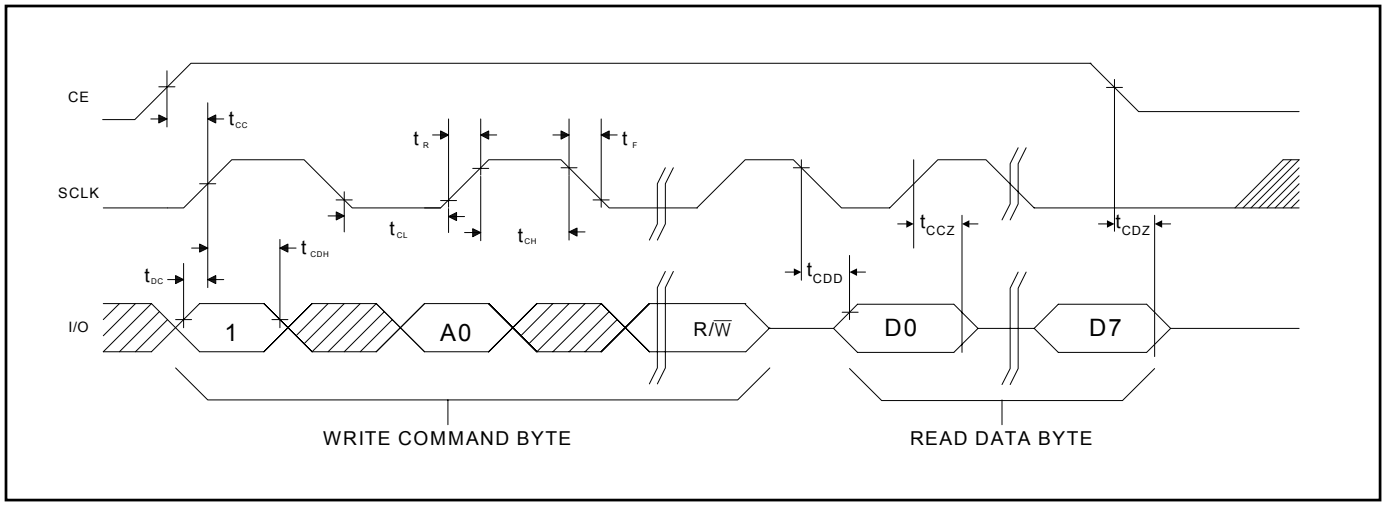
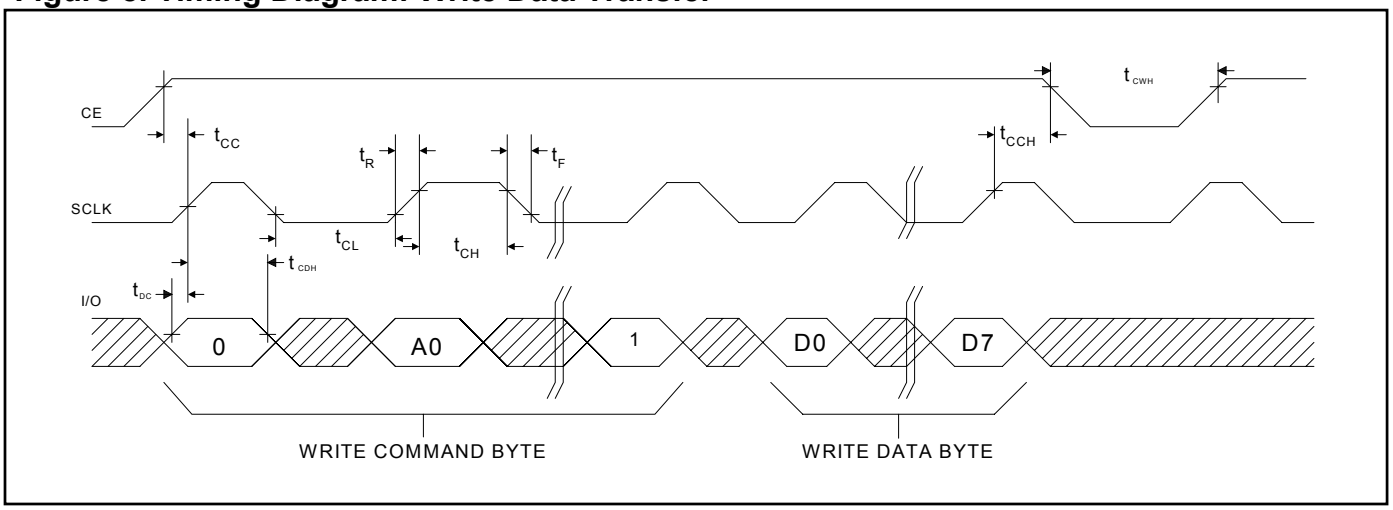


Figure 8. Timing Diagram: Write Data Transfer



CHIP INFORMATION

TRANSISTOR COUNT: 11,500

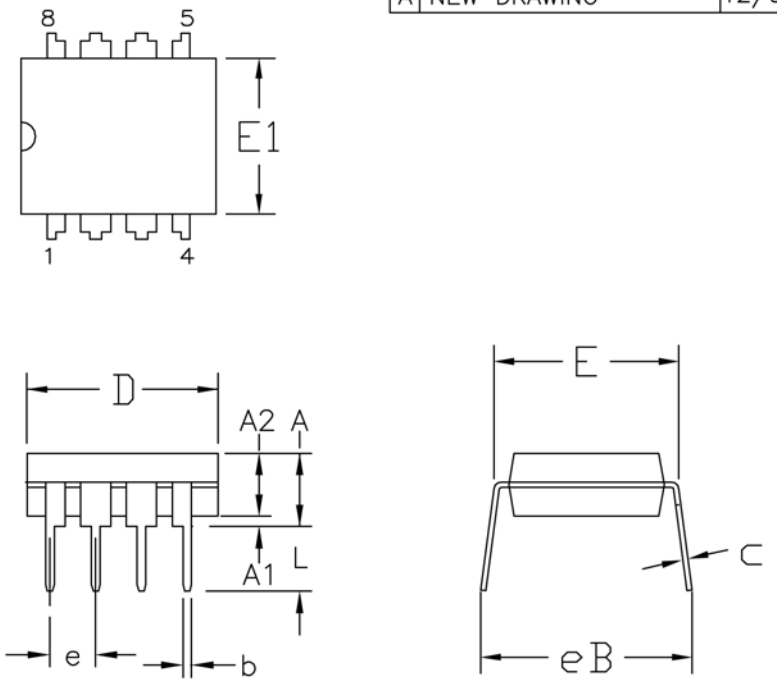
THERMAL INFORMATION

PACKAGE	THETA-JA (°C/W)	THETA-JC (°C/W)
8 DIP	110	40
8 SO (150 mils)	170	40
8 SO (208 mils)	113	31
16 SO (300 mils)	105	22

PACKAGE INFORMATION

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/DallasPackInfo**.)

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	NEW DRAWING	12/01	



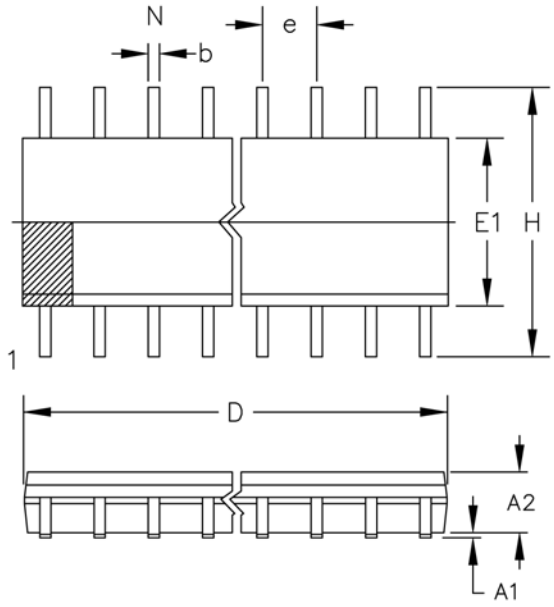
	8 PIN	
	MIN	MAX
A	–	0.170
A1	0.015	–
A2	0.115	0.195
b	0.015	0.022
c	0.008	0.012
D	0.360	0.380
E	0.300	0.325
E1	0.240	0.260
e	0.090	0.110
L	0.125	0.135
eB	–	0..430

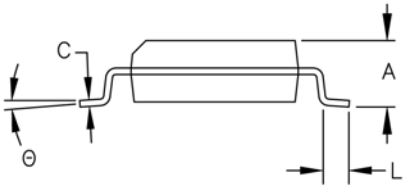
ALL DIMENSIONS ARE IN INCHES

SIGNATURE		DATE	DALLAS SEMICONDUCTOR MAXIM			
DOC. CONTROL:						
ENGR. MGR:			TITLE	MARKETING OUTLINE, 8 LEAD PLASTIC DUAL–IN–LINE PACKAGE (0.300")		
MFG. ENGR:						
CHECKED BY:	TWM	12/01	SIZE A	FSCM NO	PART NO. 56–G5005–000	REV A
DRAWN BY:	JFD	12/01				
DO NOT SCALE DWG.			SCALE N/A		SHEET 1 OF 1	

PACKAGE INFORMATION (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/DallasPackInfo**.)





REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	NEW DRAWING	2/95	J.W.
B	UPDATE DIMENSIONS		

PKG		8 PIN		14 PIN		16 PIN	
LTR		MIN	MAX	MIN	MAX	MIN	MAX
A	IN.	0.053	0.069	0.053	0.069	0.053	0.069
	MM	1.35	1.75	1.35	1.75	1.35	1.75
A1	IN.	0.004	0.010	0.004	0.010	0.004	0.010
	MM	0.10	0.25	0.10	0.25	0.10	0.25
A2	IN.	0.048	0.062	0.048	0.062	0.048	0.062
	MM	1.22	1.57	1.22	1.57	1.22	1.57
b	IN.	0.012	0.020	0.012	0.020	0.012	0.020
	MM	0.030	0.51	0.30	0.51	0.30	0.51
C	IN.	0.007	0.011	0.007	0.011	0.007	0.011
	MM	0.18	0.28	0.18	0.28	0.18	0.28
D	IN.	0.188	0.196	0.337	0.344	0.386	0.393
	MM	4.78	4.98	8.56	8.74	9.80	9.98
e	IN.	.050 BSC		.050 BSC		.050 BSC	
	MM	1.27 BSC		1.27 BSC		1.27 BSC	
E1	IN.	0.150	0.158	0.150	0.158	0.150	0.158
	MM	3.81	4.01	3.81	4.01	3.81	4.01
H	IN.	0.230	0.244	0.230	0.244	0.230	0.244
	MM	5.84	6.20	5.84	6.20	5.84	6.20
L	IN.	0.016	0.050	0.016	0.050	0.016	0.050
	MM	0.41	1.27	0.41	1.27	0.41	1.27
Θ		0°	8°	0°	8°	0°	8°

THE CHAMFER ON THE BODY IS OPTIONAL. IF IT IS NOT PRESENT, A TERMINAL 1 IDENTIFIER MUST BE POSITIONED SO THAT 1/2 OR MORE OF IT'S AREA IS CONTAINED IN THE HATCHED ZONE.

SIGNATURE		DATE
DOC. CONTROL:		
ENGR. MGR:		
MFG. ENGR:		
CHECKED BY:		
DRAWN BY:	M.W.C.	2/95
DO NOT SCALE DWG.		

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE .150" SOIC 8,14&16 LD.

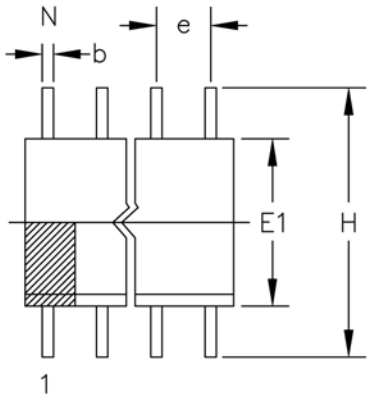
SIZE	FSCM NO	PART NO.	REV
A		56-G2008-001	B

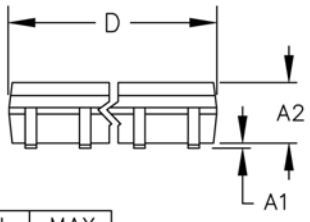
SCALE N/A | SHEET 1 OF 1

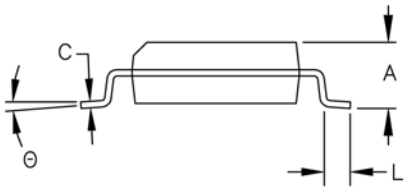
PACKAGE INFORMATION (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/DallasPackInfo**.)

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	NEW DRAWING	5/18	J.W.
B	INC. ECN NO. 8680		







LTR		MIN	MAX
A	IN.	0.094	0.105
	MM	2.39	2.67
A1	IN.	0.004	0.012
	MM	0.102	0.30
A2	IN.	0.089	0.095
	MM	2.26	2.41
b	IN.	0.013	0.020
	MM	0.33	0.51
C	IN.	0.009	0.013
	MM	0.229	0.33
D	IN.	→	
	MM		
e	IN.	.050 BSC	
	MM	1.27 BSC	
E1	IN.	0.290	0.300
	MM	7.37	7.62
H	IN.	0.398	0.416
	MM	10.11	10.57
L	IN.	0.016	0.040
	MM	0.40	1.02
Θ		0°	8°

	16 PIN		18 PIN		20 PIN		24 PIN		28 PIN	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
D IN.	0.398	0.412	0.448	0.462	0.498	0.511	0.598	0.612	0.698	0.712
D MM	10.11	10.46	11.38	11.73	12.65	12.99	15.19	15.54	17.73	18.08

THE CHAMFER ON THE BODY IS OPTIONAL.
IF IT IS NOT PRESENT, A TERMINAL 1 IDENTIFIER
MUST BE POSITIONED SO THAT 1/2 OR MORE OF
IT'S AREA IS CONTAINED IN THE HATCHED ZONE.

SIGNATURE		DATE
DOC. CONTROL:	J.WILKINS	5/94
ENGR. MGR:	B.W.MCARTY	5/94
MFG. ENGR:	C.M.SELLS	5/94
CHECKED BY:	C.M.SELLS	5/94
DRAWN BY:	M.W.C.	5/94
DO NOT SCALE DWG.		

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE .300" SOIC 16,18,20,24&28 LD.

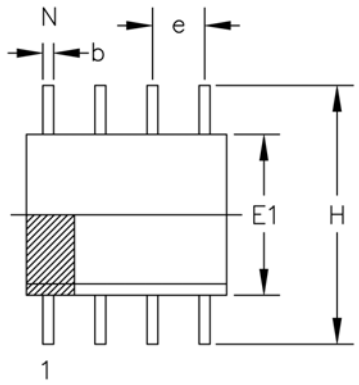
SIZE	FSCM NO	PART NO.	REV
A		56-G4009-001	B

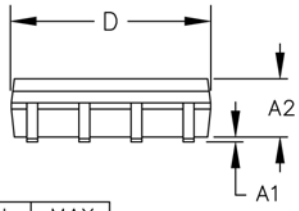
SCALE N/A | SHEET 1 OF 1

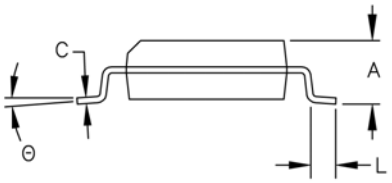
PACKAGE INFORMATION (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/DallasPackInfo**.)

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	NEW DRAWING		







LTR		MIN	MAX
A	IN.	0.072	0.084
	MM	1.83	2.13
A1	IN.	0.004	0.010
	MM	0.102	0.25
A2	IN.	0.070	0.080
	MM	1.78	2.03
b	IN.	0.013	0.020
	MM	0.33	0.51
C	IN.	0.006	0.010
	MM	0.15	0.25
D	IN.	0.203	0.215
	MM	5.16	5.46
e	IN.	.050 BSC	
	MM	1.27 BSC	
E1	IN.	0.203	0.213
	MM	5.16	5.41
H	IN.	0.302	0.318
	MM	7.67	8.07
L	IN.	0.019	0.030
	MM	0.48	0.76
Θ		0°	8°

THE CHAMFER ON THE BODY IS OPTIONAL.
IF IT IS NOT PRESENT, A TERMINAL 1 IDENTIFIER MUST BE POSITIONED SO THAT 1/2 OR MORE OF IT'S AREA IS CONTAINED IN THE HATCHED ZONE.

SIGNATURE	DATE
DOC. CONTROL:	
ENGR. MGR:	
MFG. ENGR:	
CHECKED BY:	
DRAWN BY: M.W.C.	5/94
DO NOT SCALE DWG.	

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE .208" 8 LEAD SOIC

SIZE	FSCM NO	PART NO.	REV
A		56-G4010-001	A

SCALE N/A | SHEET 1 OF 1

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