M61324SP

WIDE FREQUENCY BAND ANALOG SWITCH

DESCRIPTION

The M61324SP is a semiconductor integrated circuit for the RGBHV interface. The device features swiching signals input from two types of image sources and outputting the signals to the CRT display,etc. Synchronous signals, meeting a frequency band of 10KHz to 200KHz, are output at TTL. The frequency band of video signals is 250MHz, acquiring high-resolution images, and are optimum as an interface IC with high-resolution CRT display and various new media.
The M61324SP keeps the power saving mode, and it can reduce ICC about 10mA under the condition that all Vcc are supplied.

FEATURES

Frequency band : RGB.....250MHz
: H,V.....10KHz to 200KHz
Input level:RGB.....0.7Vp-p(Typ.)
H,V TTL input .....3 to 5Vo-p (bipolar)
Only the G channel is provided with Sync-on video output.
THe TTL format is adopted for HV output.

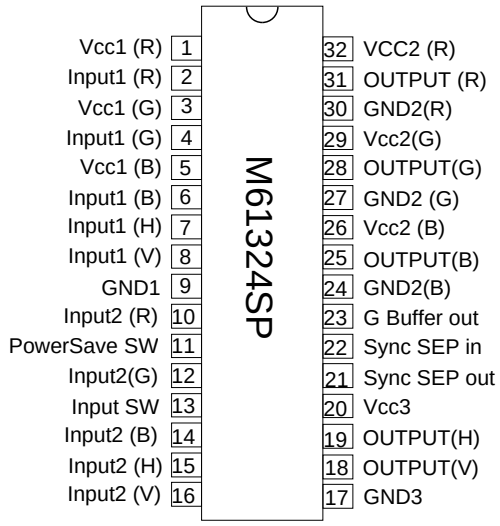
APPLICATION

Display monitor

RECOMMENDED OPERATING CONDITION

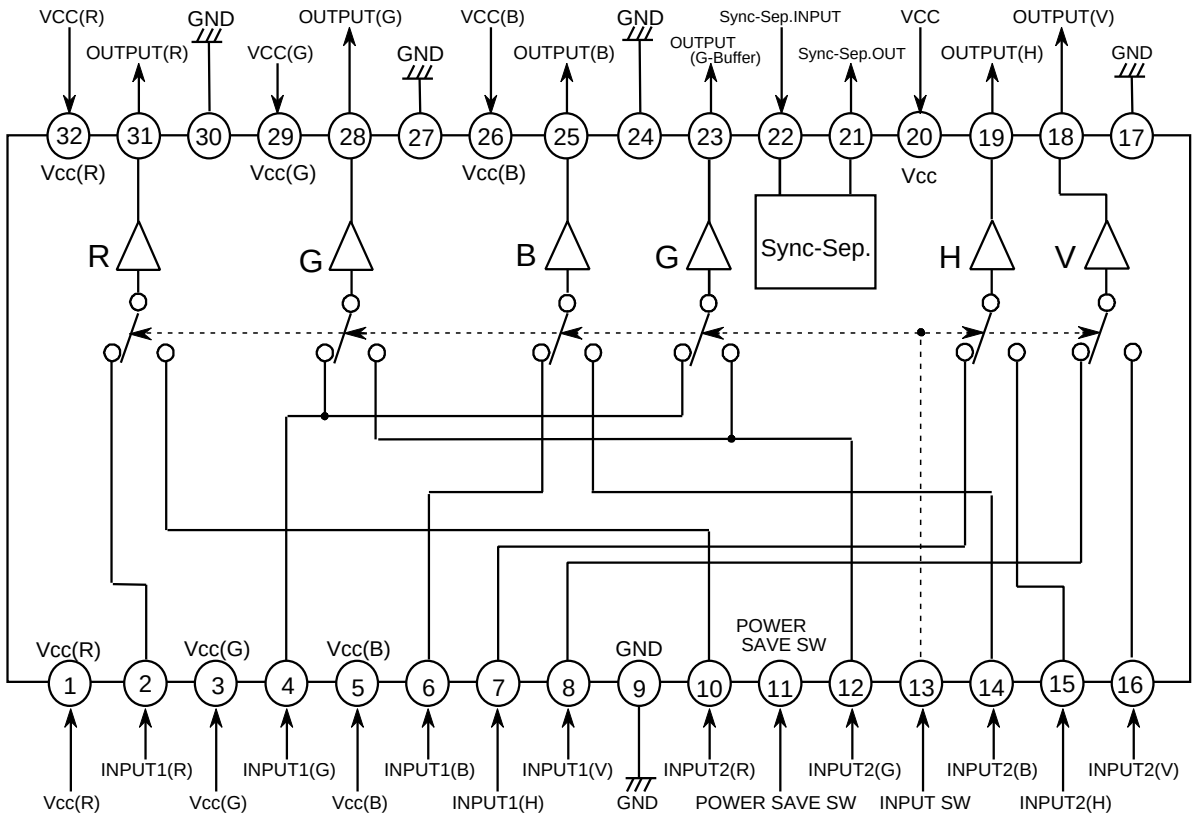
Supply voltage range.....4.75 to 5.25V
Rated voltage range.....5.0V

PIN CONFIGURATION(TOP VIEW)



OUTLINE:32P4B

BLOCK DIAGRAM



ABSOLUTE MAXMUM RATINGS (Ambient temperature: 25°C)

Parameter	Symbol	Rating	Unit
Supply voltage	Vcc	7.0	V
Power dissipation	Pd	1603	mW
Operating temperature	Topr	-20 to +80	°C
Storage temperature	Tstg	-40 to +150	°C
Electroststic discharge	Surge	+200	V
Recommended supply voltage	Vopr	5.0	V
Recommended sopply voltage range	Vopr'	4.75 to 5.25	V

ELECTRICAL CHARACTERISTICS (VCC=5.0V Ta = 25°C)

Symbol	Parameter	Test point (S)	Test conditions													Limits			Unit
			Input											SW					
			SW2 Rin1	SW4 Gin1	SW6 Bin1	SW7 Hin1	SW8 Vin1	SW10 Rin2	SW12 Gin2	SW14 Bin2	SW15 Hin2	SW16 Vin2	SW22 Sync	SW11 P.sav	SW13 Switch	Min.	Typ.	Max.	
Icc	Circuit current 1	—	b	b	b	b	b	b	b	b	b	b	b	a 3V	b	—	50	—	mA
IccSTBY	Circuit current 2	—	b	b	b	b	b	b	b	b	b	b	b	b	b	—	—	10	mA
(RGB SW)																			
Vdc1	Output DC voltage 1	31 28 25	b	b	b	b	b	b	b	b	b	b	b	a 3V	b	—	1.5	—	V
Vdc2	Output DC voltage 2	31 28 25	b	b	b	b	b	b	b	b	b	b	b	a 3V	a 3V	—	1.5	—	V
Vdc3	Output DC voltage 3	23	b	b	b	b	b	b	b	b	b	b	b	a 3V	b	—	0.9	—	V
Vdc4	Output DC voltage 4	23	b	b	b	b	b	b	b	b	b	b	b	a 3V	a 3V	—	0.9	—	V
VIMAX1	Maximum allowable input level 1	31 28 25	abb SG1	bab SG1	bba SG1	b	b	b	b	b	b	b	b	a 3V	b	—	1.8	—	Vp-p
VIMAX2	Maximum allowable input level 2	31 28 25	b	b	b	b	b	abb SG1	bab SG1	bba SG1	b	b	b	a 3V	a 3V	—	1.8	—	Vp-p
GV1	Voltage gain 1	31 28 25	abb SG2	bab SG2	bba SG2	b	b	b	b	b	b	b	b	a 3V	b	-0.1	0.7	1.3	dB
ΔGV1	Relative voltage gain 1	—	Relative to measured values above													-0.4	0	0.4	dB
GV2	Voltage gain 2	31 28 25	b	b	b	b	b	abb SG2	bab SG2	bba SG2	b	b	b	a 3V	a 3V	-0.1	0.7	1.3	dB
ΔGV2	Relative voltage gain 2	—	Relative to measured values above													-0.4	0	0.4	dB
GV3	Voltage gain 3	23	b	a SG2	b	b	b	b	b	b	b	b	b	a 3V	b	-0.6	0	0.6	dB
GV4	Voltage gain 4	23	b	b	b	b	b	b	a SG2	b	b	b	b	a 3V	a 3V	-0.6	0	0.6	dB

ELECTRICAL CHARACTERISTICS (cont.)

Symbol	Parameter	Test point (S)	Test conditions													Limits			Unit
			Input										SW						
			SW2 Rin1	SW4 Gin1	SW6 Bin1	SW7 Hin1	SW8 Vin1	SW10 Rin2	SW12 Gin2	SW14 Bin2	SW15 Hin2	SW16 Vin2	SW22 Sync	SW11 P.sav	SW13 Switch	Min.	Typ.	Max.	
Fc1	Freq.characteristic1 (100MHz)	31 28 25	abb SG4	bab SG4	bba SG4	b	b	b	b	b	b	b	b	a 3V	b	-1	0	1	dB
ΔFc1	Relative Freq.characteristic1 (100MHz)	—	Relative to measured values above													-1	0	1	dB
Fc2	Freq.characteristic2 (100MHz)	31 28 25	b	b	b	b	b	abb SG4	bab SG4	bba SG4	b	b	b	a 3V	a 3V	-1	0	1	dB
ΔFc2	Relative Freq.characteristic2 (100MHz)	—	Relative to measured values above													-1	0	1	dB
Fc3	Freq.characteristic3 (200MHz)	31 28 25	abb SG5	bab SG5	bba SG5	b	b	b	b	b	b	b	b	a 3V	b	-3	—	—	dB
Fc4	Freq.characteristic4 (200MHz)	31 28 25	b	b	b	b	b	abb SG5	bab SG5	bba SG5	b	b	b	a 3V	a 3V	-3	—	—	dB
CTI1	Crosstalk between two inputs1 (10MHz)	31 28 25	abb SG3	bab SG3	bba SG3	b	b	b	b	b	b	b	b	a 3V	a 3V	—	-60	-45	dB
CTI2	Crosstalk between two inputs2 (10MHz)	31 28 25	b	b	b	b	b	abb SG3	bab SG3	bba SG3	b	b	b	a 3V	b	—	-60	-45	dB
CTI3	Crosstalk between two inputs3 (100MHz)	31 28 25	abb SG4	bab SG4	bba SG4	b	b	b	b	b	b	b	b	a 3V	a 3V	—	-40	-30	dB
CTI4	Crosstalk between two inputs4 (100MHz)	31 28 25	b	b	b	b	b	abb SG4	bab SG4	bba SG4	b	b	b	a 3V	b	—	-40	-30	dB
CTC1	Crosstalk between channels1 (10MHz)	31 28 25	abb SG3	bab SG3	bba SG3	b	b	b	b	b	b	b	b	a 3V	b	—	-50	-40	dB
CTC2	Crosstalk between channels2 (10MHz)	31 28 25	b	b	b	b	b	abb SG3	bab SG3	bba SG3	b	b	b	a 3V	a 3V	—	-50	-40	dB
CTC3	Crosstalk between channels3 (100MHz)	31 28 25	abb SG4	bab SG4	bba SG4	b	b	b	b	b	b	b	b	a 3V	b	—	-30	-25	dB
CTC4	Crosstalk between channels4 (100MHz)	31 28 25	b	b	b	b	b	abb SG4	bab SG4	bba SG4	b	b	b	a 3V	a 3V	—	-30	-25	dB
Tr1	Pulse characteristic1	31 28 25	abb SG6	bab SG6	bba SG6	b	b	b	b	b	b	b	b	a 3V	b	—	1.6	2.5	nsec
Tf1		31 28 25	abb SG6	bab SG6	bba SG6	b	b	b	b	b	b	b	b	a 3V	b	—	1.6	2.5	nsec
Tr2	Pulse characteristic2	31 28 25	b	b	b	b	b	abb SG6	bab SG6	bba SG6	b	b	b	a 3V	a 3V	—	1.6	2.5	nsec
Tf2		31 28 25	b	b	b	b	b	abb SG6	bab SG6	bba SG6	b	b	b	a 3V	a 3V	—	1.6	2.5	nsec

ELECTRICAL CHARACTERISTICS (cont.)

Symbol	Parameter	Test point (S)	Test conditions													Limits			Unit
			Input											SW					
			SW2 Rin1	SW4 Gin1	SW6 Bin1	SW7 Hin1	SW8 Vin1	SW10 Rin2	SW12 Gin2	SW14 Bin2	SW15 Hin2	SW16 Vin2	SW22 Sync	SW11 P.sav	SW13 Switch	Min.	Typ.	Max.	
(HV SW)																			
Vdch1	High level output voltage 1	18 19	b	b	b	a SG8	a SG8	b	b	b	b	b	b	a 3V	b	3.8	4.2	—	V
Vdch2	High level output voltage 2	18 19	b	b	b	b	b	b	b	b	a SG8	a SG8	b	a 3V	a 3V	3.8	4.2	—	V
Vdcl1	Low level output voltage 1	18 19	b	b	b	a SG8	a SG8	b	b	b	b	b	b	a 3V	b	—	0.2	0.5	V
Vdcl2	Low level output voltage 2	18 19	b	b	b	b	b	b	b	b	a SG8	a SG8	b	a 3V	a 3V	—	0.2	0.5	V
VithH	Input threshold voltage H	18 19	b	b	b	a SG8	a SG8	b	b	b	b	b	b	a 3V	b	1.8	2.0	2.2	V
VithL	Input threshold voltage L	18 19	b	b	b	a SG8	a SG8	b	b	b	b	b	b	a 3V	b	1.0	1.4	1.6	V
Tr3	Rising time 3	18 19	b	b	b	a SG8	a SG8	b	b	b	b	b	b	a 3V	b	—	25	—	nsec
Tf3	Falling time 3	18 19	b	b	b	a SG8	a SG8	b	b	b	b	b	b	a 3V	b	—	15	—	nsec
HVdr	Rising deley time	18 19	b	b	b	a SG8	a SG8	b	b	b	b	b	b	a 3V	b	—	40	60	nsec
HVDf	Falling deley time	18 19	b	b	b	a SG8	a SG8	b	b	b	b	b	b	a 3V	b	—	40	60	nsec
(SYNC SEP.)																			
SYrv	Sync on G input minimum voltage	21	b	b	b	b	b	b	b	b	b	b	a SG7	a 3V	—	0.2	—	—	Vp-p
SYVH	Sync output high level voltage	21	b	b	b	b	b	b	b	b	b	b	a SG7	a 3V	—	3.8	4.3	—	V
SYVL	Sync output low level voltage	21	b	b	b	b	b	b	b	b	b	b	a SG7	a 3V	—	—	0.2	0.5	V
STr	Sync output rising time 3	21	b	b	b	b	b	b	b	b	b	b	a SG7	a 3V	—	—	25	—	nsec
STf	Sync output falling time 3	21	b	b	b	b	b	b	b	b	b	b	a SG7	a 3V	—	—	15	—	nsec
SDr	Sync output rising deley time	21	b	b	b	b	b	b	b	b	b	b	a SG7	a 3V	—	—	40	60	nsec
SDf	Sync output falling deley time	21	b	b	b	b	b	b	b	b	b	b	a SG7	a 3V	—	—	40	60	nsec
(CHANNEL SERECT SW , POWER SAVE SW)																			
Vthch1	Channel select SW threshold voltage 1	—	a SG6	a SG6	a SG6	a SG8	a SG8	b	b	b	b	b	a SG7	a 3V	a variable	2.5	—	—	V
Vthch2	Channel select SW threshold voltage 2	—	a SG6	a SG6	a SG6	a SG8	a SG8	b	b	b	b	b	a SG7	a 3V	a variable	—	—	1.0	V
VthPH	Power save SW threshold voltage 1	—	a SG6	a SG6	a SG6	a SG8	a SG8	b	b	b	b	b	a SG7	a variable	b	2.0	—	—	V
VthPL	Power save SW threshold voltage 2	—	a SG6	a SG6	a SG6	a SG8	a SG8	b	b	b	b	b	a SG7	a variable	b	—	—	1.0	V

ELECTRICAL CHARACTERISTICS TEST METHOD

Circuit current 1

No signal. Measure the total circuit current as Icc when supplying 3VDC to Pin11.

Circuit current 2

No signal. Measure the total circuit current as IccSTBY when Pin11 connected to GND.

Output DC voltage 1,2

Set SW13 to GND (or OPEN), measure the DC voltage of TP31(TP28,TP25) when there is no signal input. The DC voltage is as vdc1(vdc2).

Output DC voltage 3,4

Measure the DC voltage TP23 same as "Output DC voltage 1,2". The DC voltage is Vdc3(Vdc4).

Maximum allowableinput level 1,2

Set SW13 to GND, input SG1 to Pin2 only. Gradually increasing the SG1 amplitude, read the amplitude of the input signal when the output waveform of TP31 is strained. The value is as $Vi_{max}1$. In the same way, measure $Vi_{max}1$ in response to inputs in Pin4 and Pin6 only.

Then set SW13 to OPEN, measure $Vi_{max}2$ in response to inputs in Pin10,12 and 14 only.

Voltage gain 1,2

1. The conditions is as table.
2. Set SW13 to GND, input SG2(0.7Vp-p) to Pin2 only. Read the output amplitude of TP31. The value is as $V_{OR}1$.
3. Voltage gain G_V1 is

$$G_V1 = 20 \text{ LOG} \frac{V_{OR}1 \ [Vp\text{-}p]}{0.7} \quad (dB)$$

4. In the same way, calculate $G_V1$in response to inputs in Pin4 and Pin6 only.
5. Then set SW13 to OPEN, measure G_V2 in response to inputs in Pin10,12 and 14 only.

Relative voltage gain 1,2

1. Calculate relative voltage gain ΔG_V1 by the following formula.

$$\Delta G_V1 = G_V1R - G_V1G, \ G_V1G - G_V1B, \ G_V1B - G_V1R$$

2. In the same way, calculate ΔG_V2.

Voltage gain 3,4

1. The conditions is as table.
2. Read the output amplitude of TP23.
3. Calculate G_V3, $G_{V1}4$ same as "Voltage gain 1".

Freq.characteristic 1,2 / Relative freq.characteristic 1,2

1. The conditions is as table. This measurement shall use active probe.
2. Set SW13 to GND, input SG4(0.7Vp-p) to Pin2 only. Measure TP31 output amplitude as $V_{OR}1$.
   In the same way,input SG2(0.7Vp-p) to Pin2 only. Measure TP31 output amplitude as $V_{OR}2$.
3. Freq.characteristic1 F_C1 is

$$F_C1 = 20 \text{ LOG} \frac{V_{OR}2 \ [Vp\text{-}p]}{V_{OR}1 \ [Vp\text{-}p]} \quad (dB)$$

4. In the same way, calculate F_C1 in response to inputs in Pin4 and Pin6 only.
5. The defference between of each channel Freq.characteristic is as ΔF_C1.
6. Then set SW13 to OPEN, measure F_C2 and ΔF_C2 in response to inputs in Pin10,12 and 14 only.

Freq.characteristic 3,4

Measure the F_C3, F_C4 when SG5 of input signal. (For reference)

Crosstalk between two inputs 1,2

1. The conditions is as table. This measurement shall use active probe.
2. Set SW13 to GND, input SG3 to Pin2 only. Read the output amplitude of TP31. The value is as $V_{OR}3$.
3. Then set SW13 to OPEN, read the output amplitude of TP31. The value is as $V_{OR}3'$.
4. Crosstalk between two inputs 1 C.T.I.1 is

$$C.T.I.1 = 20\ LOG \frac{V_{OR}3'\ [Vp\text{-}p]}{V_{OR}3\ [Vp\text{-}p]} \quad (dB)$$

5. In the same way, calculate C.T.I.1 in response to inputs in Pin4 and Pin6 only.
6. Then set SW13 to OPEN, input SG2 to Pin10 only. Read the output amplitude of TP31. The value is as $V_{OR}4$.
7. Set SW13 to GND, read the output amplitude of TP31. The value is as $V_{OR}4'$.
8. Crosstalk between two inputs 1 C.T.I.2 is

$$C.T.I.2 = 20\ LOG \frac{V_{OR}4'[Vp\text{-}p]}{V_{OR}4[Vp\text{-}p]} \quad (dB)$$

9. In the same way, calculate C.T.I.2 in response to inputs in Pin12 and Pin14 only.

Crosstalk between two inputs 3,4

Set SG4 as the input signal, and then the same method astable, measure C.T.I.3, C.T.I.4.

Crosstalk between channels 1,2

1. The conditions is as table. This measurement shall use active probe.
2. Set SW13 to GND, input SG3 (0.7Vp-p) to Pin2 only. Read the output amplitude of TP31. The value is as $V_{OR}5$.
3. Next, measure TP28, TP25 in the same state, and the amplitude is as $V_{OG}5$, $V_{OB}5$.
4. Crosstalk between channels1 C.T.C1 is

$$C.T.C1 = 20\ LOG \frac{V_{OG}5\ \text{or}\ V_{OB}5}{V_{OR}5} \quad (dB)$$

5. In the same way, calculate C.T.C.1 in response to inputs in Pin4 and Pin6 only.
6. Then set SW13 to OPEN, input SG3(0.7Vp-p) to Pin10 only.
   Read the output amplitude of TP31. The value is as $V_{OR}6$.
7. Next, measure TP28, TP25 in the same state, and the amplitude is as $V_{OG}6$, $V_{OB}6$.
8. Crosstalk between two inputs 1 C.T.C.2 is

$$C.T.C2 = 20\ LOG \frac{V_{OG}6\ \text{or}\ V_{OB}6}{V_{OR}6} \quad (dB)$$

9. In the same way, calculate C.T.C.2 in response to inputs in Pin9 and Pin11 only.

Crosstalk between channels 3,4

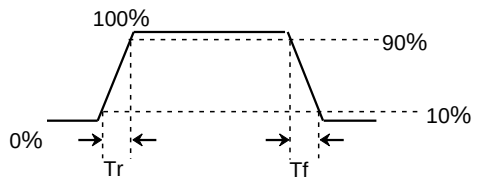
Set SG4 as the input signal, and then the same method astable, measure C.T.C3, C.T.C4.

Pulse characteristic 1,2

1. The conditions is as table. (SG5 amplitude 0.7Vp-p) Set SW13 to GND (or OPEN).
2. Measure rising Tri and falling Tfi for 10%~90% of the input pulse with active plobe.
3. Next, measure rising Tro and falling Tfo for 10%~90% of the output pulse with active plobe.
4. Pulse characteristic Tr1, Tf1(Tr2, Tf2) is

$$Tr1(Tr2) = \sqrt{(Tro)^2 - (Tri)^2} \quad (nsec)$$

$$Tf1(Tf2) = \sqrt{(Tfo)^2 - (Tfi)^2} \quad (nsec)$$



<HV-SW>

Hi level output voltage 1,2 / Lo level output voltage 1,2

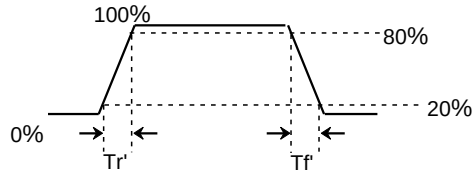
1. The conditions is as table. Input SG8 to Pin7 (or Pin8). Set SW13 to GND, read the output High level and low voltage of TP19, TP18. The value is as Vdch1, Vdcl1.
2. Input SG8 to Pin15 (or Pin16). Set SW13 to OPEN, read the output High level and low voltage of TP19, TP18. The value is as Vdch2, Vdcl2.

Input threshold voltage H / Input threshold voltage L

1. Set SW13 to GND (or OPEN). Gradually increasing the voltage of Pin7 (or Pin15) from 0V, measure the input voltage of Pin7 (or Pin15) when the TP19 voltage turnd high level (3.8V or more). The value is as VithH.
2. Gradually decreasing the voltage of Pin7 (or Pin15) from 3V, measure the input voltage of Pin7 (or Pin15) when the TP19 voltage turnd low level (0.5V or less). The value is as VithL.
3. In the same way, measure the input voltage of Pin8 (or Pin16) as VithH, VithL.

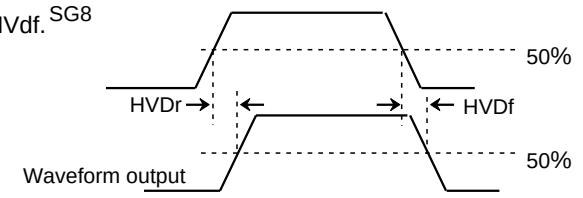
Rising time / Falling time

1. The conditions is as table. This measurement shall use active probe.
2. Measure rising Tri and falling Tfi for 20%~80% of the output pulse as Tr3, Tf3 (Tr4, Tf4) .



Rising deley time / Falling deley time

Set SW13 to GND (or OPEN), input SG8 to Pin7 (or Pin15).
Measure the rising deley time HVdr and the falling deley time HVdf.
In the same way, measure HVdr and HVdf when input SG8 to Pin8 (or Pin16).



<Sync-Separation>

Sync input minimum voltage

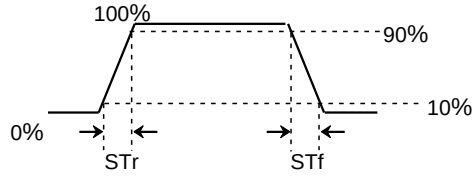
Gradually decreasing the amplitude of SG7 in Pin22, measure the amplitude of SG7 when the Sync-Sep output signal turn off . The value is as SYrv.

Sync output High level voltage / Sync output Low level voltage

Input SG7 to Pin22, read the output High level and low voltage of TP21. The value is as SYVH, SYVL.

Sync output rising time / Sync output falling time

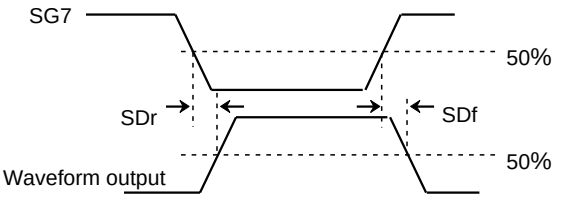
1. The conditions is as table. (SG7 amplitude 0.3Vp-p) This measurement shall use active probe.
2. Measure rising Tri and falling Tfi for 10%~90% of the input pulse as STr, STf .



Sync output rising deley time

Sync output falling deley time

Input SG7 to Pin22. Measure the rising deley time Sdr and the falling deley time Sdf.



<Others>

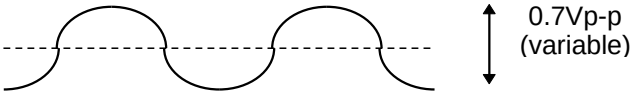
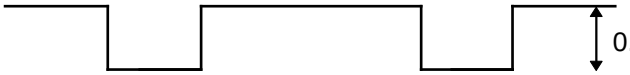
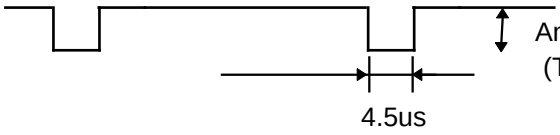
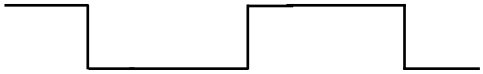
Channel select SW threshold 1,2

1. Gradually increasing the voltage of Pin13 from 0V, measure the maximum voltage of Pin13 when the channel 1 is selected. The value is as Vthch1.
2. Gradually decreasing the voltage of Pin13 from 5V, measure the minimum voltage of Pin13 when the channel 2 is selected. The value is as Vthch2.

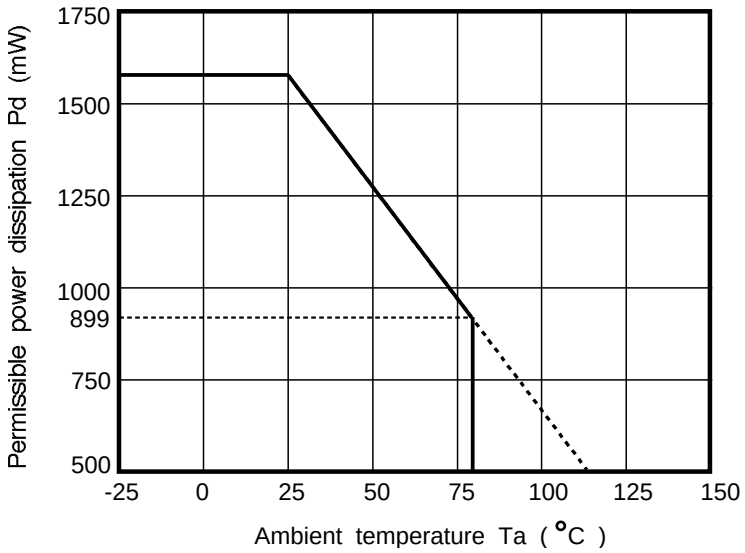
Power save SW threshold 1,2

1. Gradually increasing the voltage of Pin11 from 0V, measure the maximum voltage of Pin11 when the Power save mode . The value is as VthPL.
2. Gradually decreasing the voltage of Pin13 from 5V, measure the minimum voltage of Pin11 when the Power save mode . The value is as VthPH.

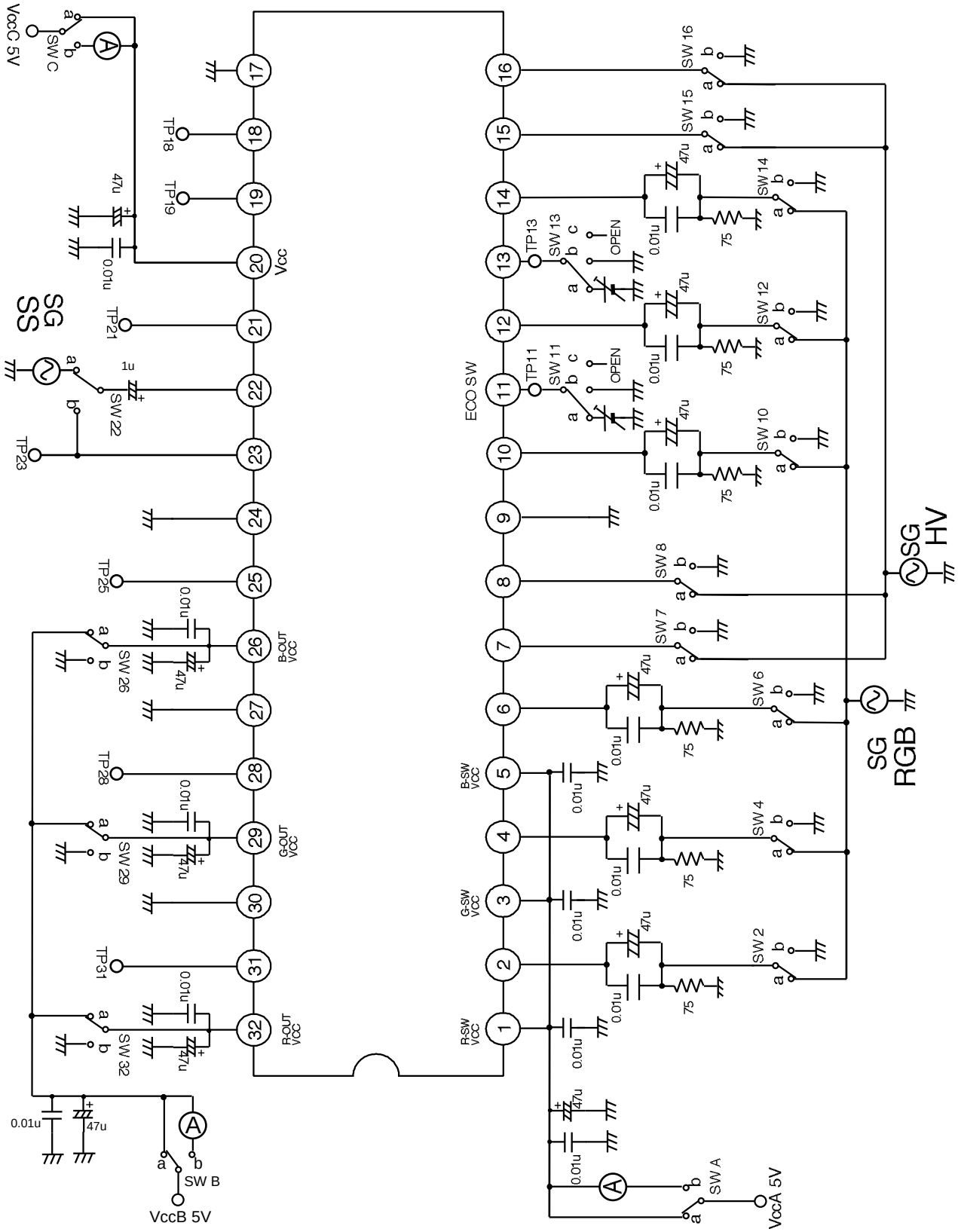
INPUT SIGNAL

SG1	Sine wave(f=60KHz, 0.7Vp-p(Amplitude variable)) 
SG2	Sine wave(f=1MHz, 0.7Vp-p(Amplitude variable))
SG3	Sine wave(f=10MHz, 0.7Vp-p(Amplitude variable))
SG4	Sine wave(f=100MHz, 0.7Vp-p(Amplitude variable))
SG5	Sine wave(f=250MHz, 0.7Vp-p(Amplitude variable))
SG6	 DUTY 80% fH=60kHz 0.7Vp-p
SG7	Sync (fH=60KHz) 
SG8	TTL  5V 0V DUTY=50% fH=60kHz

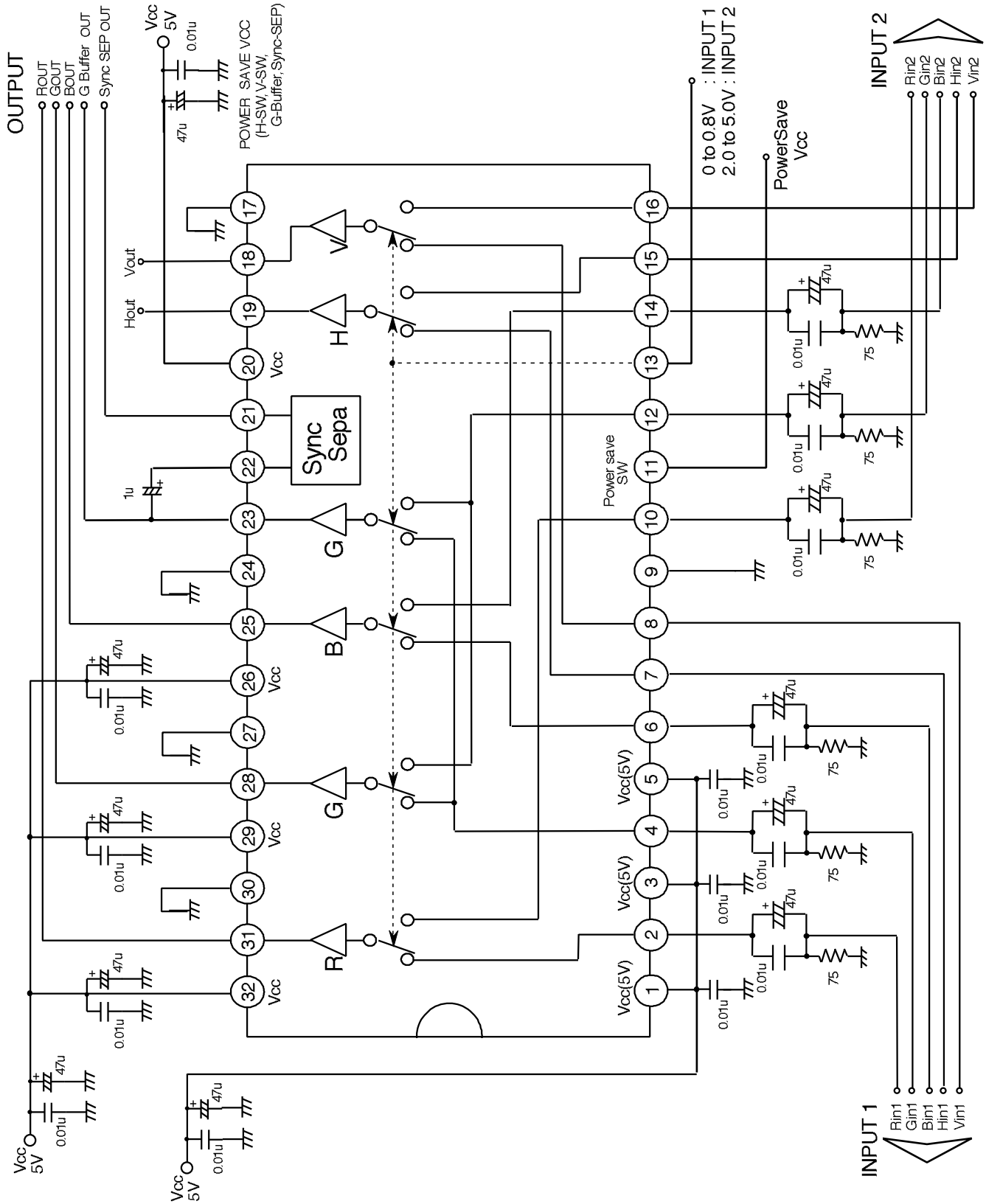
THERMAL DERATING CURVE



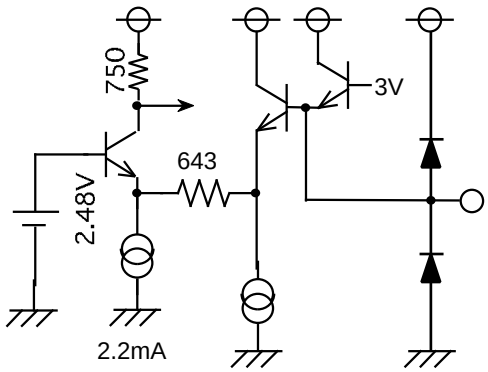
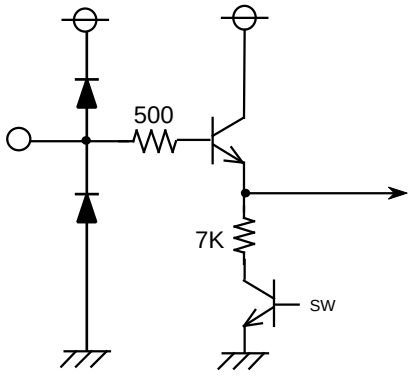
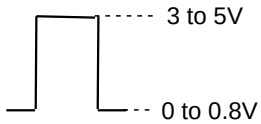
TEST CIRCUIT



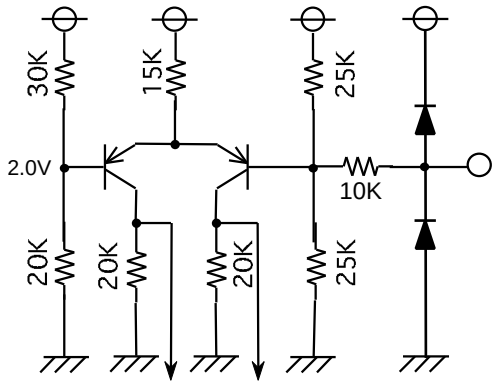
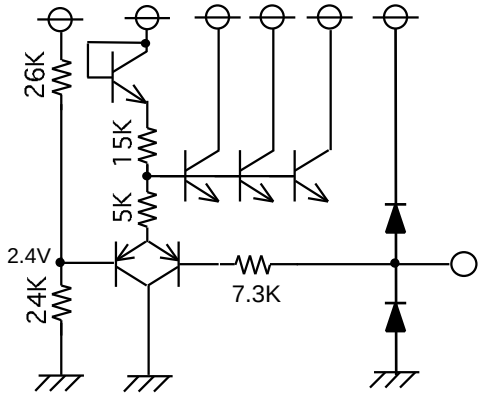
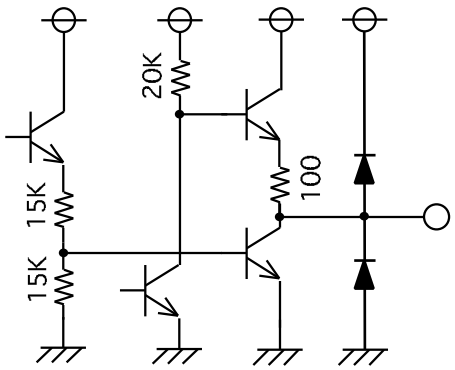
APPLICATION EXAMPLE



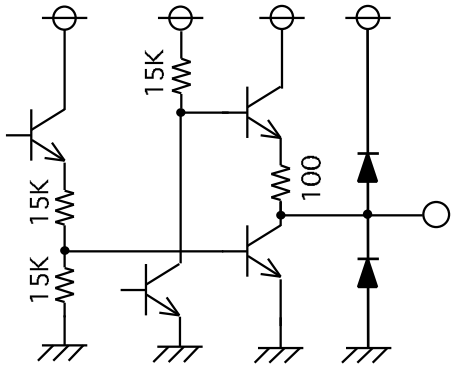
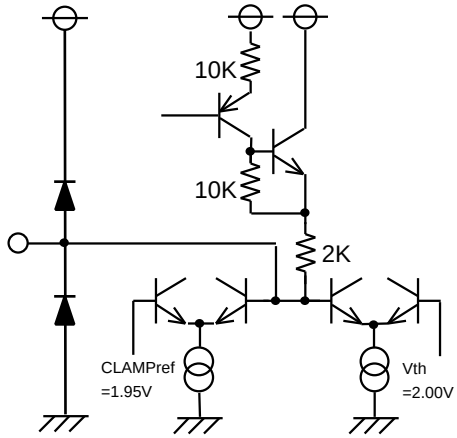
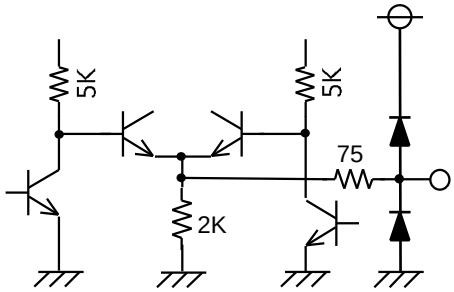
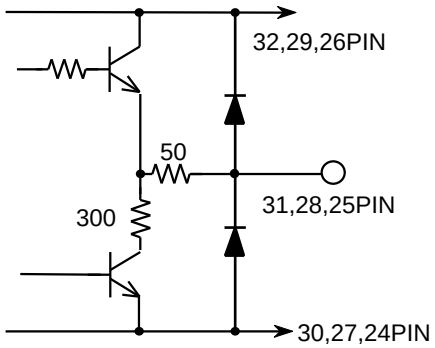
DISCRIPTION OF PIN

Pin No.	Description	DC Voltage[V]	Peripheral circuits at pins	Notes
1 3 5 20	Vcc(R) Vcc(G) Vcc(B) Vcc(H,V,Sync-Sep.)	5.0	———	
26 29 32	Vcc(ROUT) Vcc(GOUT) Vcc(BOUT)	5.0	———	
2 4 6 10 12 14	Input1(R) Input1(G) Input1(B) Input2(R) Input2(G) Input2(B)	2.3		Input signai with low impedance.
7 8 15 16	Input1(H) Input1(V) Input2(H) Input2(V)	——		Input pulse between 3V and 5V. 
9 17 24 27 30	GND(V-SW) GND (H,V,Sync-Sep.) GND(B-out) GND(G-out) GND(R-out)	GND	———	

DISCRIPTION OF PIN (cont.)

Pin No.	Description	DC Voltage[V]	Peripheral circuits at pins	Notes
11	PwrSave-SW	2.5		Do not apply more 5V DC voltage.
13	CONT-SW	2.4		Do not apply more 5V DC voltage.
18 19	Vout Hout	—		

DISCRIPTION OF PIN (cont.)

Pin No.	Description	DC Voltage[V]	Peripheral circuits at pins	Notes
21	Sync sep OUT	——		
22	Sync sep IN	——		Connect a capacitance between the pin and GND when not use SYNC-SEP.
23	G Buffer OUT	——		
25 28 31	Video OUT (B) Video OUT (G) Video OUT (R)	1.5		

NOTE HOW TO USE THIS IC

1. R,G,B input signal is 0.7Vp-p of standard video signal.

2. H,V input is 5.0V TTL type.

3. Input signal with sufficient low inpedance to input terminal.

4. The terminal of R,G,B output pin are shown as Fig.1.
   When resistance is connected between the pin31(28,25) and GND,
   Icc will be increase.

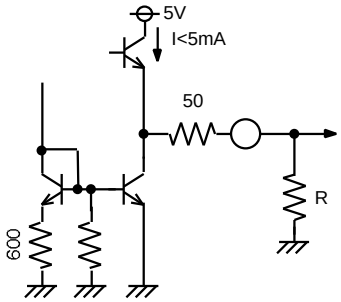


Fig.1

5. Swicth(Pin13) can be changed by supplying some voltage as Fig.2.
   0 to 0.5V:INPUT1
   2.5 to 5V:INPUT2
   Do not apply Vcc or more DC voltage.

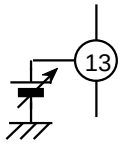


Fig.2

6. Power save mode is provided for saving Icc less than about 10mA as Fig.3.
   0 to 0.5V:Power save mode (H.V-SW,Sync-Sep.,G-Buffer)
   2.5 to 5V:Normal mode
   Do not apply 5V or more DC voltage.

7. When not use the Sync-separation circuit built in this IC, capacitance of
   several tens of pF is required between the pin22 and GND.

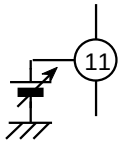


Fig.3

CAUTIONS FOR MANUFACTURING BOARDS

Built-in wide band preamplifier may cause oscillation due to the wiring shape on the board.
Be careful for the following points.

Vcc shall use a stable power supply.
(Individual Vcc should use an independent power supply.)

GND should be as wide as possible. Basically,solid earth should be used.
Make the load capacitance of output pins as small as possible.

Also ground the hold capacitance to stable GND ,wicth is as near to the pin as possible.

Insertion of a resistance of several tens of ohms between the output pin and the circuit
at the next stage makes oscillation harder.

When inserting an output pull-down resistance, make wire between the output pin and the
resistance as short as possible.