

M62457FP

Peak hold IC for 5 band spectrum analyzer displays

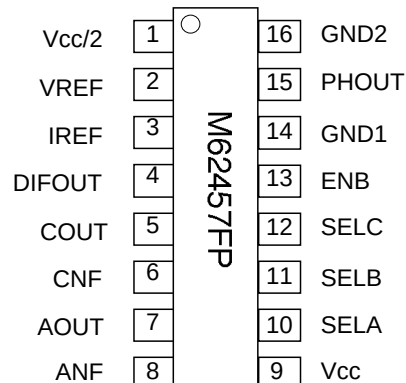
DESCRIPTION

The M62457FP is 5 band peak hold ICs that use microprocessor time division to produce serial output for spectrum analyzer displays.

FEATURES

- 5 band peak hold elements for spectrum analyzer displays.
- Discharge time constant circuit for each band is on the chip.
- Single 5V power supply.

PIN CONFIGURATION (TOP VIEW)



Outline 16P2N-A

APPLICATION

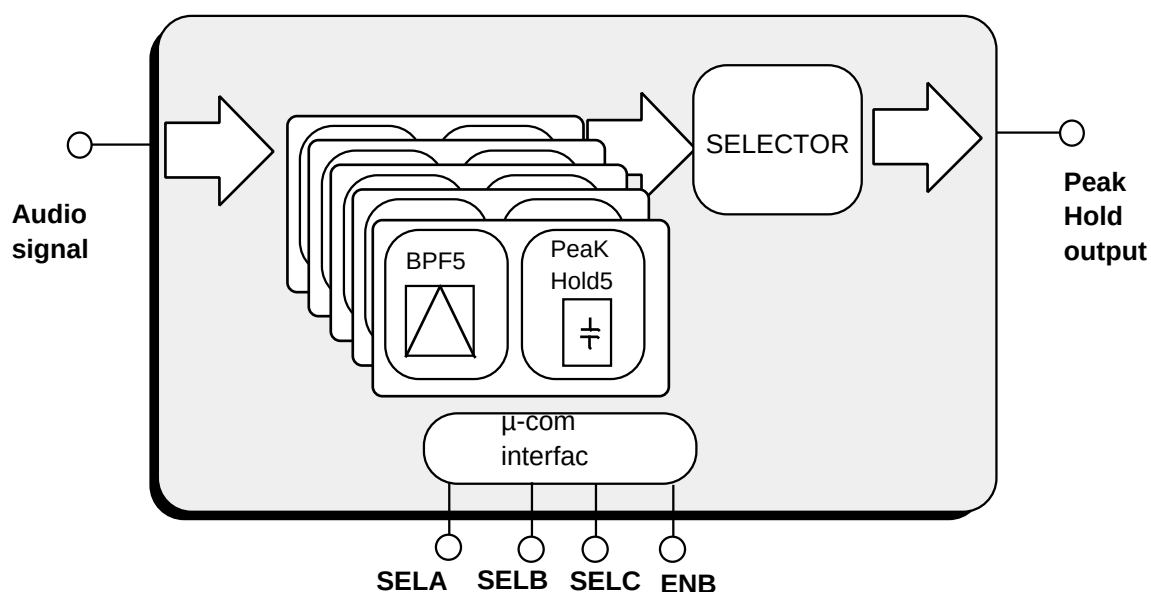
CD radio cassette players , mini-component stereo systems, car stereos

RECOMMENDED OPERATING CONDITIONS

Supply voltage range •••• 4.5 to 6.5V

Rated supply voltage •••• 5.0V

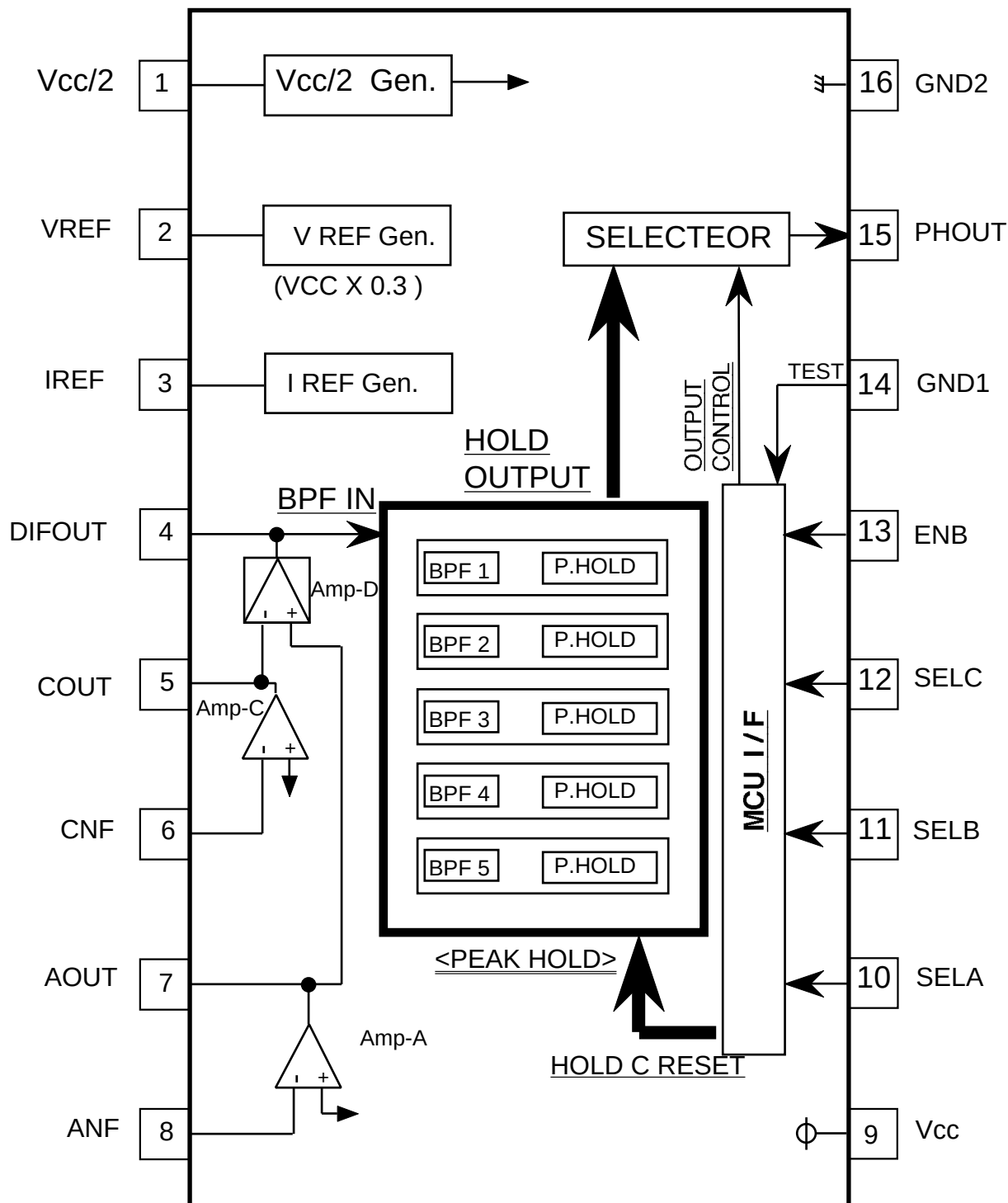
SYSTEM BLOCK DIAGRAM



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PIN CONFIGURATION AND IC INTERNAL BLOCK DIAGRAM



(Notes) f1=105Hz, f2=340Hz, f3=1KHz, f4=3.4KHz, f5=10.5KHz
(The value is the design value)

Functional description

- (1) Audio signal passes Amp-a and Amp-d, and it is input into BPF/peak hold circuit for spectrum analyzer.

Basic use examples, the last output signal is input into A/D of microprocessor. However, VCC, GND of analog series had better be common with VCC, GND of microprocessor. The microprocessor does ground isolation to analog series. Amp-C is the input amplifier to reject common-mode signal (noise), it utilizes effect of common-mode rejection of Amp-D.

- (2) BPF/peak hold circuit is setting of 5 band spectrum analyzer

< center frequency >

f1=105Hz

f2=340Hz

f3=1KHz

f4=3.4KHz

f5=10.5KHz

(The value is the design value)

Center frequency and Q of BPF is done general setting of like next.

$\omega_0 = gm/C$

gm: mutual conductance of inside amplifier circuit

(It depends on outside resistor of Pin.No.3)

C: inside capacitor

$Q = (R_1 + R_2)/R_1$; it is fixed by inside resistor ratio.

(The design value is 3.5)

- (3) The hold capacitor of peak hold circuit use inside capacitor.

When a selection of hold output is over the reset signal of hold value,

The reset signal is made automatically.

(Discharge pulse : -3dB typ. output value fall)

- (4) Output voltage of peak hold circuit is $V_{cc}/2$ (Pin.No1)

When it is selected by the output select circuit, it is converted into the voltage of GND standard and outputs it in PHout (Pin.No.15).

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PIN DESCRIPTION 1

PIN No.	Name	I / O	Function
1	Vcc / 2	I	1/2Vcc supply terminal
2	VREF	I	0.3Vcc supply terminal
3	IREF	I	BPF center frequency setting current terminal
4	DIFOPUT	O	Output of amplifier (BPF input signal)
5	COUT	O	Output of amplifier for analog COM series
6	CNF	I	Inverted input of amplifier for analog COM series
7	AOUT	O	Output of amplifier for analog signal series
8	ANF	I	Inverted input of amplifier for analog signal series
9	Vcc	I	System supply terminal
10	SELA	I	Output setting control terminal A (logic input)
11	SELB	I	Output setting control terminal B (logic input)
12	SELC	I	Output setting control terminal C (logic input)
13	ENB	I	Output setting control enable terminal (logic input)
14	GND1	I	Ground1 (it is assumed in the voltage same as PIN16)
15	PHOUT	O	Peak hold output terminal
16	GND2	I	Ground2 (signal series)

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PIN DESCRIPTION 2

PIN No.	Name	I / O	Peripheral circuit of pins
1	Vcc / 2	I	
2	VREF	I	
3	IREF	I	
4	DIFOPUT	O	
5	COUT	O	
6	CNF	I	
7	AOUT	O	
8	ANF	I	
9	Vcc	I	
10	SELA	I	
11	SELB	I	
12	SELC	I	
13	ENB	I	
14	GND1	I	_____
15	PHOUT	O	
16	GND2	I	_____

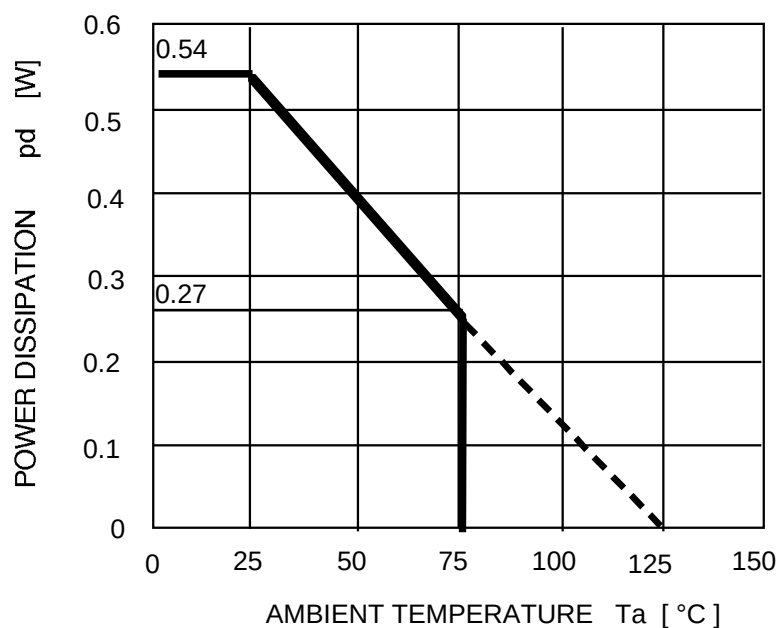
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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V _{cc(max)}	Supply Voltage		7	V
P _d	Power dissipation	T _a ≤ 25°C	540	mW
K θ	Thermal derating	T _a > 25°C	5.4	mW/°C
T _{opr}	Operating temperature		-20 to +75	°C
T _{stg}	Storage temperature		-40 to +125	°C
V _{i(max)}	Allowable input voltage range		GND-0.3 to V _{cc} +0.3	V
V _{o(max)}	Allowable output voltage range		GND to V _{cc}	V

THERMAL DERATING
(MAXIMUM RATING)



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Recommended operating conditions

(Ta=25°C unless otherwise noted)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Supply voltage	V _{CC}		4.5	5.0	6.5	V
Logic input H level voltage	V _{IH}	V _{CC} =5V	2.5	—	V _{CC}	V
Logic input L level voltage	V _{IL}	V _{CC} =5V	GND	—	0.5	V

(Note1)

The center frequency characteristics of BPF are determined by the resistor connected between 3PIN terminal and GND.If it is necessary,use a variable resistor (note:all band will shift together).

Q of BPF is fixed in 3.5 by inside circuit.

(note 2)

The output resistor of peak hold output(PIN 15) is 10KΩtyp.

You do the input resistor of microprocessor side in a value fully big for 10KΩ.

(note 3)

Set up as the control voltage from a microprocessor during GND-0.3V and 5V.

If the voltage of tolerance outside is added, conserve it resistance or diode.

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Output select logic table

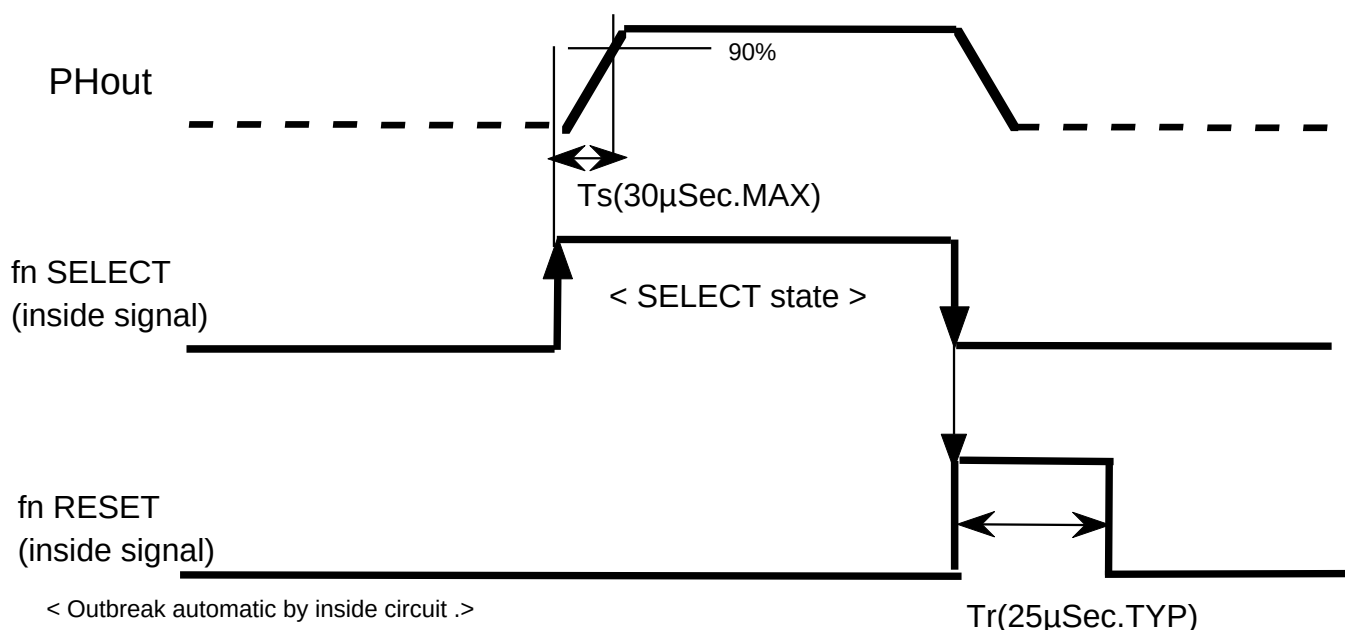
PHout (PinNo.15)	ENB	SELA	SELB	SELC	Note
GND(output stop)	0	X	X	X	Don't Care
GND	1	0	0	0	
f1 ; 105Hz	1	0	0	1	
f2 ; 340Hz	1	0	1	0	
GND	1	0	1	1	
f3 ; 1KHz	1	1	0	0	
GND	1	1	0	1	
f4 ; 3.4KHz	1	1	1	0	
f5 ; 10.5KHz	1	1	1	1	

< Note1 >

"0"=low level,"1"=high level,"X"="0"or "1"

< Note2 >

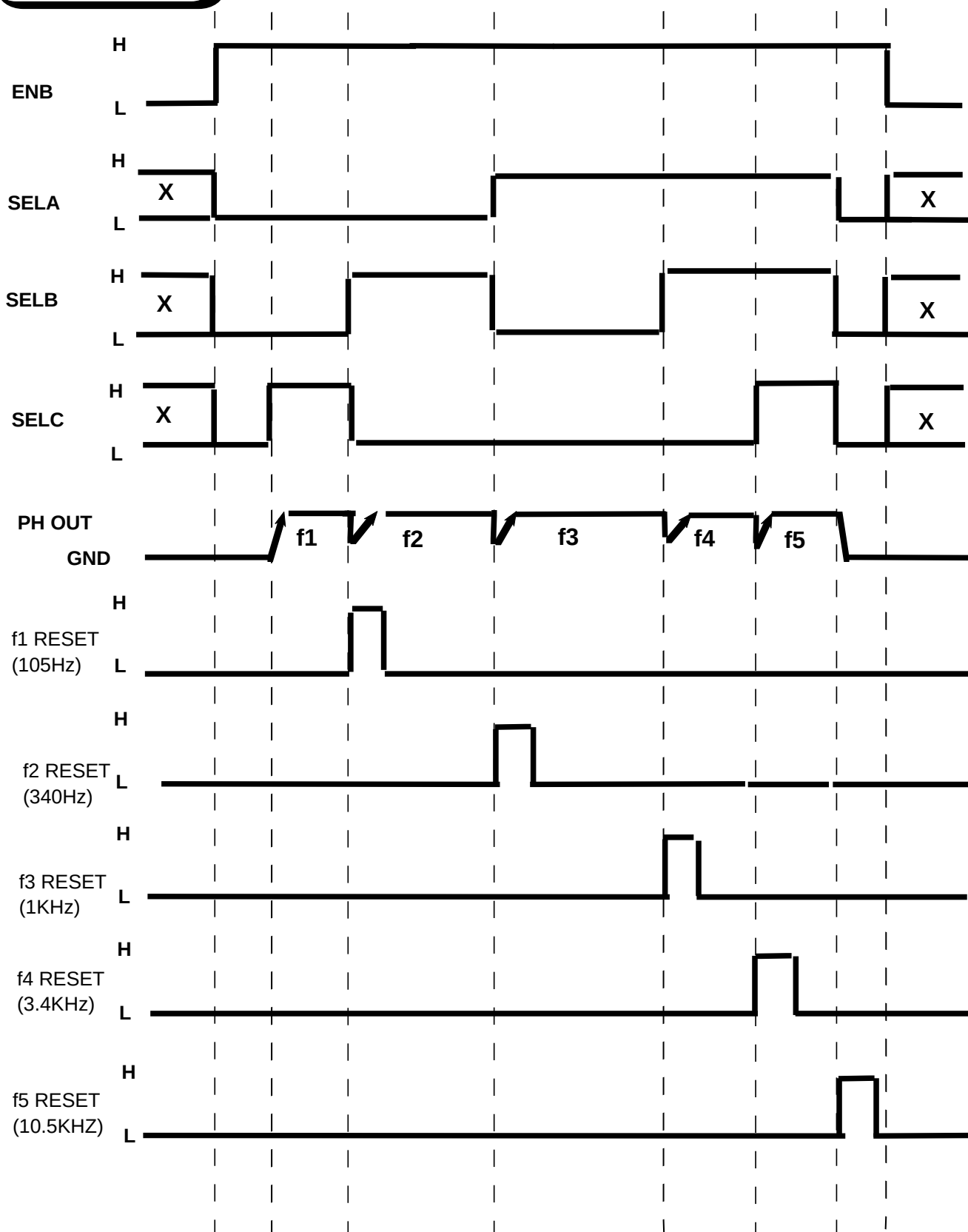
you hold the output setting state by more than 30 μ Sec for a long time
(When the output setting state is short, movement of output value and reset
signal become instable)



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Timing chart



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ELECTRICAL CHARACTERISTICS

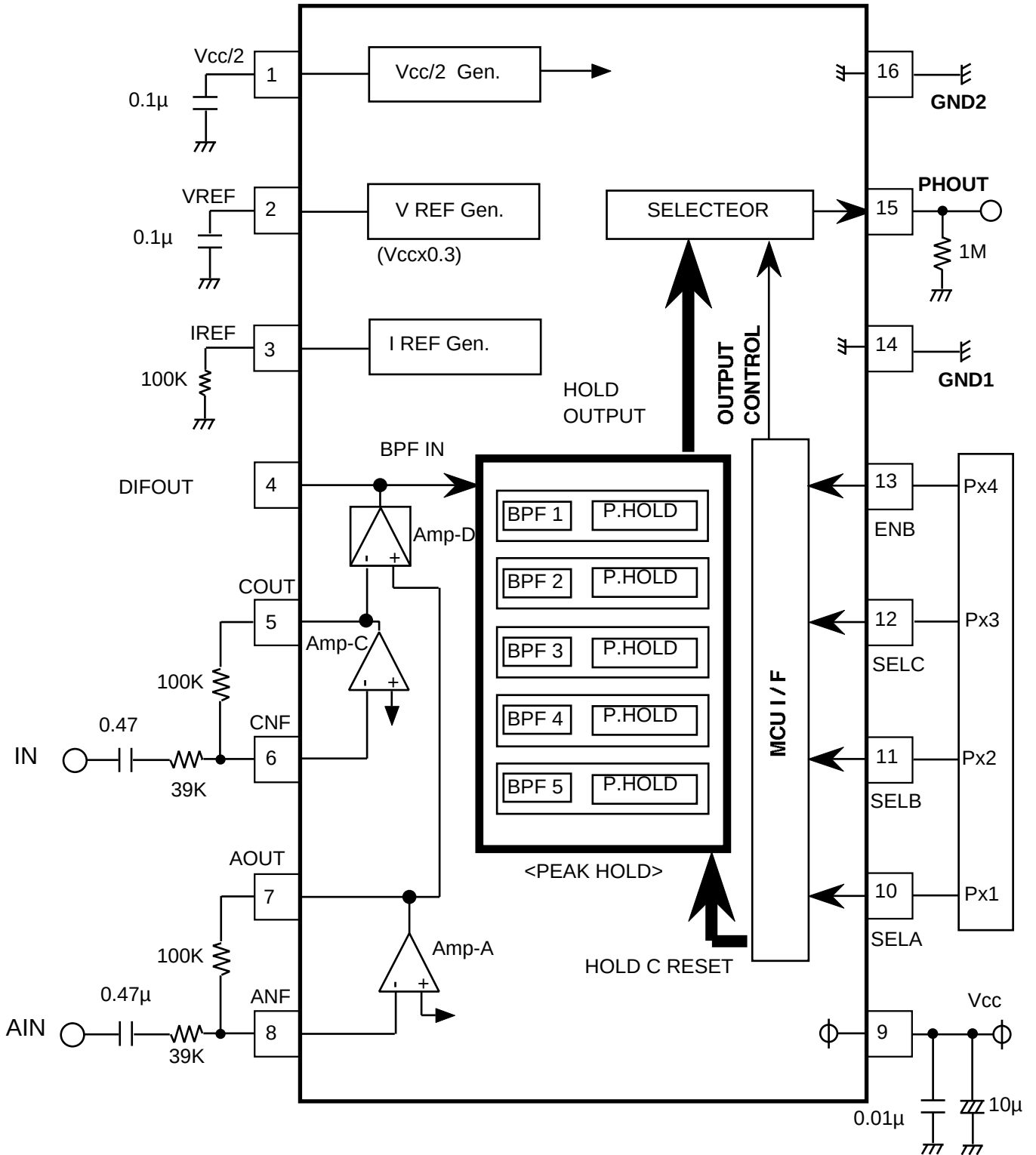
(Ta=25°C, Vcc=5.0V, PHout(Pin.No.15) RL=1MΩ unless otherwise noted.
VAIN=-30dBV, f=1KHz, ENB(Pin.No.13)=1)

Parameter	Symbol	Condition	Limits			Unit
			Min	typ	Max	
Circuit current	Icc	No signal, No select (ENB, SELA, SELB, SELC=0)	—	8	13	mA
Maximum output level	Vo	f1 to f5 Measured at each output (VAIN= -14dBV)	2.7	3.5	—	V
Output offset voltage	Vos	f1 to f5 Measured at each output (No signal, ENB=0/1)	—	30	60	mV
Logic input H level	VIH		2.5	5.0	Vcc +0.3	V
Logic input L level	VIL		GND -0.3	0	0.5	V
Common-mode rejection ratio	CMRR		25	50	—	dB
f1 output level	Vo1	f1 (fin=105Hz)	0.5	1.0	1.70	V
f2 output level	Vo2	f2 (fin=340Hz)	0.5	1.0	1.70	V
f3 output level	Vo3	f3 (fin=1KHz)	0.5	1.0	1.70	V
f4 output level	Vo4	f4 (fin=3.4KHz)	0.5	1.0	1.70	V
f5 output level	Vo5	f5 (fin=10.5KHz)	0.5	1.0	1.70	V
Output response time	Ts	The time from the rise of output selection until the rise of PHout(90% of peak)	—	20	30	μsec
Discharge level	DS	< Reference > Inside reset signal Tr=25μsecTYP	—	-3	—	dB

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TEST CIRCUIT



Units resistance; Ω
capacitance; F

APPLICATION EXAMPLE

