life.augmented

M24C08-A125

Datasheet

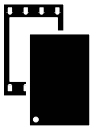
Automotive 8-Kbit serial I²C bus EEPROM with 1 MHz clock

TSSOP8 (DW)

169 mil width

SO8N (MN)

150 mil width



WFDFPN8 (MF)

DFN8 - 2 x 3 mm

Product status
M24C08-A125

Product label
LONGEVITY 10 YEARS COMMITMENT

Features

- AEC-Q100 qualified

I²C interface

- Compatible with the following I²C bus modes:
  - 1 MHz (Fast-mode Plus)
  - 400 kHz (Fast-mode)
  - 100 kHz (Standard-mode)

Memory

- 8 Kbits (1024-byte) of EEPROM
- Page size: 16-byte
- Additional 16-byte identification page

Supply voltage

- 1.7 V to 5.5 V

Temperature

- Operating temperature range: -40 °C to +125 °C

Short write cycle time

- Byte and page write within 4 ms

Advanced features

- Schmitt trigger inputs for noise filtering

Performance

- Write cycle endurance:
  - 4 million at 25 °C
  - 1.2 million at 85 °C
  - 600k at 125 °C
- Data retention:
  - 50 years at 125 °C
  - 100 years at 25 °C
- ESD protection (human body model):
  - 4000 V

Package

- SO8N, TSSOP8, and WFDFPN8 (ECOPACK2)

1 Description

The M24C08-A125 is an 8-Kbit I²C-compatible EEPROM (electrically erasable programmable memory) automotive grade device operating up to 125 °C. It is compliant with the very high level of reliability defined by the automotive standard AEC-Q100 grade 1.

The device can operate with a supply voltage from 1.7 V to 5.5 V, with a clock frequency up to 1 MHz. It is a byte-alterable memory (1024 × 8 bits) organized as 64 pages of 16 bytes, in which data integrity is significantly improved with an embedded error correction code logic.

The device offers an additional page, named identification page (16 bytes) in which the ST device identification can be read. It can be used to store sensitive application parameters, which can be later permanently locked in read-only mode.

Figure 1. Logic diagram

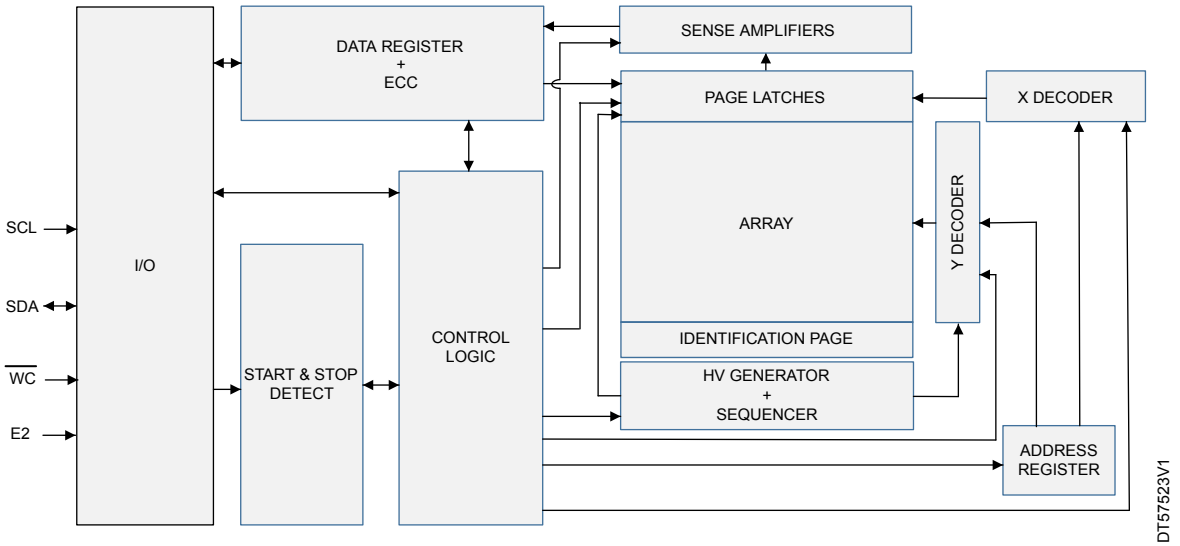
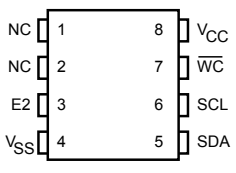


Table 1. Signal names

Signal name	Function	Direction
E2	Chip enable	Input
SDA	Serial data	I/O
SCL	Serial clock	Input
$\overline{WC}$	Write control	Input
V_{CC}	Supply voltage	-
V_{SS}	Ground	-

Figure 2. 8-pin package connections



1. See Section 9: Package mechanical data for package dimensions, and how to identify pin 1.

2 Signal description

2.1 Serial clock (SCL)

SCL is an input. The signal applied on it is used to strobe the data available on SDA(in) and to output the data on SDA(out).

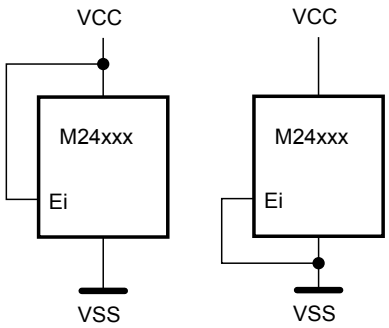
2.2 Serial data (SDA)

SDA is an input/output used to transfer data in or out of the device. SDA(out) is an open drain output that can be wired-AND with other open drain or open collector signals on the bus. A pull-up resistor must be connected from SDA to V_{CC} (Figure 10 and Figure 11 indicate how to calculate the value of the pull-up resistor).

2.3 Chip enable (E2)

This input signal is used to set the value that can be looked for on bit b3 of the device select code (see Table 2). This input must be tied to V_{CC} or V_{SS} to establish the device select code, as shown in Figure 3. When not connected (left floating), it is read as low (0).

Figure 3. Device select code



2.4 Write control ($\overline{WC}$)

This input signal is useful for protecting the content of the memory from inadvertent write operations. All write operations are disabled when the $\overline{WC}$ is driven high. All write operations are enabled when it is either driven low or left floating.

When write control is driven high, device select and address bytes are acknowledged, but data bytes are not acknowledged.

2.5 V_{SS} (ground)

V_{SS} is the reference for the V_{CC} supply voltage.

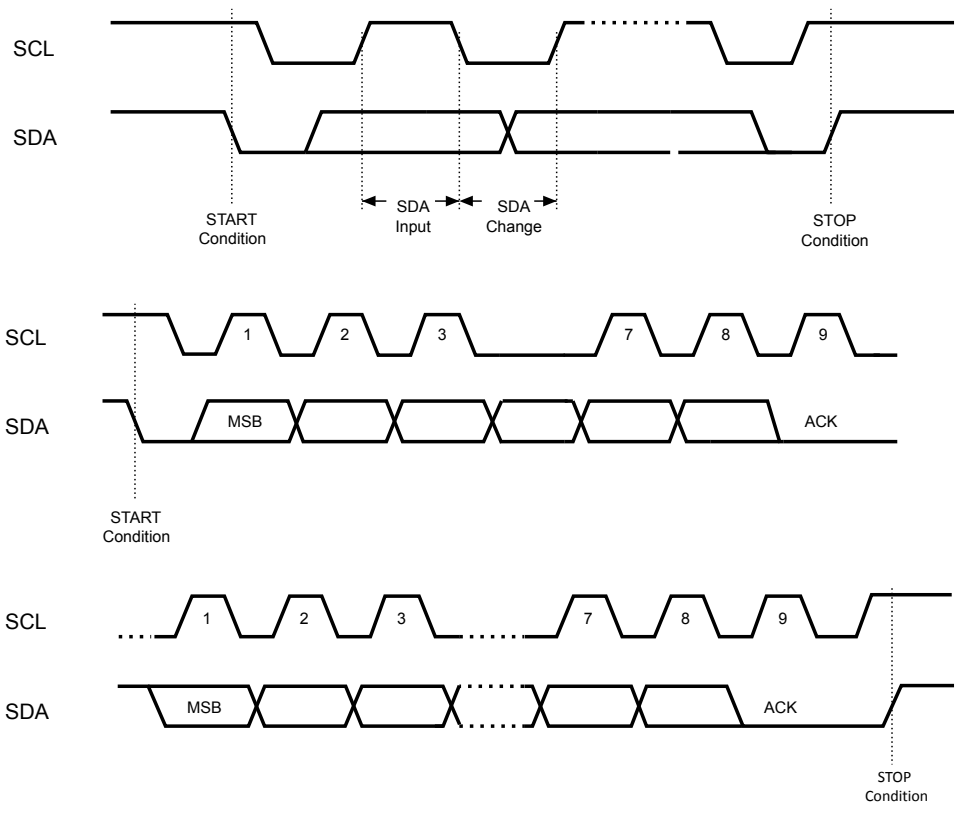
2.6 Supply voltage (V_{CC})

V_{CC} is the supply voltage pin.

3 Device operation

The device supports the I²C protocol summarized in Figure 4. Any device that sends data onto the bus is defined as a transmitter, and any device that reads the data is defined as a receiver. The device that controls the data transfer is known as the bus controller, and the other as the target device. A data transfer can only be initiated by the bus controller, which also provides the serial clock for synchronization. The device is always a target in all communications.

Figure 4. I²C bus protocol



3.1 Start condition

The start condition is identified by a falling edge of serial data (SDA) while the serial clock (SCL) is stable in the high state. This condition must precede any data transfer instruction. The device continuously monitors the SDA and SCL for a start signal, except during a write cycle.

3.2 Stop condition

The stop condition is identified by a rising edge of serial data (SDA) while the serial clock (SCL) is stable in the high state. This condition terminates the communication between the device and the bus controller. A read instruction followed by NO ACK can be followed by a stop condition to force the device into the standby mode. A stop condition at the end of a write instruction triggers the internal write cycle.

3.3 Data input

During data input, the device samples the serial data (SDA) on the rising edge of the serial clock (SCL). For proper device operation, the SDA must be stable during the rising edge of the SCL, and the SDA signal must change only when the SCL is driven low.

3.4 Acknowledge bit (ACK)

The acknowledge bit is used to indicate a successful byte transfer. The bus transmitter, whether a controller or target device, releases the serial data (SDA) after sending eight bits of data. During the ninth clock pulse period, the receiver pulls SDA low to acknowledge the receipt of the eight data bits.

3.5 Device addressing

To start communication between the bus controller and the target device, the bus controller must initiate a start condition. Following this, the bus controller sends the device select code, as specified in Table 2.

The device select code consists of a 4-bit device type identifier and a chip enable address (E2). It is not acknowledged by the memory device with any value other than 1010 (to select the memory) or 1011 (to select the identification page). Up to two memory devices can be connected on a single I²C bus

When the device select code is received, the memory device only responds if the chip enable address is the same as the value decoded on the E2 input.

If a match occurs, the corresponding device gives an acknowledgment on the serial data (SDA) during the ninth SCL clock period. Once the memory device has acknowledged the device select code, it waits for the controller to send the address byte. The memory device responds to the address byte with an acknowledge bit.

If the device does not match the device select code, it deselects itself from the bus and enters into standby mode.

The eighth bit is the read/write bit ($R\overline{W}$). This bit is set to 1 for read and 0 for write operations.

Table 2. Device select code

Features	Device type identifier (1)				Chip enable address (2)			RW
	b7	b6	b5	b4	b3	b2	b1	b0
When accessing the memory	1	0	1	0	E2	A9	A8	$R\overline{W}$
When accessing the identification page	1	0	1	1	E2	X	X	$R\overline{W}$

1. *The most significant bit, b7, is sent first.*
2. *X bit is a don't care bit.*

Table 3. Significant address bits

Addresses		Memory (Device type identifier = 1010)		Identification page (Device type identifier = 1011)			
		Random address read	Write	Read identification page	Write identification page	Lock identification page	Read lock status
Most significant address bits	b2(1)	A9(2)	A9	X	X	X	see Section 4.2.5
	b1(1)	A8	A8	X	X	X	
Address byte	b7	A7	A7	0	0	1	
	b6	A6	A6	X	X	X	
	b5	A5	A5	X(3)	X	X	
	b4	A4	A4	X	X	X	
	b3	A3	A3	A3	A3	X	
	b2	A2	A2	A2	A2	X	
	b1	A1	A1	A1	A1	X	
	b0	A0	A0	A0	A0	X	

1. *Address bits defined inside the device select code (see Table 2)*
2. *A = Significant address bit.*
3. *X = Don't care bit.*

3.6 Identification page

The M24C08-A125 offers an identification page (16 bytes) in addition to the 8-Kbit memory.

The identification page contains two fields:

- Device identification code: the first three bytes are programmed by STMicroelectronics with the device identification code, as shown in Table 4.
- Application parameters: the bytes after the device identification code are available for application-specific data.

Note: If the end application does not need to read the device identification code, this field can be overwritten and used to store application-specific data. Once the application-specific data are written in the identification page, the whole identification page should be permanently locked in read-only mode.

The instructions to read, write, and lock the identification page are detailed in Section 4: Instructions.

Table 4. Device identification code

Address	Content	Value
00h	ST manufacturer code	20h
01h	I²C family code	E0h
02h	Memory density code	0Ah (8-Kbit)

4 Instructions

4.1 Write operations

Following a start condition the bus controller sends a device select code with the R/$\overline{W}$ bit reset to 0. The device acknowledges this, as shown in Figure 5, and waits for the controller to send the address byte with an acknowledge bit, and then waits for the data byte.

When the bus controller generates a stop condition immediately after a data byte ACK bit (in the tenth bit time slot), either at the end of a byte write or a page write, the internal write cycle t_W is then triggered. A stop condition at any other time slot does not trigger the internal write cycle.

During the internal write cycle, serial data (SDA) is disabled internally, and the device does not respond to any requests.

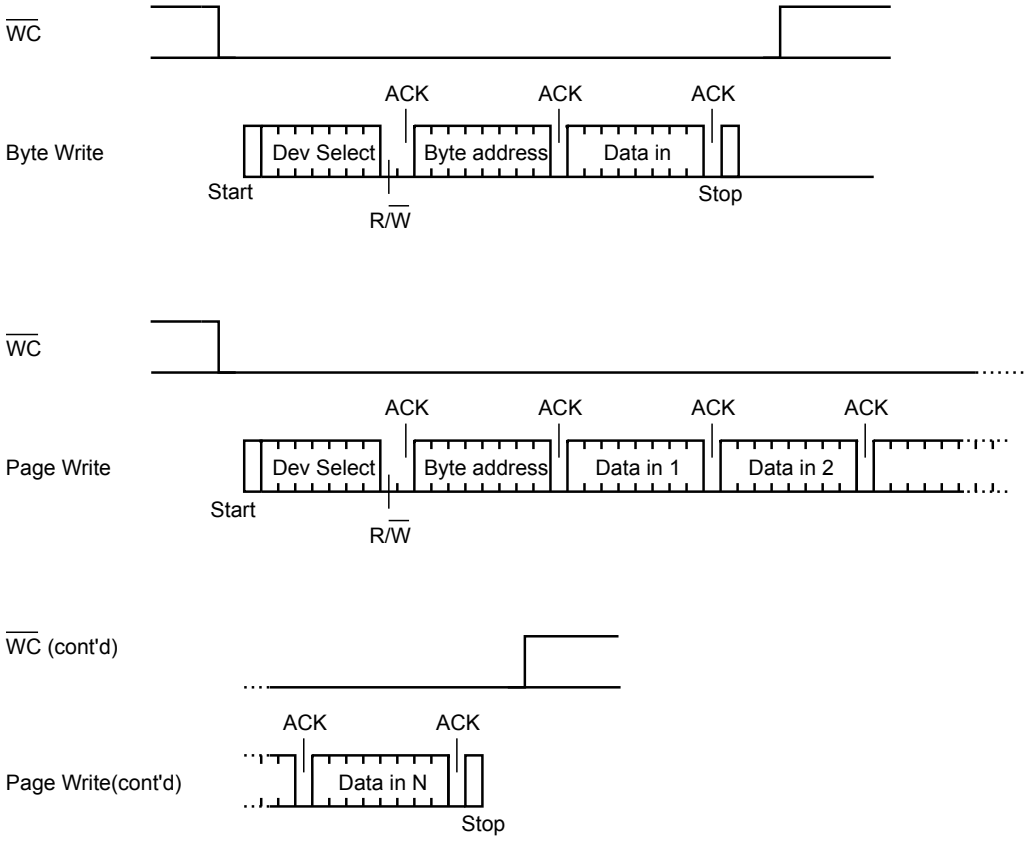
After the successful completion of an internal write cycle (t_W), the device internal address counter is automatically incremented to point to the next byte after the last modified byte.

If the write control input ($\overline{WC}$) is driven high, the write instruction is not executed and the accompanying data bytes are *not* acknowledged, as shown in Figure 6.

4.1.1 Byte write

After the device select code and the address byte, the bus controller sends one data byte. If the addressed location is write-protected, through the $\overline{WC}$ pin being driven high, the device replies with NO ACK, and the location is not modified (see Figure 6). If, instead, the addressed location is not write-protected, the device replies with ACK. The bus controller terminates the transfer by generating a stop condition, as shown in Figure 5.

Figure 5. Write mode sequences with $\overline{WC}$ = 0 (data write enabled)

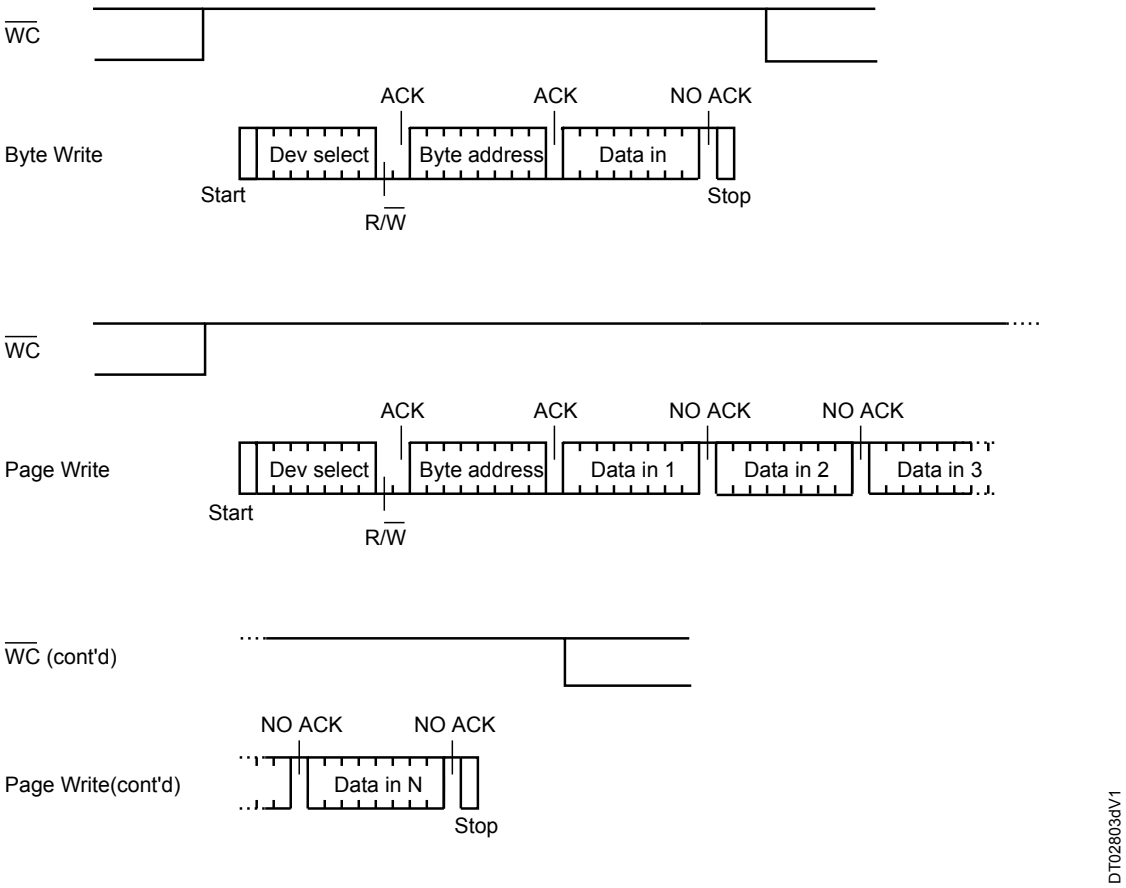


4.1.2 Page write

The page write mode allows up to 16 bytes to be written in a single write cycle, provided they are all located on the same page in the memory. This means that the most significant memory address bits, from A9 to A4, are the same. If more bytes are sent than fit up to the end of the page, a condition known as roll-over occurs. In case of roll-over, the first bytes of the page are overwritten.

Note: The bus controller sends from 1 to 16 bytes of data, each of which is acknowledged by the device if write control ($\overline{WC}$) is low. If $\overline{WC}$ is high, the contents of the addressed memory location are not modified, and each data byte received by the device is not acknowledged, as shown in Figure 6. After each byte is transferred, the internal byte address counter is incremented. The transfer is terminated by the bus controller generating a stop condition.

Figure 6. Write mode sequences with $\overline{WC}$ = 1 (data write inhibited)



4.1.3 Write identification page

The identification page (16 bytes) is an additional page that can be written and later permanently locked in read-only mode. It is written by issuing the write identification page instruction. This instruction uses the same protocol and format as a page write into a memory array, except for the following differences:

- Device type identifier = 1011
- The most significant address bits from A9 to A4 are don't care, except for address bit A7, which must be 0.
- The least significant address bits from A3 to A0 define the byte location inside the identification page.

If the identification page is locked, the data bytes transferred during the write identification page instruction are not acknowledged (NO ACK).

4.1.4 Lock identification page

The lock identification page instruction (lock ID) permanently locks the identification page in read-only mode. The lock ID instruction is similar to byte write (into memory array) with the following specific conditions:

- Device type identifier = 1011b
- Address bit A7 must be ‘1’; all other address bits are don't care
- The data byte must be equal to the binary value xxxx xx1x, where x is don't care

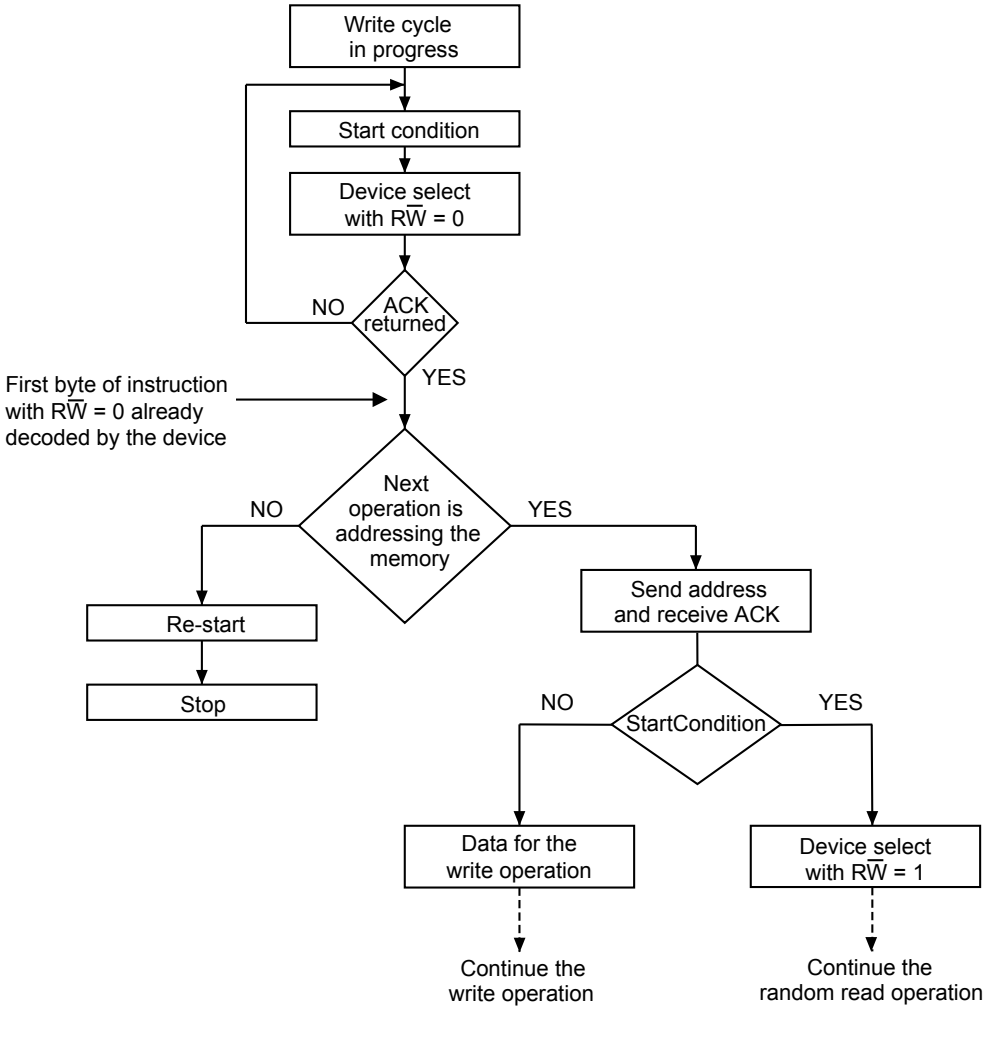
4.1.5 Minimizing write delays by polling on ACK

The maximum write time (t_w) is shown in the AC characteristics tables in Section 8: DC and AC parameters, but the typical time is shorter. The bus controller can implement a polling sequence to utilize this feature.

The sequence, as shown in Figure 7, is:

- Initial condition: A write cycle is in progress.
- Step 1: The bus controller issues a start condition followed by a device select code (the first byte of the new instruction).
- Step 2: If the device is busy with the internal write cycle, no ACK is returned and the bus controller goes back to step 1. If the device has terminated the internal write cycle, it responds with an ACK, indicating that the device is ready to receive the second part of the instruction (the first byte of this instruction having been sent during step 1).

Figure 7. Write cycle polling flowchart using ACK



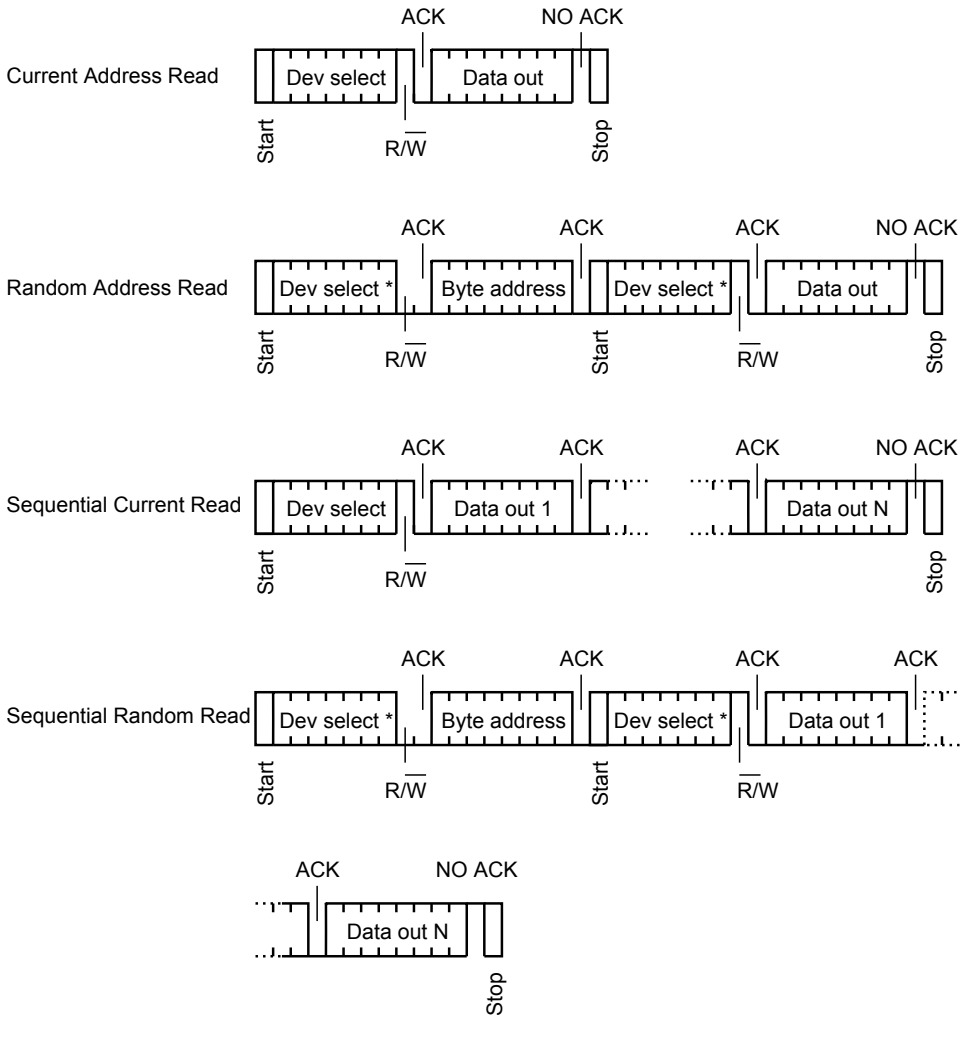
The seven most significant bits of the first device select code in a random read (bottom-right box in the figure) must match those of the device select code in the write operation (polling instruction in the figure).

4.2 Read operations

Read operations are performed independently of the state of the write control ($\overline{WC}$) signal.

After the successful completion of a read operation, the device's internal address counter is incremented by one, to point to the next byte address.

Figure 8. Read mode sequences



4.2.1 Random address read

The random address read is a sequence composed of a truncated write sequence, which defines a new address pointer value (see Table 3), followed by a current read.

The random address read sequence is the sum of [start + device select code with R/$\overline{W}$ = 0 + address byte] (without stop condition, as shown in Figure 8) and [start condition + device select code with R/$\overline{W}$ = 1].

The memory device acknowledges the sequence and then outputs the contents of the addressed byte.

To terminate the data transfer, the bus controller does not acknowledge the last data byte and then issues a stop condition.

4.2.2 Current address read

For the current address read operation, following a start condition, the bus controller only sends a device select code with the R/W bit set to 1. The device acknowledges this, and outputs the byte pointed by the internal address counter. The counter is then incremented. The bus controller terminates the transfer with a stop condition, as shown in Figure 8, without acknowledging the byte.

Note: The address counter value is defined by instructions accessing either the memory or the identification page. When accessing the identification page, the address counter value is loaded with the identification page byte location, when accessing the memory, it is safer to use the random address read instruction (this instruction loads the address counter with the byte location to read in the memory) instead of the current address read instruction.

4.2.3 Sequential read

This operation can be used after a current address read or a random address read.

After a read instruction, the device can continue to output one or more bytes in sequence if the bus controller sends additional clock pulses and acknowledges each transmitted data byte. To terminate the stream of bytes, the bus controller must not acknowledge the last byte, and must generate a stop condition, as shown in Figure 8.

The sequential read is controlled with the device internal address counter, which is automatically incremented after each byte output. After the last memory address, the address counter rolls-over, and the device continues to output data from memory address 00h.

4.2.4 Read identification page

The identification page can be read by issuing a read identification page instruction. This instruction uses the same protocol and format as the random address read from a memory array, with the device type identifier defined as 1011. The most significant address bits from A9 to A4 are don't care except bit A7, which must be 0. The least significant address bits from A3 to A0 define the byte location inside the identification page. The number of bytes read in the ID page must not exceed the page boundary.

4.2.5 Read the lock status

The lock/unlock status of the identification page can be checked by transmitting a specific truncated command that is: [identification page write instruction + one data byte] to the device. The device returns an acknowledgment bit after the data byte if the identification page is unlocked (unlock status), otherwise it returns a NO ACK bit if the identification page is locked.

Right after this, it is recommended to transmit to the device a start condition followed by a stop condition, so that:

- Start: the truncated command is not executed because the start condition resets the device internal logic
- Stop: the device is then set back into standby mode by the stop condition

4.2.6 Acknowledge in read mode

For all read instructions, the device waits for an acknowledgment from the bus controller after each byte is sent out during the ninth bit time slot. If the bus controller does not send the acknowledgment (drives SDA high during the ninth bit time), the device terminates the data transfer and enters standby mode after a stop condition.

5 Application design recommendations

5.1 Supply voltage

5.1.1 Operating supply voltage (V_{CC})

Before to selecting the memory and issuing instructions to it, a valid and stable V_{CC} voltage within the specified [V_{CC}(min), V_{CC}(max)] range must be applied (see Table 6).

This voltage must remain stable and valid until the end of the transmission of the instruction and, for a write instruction, until the completion of the internal write cycle (t_W). To secure a stable DC supply voltage, it is recommended to decouple the V_{CC} line with a suitable capacitor (usually from 10 nF to 100 nF) close to the VCC/VSS package pins.

5.1.2 Power-up conditions

When the power supply is turned on, the V_{CC} voltage must rise continuously from 0 V up to the minimum V_{CC} operating voltage defined in Table 6.

To prevent inadvertent write operations during power-up, a power-on-reset (POR) circuit is included.

At power-up, the device does not respond to any instruction until V_{CC} reaches the internal threshold voltage (this threshold is defined in the DC characteristic Table 10 as V_{RES}).

When V_{CC} passes over the POR threshold, the device is reset and in the following state:

- In the standby power mode
- Deselected

Once the V_{CC} voltage reaches a stable value within the [V_{CC}(min), V_{CC}(max)] range (defined in Table 6), the device is ready for operation.

5.1.3 Power-down condition

During power-down, when the V_{CC} decreases below the minimum V_{CC} operating voltage defined in Table 6), the device must be in standby power mode (the mode is reached after decoding a stop condition or after the completion of the write cycle t_W if an internal write cycle is in progress).

5.2 Error correction code (ECC x 1)

The error correction code (ECC x 1) is an internal logic function that is transparent for the I²C communication protocol.

It is implemented on each byte of the memory array. If a single bit out of the byte is erroneous during a read operation, the ECC x 1 detects this bit and replaces it with the proper value. Therefore, read reliability is much improved.

6 Delivery state

The device is delivered as follows:

- The memory array is set to all 1s (each byte contains FFh).
- Identification page: the first three bytes define the device identification code (value defined in Table 4). The content of the following bytes is FFh.

7 Maximum ratings

Stressing the device outside the ratings listed in Table 5 may permanently damage it. These are stress ratings only, and operation of the device at these, or any other conditions outside those indicated in the operating sections of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 5. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
-	Ambient operating temperature	-40	130	°C
T_{STG}	Storage temperature	-65	150	°C
T_{LEAD}	Lead temperature during soldering	See note (1)		°C
V_{IO}	Input or output range	-0.50	6.5	V
I_{OL}	DC output current (SDA = 0)	-	5	mA
V_{CC}	Supply voltage	-0.50	6.5	V
V_{ESD}	Electrostatic pulse (human body model) (2)	-	4000	V

1. *Compliant with JEDEC Std J-STD-020 (for small body, Sn-Pb or Pb-free assembly), the ST ECOPACK 7191395 specification, and the European directive on restrictions on hazardous substances (RoHS directive 2011/65/EU of July 2011).*
2. *Positive and negative pulses applied on pin pairs, according to AEC-Q100-002 (compliant with ANSI/ESDA/JEDEC JS-001, C1 = 100 pF, R1 = 1500 Ω, R2 = 500 Ω).*

8 DC and AC parameters

This section summarizes the operating and measurement conditions, and the DC and AC characteristics.

Table 6. Operating conditions

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage	1.7	5.5	V
T_A	Ambient operating temperature	-40	125	°C

Table 7. AC measurement conditions

Symbol	Parameter	Min.	Max.	Unit
C_{bus}	Load capacitance	-	100	pF
-	SCL input rise/fall time, SDA input fall time	-	50	ns
-	Input levels	0.2 V_{CC} to 0.8 V_{CC}		V
-	Input and output timing reference levels	0.3 V_{CC} to 0.7 V_{CC}		V

Figure 9. AC measurement I/O waveform

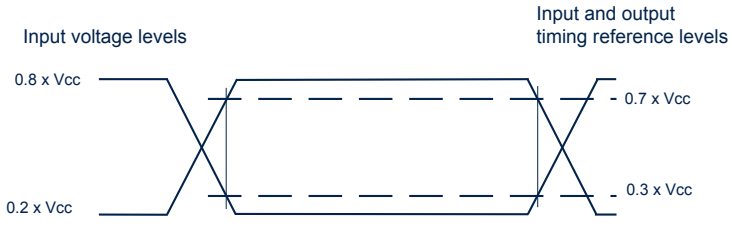


Table 8. Input parameters

Symbol	Parameter	Test condition	Min.	Max.	Unit
C_{IN} (1)	Input capacitance (SDA)	-	-	8	pF
C_{IN} (1)	Input capacitance (other pins)	-	-	6	pF
Z_L (2)	Input impedance ($\overline{WC}$)	$V_{IN} < 0.3\ V_{CC}$	30	-	kΩ
Z_H (2)		$V_{IN} > 0.7\ V_{CC}$	500	-	kΩ

1. *Specified by design - Not tested in production.*
2. *Evaluated by characterization - Not tested in production.*

Table 9. Cycling performance

Symbol	Parameter	Test condition	Min.	Max.	Unit
Ncycle	Write cycle endurance	$T_A \leq 25$ °C, 1.7 V < V_{CC} < 5.5 V	-	4,000,000	Write cycle (1)
		T_A = 85 °C, 1.7 V < V_{CC} < 5.5 V	-	1,200,000	
		T_A = 125 °C, 1.7 V < V_{CC} < 5.5 V	-	600,000	

1. *A write cycle is executed when either a page write, a byte write, a write identification page, or a lock identification page instruction is decoded.*

Table 10. DC characteristics

Symbol	Parameter	Test conditions (in addition to those in Table 6 and Table 7)	Min.	Max.	Unit
I_{LI}	Input leakage current (SCL, SDA, Ei)	V_{IN} = V_{SS} or V_{CC}, device in standby mode	-	± 2	µA
I_{LO}	Output leakage current	SDA in Hi-Z, external voltage applied on SDA: V_{SS} or V_{CC}	-	± 2	µA
I_{CC}	Supply current (Read)	f_C = 400 kHz, V_{CC} = 5.5 V	-	2	mA
		f_C = 400 kHz, V_{CC} = 2.5 V	-	2	mA
		f_C = 400 kHz, V_{CC} = 1.7 V	-	1	mA
		f_C = 1 MHz, V_{CC} = 5.5 V	-	2	mA
		f_C = 1 MHz, V_{CC} = 2.5 V	-	2	mA
		f_C = 1 MHz, V_{CC} = 1.7 V	-	2	mA
I_{CC0}	Supply current (Write)	During t_W	-	2	mA
I_{CC1}	Standby supply current	Device not selected(1), T_A = 85 °C, V_{IN} = V_{SS} or V_{CC}, V_{CC} = 1.7 V	-	1	µA
		Device not selected(1), T_A = 85 °C V_{IN} = V_{SS} or V_{CC}, V_{CC} = 2.5 V	-	2	µA
		Device not selected(1), T_A = 85 °C, V_{IN} = V_{SS} or V_{CC}, V_{CC} = 5.5 V	-	3	µA
		Device not selected(1), T_A = 125 °C, V_{IN} = V_{SS} or V_{CC}, V_{CC} = 1.7 V	-	15	µA
		Device not selected(1), T_A = 125 °C, V_{IN} = V_{SS} or V_{CC}, V_{CC} = 2.5 V	-	15	µA
		Device not selected(1), T_A = 125 °C, V_{IN} = V_{SS} or V_{CC}, V_{CC} = 5.5 V	-	20	µA
V_{IL}	Input low voltage (SCL, SDA, $\overline{WC}$, Ei) (2)	-	–0.45	0.3 V_{CC}	V
V_{IH}	Input high voltage (SCL, SDA)	-	0.7 V_{CC}	6.5	V
	Input high voltage ($\overline{WC}$, Ei) (3)	-	0.7 V_{CC}	V_{CC} +0.6	V
V_{OL}	Output low voltage	I_{OL} = 2.1 mA, V_{CC} = 2.5 V or I_{OL} = 3 mA, V_{CC} = 5.5 V	-	0.4	V
		I_{OL} = 1 mA, V_{CC} = 1.7 V	-	0.3	V
V_{RES} (4)	Internal reset threshold voltage	-	0.5	1.5	V

1. *The device is not selected after power-up, after a read instruction (after the stop condition), or after the completion of the internal write cycle t_W (t_W is triggered by the correct decoding of a write instruction).*
2. *Ei inputs should be tied to V_{ss} (see Section 2.3).*
3. *Ei inputs should be tied to V_{CC} (see Section 2.3).*
4. *Evaluated by characterization - Not tested in production.*

Table 11. AC characteristics in Fast-mode

Symbol	Alt.	Parameter	Min.	Max.	Unit
f_C	f_{SCL}	Clock frequency	-	400	kHz
t_{CHCL}	t_{HIGH}	Clock pulse width high	600	-	ns
t_{CLCH}	t_{LOW}	Clock pulse width low	1300	-	ns
t_{QL1QL2} (1)	t_F	SDA (out) fall time (2)	20	120	ns
t_{XH1XH2}	t_R	Input signal rise time	(3)	(3)	ns
t_{XL1XL2}	t_F	Input signal fall time	(3)	(3)	ns
t_{DXCH}	$t_{SU:DAT}$	Data in setup time	100	-	ns
t_{CLDX}	$t_{HD:DAT}$	Data in hold time	0	-	ns
t_{CLQX} (4)	t_{DH}	Data out hold time	100	-	ns
t_{CLQV} (5)	t_{AA}	Clock low to next data valid (access time)	-	900	ns
t_{CHDL}	$t_{SU:STA}$	Start condition setup time	600	-	ns
t_{DLCL}	$t_{HD:STA}$	Start condition hold time	600	-	ns
t_{CHDH}	$t_{SU:STO}$	Stop condition setup time	600	-	ns
t_{DHDL}	t_{BUF}	Time between stop condition and next start condition	1300	-	ns
t_{WLDL} (1)(6)	$t_{SU:WC}$	$\overline{WC}$ setup time (before the start condition)	0	-	µs
t_{DHWH} (1)(7)	$t_{HD:WC}$	$\overline{WC}$ hold time (after the stop condition)	1	-	µs
t_W	t_{WR}	Write time	-	4	ms
t_{NS} (1)	-	Pulse width ignored (input filter on SCL and SDA) - single glitch	-	80	ns

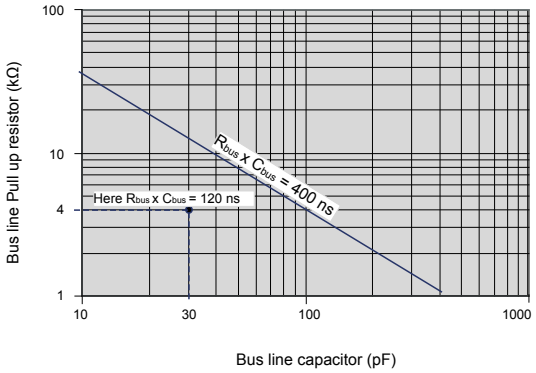
1. *Evaluated by characterization - Not tested in production.*
2. *With C_L = 10 pF.*
3. *There is no minimum or maximum values for the input signal rise and fall times. It is, however, recommended by the I²C specification that the input signal rise and fall times be more than 20 ns and less than 300 ns, respectively, when f_C < 400 kHz.*
4. *To avoid spurious start and stop conditions, a minimum delay is implemented between SCL = 1 and any falling or rising edge of SDA.*
5. *t_{CLQV} is the time (from the falling edge of SCL) required by the SDA bus line to reach either 0.3 V_{CC} or 0.7 V_{CC}, assuming that R_{bus} × C_{bus} time constant is within the values specified in Figure 10.*
6. *$\overline{WC}$ = 0 setup time condition to enable the execution of a write command.*
7. *$\overline{WC}$ = 0 hold time condition to enable the execution of a write command.*

Table 12. AC characteristics in Fast-mode Plus

Symbol	Alt.	Parameter	Min.	Max.	Unit
f_C	f_{SCL}	Clock frequency	0	1	MHz
t_{CHCL}	t_{HIGH}	Clock pulse width high	260	-	ns
t_{CLCH}	t_{LOW}	Clock pulse width low	500	-	ns
t_{XH1XH2}	t_R	Input signal rise time	(1)	(1)	ns
t_{XL1XL2}	t_F	Input signal fall time	(1)	(1)	ns
t_{QL1QL2} (2)	t_F	SDA (out) fall time	20	120	ns
t_{DXCH}	$t_{SU:DAT}$	Data in setup time	50	-	ns
t_{CLDX}	$t_{HD:DAT}$	Data in hold time	0	-	ns
t_{CLQX} (3)	t_{DH}	Data out hold time	100	-	ns
t_{CLQV} (4)	t_{AA}	Clock low to next data valid (access time)	-	450	ns
t_{CHDL}	$t_{SU:STA}$	Start condition setup time	250	-	ns
t_{DLCL}	$t_{HD:STA}$	Start condition hold time	250	-	ns
t_{CHDH}	$t_{SU:STO}$	Stop condition setup time	250	-	ns
t_{DHDL}	t_{BUF}	Time between Stop condition and next Start condition	500	-	ns
t_{WLDL} (2)(5)	$t_{SU:WC}$	$\overline{WC}$ setup time (before the Start condition)	0	-	µs
t_{DHWH} (2)(6)	$t_{HD:WC}$	$\overline{WC}$ hold time (after the Stop condition)	1	-	µs
t_W	t_{WR}	Write time	-	4	ms
t_{NS} (2)	-	Pulse width ignored (input filter on SCL and SDA)	-	80	ns

1. *There is no minimum or maximum values for the input signal rise and fall times. It is, however, recommended by the I²C specification that the input signal rise and fall times be more than 20 ns and less than 120 ns, respectively ,when f_C < 1 MHz.*
2. *Evaluated by characterization - Not tested in production.*
3. *To avoid spurious Start and Stop conditions, a minimum delay is placed between SCL = 1 and any falling or rising edge of SDA.*
4. *t_{CLQV} is the time (from the falling edge of SCL) required by the SDA bus line to reach either 0.3 V_{CC} or 0.7 V_{CC}, assuming that the Rbus × Cbus time constant is within the values specified in Figure 11.*
5. *$\overline{WC}$ = 0 setup time condition to enable the execution of a write command.*
6. *$\overline{WC}$ = 0 hold time condition to enable the execution of a write command.*

Figure 10. R_{bus} value versus bus parasitic capacitance (C_{bus}) for an I^2C_{bus} (f_C = 400 kHz)



The R_{bus} x C_{bus} time constant must be below the 400 ns time constant line displayed on the left

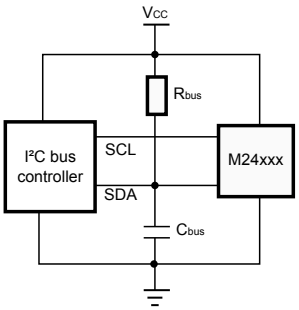


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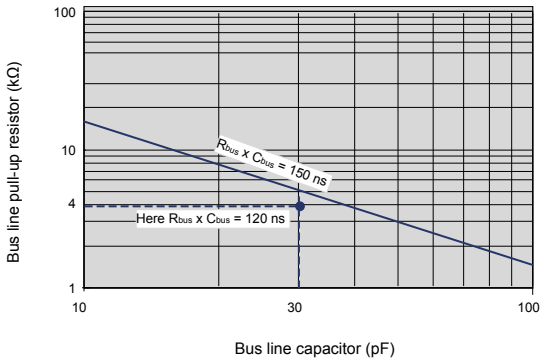
Figure 11. R_{bus} value versus bus parasitic capacitance (C_{bus}) for an I^2C bus (f_C = 1 MHz)



The R_{bus} x C_{bus} time constant must be below the 150 ns time constant line displayed on the left

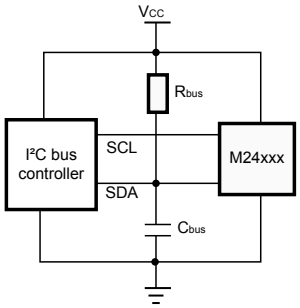


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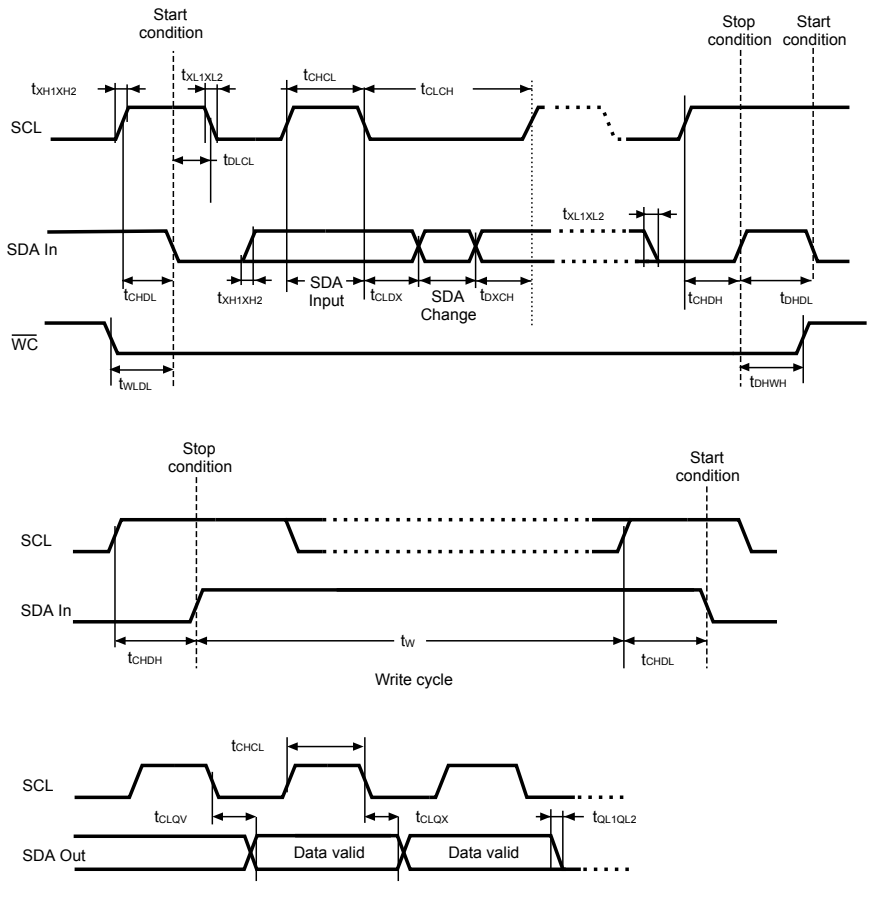
Figure 12. **AC waveforms**



DT00795IV1

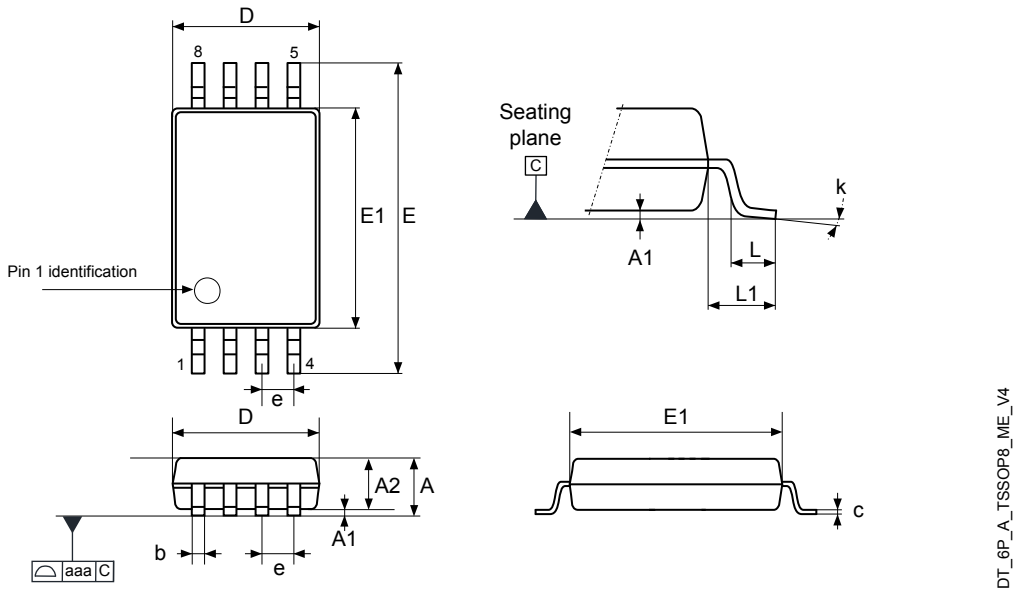
9 Package mechanical data

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

9.1 TSSOP8 package information

This TSSOP is an 8-lead, 3 x 6.4 mm, 0.65 mm pitch, thin shrink small outline package.

Figure 13. TSSOP8 – Outline



1. *Drawing is not to scale.*

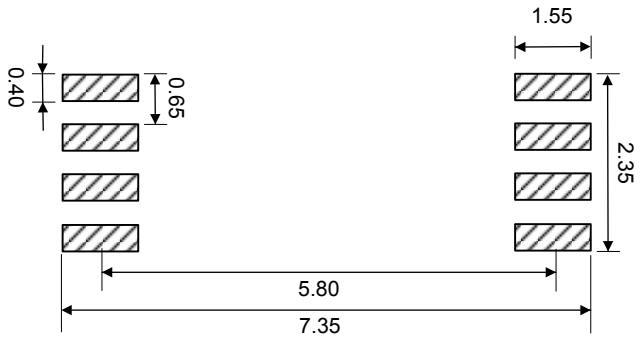
Table 13. **TSSOP8 - Mechanical data**

Symbol	millimeters			inches [1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	1.200	-	-	0.0472
A1	0.050	-	0.150	0.0020	-	0.0059
A2	0.800	1.000	1.050	0.0315	0.0394	0.0413
b	0.190	-	0.300	0.0075	-	0.0118
c	0.090	-	0.200	0.0035	-	0.0079
D[2]	2.900	3.000	3.100	0.1142	0.1181	0.1220
e	-	0.650	-	-	0.0256	-
E	6.200	6.400	6.600	0.2441	0.2520	0.2598
E1[3]	4.300	4.400	4.500	0.1693	0.1732	0.1772
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	-	8°	0°	-	8°
aaa	-	-	0.100	-	-	0.0039

1. *Values in inches are converted from mm and rounded to four decimal digits.*
2. *Dimension D does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.*
3. *Dimension E1 does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25 mm per side.*

Note: The package top may be smaller than the package bottom. Dimensions D and E1 are determinated at the outermost extremes of the plastic body exclusive of the mold flash, tie bar burrs, gate burrs, and interleads flash, but including any mismatch between the top and bottom of the plastic body. The measurement side for the mold flash, protrusions, or gate burrs is the bottom side.

Figure 14. **TSSOP8 – Footprint example**

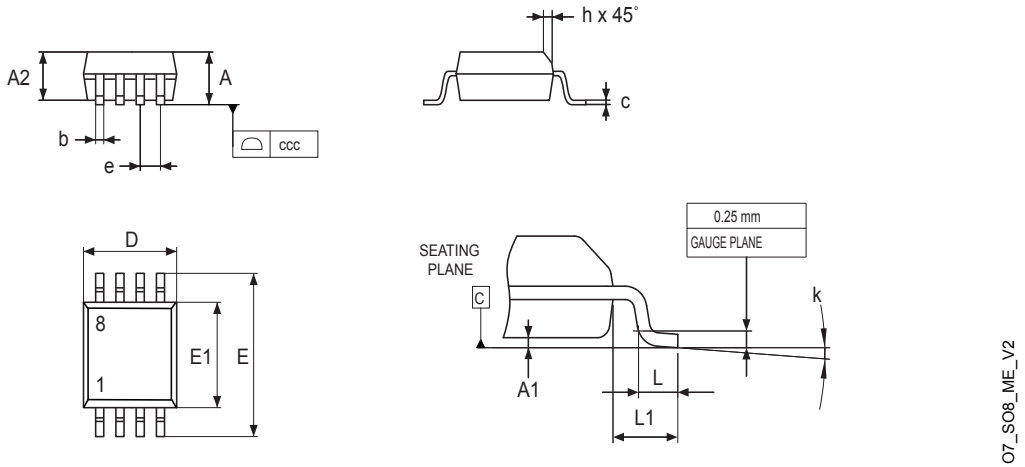


1. *Dimensions are expressed in millimeters.*

9.2 SO8N package information

This SO8N is an 8-lead, 4.9 x 6 mm, plastic small outline, 150 mils body width, package.

Figure 15. SO8N - Outline



1. *Drawing is not to scale.*

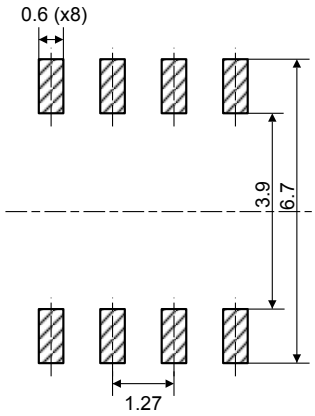
Table 14. SO8N - Mechanical data

Symbol	millimeters			inches [1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	1.750	-	-	0.0689
A1	0.100	-	0.250	0.0039	-	0.0098
A2	1.250	-	-	0.0492	-	-
b	0.280	-	0.480	0.0110	-	0.0189
c	0.170	-	0.230	0.0067	-	0.0091
D[2]	4.800	4.900	5.000	0.1890	0.1929	0.1969
E	5.800	6.000	6.200	0.2283	0.2362	0.2441
E1[3]	3.800	3.900	4.000	0.1496	0.1535	0.1575
e	-	1.270	-	-	0.0500	-
h	0.250	-	0.500	0.0098	-	0.0197
k	0°	-	8°	0°	-	8°
L	0.400	-	1.270	0.0157	-	0.0500
L1	-	1.040	-	-	0.0409	-
ccc	-	-	0.100	-	-	0.0039

1. *Values in inches are converted from mm and rounded to four decimal digits.*
2. *Dimension D does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side*
3. *Dimension E1 does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25 mm per side.*

Note: The package top may be smaller than the package bottom. Dimensions D and E1 are determinated at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and interleads flash, but including any mismatch between the top and bottom of the plastic body. The measurement side for mold flash, protusions, or gate burrs is the bottom side.

Figure 16. **SO8N - Footprint example**

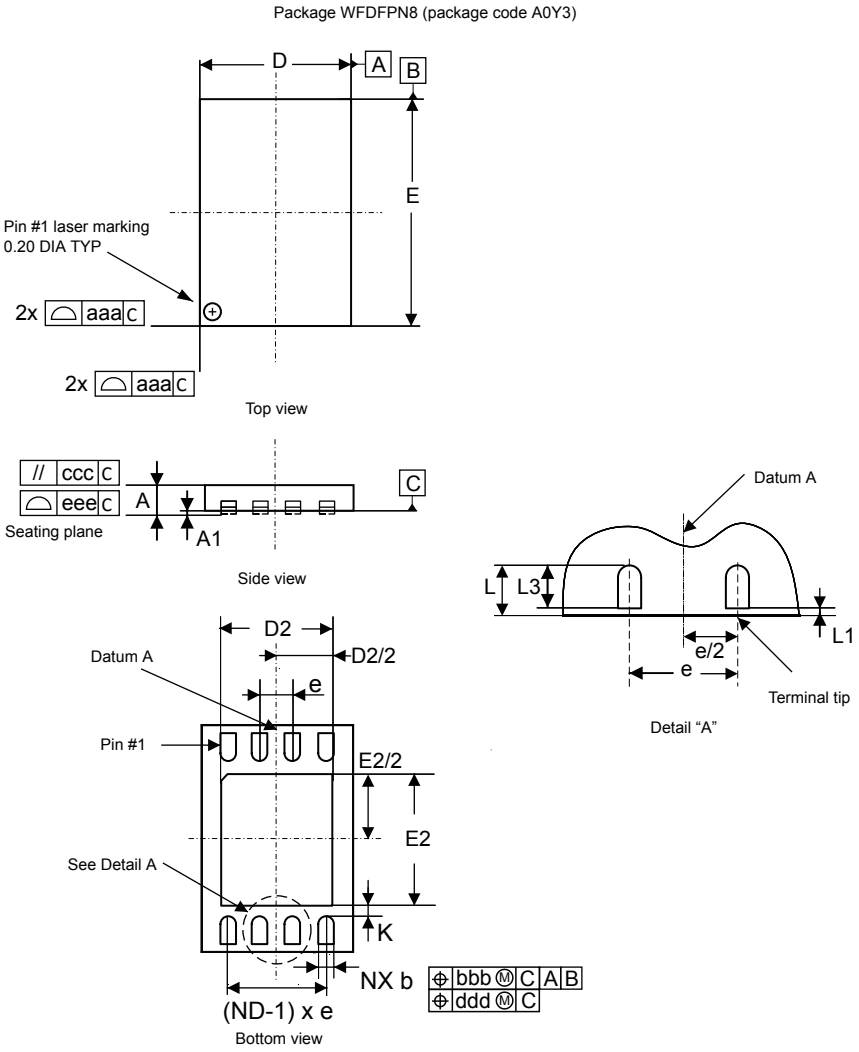


1. *Dimensions are expressed in millimeters.*

9.3 WFDFPN8 (DFN8) package information

This WFDFPN is a 8-lead, 2 x 3 mm, 0.5 mm pitch very very thin fine pitch dual flat package.

Figure 17. WFDFPN8 (DFN8) – Outline



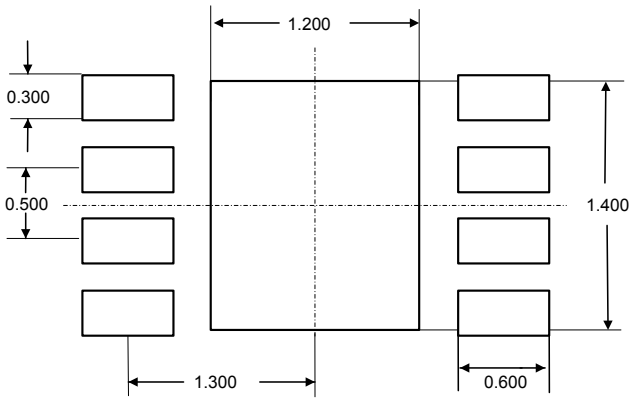
1. *Drawing is not to scale.*
2. *Exposed copper is not systematic and can appear partially or totally according to the cross section.*

Table 15. WFDFPN8 (DFN8) – Mechanical data

Symbol	millimeters			inches [1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.700	0.750	0.800	0.0276	0.0295	0.0315
A1	0.025	0.045	0.065	0.0010	0.0018	0.0026
b[2]	0.200	0.250	0.300	0.0079	0.0098	0.0118
D	1.900	2.000	2.100	0.0748	0.0787	0.0827
E	2.900	3.000	3.100	0.1142	0.1181	0.1220
e	-	0.500	-	-	0.0197	-
L1	-	-	0.150	-	-	0.0059
L3	0.300	-	-	0.0118	-	-
D2	1.400	-	1.600	0.0551	-	0.0630
E2	1.200	-	1.400	0.0472	-	0.0551
K	0.400	-	-	0.0157	-	-
L	0.300	-	0.500	0.0118	-	0.0197
NX [3]	8					
ND [3]	4					
aaa	-	-	0.150	-	-	0.0059
bbb[4]	-	-	0.100	-	-	0.0039
ccc	-	-	0.100	-	-	0.0039
ddd	-	-	0.050	-	-	0.0020
eee [5]	-	-	0.080	-	-	0.0031

1. *Values in inches are converted from mm and rounded to four decimal digits.*
2. *Dimension b applies to plated terminal and is measured between 0.15 and 0.30 mm from the terminal tip.*
3. *N is the number of terminals, ND is the number of terminals on “D” sides.*
4. *Max package warpage is 0.05 mm.*
5. *Applied for exposed die paddle and terminals. Exclude embedding part of exposed die paddle from measuring.*

Figure 18. WFDFPN8 (DFN8) – Footprint example



Note: The central pad (the area E2 by D2 in the Figure 17) must be either connected to V_{SS} or left floating (not connected) in the end application.

10 Ordering information

Table 16. Ordering information scheme

Example: M24 C08-D R MN 3 T P /K

Device type

M24 = I²C serial access EEPROM

Device function

C08-D = 8 Kbits (1024 x 8 bits) plus identification page

Operating voltage

R = V_{CC} = 1.7 V to 5.5 V

Package(1)

MN = SO8 (150 mil width)

DW = TSSOP8 (169 mil width)

MF = WFDFPN8 (DFN8 2 x 3 mm)

Device grade

3 = -40 to 125 °C. Automotive grade.

Option

T = Tape and reel packing

blank = tube packing

Plating technology

P or G = ECOPACK2

Process

/K = Manufacturing technology code

1. *All packages are ECOPACK2 (RoHS compliant and free of brominated, chlorinated and antimonyoxide flame retardants).*

Note: For a list of available options (speed, package, etc.) or for further information on any aspect of the devices, please contact your nearest ST sales office.

Engineering samples

Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Revision history

Table 17. **Document revision history**

Date	Revision	Changes
17-Feb-2014	1	Initial release
05-May-2014	2	Added note 2 on *Figure 8*. Updated *Table 16: Orderinginformation scheme*.
12-Aug-2014	3	Changed product maturity from Target spec to Preliminary data
16-Sep-2014	4	Changed product maturity from Preliminary to Production data. Updated Package information on Cover page. Updated *Table 15: WFDFPN8 (MLP8) – 8-lead thin fine pitch dual flat package no lead 2 x 3 mm, mechanical data* and *Table 16: Ordering information scheme*.
07-Jan-2015	5	Updated: • Note 2 on *Table 5* • *Figure 8* • *Table 12* Added sentence about Engineering sample on *Section 10*.
15-Mar-2016	6	Updated: • *Features* • *Table 9:Cycling performance*, *Table 10: DC characteristics*, *Table 16: Ordering information scheme*
03-Apr-2023	7	Updated: Note 1 and 2 of Table 5. Absolute maximum ratings, Figure 1. Logic diagram, Section 9.1: TSSOP8 package information, Section 9.2: SO8N package information, Section 9.3: WFDFPN8 (DFN8) package information
02-Oct-2024	8	Updated: • Features • Section 1: Description • Table 16. Ordering information scheme

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