RF25B

Tx ASIC for CDMA and AMPS Applications

The RF25B device includes the following functional blocks:

- In-Phase and Quadrature (I/Q) modulator
- A Very High Frequency (VHF) Voltage Controlled Oscillator (VCO)
- Intermediate Frequency (IF) Variable Gain Amplifier (VGA)
- Cellular upconverters with RF gain control
- Cellular Power Amplifier (PA) drivers

The RF25B Tx Application-Specific Integrated Circuit (ASIC) is a dual-mode transmitter (Tx) intended to be used in cellular band phones. As a dual-mode IC, it can be used in Code Division Multiple Access (CDMA) or Advanced Mobile Phone System (AMPS) mode. The ASIC provides excellent RF performance and is packaged in a low cost, high performance, 40-pin Land Grid Array (LGA), 6x6 mm package.

The device incorporates all the components to implement the complete transmitter chain; from the In-Phase and Quadrature (I/Q) modulator to the PA driver amplifier, except for external IF and RF SAW filters. The I/Q modulator receives differential inputs from the baseband and upconverts to IF band. The IF VGA amplifies the IF signal with a minimum dynamic range of 90 dB. It also provides a compensation for gain variation of off-chip components. After external IF filtering, the signal is upconverted to RF band frequency through a mixer. The mixer has an adjusted variable gain option. With this option and the VGA, the transmitted path's gain can be redistributed for optimum Adjacent Channel Power Rejection (ACPR) and Signal-to-Noise (S/N) performance. The RF signal is filtered through an external filter and inputs to the drive amplifier.

There is a single on-chip Very High Frequency (VHF) Voltage Controlled Oscillator (VCO), which operates with an external tank circuit and a varactor diode to generate the Local Oscillator (LO) signal for I/Q modulator.

The Gain, ACPR and Noise Figure (NF) of each stage in the transmitter chip are optimized to meet the system requirements per TIA/EIA-98B.Employing silicon bipolar technology, the chip is designed for high performance with a high level integration and a cost-effective RF solution for dual-mode phone application.

The RF25B pin-out is shown in Figure 1, a functional block diagram in Figure 2, and a schematic diagram in Figure 3.

Features

- Dual-mode operation with high linearity that meets the requirements of the IS-95A and IS-98 standards
- 90 dB dynamic range from the VGA
- Power saving operation in gated output power mode
- RF mixer variable gain
- Lower power consumption in all modes
- Enable line for the entire chip
- Cellular band driver
- 40-pin Land Grid Array (LGA) package

Applications

- Cellular band phones.
- CDMA and AMPS modes in the cellular band:
  - CDMA (US)
  - CDMA (Japan)

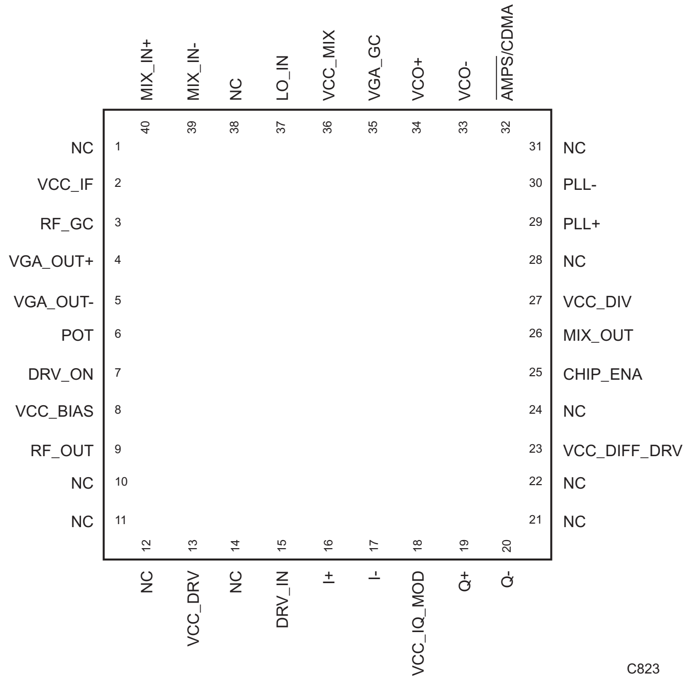


Figure 1. RF25B Tx ASIC Pinout – 40-Pin LGA 6 x 6 mm Package

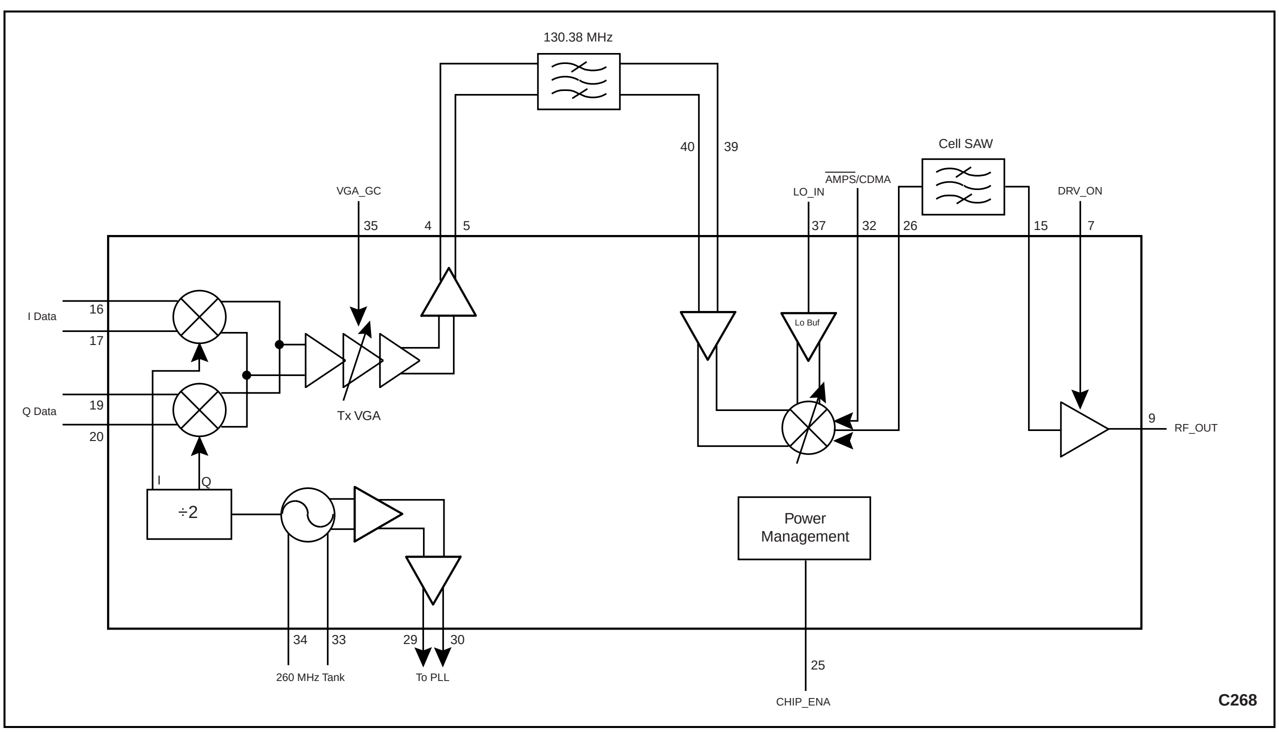


Figure 2. RF25B Tx ASIC Block Diagram

Technical Description

I/Q Modulator. The I/Q modulator converts the incoming analog baseband signals to balanced IF signals using the on-chip VHF local oscillator. The I/Q modulator is internally connected to the VGA, and its outputs are fully differential to reduce common mode noise. The modulator is also designed to have very low amplitude and phase imbalances.

VHF VCOs. The on-chip Local Oscillator (LO) is a voltage controlled oscillator (VCO). It has a frequency range of 100 to 640 MHz. With external tank circuits and a varactor diode, it provides the LO signal to drive the I/Q modulator and the prescalar of an external Phase Locked Loop (PLL) circuitry. The oscillator typically operates at twice the IF frequency.

VGA. The VGA is a differential amplifier that receives its signal from the I/Q modulator, amplifies it, and sends it to the IF output pins. A filter should be attached to the IF output pins for noise reduction. The VGA has a minimum dynamic range of 90 dB and a control voltage of 0.5 to 2.5 V. It provides compensation for any part-to-part and temperature gain variation in the transmitted path.

Upconverters. The cellular variable gain upconverter receives the IF signal from the VGA after passing through an external filter. The upconverter uses an external LO controlled by an external PLL. With the variable mixer gain and the VGA, the transmitted path's gain can be redistributed for optimum ACPR and S/N performance. The output RF signal is sent to an output pin to be filtered before driver amplification.

PA Driver. The driver takes its input from the upconverter after passing through an image rejection filter. The driver amplifies the signal and sends it to an external PA.

The DRIVER_ON command is used during gated output power mode to deactivate the drivers in periods of no transmission—a feature intended for current saving. The pot (pin 6) accompanied with an external resistor would alter the driver bias point. The result is to change the driver gain and ACPR. A Surface Acoustic Wave (SAW) filter for noise and spurious rejection should be placed between the driver and the external PA.

ESD Sensitivity

The RF25B is a Class 1 device. The following extreme Electrostatic Discharge (ESD) precautions are required according to the Human Body Model (HBM):

- Protective outer garments.
- Handle device in ESD safeguarded work area.
- Transport device in ESD shielded containers.
- Monitor and test all ESD protection equipment.

The HBM ESD withstand threshold value, with respect to ground, is ±1.5 kV. The HBM ESD withstand threshold value, with respect to VDD (the positive power supply terminal) is also ±1.5 kV.

Electrical and Mechanical Specifications

Included in this document are Tables 1 through 5 and Figures 1 through 5, which define the electrical and mechanical specifications of the RF25B.

Table 1:	RF25B Pin Assignments and Signal Descriptions
Table 2:	Absolute Maximum Ratings
Table 3:	Recommended Operating Conditions
Table 4:	Mode Control Select Signal Switching
Table 5:	RF25B Tx ASIC Electrical Specifications
Figure 1:	RF25B Tx ASIC Pinout – 40_Pin LGA 6 x 6 mm Package
Figure 2:	RF25B Tx ASIC Block Diagram
Figure 3 – 15:	Typical Functional Block Performance
Figure 16:	RF25B Schematic Diagram
Figure 17:	RF25B Tx ASIC Pin Package Dimensions 40-Pin LGA 6x6 mm Package
Figure 18:	40-Pin LGA Tape and Reel Dimensions

Table 1. Pin Assignments and Signal Descriptions (1 of 3)

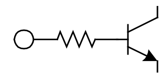
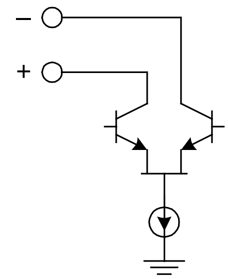
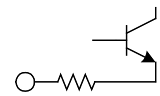
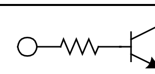
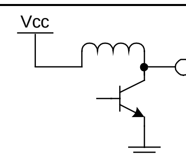
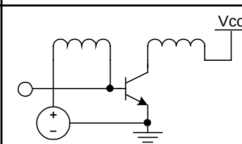
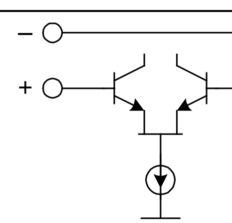
Pin #	Name	Description	Equivalent Circuit
1	NC	No connect.	
2	VCC_IF	Supply voltage for the VGA, IF mux, and bias circuitry. A bypass capacitor with a short trace is required.	
3	RF_GC	The gain control pin for the RF upconverters. A DC voltage of 1 to 2.5 V is needed to cover the mixer RF range.	
4	VGA_OUT+	The output pin for the 130.38 MHz VGA. This is a balanced output. It should be connected to an external bandpass filter for noise reduction. Requires an inductor choke to VCC IF on both differential lines. Both outputs are open collectors.	
5	VGA_OUT-	Same as pin 4, except complementary output.	
6	POT	This pin is connected to an external resistor. The value of the resistor varies the bias current of the driver, which affects gain and Adjacent Channel Power Rejection (ACPR). For CDMA mode, the resistor range is 330 to 3.9 K ohms.	
7	DRV_ON	This is the driver control signal. When the pin is low, the driver is deactivated during no transmission. During transmission the pin should be high to enable the driver. DRIVER_ON = On to DRIVER_ON = Off can be used to provide a 33 dB step in cellular CDMA mode.	
8	VCC_BIAS	Supply voltage for the cellular driver bias. A bypass capacitor with a short trace is required.	
9	RF_OUT	This is the output pin for the cellular RF signal. The pin is connected to the output of the cellular driver amplifier. Impedance matching is required.	
10	NC	No connect.	
11	NC	No connect.	
12	NC	No connect.	
13	VCC_DRV	Supply voltage for the driver. A bypass capacitor with short trace is required.	
14	NC	No connect.	
15	DRV_IN	This is the input for the cellular band driver. The input signal should pass through a SAW filter before being connected to the driver. Impedance matching is required.	
16	I+	The I/Q modulator baseband balanced input for the I channel. A ±1.85 V typical DC bias is required at both differential input pins.	
17	I-	Same as pin 16, except complementary input.	
18	VCC_IQ_MOD	Supply voltage for the I/Q modulator. A bypass capacitor with a short trace is required.	

Table 1. Pin Assignments and Signal Descriptions (2 of 3)

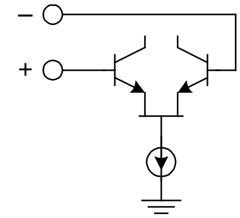
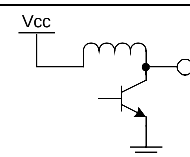
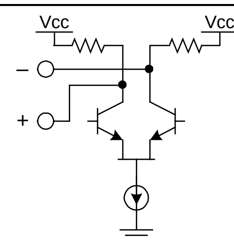
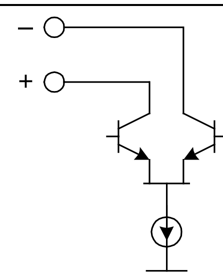
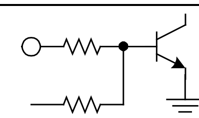
Pin #	Name	Description	Equivalent Circuit
19	Q+	The I/Q modulator baseband balanced input for the Q channel. A ±1.85 V typical DC bias is required at both differential input pins.	
20	Q-	Same as pin 19, except complementary input.	
21	NC	No connection.	
22	NC	No connection.	
23	VCC_DIFF_DRV	Supply voltage for a differential amplifier in the upconverter block. A bypass capacitor with a short trace is required.	
24	NC	No connection.	
25	CHIP_ENA	This is the IQ modulator, VGA, and upconverter enable signal. When the input is low, the chip is disabled. When the input is high, the chip is enabled.	
26	MIX_OUT	This is the output pin for the cellular upconverter. The RF output signal should be routed through an image rejection filter before being connected to the driver input.	
27	VCC_DIV	Supply voltage for the divider and VCO buffer. A bypass capacitor with a short trace is required.	
28	NC	No connection.	
29	PLL+	This is the balanced output pin for the VCO. This output goes to an external PLL that locks the VCO frequency.	
30	PLL-	Same as pin 29, except complementary input.	
31	NC	No connection.	
32	$\overline{\text{AMPS}}$/CDMA	This is the cellular mode control signal input. When the input is low, the AMPS mode is selected. If the input is high, CDMA mode is selected.	
33	VCO-	This is the balanced input pin for an external VCO tank circuit. The tank circuit values estimate the frequency of oscillation (and the Q factor) of the LO. This tank circuit should contain a varactor to modulate the IF frequency directly at the modulator output. The output frequency of the external VCO is divided by 2 before applying to the I/Q modulator.	
34	VCO+	Same as pin 33, except a complementary input.	
35	VGA_GC	The VGA gain control signal. A DC control voltage should be applied to this pin to vary the gain of the VGA.	

Table 1. Pin Assignments and Signal Descriptions (3 of 3)

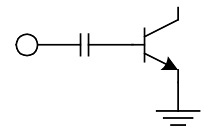
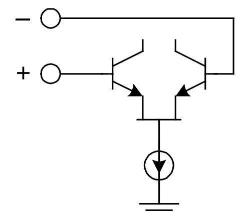
Pin #	Name	Description	Equivalent Circuit
36	VCC_MIX	Supply voltage for the mixer in the upconverter block and for the LO buffer. A bypass capacitor with a short trace is required.	
37	LO_IN	This is the LO input pin for the mixer. A typical –10 dBm LO power is needed.	
38	NC	No connection.	
39	MIX_IN-	This is the balanced input to the upconverter. The input impedance is high.	
40	MIX_IN+	Same as pin 39, except a complementary input.	

Table 2. Absolute Maximum Ratings

Parameter	Minimum	Maximum	Units
Supply voltage (VCC)	-0.3	5.0	V
Input voltage range	-0.3	VCC	V
Power dissipation	--	600	mW
Ambient operating temperature	-30	+80	°C
Storage temperature	-40	+125	°C

Table 3. Recommended Operating Conditions

Parameter	Min	Typical	Max	Units
Supply voltage	2.85	3.0	3.3	V
Logic level high	1.9			V
Logic level low			0.6	V
Supply current in 800 MHz CDMA @ 7 dBm	89	102	115	mA
Supply current in 800 MHz AMPS @ 11 dBm	96	110	124	mA
Supply current in 800 MHz (DRIVER_ON = Off)	57	68	79	mA
Supply current in sleep mode (CHIP_ENA = Off, DRIVER_ON = Off)			10	µA

Table 4. Mode Control Select Signal Switching

Pin #	Name	AMPS	CDMA
25	CHIP_ENA	1	1
32	$\overline{\text{AMPS}}$/CDMA	0	1
Key: 0 = LOW 1 = HIGH			

Table 5. RF25B Tx ASIC Electrical Specifications (1 of 2)
TA = 25° C, VCC = 3.3 V, PLO = -10 dBm, input externally matched

Parameter	Test Condition	Min	Typical	Max	Units
VCO (external tank)/Wideband Divide-By-2					
Frequency range for VCOs		100		640	MHz
2nd harmonic (measured @ tank circuit)			-30	-26	dBc
3rd harmonic (measured @ tank circuit)			-20		dBc
Phase noise @100 kHz offset, Fc = 260 MHz, unloaded tank Q = 20			-113		dBc/Hz
Input frequency range to /2 circuit		100		640	MHz
Output impedance of buffer to PLL (differential)			300		Ω
Output signal level to PLL (differential)			300		mVp-p
I/Q Modulator					
Input voltage level, differential			1		Vp-p
Common mode input voltage level		1.6	1.85	2.1	V
Input DC offset				4	mV
Input impedance		100K			Ω
Gain variation over process, temperature, VCC			0.4		dB
I/Q gain mismatch			0.3	0.4	dB
I/Q phase imbalance			2	4	degree
Tx VGA					
VGA frequency range (-1 dB bandwidth)		50		320	MHz
VGA gain (with 510 Ω load resistor): Maximum Minimum		 25 -65	 28 -62	 30 -60	 dB dB
VGA gain variation with VCC 3.0 to 3.6 V @ V_{CTRL} 2 V		-3		3	dB
Gain variation with temperature		-1.5		1.5	dB
Gain control input impedance			40K		Ω
VGA gain slope		40	45	50	dB/V
VGA gain control range		0.2		2.7	V
Gain slope variation over any 6 dB segment		-3		+3	dB/V
Output power level @ 26dB gain Minimum controllable output power (thermal noise: -113dBm)			-13 -107		dBm
ACPR in 30 kHz band at 885 kHz offset, maximum gain			-61	-60	dBc
ACPR in 30 kHz band at 1.98 MHz offset, maximum gain			-72	-71	dBc
NF at maximum gain			5	6	dB
NF at -52 dB gain			52	53	dB

Table 5. RF25B Tx ASIC Electrical Specifications (2 of 2)
TA = 25° C, VCC = 3.3 V, PLO = -10 dBm, input externally matched

Parameter	Test Condition	Min	Typical	Max	Units
Variable Gain Upconverter					
LO frequency range		700		1000	MHz
LO input return loss (reference to 50 Ω)			-10		dB
Terminating resistor across IF inputs		485	510	535	Ω
Output frequency		824		925	MHz
CDMA mode conversion gain, maximum		20	21		dB
CDMA mode conversion gain, minimum			-10		dB
ACPR in 30 kHz at 885 kHz offset @ -2 dBm output			-53	-52	dBc
ACPR in 30 kHz at 1.98 MHz offset @ -2 dBm output				-66	dBc
FM mode conversion gain, maximum		22	25		dB
FM mode conversion gain, minimum			-6		dB
FM mode output P1dB		+5	+6		dBm
Noise figure @ 22 dB gain CDMA/22 dB gain FM			10	11	dB
Noise figure @ 12 dB gain CDMA/14 dB gain FM			16	18	dB
LO to RF leakage @ maximum gain, LO = -10 dBm			-35		dBm
PA Driver					
Output frequency		824		925	MHz
Gain (@ POT800 = 330 Ω)		12.5	13.5		dB
Output power level		8	10		dBm
Saturated output power level (FM)		12	14		dBm
Output power level @ maximum gain		7	8		dBm
ACPR in 30 kHz band at 885 kHz offset @ 7 dBm output			-54	-53	dBc
ACPR in 30 kHz band at 1.98 MHz offset @ 7 dBm output			-67	-66	dBc
Output return loss (reference to 50 Ω)			-15		dB
Noise figure			6	8	dB

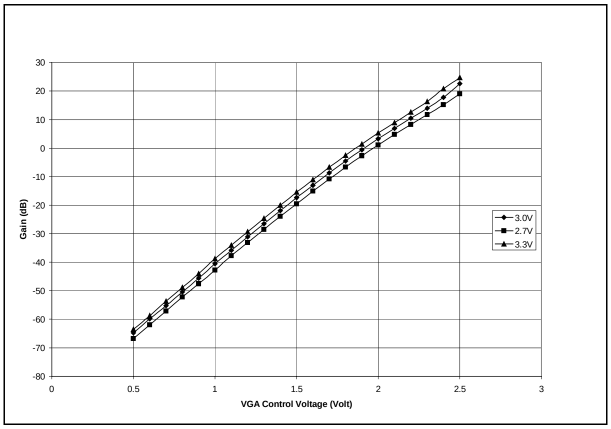


Figure 3. VGA Gain vs. Control Voltage Over Vcc

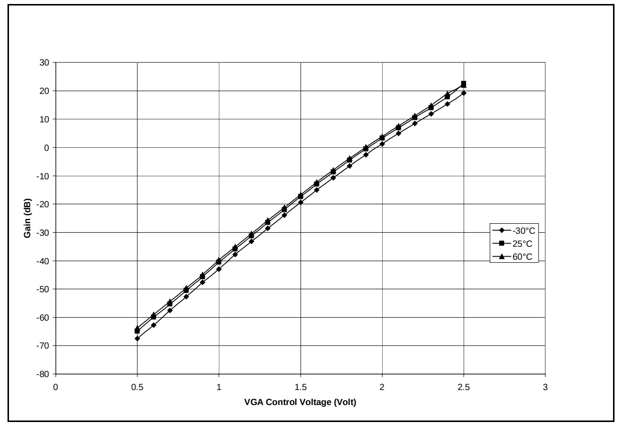


Figure 4. VGA Gain vs. Control Voltage Over Temperature

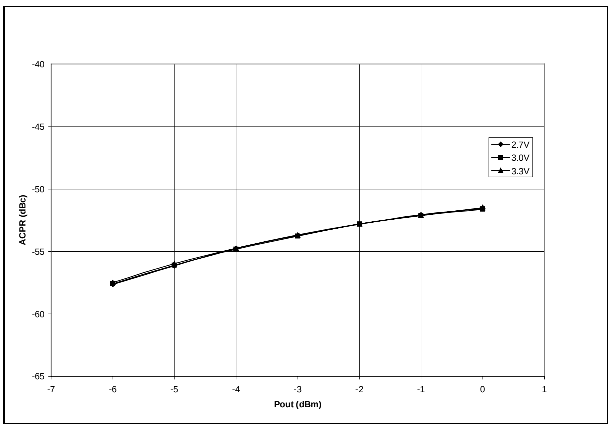


Figure 5. Mixer ACPR vs. Pout Over Vcc

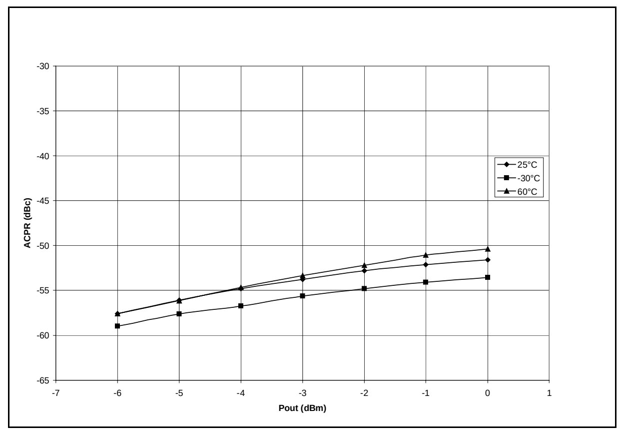


Figure 6. Mixer ACPR vs. Pout Over Temperature

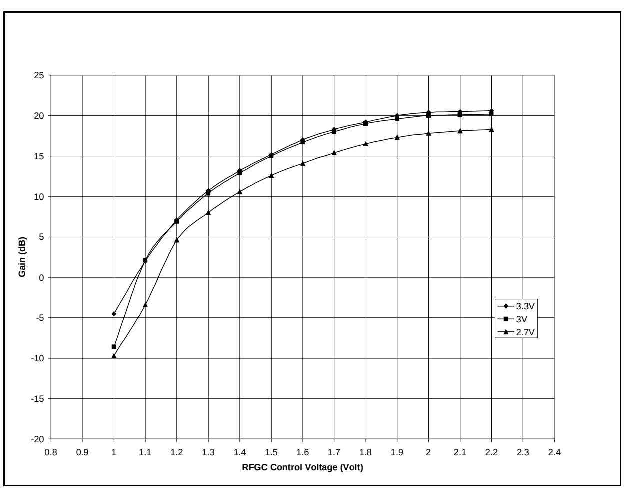


Figure 7. Mixer Gain vs. RFGC Control Voltage Over Vcc

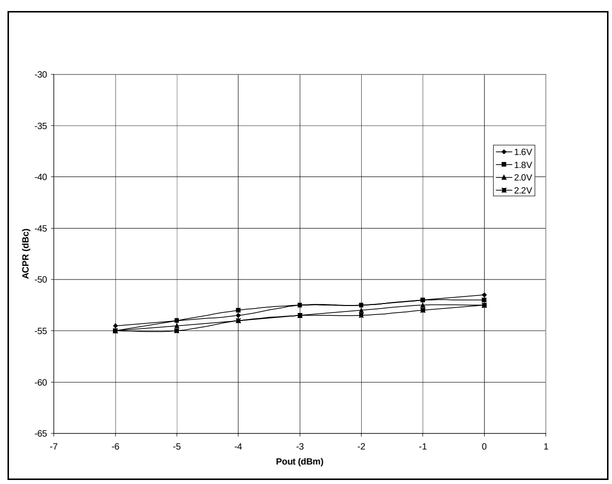


Figure 8. Mixer ACPR vs. Pout Over RFGC Control Voltage

Note: Unless otherwise specified, all graphs depict testing at Fc = 836.5 MHz, ΔF = ±0.885 MHz, Vcc = 3.0 V, 25 °C.

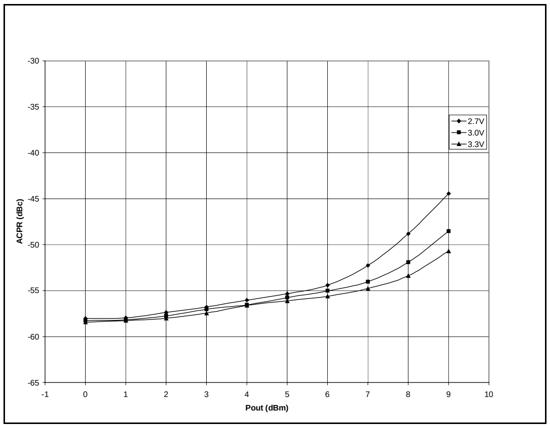


Figure 9. Driver ACPR vs. Pout Over Vcc

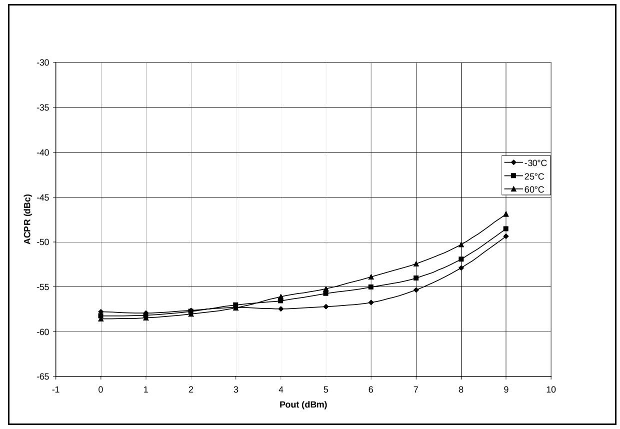


Figure 10. Driver ACPR vs. Pout Over Temperature

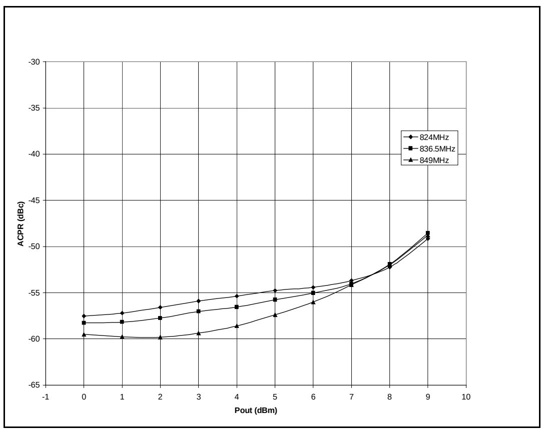


Figure 11. Driver ACPR vs. Pout Over Frequency

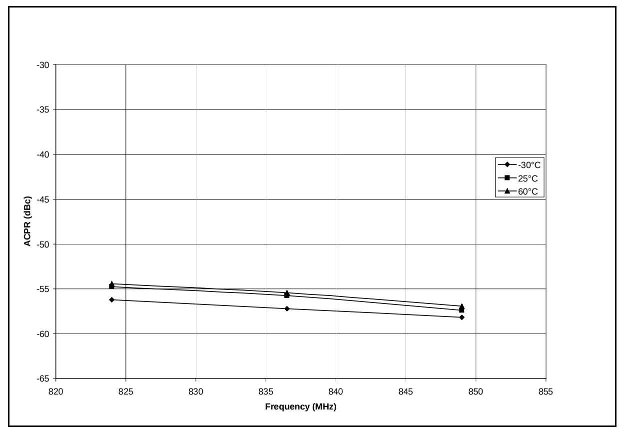


Figure 12. Driver ACPR vs. Frequency Over Temperature (Pout = 5 dBm)

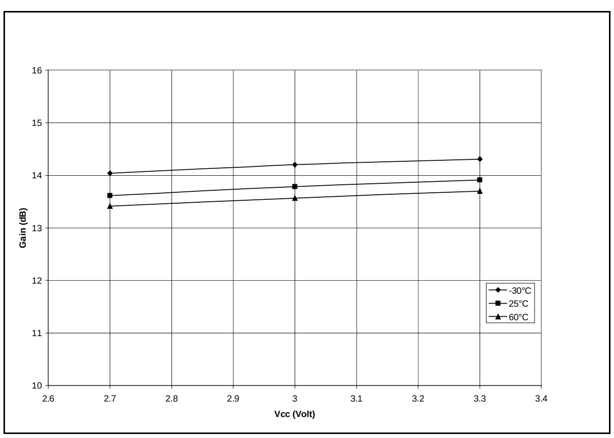


Figure 13. Driver Gain vs. Vcc Over Temperature (Po = 5 dBm)

Note: Unless otherwise specified, all graphs depict testing at Fc = 836.5 MHz, ΔF = ±0.885 MHz, Vcc = 3.0 V, 25 °C.

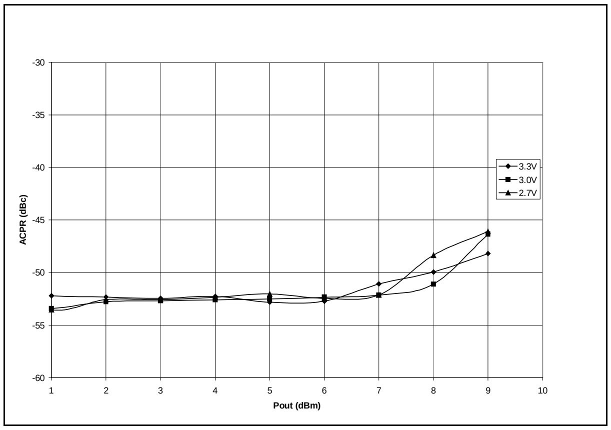


Figure 14. Cascaded ACPR vs. Pout Over Vcc

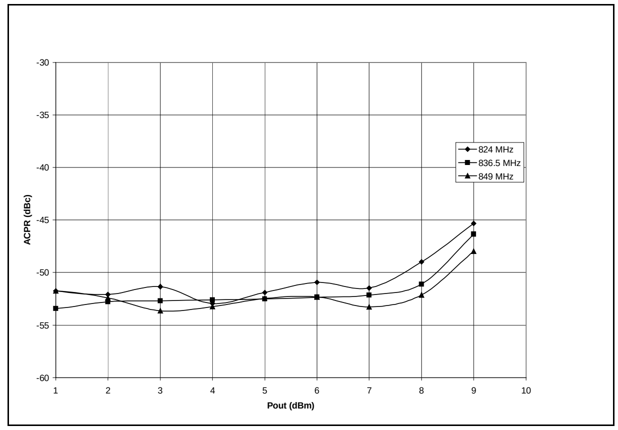


Figure 15. Cascaded ACPR vs. Pout Over Frequency (Vcc = 3.3V)

Notes: Unless otherwise specified, all graphs depict testing at Fc = 836.5 MHz, ΔF = $\pm$0.885 MHz, Vcc = 3.0 V, 25 °C.
Cascaded performance was measured with RF and IF filters connected.

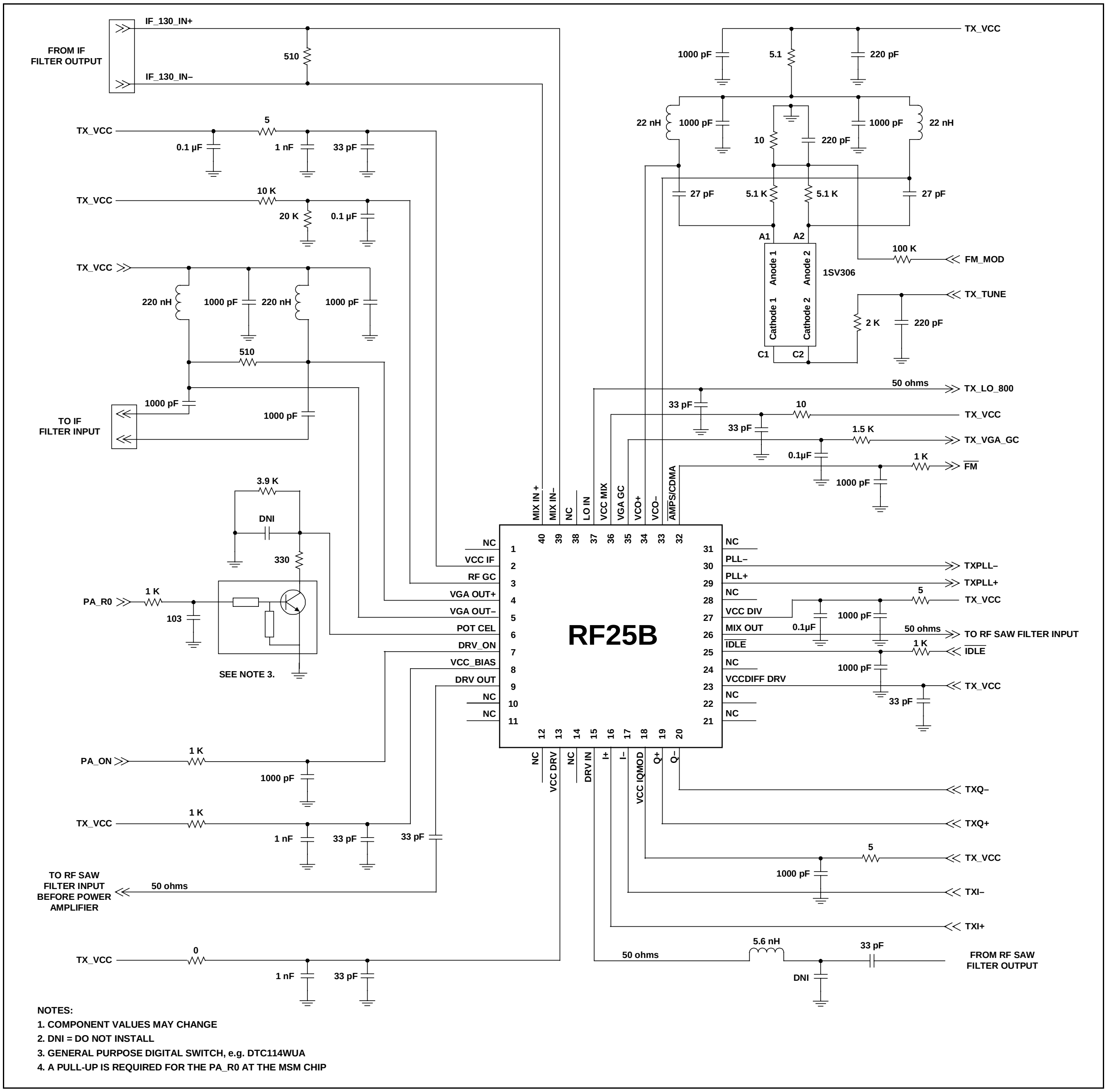


Figure 16. RF25B Schematic Diagram

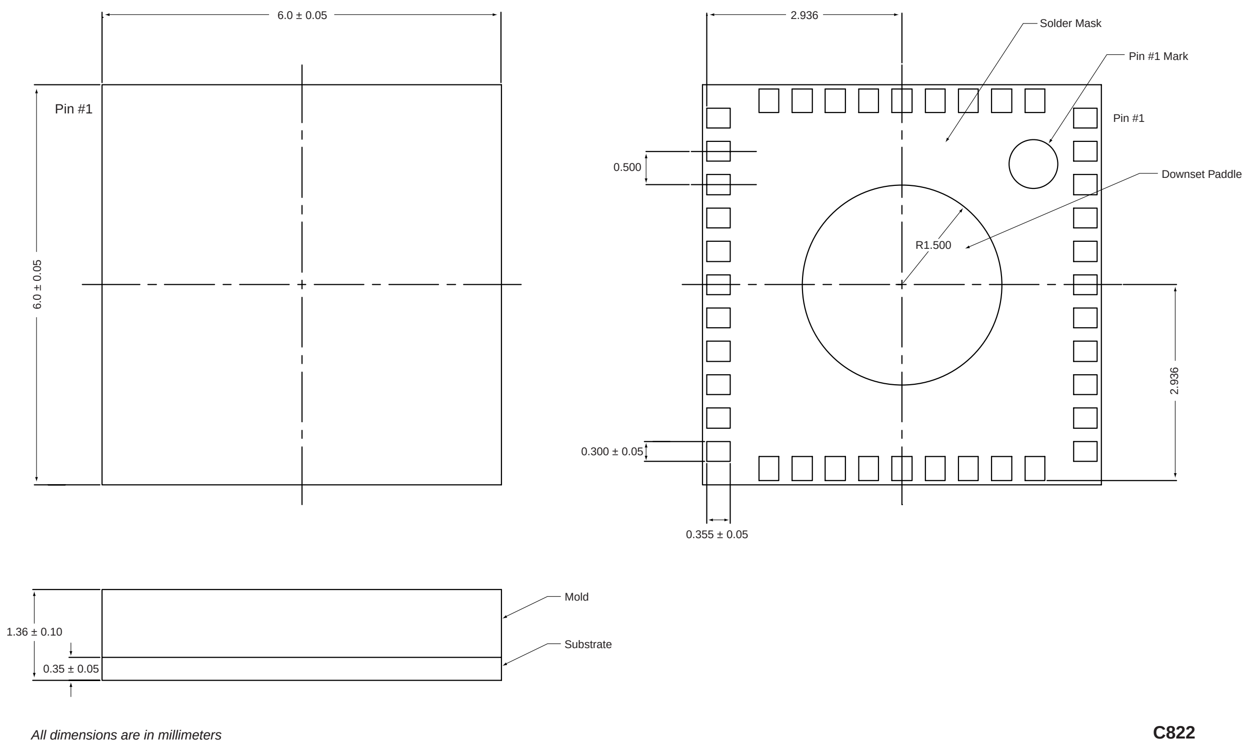
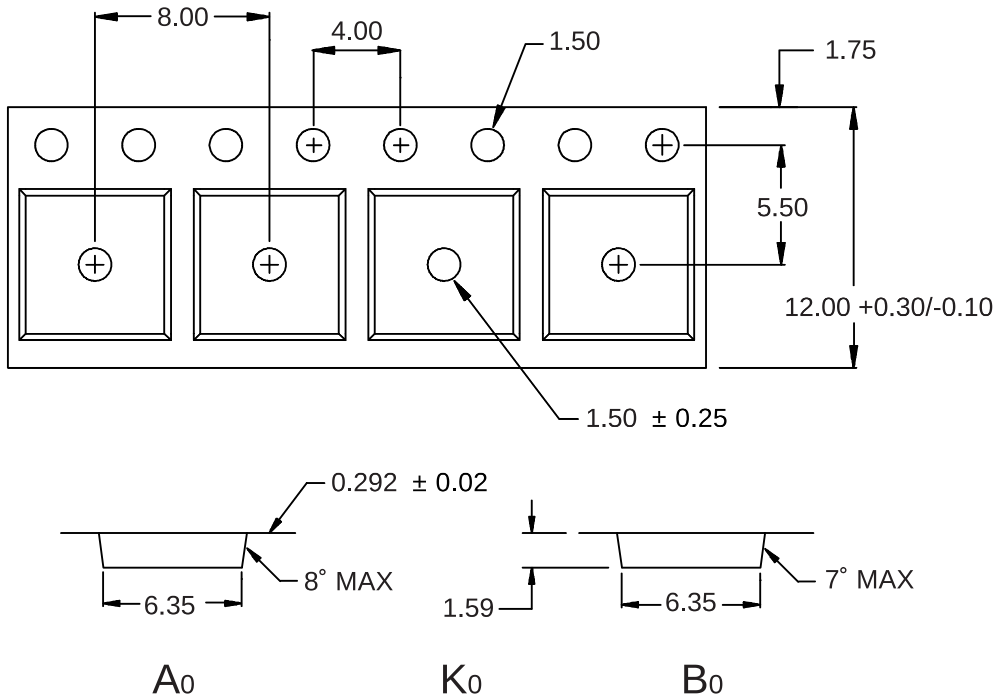


Figure 17. RF25B Tx ASIC Package Dimensions - 40-pin LGA 6x6 Package



NOTES:

1. Carrier Tape Material: Black Conductive Polycarbonate
2. Cover Tape Material: Transparent Conductive PSA
3. Cover Tape Size: 9.3 mm width
4. Tolerance: .XX = ± 0.10
5. All dimensions are in millimeters

CNXT022

Figure 18. 40-pin LGA Tape and Reel Dimensions

Ordering Information

Model Name	Manufacturing Part Number	Product Revision
RF25B	RF25B-21	21

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