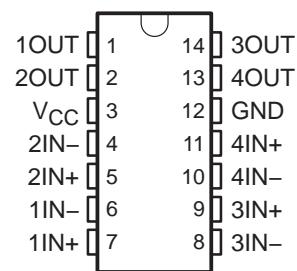


- Single Supply or Dual Supplies
- Wide Range of Supply Voltage . . . 2 V to 28 V
- Low Supply-Current Drain Independent of Supply Voltage . . . 0.8 mA Typ
- Low Input Bias Current . . . 25 nA Typ
- Low Input Offset Current . . . 3 nA Typ
- Low Input Offset Voltage . . . 3 mV Typ
- Common-Mode Input Voltage Range Includes Ground
- Differential Input Voltage Range Equal to Maximum-Rated Supply Voltage . . . ± 28 V
- Low Output Saturation Voltage
- Output Compatible With TTL, MOS, and CMOS

D OR N PACKAGE
(TOP VIEW)



description/ordering information

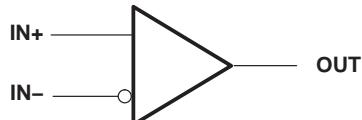
This device consists of four independent voltage comparators that are designed to operate from a single power supply over a wide range of voltages. Operation from dual supplies also is possible as long as the difference between the two supplies is 2 V to 28 V and V_{CC} is at least 1.5 V more positive than the input common-mode voltage. Current drain is independent of the supply voltage. The outputs can be connected to other open-collector outputs to achieve wired-AND relationships.

ORDERING INFORMATION

T_A	V_{IOmax} AT 25°C	PACKAGE ^T		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	20 mV	PDIP (N)	Tube of 25	LM3302N	LM3302N
		SOIC (D)	Tube of 50	LM3302D	LM3302
			Reel of 2500	LM3302DR	

^T Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

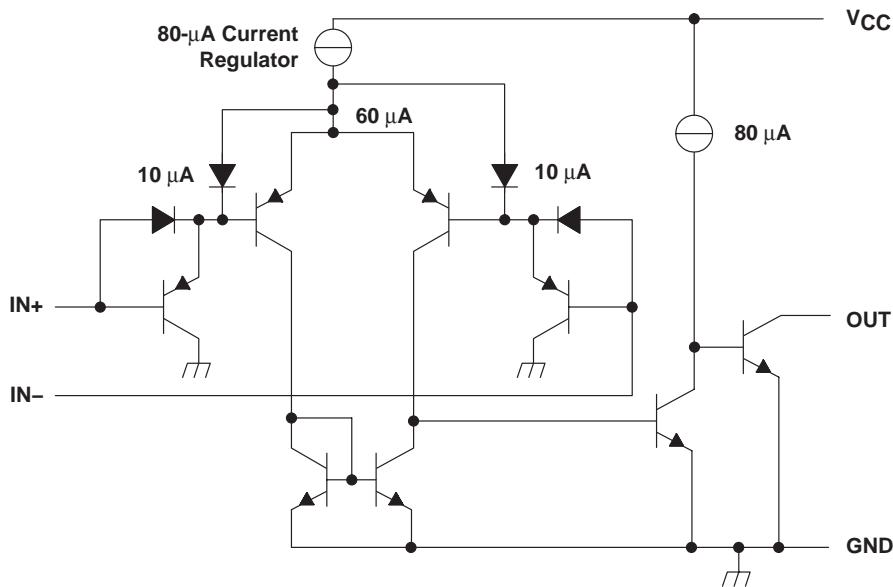
symbol (each comparator)



LM3302 QUADRUPLE DIFFERENTIAL COMPARATOR

SLCS014A –OCTOBER 1977 –REVISED AUGUST 2003

schematic



Current values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{CC} (see Note 1)	28 V
Differential input voltage, V_{ID} (see Note 2)	± 28 V
Input voltage range, V_I (either input)	-0.3 V to 28 V
Output voltage, V_O	28 V
Output current, I_O	20 mA
Duration of output short-circuit to ground (see Note 3)	Unlimited
Package thermal impedance, θ_{JA} (see Notes 4 and 5): D package	86°C/W
	N package
Operating virtual junction temperature, T_J	150°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds: D or N package	260°C
Storage temperature range, T_{stg}	-65°C to 150°C

[†] Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. There are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the recommended operating conditions section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground.

2. Differential voltages are at $IN+$ with respect to $IN-$.
3. Short circuits from the output to V_{CC} can cause excessive heating and eventual destruction.
4. Maximum power dissipation is a function of $T_J(\max)$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(\max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
5. The package thermal impedance is calculated in accordance with JEDEC 51-7.

electrical characteristics at specified free-air temperature, $V_{CC} = 5$ V (unless otherwise noted)

PARAMETER	TEST CONDITIONS [†]	TA	MIN	TYP	MAX	UNIT
V_{IO} Input offset voltage	$V_{CC} = 5$ V to 28 V, $V_{IC} = V_{ICR\min}$, $V_O = 1.4$ V	25°C		3	20	mV
		–40°C to 85°C			40	
I_{IO} Input offset current	$V_O = 1.4$ V	25°C		3	100	nA
		–40°C to 85°C			300	
I_{IB} Input bias current		25°C		–25	–500	nA
		–40°C to 85°C			–1000	
V_{ICR} Common-mode input voltage range		25°C	0 to $V_{CC} – 1.5$			V
		–40°C to 85°C	0 to $V_{CC} – 2$			
A_{VD} Large-signal differential voltage amplification	$V_{CC} = 15$ V, $R_L = 15 \Omega$ to V_{CC}	25°C	2	30		V/mV
I_{OH} High-level output current	$V_{ID} = 1$ V, $V_{OH} = 5$ V	25°C		0.1		nA
		–40°C to 85°C			1	μA
V_{OL} Low-level output voltage	$V_{ID} = –1$ V, $I_{OL} = 4$ mA	25°C	150	500		mV
		–40°C to 85°C			700	
I_{OL} Low-level output current	$V_{ID} = 1$ V, $V_{OL} = 1.5$ V	25°C	6	16		mA
I_{CC} Supply current (four comparators)	$V_O = 2.5$ V, No load	25°C		0.8		mA

[†] All characteristics are measured with zero common-mode input voltage unless otherwise specified.

switching characteristics, $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS		TYP	UNIT
Response time	$R_L = 5.1 \text{ k}\Omega$ to 5 V, $C_L = 15 \text{ pF}^\ddagger$, See Note 6	100-mV input step with 5-mV overdrive	1.3	μs
		TTL-level input step	0.3	

[‡] C_L includes probe and jig capacitance.

NOTE 6: The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM3302D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LM3302	Samples
LM3302DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LM3302	Samples
LM3302DRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LM3302	Samples
LM3302DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LM3302	Samples
LM3302N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	LM3302N	Samples
LM3302NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	LM3302N	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

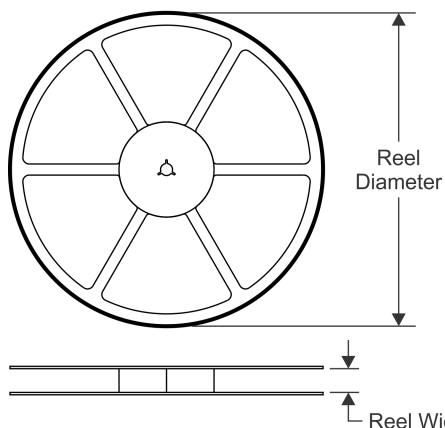
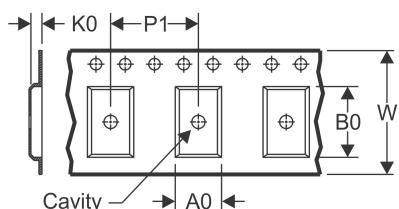
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

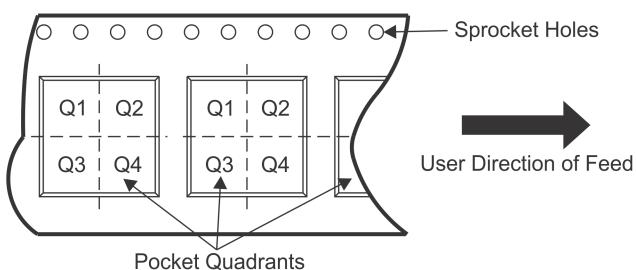
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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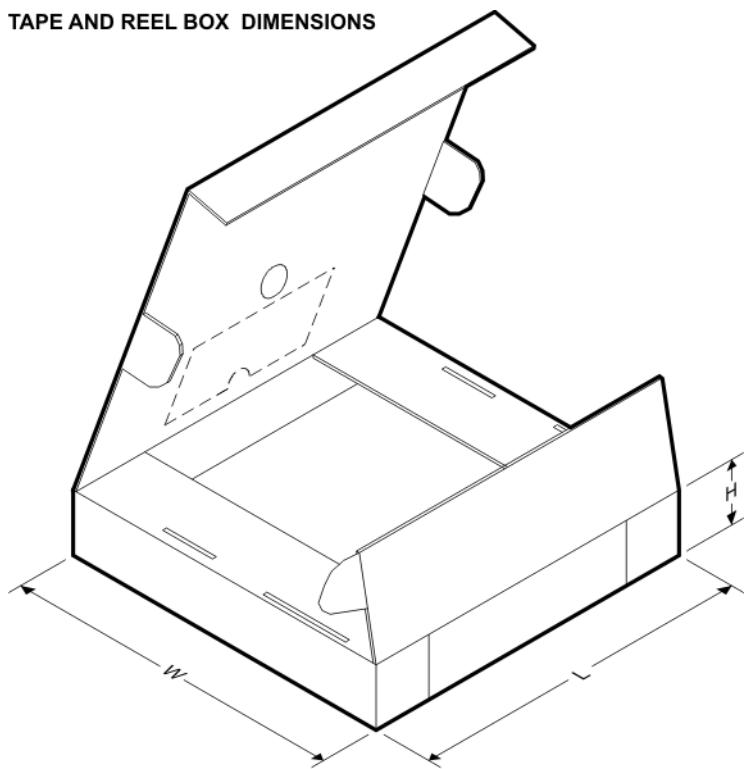
TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3302DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM3302DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

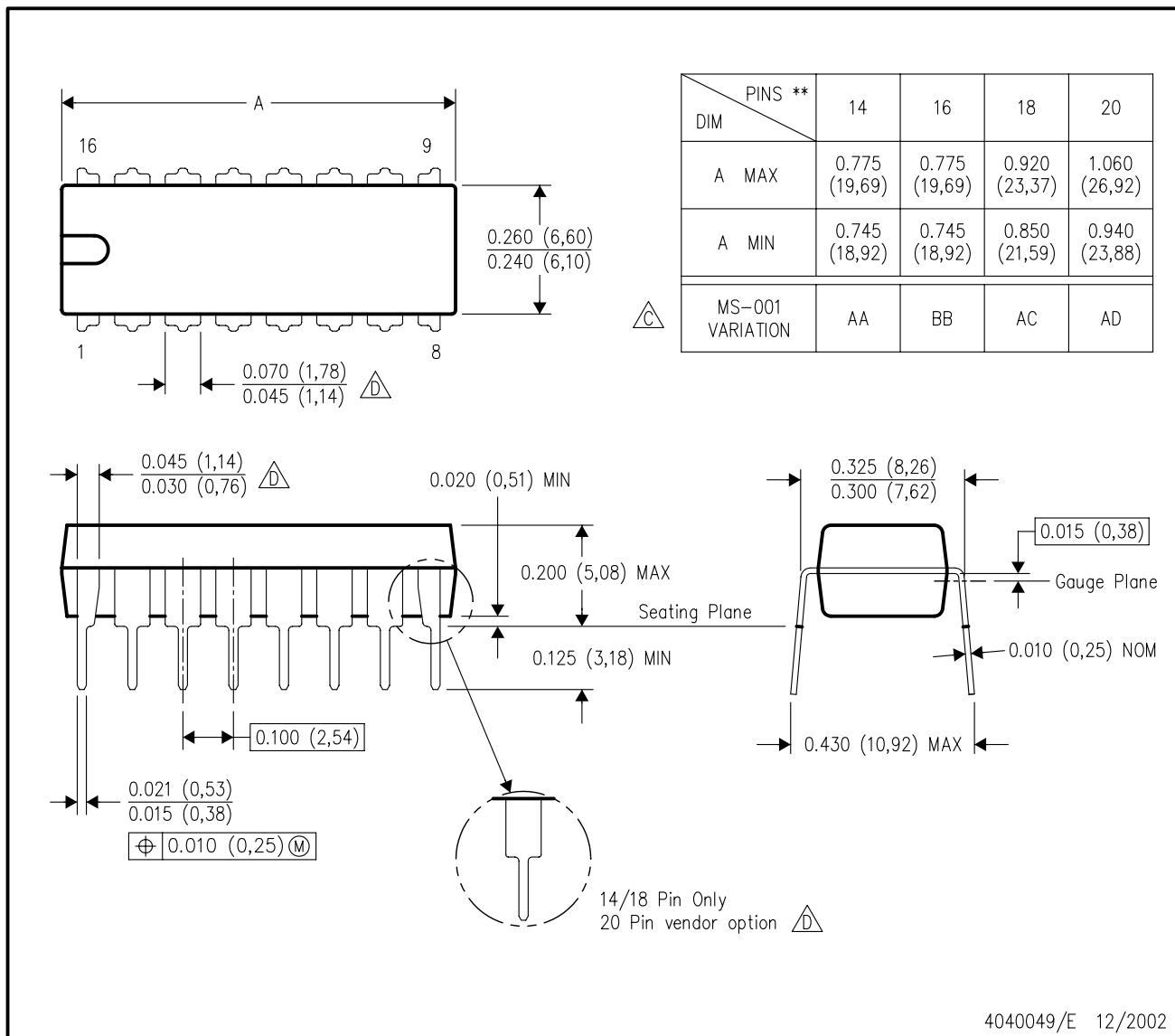
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3302DR	SOIC	D	14	2500	333.2	345.9	28.6
LM3302DR	SOIC	D	14	2500	367.0	367.0	38.0

N (R-PDIP-T**)

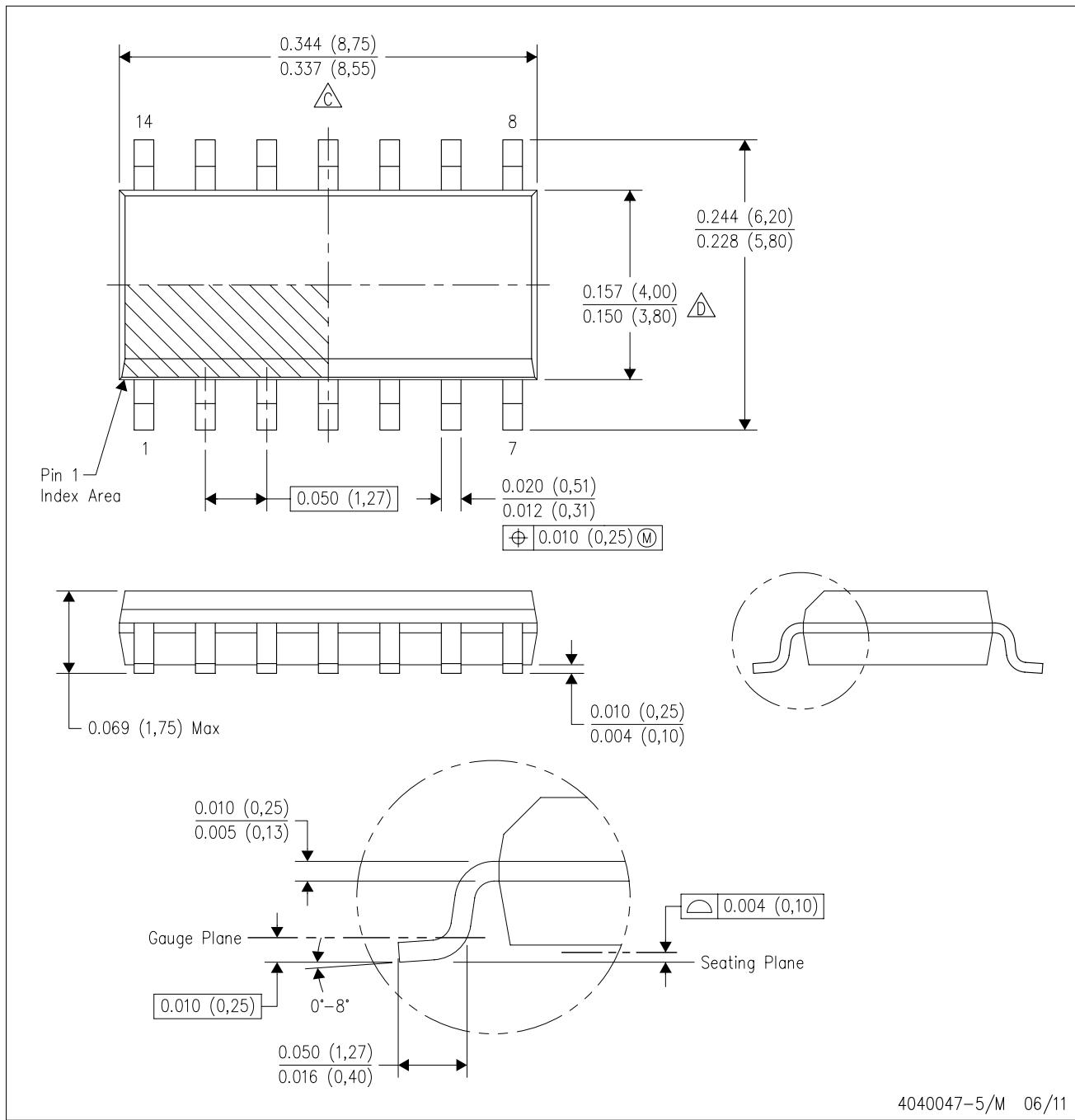
16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

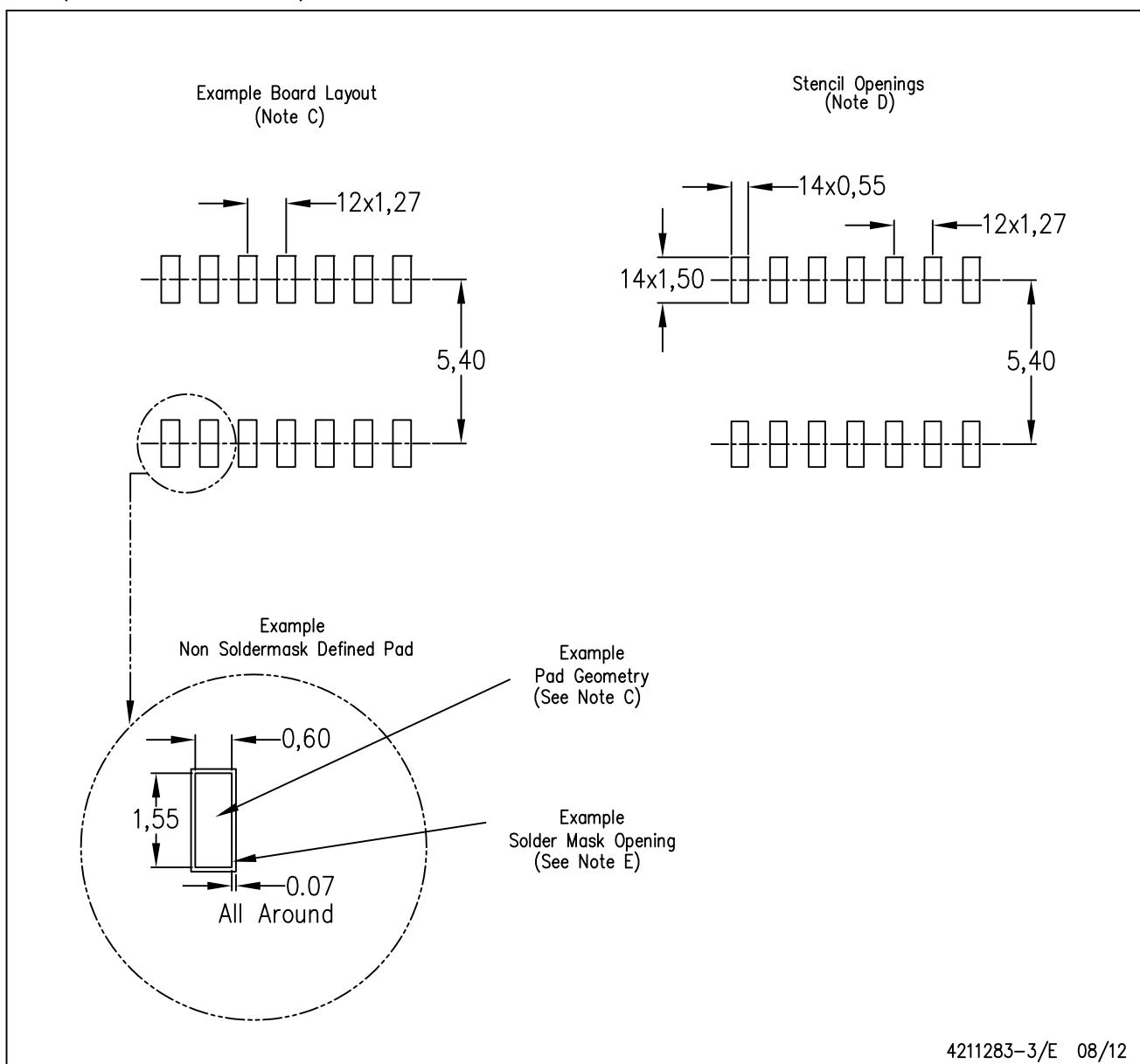
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.

D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.

E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211283-3/E 08/12

NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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