19-4473; Rev 0; 2/09

EVALUATION KIT AVAILABLE

Dual, High-Voltage Scan Driver for TFT LCD

General Description

The MAX17109 includes two high-voltage, level-shifting scan drivers for TFT panel integrated gate logic. Each scan driver has 2 channels that switch complementarily. The scan driver outputs swing from +40V to -30V and can swiftly drive capacitive loads. To save power, the scan driver's complementary outputs share the charge of their capacitive load before they change states.

The MAX17109 is available in a 32-pin, 5mm x 5mm, thin QFN package with a maximum thickness of 0.8mm for ultra-thin LCD panels.

Features

- **+40V to -30V Output Swing Range**
- **Fast Slew Rate for High Capacitive Load**
- **Load Charge Sharing for Power Saving**
- **32-Pin, 5mm x 5mm, Thin QFN Package**

Applications

Notebook Computer Displays

LCD Monitor and TV Panels

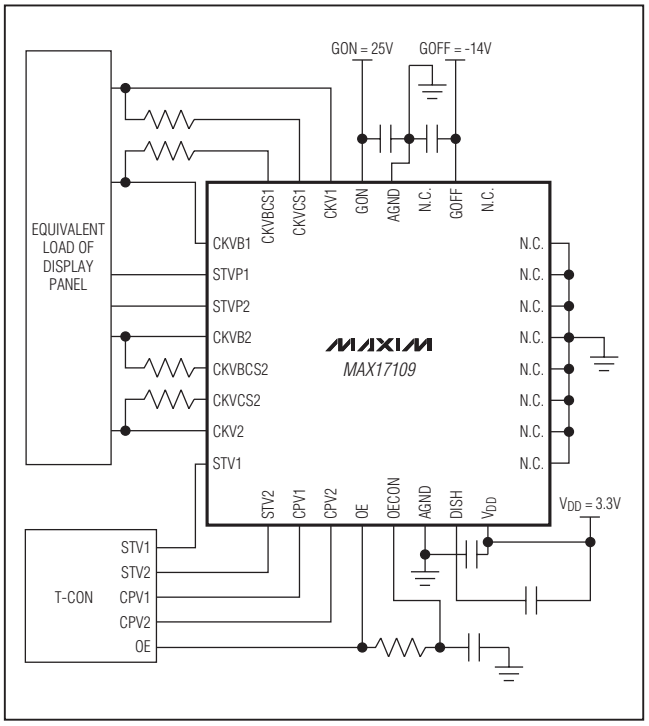
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX17109ETJ+	-40°C to +85°C	32 Thin QFN-EP*

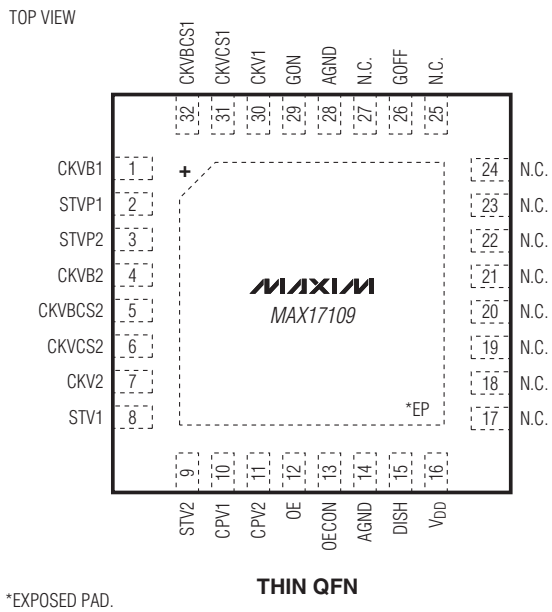
+Denotes a lead(Pb)-free/RoHS-compliant package.

**EP = Exposed pad.*

Simplified Operating Circuit



Pin Configuration



Dual, High-Voltage Scan Driver for TFT LCD

ABSOLUTE MAXIMUM RATINGS

V_{DD} to AGND ..... -0.3V to +6V
OECON, CPV1, CPV2, OE, STV1, STV2 to AGND... -0.3V to +6V
DISH to AGND..... -6V to (V_{VDD} + 0.3V)
GON to AGND..... -0.3V to +45V
GOFF to AGND ..... -35V to + 0.3V
GON to GOFF..... +70V
CKV1, CKV2, CKVB1,
CKVB2 to GOFF ..... -0.3V to (V_{GON} + 0.3V)
STVP1, STVP2 to GOFF ..... (V_{GON} + 0.3V)
CKVCS1, CKVCS2 to GOFF..... -0.3V to (V_{GON} + 0.3V)
CKVBCS1, CKVBCS2 to GOFF..... -0.3V to (V_{GON} + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
32-Pin, 5mm x 5mm Thin QFN
(derate 34.5mW/°C above +70°C)..... 2758.6mW
Operating Temperature Range ..... -40°C to +85°C
Junction Temperature..... +150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s)..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +3.3V, V_{GON} = 25V, V_{GOFF} = -14V, STV1 = STV2 = CPV1 = CPV2 = OE = OECON = AGND, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VDD Input-Voltage Range		2.2		3.6	V
VDD Quiescent Current			160	300	µA
VDD Undervoltage Lockout	V_{VDD} rising, typ hysteresis = 50mV		1.9	2.15	V
Thermal Shutdown	Rising edge, hysteresis = 15°C		+160		°C
HIGH-VOLTAGE SCAN DRIVER					
GON Input-Voltage Range		13		40	V
GOFF Input-Voltage Range		-30		-3	V
GON-to-GOFF Input-Voltage Range				65	V
GON UVLO	V_{GON} rising		12.2	13	V
	V_{GON} falling	10	11		
GON Supply Current			300	500	µA
GOFF Supply Current			200	350	µA
CKV Output Impedance Low	CKV1, CKVB1, CKV2, CKVB2; -20mA output current		6	12	Ω
CKV Output Impedance High	CKV1, CKVB1, CKV2, CKVB2; +20mA output current		8	15	Ω
STV Output Impedance Low	STVP1, STVP2; -20mA output current		25	50	Ω
STV Output Impedance High	STVP1, STVP2; +20mA output current		35	70	Ω
Driver Output Three-State Current	CKV1, CKVB1, CKVCS1, CKVBCS1, STVP1, CKV2, CKVB2, CKVCS2, CKVBCS2, STVP2, T_A = +25°C	-1		1	µA
Charge-Sharing Switch Resistance	CKVCS_ to CKVBCS_ at 10mA		50	100	Ω
DISH Switch Resistance	GOFF = -5V, DISH = -3V		200	400	Ω
SCAN DRIVER PROPAGATION DELAYS (Note 1)					
OE Rising Edge to CKV/CKVB Rising Edge	STV = 0		100	300	ns
OE Rising Edge to CKV/CKVB Falling Edge	STV = 0		100	300	ns
CPV_ Rising Edge to CKVCS_/ CKVBCS_ Rising Edge	STV = 0		50	120	ns
CPV_ Rising Edge to CKVCS_/ CKVBCS_ Falling Edge	STV = 0		50	120	ns

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +3.3V, V_{GON} = 25V, V_{GOFF} = -14V, STV1 = STV2 = CaPV1 = CPV2 = OE = OECON = AGND, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CPV_ Falling Edge to CKVCS_/ CKVBCS_ Rising Edge	STV = 0		100	300	ns
CPV_ Falling Edge to CKVCS_/ CKVBCS_ Falling Edge	STV = 0		100	300	ns
STV_ Rising Edge to STVP_ Rising Edge			150	300	ns
STV_ Falling Edge to STVP_ Falling Edge			150	300	ns
SCAN DRIVER FREQUENCIES					
CPV Input Frequency				85	kHz
OE Input Frequency				170	kHz
SCAN DRIVER SLEW RATES					
Positive Slew Rate (CKV1, CKVB1, CKV2, CKVB2)	STV = 1, C_{LOAD} = 4.7nF, R_{LOAD} = 50Ω, 20% to 80%	100	1000		V/µs
	STV = 1, C_{LOAD} = 15nF, 100Ω, 15% to 85% (Note 1)		2000		
	STV = 1, C_{LOAD} = 4.7nF, 20% to 80%	100	170		
Negative Slew Rate (CKV1, CKVB1, CKV2, CKVB2)	STV = 1, C_{LOAD} = 4.7nF, R_{LOAD} = 50Ω, 80% to 20%	100	1000		V/µs
	STV = 1, C_{LOAD} = 15nF, 100Ω, 15% to 85% (Note 1)		2000		
	STV = 1, C_{LOAD} = 4.7nF, 80% to 20%	70	130		
Positive Slew Rate (CKV1, CKVB1, CKV2, CKVB2)	STV = 0, C_{LOAD} = 4.7nF, R_{LOAD} = 50Ω, 20% to 80%	100	1000		V/µs
	STV = 1, C_{LOAD} = 15nF, 100Ω, 15% to 85% (Note 1)		2000		
	STV = 0, C_{LOAD} = 4.7nF, 20% to 80%	70	120		
Negative Slew Rate (CKV1, CKVB1, CKV2, CKVB2)	STV = 0, C_{LOAD} = 4.7nF, R_{LOAD} = 50Ω, 80% to 20%	100	1000		V/µs
	STV = 1, C_{LOAD} = 15nF, 100Ω, 15% to 85% (Note 1)		2000		
	STV = 0, C_{LOAD} = 4.7nF, 80% to 20%	45	100		
Positive Slew Rate (STVP1, STVP2)	C_{LOAD} = 4.7nF, R_{LOAD} = 200Ω, 20% to 80% (Note 1)	20	300		V/µs
	C_{LOAD} = 4.7nF, 20% to 80%	20	40		
Negative Slew Rate (STVP1, STVP2)	C_{LOAD} = 4.7nF, R_{LOAD} = 200Ω, 80% to 20% (Note 1)	20	300		V/µs
	C_{LOAD} = 4.7nF, 80% to 20%	15	30		
INPUT LOGIC THRESHOLDS					
Input Low Voltage	CPV1, CPV2, OE, STV1, STV2			0.3 x V_{VDD}	V
	OECON			V_{DD} - 1.1	
	DISH			-1.0	
Input High Voltage	CPV1, CPV2, OE, STV1, STV2	0.7 x V_{VDD}			V
	OECON	V_{VDD} - 0.5			
Input Hysteresis	CPV1, CPV2, OE, STV1, STV2		100		mV
Input Bias Current	$V_{STV\_}$ = 0 or VDD, $V_{CPV\_}$ = 0 or VDD, V_{OE} = 0 or VDD	-1		+1	µA
OECON Input Bias Current	V_{OECON} = 0V or VDD, STV_ = 0, T_A = +25°C	-1		+1	µA
	STV1 or STV2 = VDD, OECON = 0.4V	25	40		mA
DISH Input Impedance	DISH = -1.5V		250	400	kΩ

Dual, High-Voltage Scan Driver for TFT LCD

ELECTRICAL CHARACTERISTICS

(VDD = +3.3V, GON = 25V, GOFF = -14V, STV1 = STV2 = CPV1 = CPV2 = OE = OECON = AGND, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VDD Input-Voltage Range		2.2		3.6	V
VDD Quiescent Current	V_{VDD} = 3V			300	µA
VDD Undervoltage Lockout	V_{VDD} rising, hysteresis = 50mV			2.15	V
HIGH-VOLTAGE SCAN DRIVER					
GON Input-Voltage Range		13		40	V
GOFF Input-Voltage Range		-30		-3	V
GON-to-GOFF Input-Voltage Range				65	V
GON UVLO	V_{GON} rising			13	V
	V_{GON} falling	10			
GON Supply Current				500	µA
GOFF Supply Current				350	µA
CKV Output Impedance Low	CKV1, CKVB1, CKV2, CKVB2; -20mA output current			12	Ω
CKV Output Impedance High	CKV1, CKVB1, CKV2, CKVB2; +20mA output current			15	Ω
STV Output Impedance Low	STVP1, STVP2; -20mA output current			50	Ω
STV Output Impedance High	STVP1, STVP2; +20mA output current			70	Ω
Charge-Sharing Switch Resistance	CKV_ to CKVCS_ and CKVB_ to CKVBCS_ at 10mA			100	Ω
DISH Switch Resistance	GOFF to -5V, DISH = -3V			400	Ω
SCAN DRIVER PROPAGATION DELAYS					
OE Rising Edge to CKV/CKVB Rising Edge	STV = 0			300	ns
OE Rising Edge to CKV/CKVB Falling Edge	STV = 0			300	ns
CPV_ Rising Edge to CKVCS_/ CKVBCS_ Rising Edge	STV = 0			120	ns
CPV_ Rising Edge to CKVCS_/ CKVBCS_ Falling Edge	STV = 0			120	ns
CPV_ Falling Edge to CKVCS_/ CKVBCS_ Rising Edge	STV = 0			300	ns
CPV_ Falling Edge to CKVCS_/ CKVBCS_ Falling Edge	STV = 0			300	ns
STV_ Rising Edge to STVP_ Rising Edge				300	ns
STV_ Falling Edge to STVP_ Falling Edge				300	ns

ELECTRICAL CHARACTERISTICS (continued)

(VDD = +3.3V, GON = 25V, GOFF = -14V, STV1 = STV2 = CPV1 = CPV2 = OE = OECON = AGND, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SCAN DRIVER FREQUENCIES					
CPV Input Frequency				85	kHz
OE Input Frequency				170	kHz
SCAN DRIVER SLEW RATES					
Positive Slew Rate (CKV1, CKVB1, CKV2, CKVB2)	STV = 1, C_{LOAD} = 4.7nF, R_{LOAD} = 50Ω, 20% to 80%	100			V/µs
	STV = 1, C_{LOAD} = 4.7nF, 20% to 80%	100			
Negative Slew Rate (CKV1, CKVB1, CKV2, CKVB2)	STV = 1, C_{LOAD} = 4.7nF, R_{LOAD} = 50Ω, 80% to 20%	100			V/µs
	STV = 1, C_{LOAD} = 4.7nF, 80% to 20%	70			
Positive Slew Rate (CKV1, CKVB1, CKV2, CKVB2)	STV = 0, C_{LOAD} = 4.7nF, R_{LOAD} = 50Ω, 20% to 80%	100			V/µs
	STV = 0, C_{LOAD} = 4.7nF, 20% to 80%	70			
Negative Slew Rate (CKV1, CKVB1, CKV2, CKVB2)	STV = 0, C_{LOAD} = 4.7nF, R_{LOAD} = 50Ω, 80% to 20%	100			V/µs
	STV = 0, C_{LOAD} = 4.7nF, 80% to 20%	45			
Positive Slew Rate (STVP1, STVP2)	C_{LOAD} = 4.7nF, R_{LOAD} = 200Ω, 20% to 80%	20			V/µs
	C_{LOAD} = 4.7nF, 20% to 80%	20			
Negative Slew Rate (STVP1, STVP2)	C_{LOAD} = 4.7nF, R_{LOAD} = 200Ω, 80% to 20%	20			V/µs
	C_{LOAD} = 4.7nF, 80% to 20%	15			
INPUT LOGIC THRESHOLDS					
Input Low Voltage	CPV1, CPV2, OE, STV1, STV2			0.3 x V_{VDD}	V
	OECON			V_{DD} - 1.1	
	DISH			-1.0	
Input High Voltage	CPV1, CPV2, OE, STV1, STV2	0.7 x V_{VDD}			V
	OECON	V_{VDD} - 0.5			
OECON Input Bias Current	STV1 or STV2 = VDD, OECON = 0.4V	25			mA
DISH input Impedance	DISH = -1.5V			400	kΩ

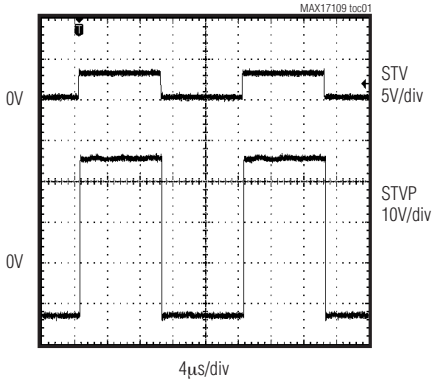
Note 1: Guaranteed by design, not production tested.

Dual, High-Voltage Scan Driver for TFT LCD

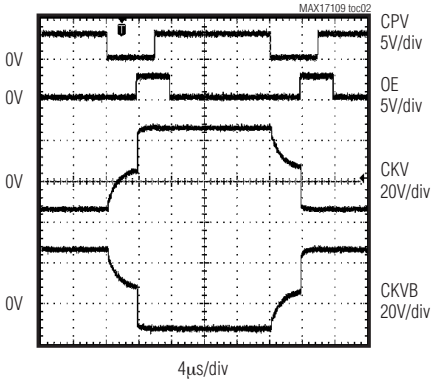
Typical Operating Characteristics

(Circuit of Figure 1, V_{IN} = 3.3V, V_{GON} = 25V, V_{GOFF} = -14V, T_A = +25°C, unless otherwise noted.)

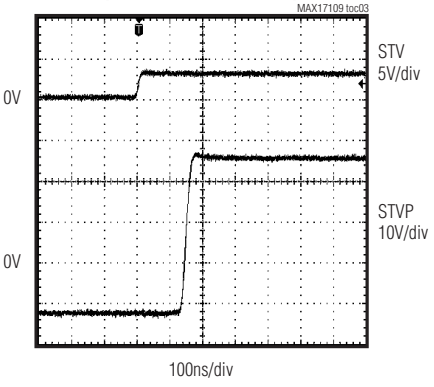
STV/STVP INPUT/OUTPUT WAVEFORMS WITH LOGIC INPUT



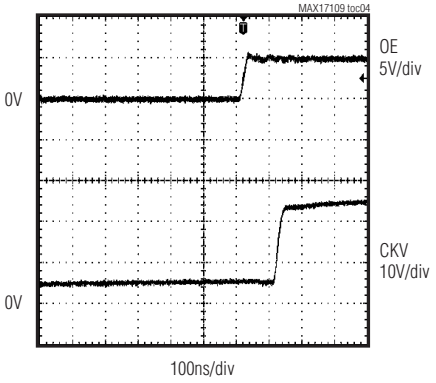
CPV AND OE/CKV AND CKVB INPUT/OUTPUT WAVEFORMS WITH LOGIC INPUT (S_{TV} = 0V, C_{LOAD} = 5.0nF, 50Ω, R_{CS} = 200Ω)



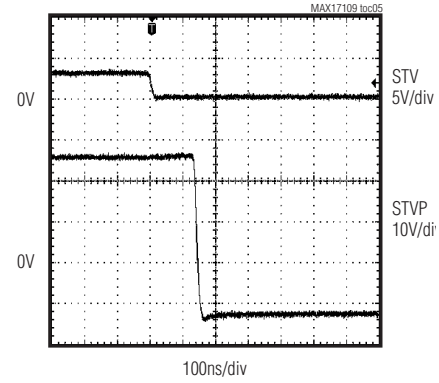
STV RISING EDGE PROPAGATION DELAY (C_{LOAD} = 5.0nF, 200Ω)



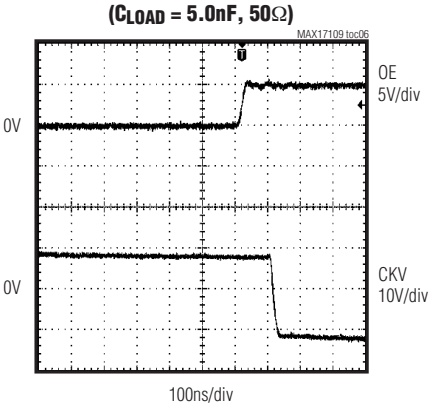
OE/CKV RISING EDGE PROPAGATION DELAY (C_{LOAD} = 5.0nF, 50Ω)



STV FALLING EDGE PROPAGATION DELAY (C_{LOAD} = 5.0nF, 200Ω)



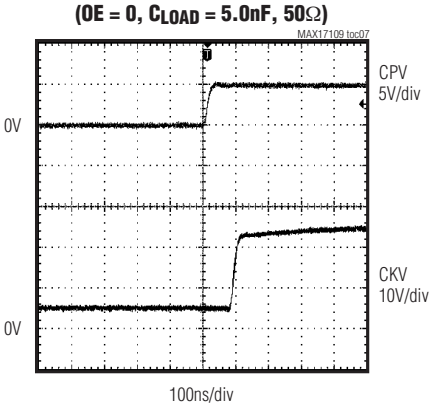
OE/CK FALLING EDGE PROPAGATION DELAY (C_{LOAD} = 5.0nF, 50Ω)



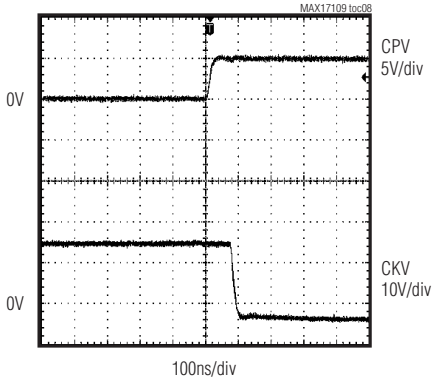
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{IN} = 3.3V, V_{GON} = 25V, V_{GOFF} = -14V, T_A = +25°C, unless otherwise noted.)

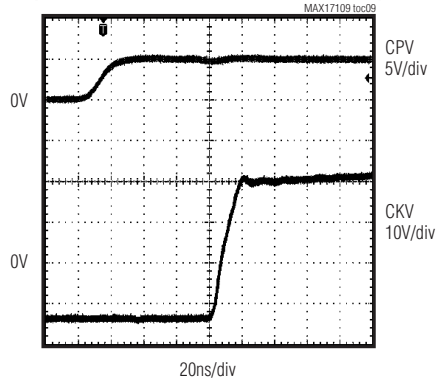
CPV/CKV RISING EDGE PROPAGATION DELAY
(OE = 0, C_{LOAD} = 5.0nF, 50Ω)



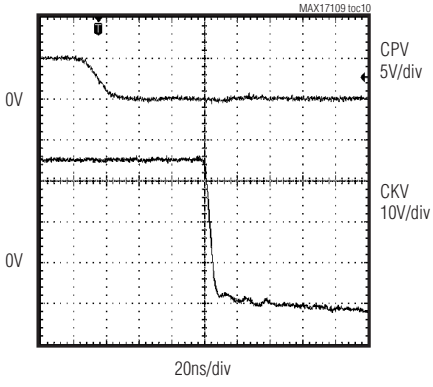
CPV/CKV FALLING EDGE PROPAGATION DELAY
(OE = 0, C_{LOAD} = 5.0nF, 50Ω)



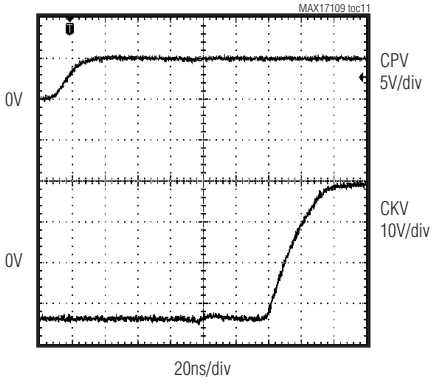
CKV SLEW RATE ON RISING EDGE
(OE = 0, STV = V_{DD}, C_{LOAD} = 5.0nF, 50Ω)



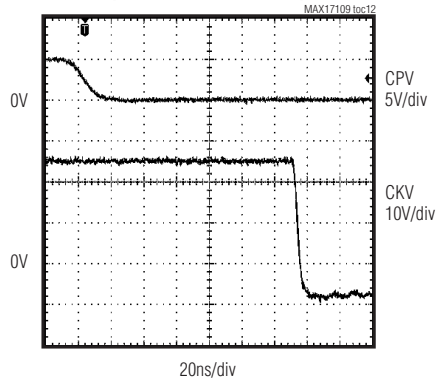
CKV SLEW RATE ON FALLING EDGE
(OE = 0, STV = V_{DD}, C_{LOAD} = 5.0nF, 50Ω)



STVP SLEW RATE ON RISING EDGE
(C_{LOAD} = 5.0nF, 200Ω)



STVP SLEW RATE ON FALLING EDGE
(C_{LOAD} = 5.0nF, 200Ω)



Dual, High-Voltage Scan Driver for TFT LCD

Pin Description

PIN	NAME	FUNCTION
1	CKVB1	High-Voltage Gate Pulse Output. CKVB1 is the inverse of CKV1 during active states and is high impedance whenever CKV1 is high impedance.
2	STVP1	High-Voltage Start Pulse Output. STVP1 is connected to GOFF when STV1 is low and is connected to GON when STV1 is high and CPV1 and OE are both low. When STV1 is high and either CPV1 or OE is high, STVP1 is high impedance.
3	STVP2	High-Voltage Start Pulse Output. STVP2 is connected to GOFF when STV2 is low and is connected to GON when STV2 is high and CPV2 and OE are both low. When STV2 is high and either CPV2 or OE is high, STVP2 is high impedance.
4	CKVB2	High-Voltage Gate Pulse Output. CKVB2 is the inverse of CKV2 during active states and is high impedance whenever CKV2 is high impedance.
5	CKVBCS2	CKVB2 Charge-Sharing Connection. CKVBCS2 connects to CKVB2 whenever CKVB2 and OE are both low or whenever CPV2 is low and OECON is high (to make CKV2 and CKVB2 float), to allow CKV2 to connect to CKVB2, sharing charge between the capacitive loads on these two outputs.
6	CKVCS2	CKV2 Charge-Sharing Connection. CKVCS2 connects to CKVB2 whenever CPV2 and OE are both low or whenever CPV2 is low and OECON is high (to make CKV2 and CKVB2 float), to allow CKVB2 to connect to CKV2, sharing charge between the capacitive loads on these two outputs.
7	CKV2	High-Voltage Gate Pulse Output. When enabled, CKV2 toggles between its high state (connected to GON) and its low state (connected to GOFF) on each falling edge of the CPV2 input. Further, CKV2 floats whenever CPV2 and OE are both low or whenever CPV2 is low and OECON is high.
8	STV1	Vertical Sync Input. The rising edge of STV1 begins a frame of data. The STV1 input is used to generate the high-voltage STVP1 output.
9	STV2	Vertical Sync Input. The rising edge of STV2 begins a frame of data. The STV2 input is used to generate the high-voltage STVP2 output.
10	CPV1	Vertical Clock Pulse Input. CPV1 controls the timing of the CKV1 and CKVB1 outputs that change state (by first sharing charge) on its falling edge.
11	CPV2	Vertical Clock Pulse Input. CPV2 controls the timing of the CKV2 and CKVB2 outputs that change state (by first sharing charge) on its falling edge.
12	OE	Active-High Gate-Pulse Output Enable. CKV_ and CKVB_ leave the floating charge-sharing state on the rising edge of OE.
13	OECON	Active-Low Output-Enable Timing Input. OECON is driven by an RC-filtered version of the OE input signal. If OE remains high long enough for the resistor to charge the capacitor up to the OECON threshold, the OE signal is masked until OE goes low and the capacitor is discharged below the threshold through the resistor.
14, 28	AGND	Ground
15	DISH	GOFF Discharge Connection. Pulling DISH below ground activates an internal connection between GOFF and AGND, rapidly discharging the GOFF supply. Typically, DISH is capacitively connected to V_{DD}, so that when V_{VDD} falls, GOFF is discharged.
16	V_{DD}	Supply Input. V_{DD} is the logic-supply input for the scan driver. Bypass to AGND through a minimum 0.1µF capacitor.
17–25, 27	N.C.	No Connection
26	GOFF	Gate-Off Supply. GOFF is the negative supply voltage for the CKV_, CKVB_, and STVP_ high-voltage driver outputs. Bypass to AGND with a minimum of 1µF ceramic capacitor.

Pin Description (continued)

PIN	NAME	FUNCTION
29	GON	Gate-On Supply. GON is the positive supply voltage for the CKV_, CKVB_, and STVP_ high-voltage driver outputs. Bypass to AGND with a minimum of 1µF ceramic capacitor.
30	CKV1	High-Voltage Gate Pulse Output. When enabled, CKV1 toggles between its high state (connected to GON) and its low state (connected to GOFF) on each falling edge of the CPV1 input. Further, CKV1 floats whenever CPV1 and OE are both low or whenever CPV1 is low and OECON is high.
31	CKVCS1	CKV1 Charge-Sharing Connection. CKVCS1 connects to CKVB1 whenever CPV1 and OE are both low or whenever CPV1 is low and OECON is high (to make CKV1 and CKVB1 float), to allow CKVB1 to connect to CKV1, sharing charge between the capacitive loads on these two outputs.
32	CKVBCS1	CKVB1 Charge-Sharing Connection. CKVBCS1 connects to CKVB1 whenever CKVB1 and OE are both low or whenever CPV1 is low and OECON is high (to make CKV1 and CKVB1 float), to allow CKV1 to connect to CKVB1, sharing charge between the capacitive loads on these two outputs.
—	EP	Exposed Pad. EP is not connected in the IC. EP should be connected to the AGND plane on the PCB to improve thermal performance.

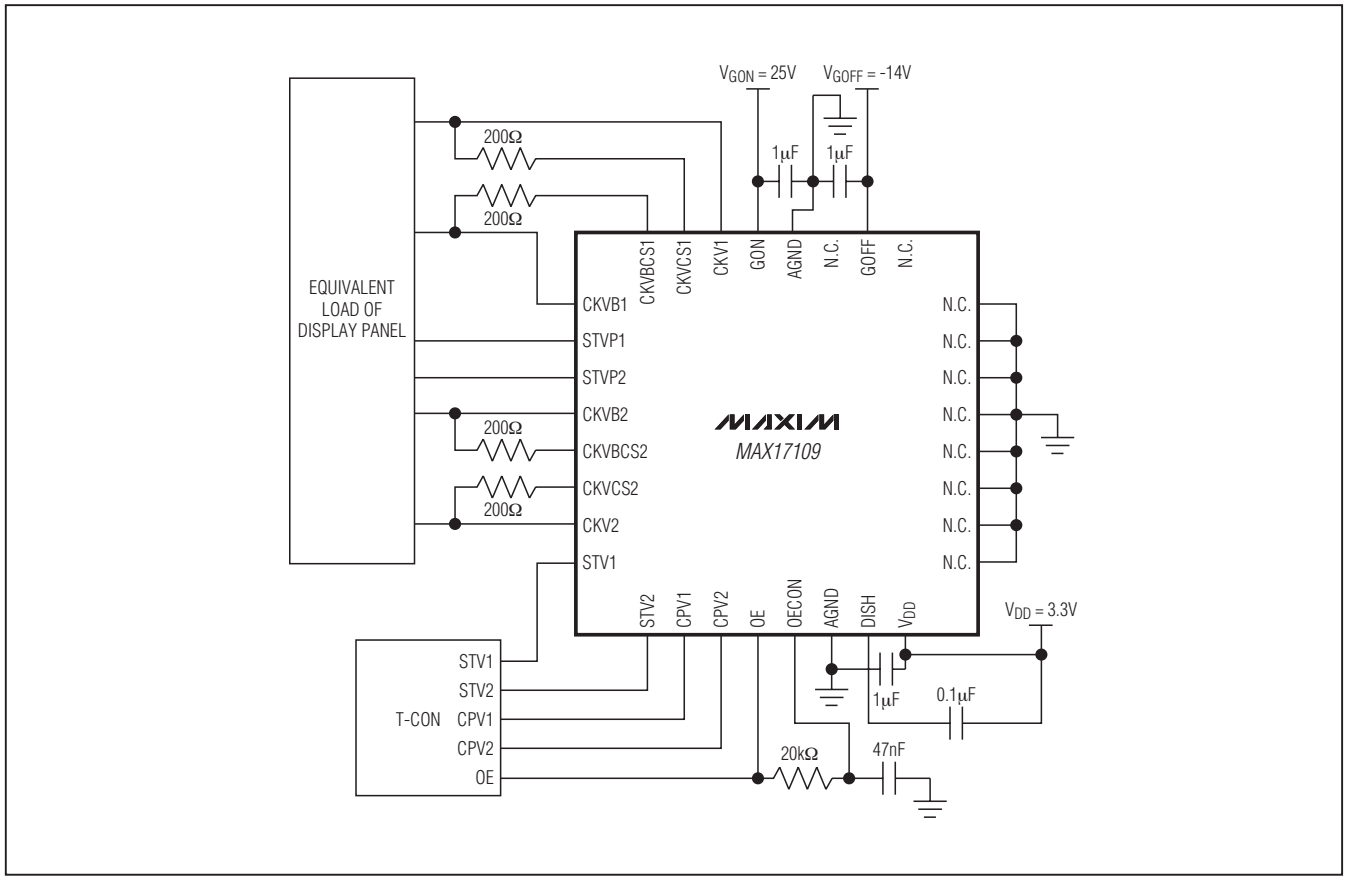


Figure 1. Typical Operating Circuit

Dual, High-Voltage Scan Driver for TFT LCD

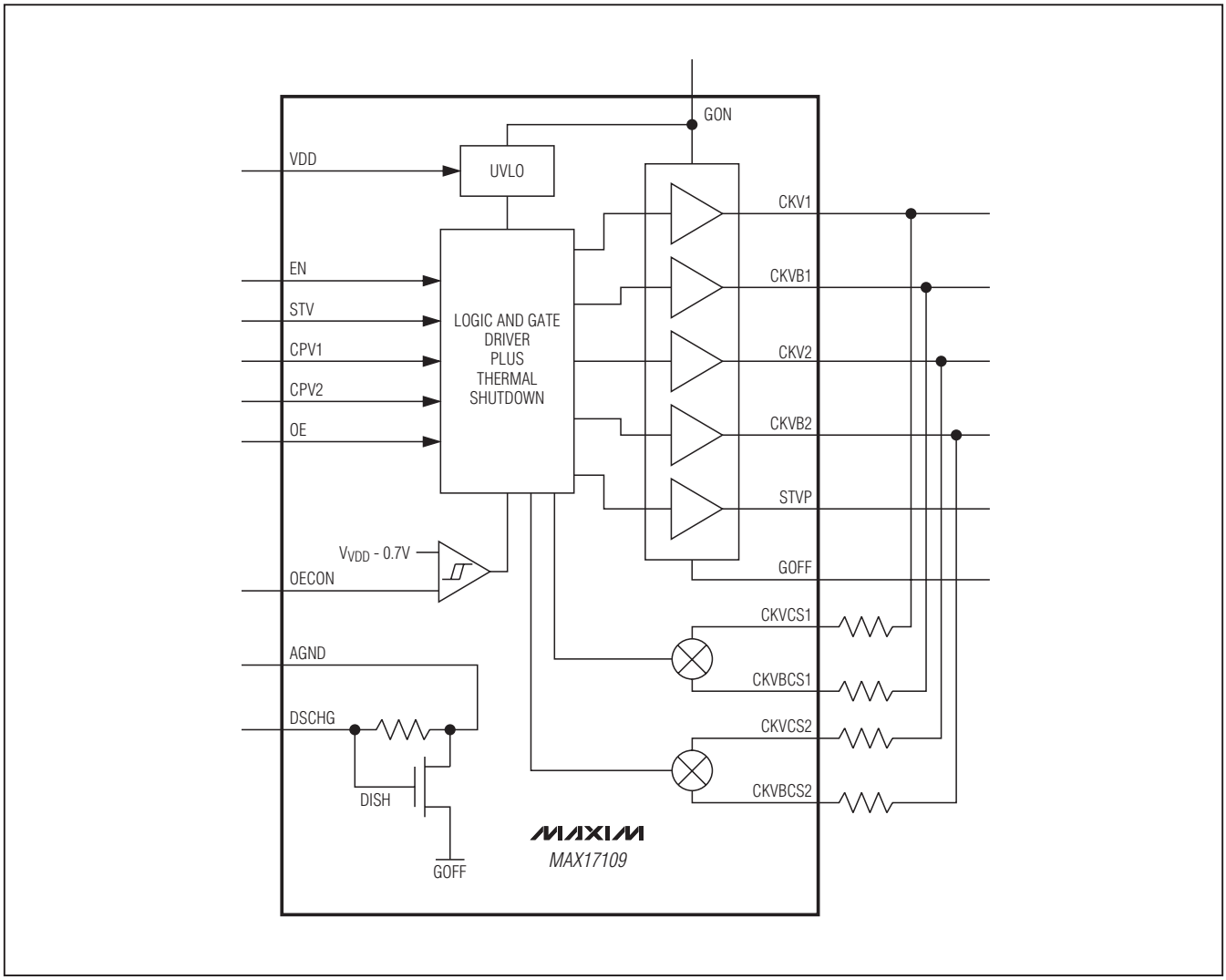


Figure 2. Functional Diagram

Detailed Description

The MAX17109 contains two high-voltage, level-shifting scan drivers for active-matrix TFT LCDs.

Undervoltage Lockout on VDD

The undervoltage lockout (VDD-UVLO) circuit on VDD compares the input voltage at VDD with the VDD-UVLO (2V, typ) to ensure that the input voltage is high enough for reliable operation. There is 50mV hysteresis to prevent supply transients from causing a restart. When the VDD voltage is below VDD-UVLO, the scan driver outputs are high impedance.

Undervoltage Lockout on GON

The undervoltage lockout (GON-UVLO) circuit on GON compares the input voltage at GON with the GON-UVLO (12V, typ) to ensure that the input voltage is high enough for reliable operation. There is 1V of hysteresis to prevent supply transients from causing a restart. When the GON voltage is below GON-UVLO, the scan driver outputs are high impedance.

High-Voltage Level-Shifting Scan Driver

The MAX17109 includes two, 3-channel, high-voltage, level-shifting scan drivers. The scan driver outputs (CKV1, CKV2, CKVB1, CKVB2, STVP1, and STVP2) swing between the power-supply rails (V_{GON} and V_{GOFF}) according to their corresponding input logic levels. The states of the CKV1, CKVB1, and STVP1 outputs are determined by the input logic levels present on OE, OECON, STV1, and CPV1. The states of the CKV2, CKVB2, and STVP2 outputs are determined by the input logic levels present on OE, OECON, STV2, and CPV2 (See Figure 3, Tables 1 and 2.)

STV1 and STV2 are the vertical timing signals. CPV1 and CPV2 are the horizontal timing signals. OE is the output-enable signal. OECON is a timing signal derived through an RC filter from OE that blanks OE if OE stays high for too long. These signals have CMOS input logic levels set by the VDD supply voltage. CKV1 and CKV2 are scan clock outputs, which are complementary to scan clock outputs CKVB1 and CKVB2, respectively. STVP1 and STVP2 are the output scan start signals. These output signals swing from V_{GON} to V_{GOFF}, which have a maximum upper level of +40V, a minimum lower level of -30V, and a combined maximum range of V_{GON} - V_{GOFF} = 65V. Their low output impedance enables them to swiftly drive capacitive loads. The input pins CKVCS1, CKVBSC1, CKVBCS2, and CKVBCS2 allow the charge in the panel equivalent capacitors to be shared. This reduces the power loss in state transition.

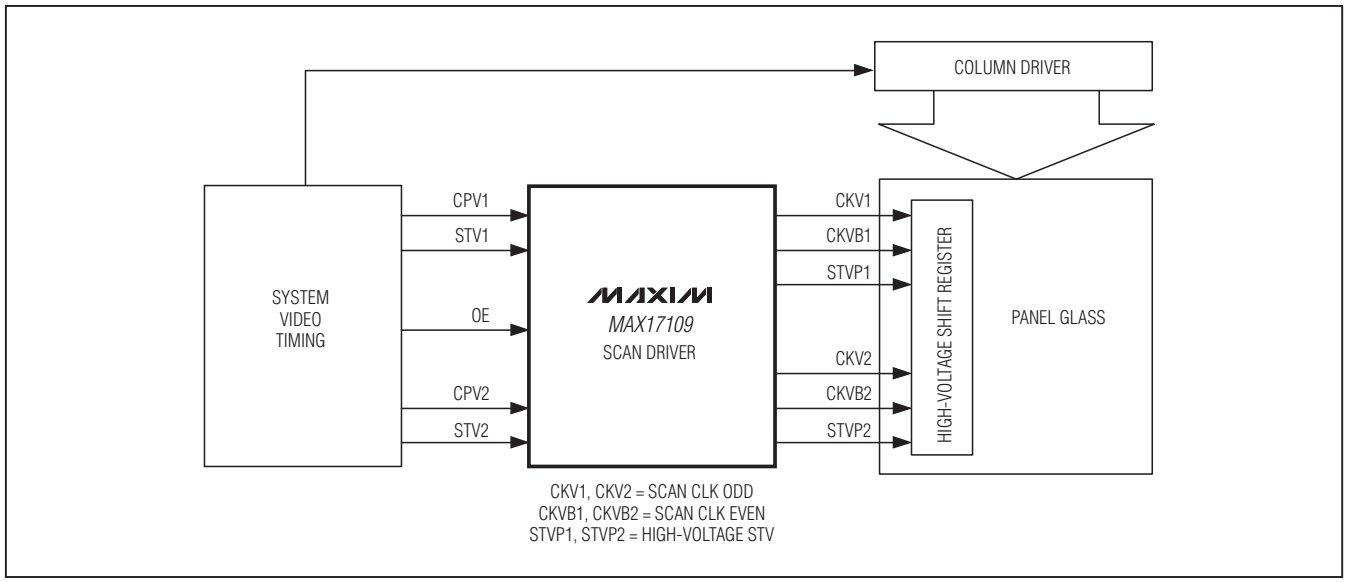


Figure 3. Scan Driver System Diagram

Table 1. STVP_ Logic

INPUT SIGNAL				OUTPUT
STV_	**OECON**	**CPV_**	**OE**	**STVP_**
H	X	L	L	H
H	X	H	X	Hi-Z
H	X	X	H	Hi-Z
L	X	X	X	L

H = High, L = Low, High-Z = High impedance, X = Don't care.

Table 2. CKV_, CKVB_ Logic

INPUT SIGNAL				OUTPUT	
STV_	**OECON**	**CPV_**	**OE**	**CKV_**	**CKVB_**
H	X	L	L	L	H
H	X	H	X	H	L
H	X	X	H	H	L
L	L	L	L	CS	CS
L	L	↑	X	Toggle	Toggle
L	L	X	↑	Toggle	Toggle
L	H	L	X	CS	CS
L	H	↑	X	Toggle	Toggle

H = High, L = Low, High-Z = High impedance, ↑ = Rising edge, X = Don't care. CS = Charge share state.

GOFF Rapid Discharge Function (DISH Input)

The DISH input controls a switch between GOFF and AGND. When DISH is pulled below ground by at least 1V, V_{GOFF} is rapidly discharged to AGND. Typically DISH is capacitively coupled to VDD so that if VDD falls suddenly, V_{GOFF} is quickly discharged to AGND.

Thermal-Overload Protection

The thermal-overload protection prevents excessive power dissipation from overheating the device. When the junction temperature exceeds T_J = +160°C, a thermal sensor immediately shuts down the scan driver outputs. The outputs are set to high impedance. Once the device cools down by approximately 15°C, the device reactivates.

The thermal-overload protection protects the IC in the event of overheat conditions. For continuous operation, do not exceed the absolute maximum junction temperature rating of T_J = +150°C.

Applications Information

Power Dissipation

An IC's maximum power dissipation depends on the thermal resistance from the die to the ambient environment and the ambient temperature. The thermal resistance depends on the IC package, PCB copper area, other thermal mass, and airflow.

The MAX17109, with its exposed backside pad soldered to 1in^2 of PCB copper, can dissipate about 34.5mW into +70°C still air. More PCB copper, cooler ambient air, and more airflow increase the possible dissipation, while less copper or warmer air decreases the IC's dissipation capability.

Scan Driver Outputs

The power dissipated by the scan driver outputs (CKV1, CKVB1, STVP1, CKV2, CKVB2, and STVP2) depends on the scan frequency, the capacitive load, and the difference between the GON and GOFF supply voltages:

$$PD_{SCAN} = 6 \times f_{SCAN} \times C_{PANEL} \times \left(V_{GON} - V_{GOFF}\right)^2$$

where f_{SCAN} is the scan frequency of the panel, C_{PANEL} is the panel model capacitive load, V_{GON} and V_{GOFF} are the positive gate-on and negative gate-off voltages.

If both scan drivers operate at a frequency of f_{SCAN} = 50kHz, the load of the six outputs is C_{PANEL} = 5nF, and the supply voltage difference is V_{GON} - V_{GOFF} = 30V, then the power dissipated is 1.35W.

PCB Layout and Grounding

Careful PCB layout is important for proper operation. Use the following guidelines for good PCB layout:

1) Place the GON, GOFF, and V_{DD} pin bypass capacitors as close as possible to the device. The ground connections of the GON, GOFF, and V_{DD} bypass capacitors should be connected directly to the AGND pin with a wide trace.
2) Avoid using vias in the high-current paths. If vias are unavoidable, use many vias in parallel to reduce resistance and inductance.
3) Connect the MAX17109's exposed paddle to AGND copper plane and the copper plane area should be maximized to improve thermal dissipation.
4) Minimize the length and maximize the width of the traces between the CKV, CKVB, and STV output nodes and the panel load for best transient responses.

Refer to the MAX17109 evaluation kit for an example of proper board layout.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
32 TQFN-EP	T3255N+1	**21-0140**

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