CMOS 4-Bit Microcontroller

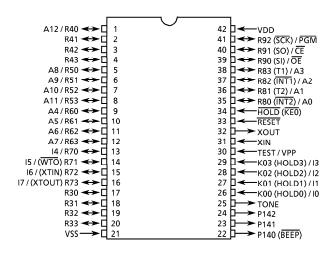
# TMP47P857VN **TMP47P857VF**

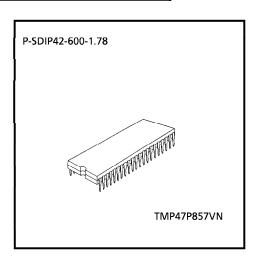
The TMP47P857V is the OTP microcontroller with 64 kbits PROM. For program operation, the programming is achieved by using with EPROM programmer (TMM2764AD type) and adapter socket (BM1120, BM1121). AC/DC characteristics are equivalent to Mask-programed ROM device.

Part No.	ROM	RAM	Package	Adapter Socket
TMP47P857VN	ОТР	10244 hit	P-SDIP42-600-1.78	BM1120
TMP47P857VF	8192 × 8-bit	1024 × 4-bit	P-QFP44-1414-0.80D	BM1121

## Pin Assignment (Top View)

P-SDIP42-600-1.78





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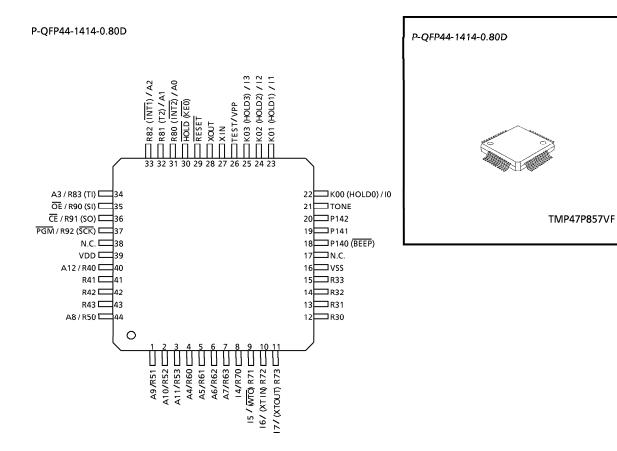
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3-57-19 2000-10-19

# Pin Assignment (Top View)



## **Pin Function**

The TMP47P857V has MCU mode and PROM mode.

(1) MCU mode
The TMP47C857V and the TMP47P857V are pin compatible (TEST pin for out-going test. Be fixed to low level).

# (2) PROM mode

Pin Name	Input/Output	Functions	Pin Name (MCU Mode)
A12			R40
A11 to A8	Input	Address inputs	R53 to R50
A7 to A4		Address riputs	R63 to R60
A3 to A0			R83 to R80
17 to 14	1/0	Data inputs / outputs	R73 to R70
13 to 10		Data Imparis / Garparis	K03 to K00
PGM		Program control input	R92
CE	Input	Chip Enable input	R91
ŌĒ		Output Enable input	R90
VPP		+ 12.5 V / 5 V (Program supply voltage)	TEST
vcc	Power supply	+5 V	VDD
VSS		ov	VSS
TONE	Output	Open	
R33 to R30	1/0	Do fived to level and	
R43 to R41	I/O	Be fixed to low level	
P142 to P140	Output	Open	
RESET	Input	DROM made setting rips. Be fived to level and	
HOLD	Input	PROM mode setting pins. Be fixed to low level.	
XIN	Input	External clock input (to keep the internal state stable)	
хоит	Output	Open	

#### **Operational Description**

The following is an explanation of hardware configuration and operation in relation to the TMP47P857V. The TMP47P857V is the same as the TMP47C457/857 except that an OTP is used instead of a Mask ROM.

#### 1. Operation Mode

The TMP47P857V has an MCU mode and a PROM mode.

#### 1.1 MCU Mode

The MCU mode is set by fixing the TEST / VPP pin at the "L" level. Operation in the MCU mode is the same as for the TMP47C457/857, except that the TEST / VPP pin does not have pull-down resistor and cannot be used open.

## 1.1.1 Program memory

The program storage area is the same as for the TMP47C857. Data conversion tables must be set in two locations when using the TMP47P857V to check TMP47C457 operation.

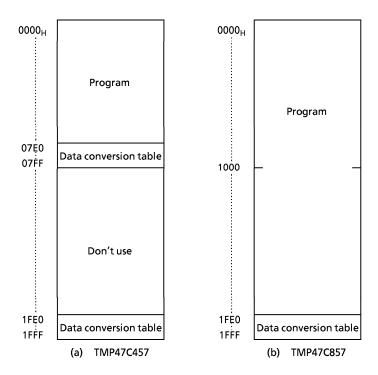


Figure 1-1. Program area

# 1.1.2 Data Memory

The TMP47P857V has 1024 × 4-bit data memory.

When using the TMP47P857V as a TMP47C457 evaluator, do not write data to address  $80_{\rm H}$  and following, even though the DMB1 addresses are  $00\text{-}FF_{\rm H}$ . There is no necessary to take into consideration a special function Shared area because one is built in DMB0.

## 1.1.3 Input/Output Circuitry

# (1) Control pins

This is the same as for the TMP47C457/857 except that there is no built-in pull-down resistance for the TEST pin.

#### (2) I/O Ports

The input/output circuit of the TMP47P857V is the same as I/O code WB of the TMP47C457/857. External resistance, for example, is required when using as evaluator of other I/O codes (WE, WH) (Refer to Figure 1-2).

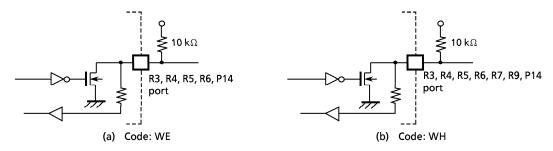


Figure 1-2. I/O code and external circuitry

#### 1.2 PROM Mode

The PROM mode is set by setting the RESET, HOLD pins to the "L" level. The PROM mode can be used as a general-purpose PROM writer for program writing and verification (A high-speed program mode is used set the ROM type the same as for the TMM2764AD).

An adapter socket (part No. BM1120/BM1121) is available for connecting a PROM writer.

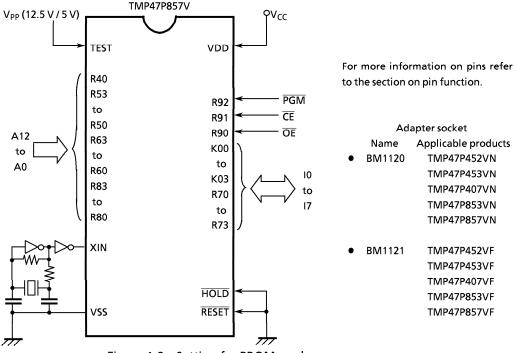


Figure 1-3. Setting for PROM mode

#### 1.2.1 Writing

Set the PROM writer ROM to TMM2764AD (64 kbit), or equivalent.

## 1.2.2 High-speed programming mode

The device is set up in the high-speed programming mode when the programming voltage (12.5 V) is applied to the Vpp terminal with Vcc = 6 V and  $\overline{PGM} = V_{IH4}$ . The programming is achieved by applying a Single TTL low level 1 ms, pulse the  $\overline{PGM}$  input after addresses and data are stable. Then the programmed data is verified by using program Verify Mode. If the programmed data is not correct, another program pulse of 1 ms is applied and then programmed data is verified. This should be repeated until the program operates correctly (max 15 times). After correctly programming the selected address, one additional program pulse with pulse width 4 times that needed for programming is applied. When programming has been completed, the data in all addresses should be verified with Vcc = Vpp = 5 V.

Start  $V_{CC} = 6 V$  $V_{pp} = 12.5 V$ Address = Start Address Yes Data = FF? No N = 0Program 1 ms Pulse N = N + 1Yes N = 15? No NG Verify? ок₹ Overprogram 4N PulseS of 1 ms or One Pulse of 4N ms Duration NG Verify? Address = Address + 1 OK. No Last Address?  $V_{CC} = \overline{5} \, \overline{V}$  $V_{pp} = 5 V$ Read NG Fail All Byte? ОК Pass Figure 1-4. Flowchart

3-57-24 2000-10-19

## **Electrical Characteristics**

Absolute Maximum Ratings  $(V_{SS} = 0 V)$ 

Parameter	Symbol	Pins	Ratings	Unit
Supply Voltage	$V_{DD}$		- 0.3 to 7	٧
Program Voltage	V <sub>PP</sub>	TEST/VPP pin	- 0.3 to 14.0	V
Input Voltage	V <sub>IN</sub>		- 0.3 to V <sub>DD</sub> + 0.3	٧
Output Voltage	V <sub>OUT1</sub>	Except sink open drain pin	- 0.3 to V <sub>DD</sub> + 0.3	
	V <sub>OUT2</sub>	Sink open drain pin	- 0.3 to 10	V
Output Current (per 1 pin)	I <sub>OUT</sub>		3.2	mA
Power Dissipation (T <sub>opr</sub> = 60°C)	PD		600	mW
Soldering Temperature (time)	T <sub>sld</sub>		260 (10 s)	°C
Storage Temperature	T <sub>stg</sub>		– 55 to 125	°C
Operating Temperature	T <sub>opr</sub>		- 30 to 60	°C

Note 1: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

Note 2: Characteristic of R7 is different from TMP47C857

**Recommended Operating Conditions** 

 $(V_{SS} = 0 \text{ V}, T_{opr} = -30 \text{ to } 60^{\circ}\text{C})$ 

Parameter	Symbol	Pins	Conditions	Min	Max	Unit
			In the Normal mode	2.7		
Supply Voltage	V <sub>DD</sub>		In the SLOW mode	2.7	6.0	V
			In the HOLD mode	2.0		
	V <sub>IH1</sub>	Except hysteresis input	V > 4.5.V	V <sub>DD</sub> × 0.7		
	V <sub>IH2</sub>	$V_{DD} \ge 4.5 \text{ N}$ Hysteresis input		V <sub>DD</sub> × 0.75 V <sub>DD</sub>		V
	V <sub>IH3</sub>		V <sub>DD</sub> < 4.5 V	V <sub>DD</sub> × 0.9		
	V <sub>IL1</sub>	Except hysteresis input	V > 4.5.V		V <sub>DD</sub> × 0.3	
Input Low Voltage	V <sub>IL2</sub>	Hysteresis input	$V_{DD} \ge 4.5 V$	0	V <sub>DD</sub> × 0.25	v
	V <sub>IL3</sub>		V <sub>DD</sub> < 4.5 V		V <sub>DD</sub> × 0.1	
	fc	XIN, XOUT		3.84	/ 1.92	MHz
Clock Frequency	fs	XTIN, XTOUT		30	34	kHz

Note: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

3-57-25 2000-10-19

**DC Characteristics** 

 $(V_{SS} = 0 \text{ V}, V_{DD} = 2.7 \text{ to } 6.0 \text{ V}, T_{opr} = -30 \text{ to } 60^{\circ}\text{C})$ 

Parameter	Symbol	Pins	Conditions	Min	Тур.	Max	Unit
Hysteresis Voltage	V <sub>HS</sub>	Hysteresis Input		_	0.7	_	V
Input Current	I <sub>IN1</sub>	Port, K0 TEST, RESET, HOLD	V <sub>DD</sub> = 5.5 V,	_	_	± 2	
input current	I <sub>IN2</sub>	Port R (open drain)	V <sub>IN</sub> = 5.5 V / 0 V	_	_	±2	μΑ
Input Low Current	I <sub>IL</sub>	Port R (push-pull)	$V_{DD} = 5.5 \text{ V}, \ V_{IN} = 0.4 \text{ V}$	_	_	- 2	mA
In cont Designation	R <sub>IN1</sub>	Port K0		30	70	150	kΩ
Input Resistance R <sub>IN2</sub>		RESET		100	220	450	K42
Output Leakage Current	I <sub>LO</sub>	Ports P, R (open drain)	V <sub>DD</sub> = 5.5 V, V <sub>OUT</sub> = 5.5 V	_	_	2	μΑ
Output High Voltage	V <sub>OH</sub>	Port R (push-pull)	$V_{DD} = 4.5 \text{ V}, I_{OH} = -200 \mu\text{A}$	2.4	_	_	<
Output Low Voltage	V <sub>OL2</sub>	Except XOUT	$V_{DD} = 4.5 \text{ V}, I_{OL} = 1.6 \text{ mA}$	_	_	0.4	V
Supply Current	I <sub>DD</sub>		Except TONE generating $V_{DD} = 5.5 V$ , fc = 3.84 MHz	_	3	6	mA
(in the Normal mode)	I <sub>DDT</sub>		TONE generating V <sub>DD</sub> = 5.5 V, fc = 3.84 MHz	_	5	10	
Supply Current (in the SLOW mode)	I <sub>DDS</sub>		$V_{DD} = 3.0 \text{ V}, \ V_{LC} = V_{SS}$ fs = 32.768 kHz	_	30	60	
Supply Current (in the HOLD mode)	I <sub>DDH</sub>		V <sub>DD</sub> = 5.5 V	_	0.5	10	μΑ

Note 1: Typ. values show those at  $T_{opr} = 25$ °C,  $V_{DD} = 5$  V

Note 2: Input Current I<sub>IN1</sub>; The current through resistor is not included, when the pull-up / pull-down resistor is

contained.

Note 3: Supply Current;  $V_{IN} = 5.3 / 0.2 \text{ V}$ 

The K0 port is opened when the pull-up/pull-down resistor is contained. The voltage applied to the R port is within the valid range  $V_{IL}$  or  $V_{IH}$ .

Note 4: Supply Current  $I_{DDS}$ ;  $V_{IN} = 2.8 \text{ V} / 0.2 \text{ V}$ , low frequency clock is only oscillated

(connecting XTIN, XTOUT).

**Tone Output Characteristics** 

 $(V_{SS} = 0 \text{ V}, V_{DD} = 2.7 \text{ to } 6.0 \text{ V}, T_{opr} = -30 \text{ to } 60^{\circ}\text{C})$ 

Parameter	Symbol	Conditions	Min	Тур.	Max	Unit
Tone Output Voltage (ROW)	V <sub>TONE</sub>	$RL \ge 10  k\Omega$ , $V_{DD} = 3.0  V$	135	200	260	mVrms
Tone Output Pre-Emphasis High Band	РЕНВ	PEHB = 20 log (COL/ROW)	1	2	3	dB
Tone Output Distortion	DIS		_	_	10	%
Tone Output Frequency Stability	Δf	Except error of osc. frequency	_	_	0.7	%

3-57-26 2000-10-19

**AC Characteristics** 

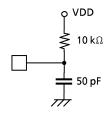
 $(V_{SS} = 0 \text{ V}, V_{DD} = 2.7 \text{ to } 6.0 \text{ V}, T_{opr} = -30 \text{ to } 60^{\circ}\text{C})$ 

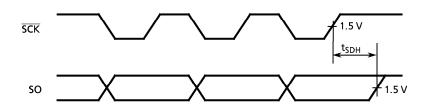
Parameter	Symbol	Conditions	Min	Тур.	Max	Unit
Instruction Code Time	_	in the Normal operating mode	2.1 / 4.2			
Instruction Cycle Time	t <sub>cy</sub>	in the SLOW operating mode	235	_	267	μS
High Level Clock Pulse Width	t <sub>WCH</sub>	For enternal closely execution	90			
Low Level Clock Pulse Width	t <sub>WCL</sub>	For external clock operation	80	_	_	ns
Shift Data Hold Time	t <sub>SDH</sub>		0.5tcy – 0.3	-	_	μs

Note: Shift Data Hold Time:

External circuit for SCK pin and SO pin

Serial port (completion of transmisson)





**Recommended Oscillating Conditions** 

 $(V_{SS} = 0 \text{ V}, V_{DD} = 2.7 \text{ to } 6.0 \text{ V}, T_{opr} = -30 \text{ to } 60^{\circ}\text{C})$ 

Recommended oscillating conditions of the TMP47P857V are equal to the TMP47C457/857.

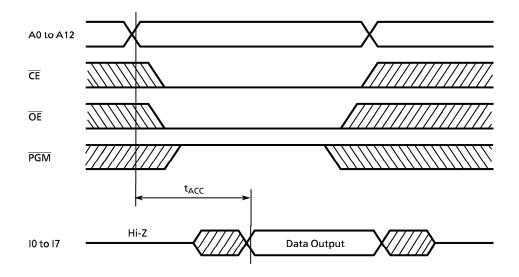
**DC/AC Characteristics** 

 $(V_{SS} = 0 V)$ 

## (1) Read Operation

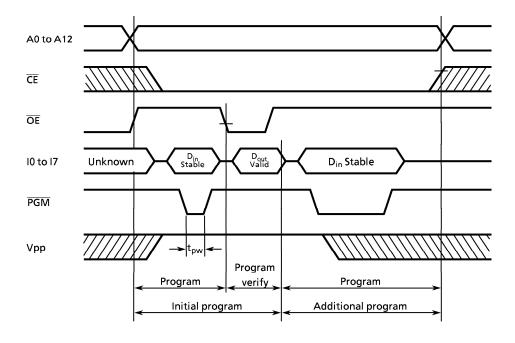
Parameter	Symbol	CONDITION	Min	Тур.	Max	Unit
Output Level High Voltage	V <sub>IH4</sub>		V <sub>CC</sub> × 0.7	-	V <sub>CC</sub>	V
Output Level Low Voltage	V <sub>IL4</sub>		0	_	V <sub>CC</sub> × 0.3	V
Supply Voltage	V <sub>CC</sub>		4.75		6.0	V
Programming Voltage	$V_{PP}$		4.73	_	0.0	V
Address Access Time	t <sub>ACC</sub>	V <sub>CC</sub> = 5.0 ± 0.25 V	-	-	350	ns

3-57-27 2000-10-19



# (2) High-Speed Programming Operation

Parameter	Symbol	Condition	Min	Тур.	Max	Unit
Input High Voltage	V <sub>IH4</sub>		V <sub>CC</sub> × 0.7	-	V <sub>CC</sub>	٧
Input Low Voltage	V <sub>IL4</sub>		0	-	$V_{CC} \times 0.3$	٧
Supply Voltage	V <sub>CC</sub>		4.75	-	6.0	٧
V <sub>PP</sub> Power Supply Voltage	V <sub>PP</sub>		12.0	12.5	13.0	٧
Programming Pulse Width	t <sub>PW</sub>	V <sub>CC</sub> = 6.0 ± 0.25 V	0.95	1.0	1.05	ms



# **Typical Characteristics**

