FEATURES
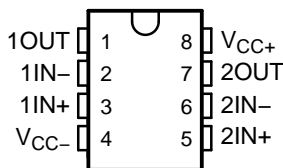
- **Operating Voltage…±2 V to ±18 V**
- **Low Offset Voltage…1 mV Max at 25°C, TL5580A**
- **Wide GBW…12 MHz Typ**
- **Slew Rate…5 V/μs Typ**
- **Low THD…0.0005% Typ**
- **Low-Noise Voltage…7 nV/√Hz at 1 kHz Typ**

APPLICATIONS

- **Audio**
- **Test Equipment**
- **Industrial Process Controls**
- **Data-Acquisition Systems**
- **Active Filters**
- **Power-Supply Regulation**

D, P, OR PW PACKAGE
(TOP VIEW)

1OUT	1	8	V_{CC+}
1IN−	2	7	2OUT
1IN+	3	6	2IN−
$V_{CC−}$	4	5	2IN+

DESCRIPTION/ORDERING INFORMATION

The TL5580 is a dual bipolar operational amplifier that combines both high dc and ac performance with its low offset voltage, high-gain bandwidth, low harmonic distortion, and low-noise characteristics. In addition, its output is capable of driving 600-Ω loads. All these characteristics make the device ideally suited for use in audio, active filtering, and industrial measurement applications.

ORDERING INFORMATION

T_A	V_{IO} (25°C, MAX)	PACKAGE[1]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	Standard grade 1.5 mV	PDIP – P	Tube of 50	TL5580IP	TL5580IP
		SOIC – D	Tube of 75	TL5580ID	Z5580
			Reel of 2500	TL5580IDR	
		TSSOP – PW	Tube of 150	TL5580IPW	Z5580
			Reel of 2000	TL5580IPWR	
	A grade 1 mV	PDIP – P	Tube of 50	TL5580AIP	TL5580AIP
		SOIC – D	Tube of 75	TL5580AID	Z5580A
			Reel of 2500	TL5580AIDR	
		TSSOP – PW	Tube of 150	TL5580AIPW	Z5580A
			Reel of 2000	TL5580AIPWR	

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.
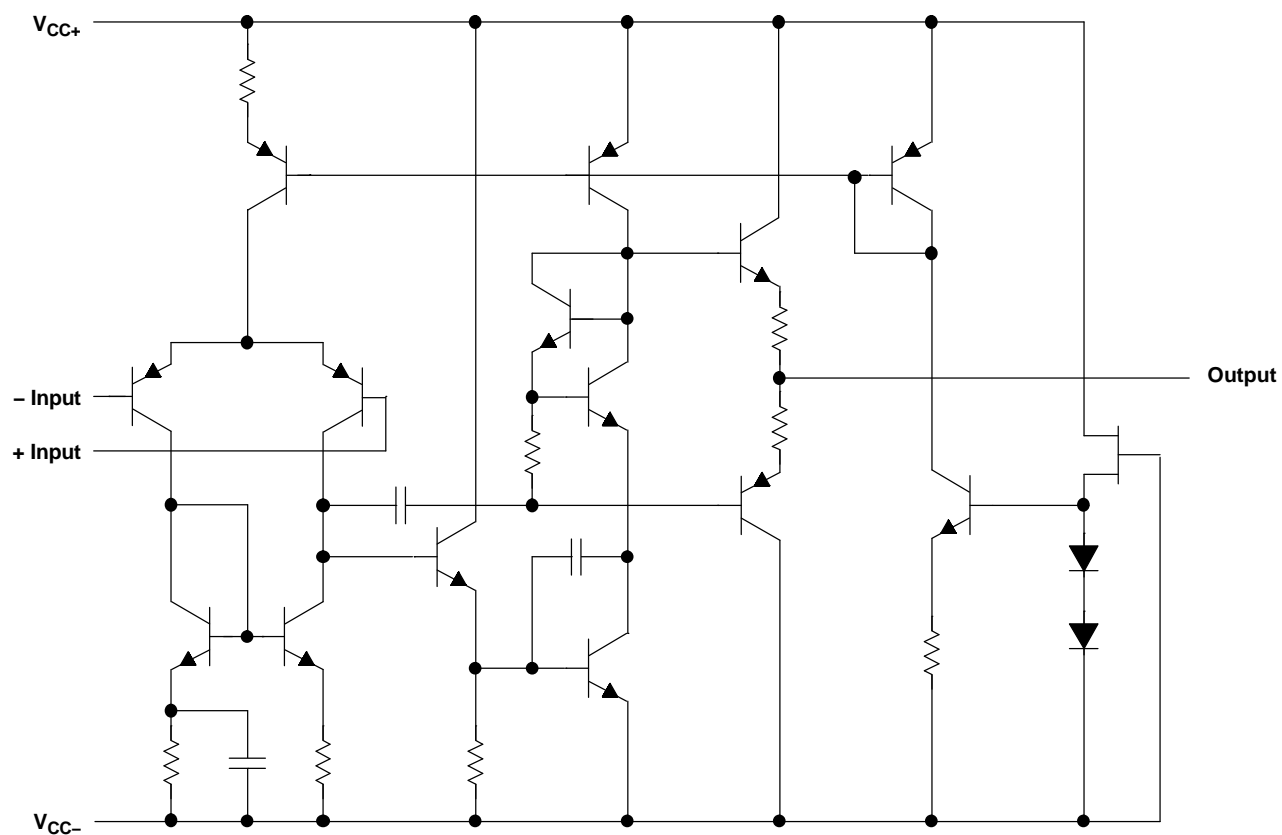
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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EQUIVALENT SCHEMATIC

DUAL LOW-NOISE WIDE-BANDWIDTH PRECISION AMPLIFIER

Absolute Maximum Ratings[1]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
$V_{CC\pm}$	Supply voltage			±18	V
V_I	Input voltage (any input)			±15	V
V_{ID}	Differential input voltage			±30	V
I_O	Output current			±50	mA
θ_{JA}	Package thermal impedance[2][3]	D package		97	°C/W
		P package		85	
		PW package		149	
T_J	Operating virtual junction temperature			150	°C
T_{stg}	Storage temperature range		−60	125	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Maximum power dissipation is a function of T_J(max), θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.

(3) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions

		MIN	MAX	UNIT
V_{CC+}	Supply voltage	2	16	V
V_{CC-}		−2	−16	
T_A	Operating free-air temperature	−40	85	°C

Electrical Characteristics

$V_{CC\pm} = \pm15$ V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TL5580A	$R_S \leq 10$ kΩ	25°C		0.3	1	mV
				−40°C to 85°C			1.35	
		TL5580		25°C		0.3	1.5	
				−40°C to 85°C			2	
αV_{IO}	Average temperature coefficient of input offset voltage			−40°C to 85°C		1.8	5	μV/°C
I_{IO}	Input offset current			25°C		5	75	nA
				−40°C to 85°C			100	
I_{IB}	Input bias current			25°C		100	500	nA
				−40°C to 85°C			800	
A_{VD}	Large-signal differential-voltage amplification		$R_L \geq 2$ kΩ, $V_O = \pm10$ V	25°C	90	110		dB
				−40°C to 85°C	87			
V_{OM}	Output voltage swing		$R_L \geq 2$ kΩ	25°C	12.75 − 12.25	±13.5		V
				−40°C to 85°C	12.5 −12			
V_{ICR}	Common-mode input voltage range			25°C	±13	±13.5		V
				−40°C to 85°C	±12			
CMRR	Common-mode rejection ratio		$R_S \leq 10$ kΩ, $V_{ICR} = -12$ V to 12 V	25°C	90	110		dB
				−40°C to 85°C	85			
k_{SVR}[1]	Supply-voltage rejection ratio		$R_S \leq 10$ kΩ	25°C	85	110		dB
				−40°C to 85°C	83			
I_{CC}	Supply current (all amplifiers)			25°C		6	9	mA
				−40°C to 85°C			12	

(1)　Measured with $V_{CC\pm}$ varied simultaneously

Operating Characteristics

$V_{CC\pm} = \pm15$ V, $T_A = 25$°C (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	TYP	UNIT
SR	Slew rate at unity gain	$R_L \geq 2$ kΩ	5	V/μs
GBW	Gain bandwidth product	f = 10 kHz	12	MHz
THD	Total harmonic distortion	$V_O = 5$ V, $R_L = 2$ kΩ, f = 1 kHz, $A_{VD} = 20$ dB	0.0005	%
V_n	Equivalent input noise voltage	f = 1 kHz	7	nV/√Hz

TYPICAL CHARACTERISTICS

MAXIMUM OUTPUT VOLTAGE SWING
vs
LOAD RESISTANCE

Figure 1.

MAXIMUM OUTPUT VOLTAGE SWING
vs
FREQUENCY

Figure 2.

OUTPUT VOLTAGE SWING
vs
OUTPUT CURRENT

Figure 3.

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY
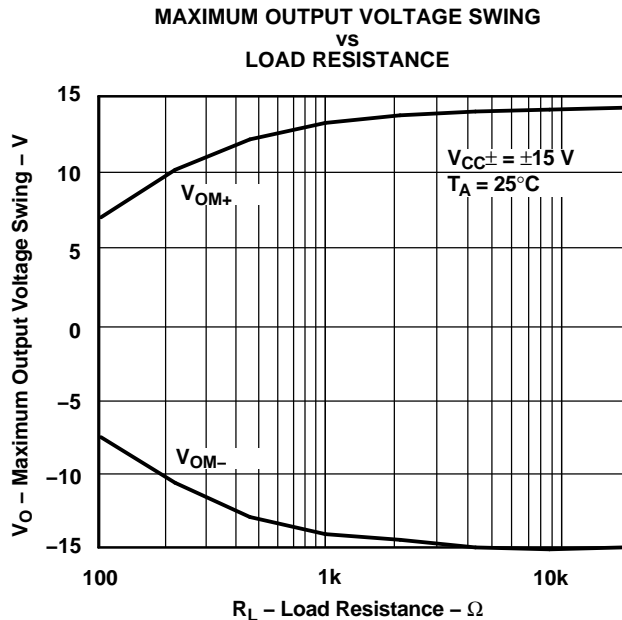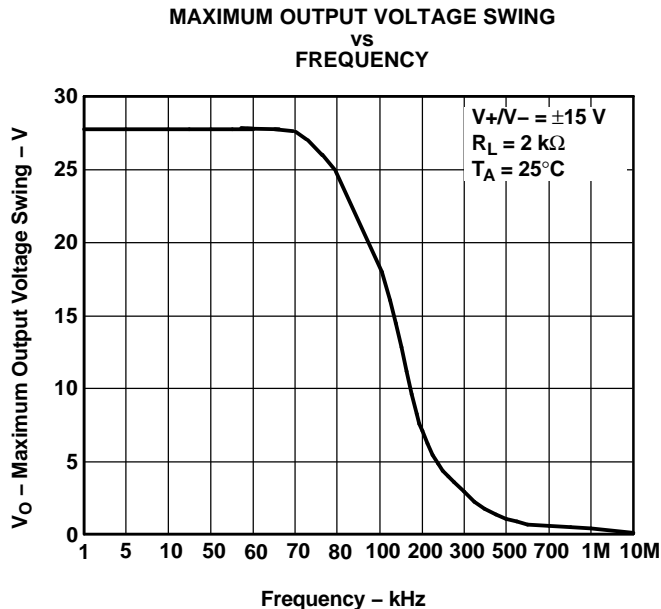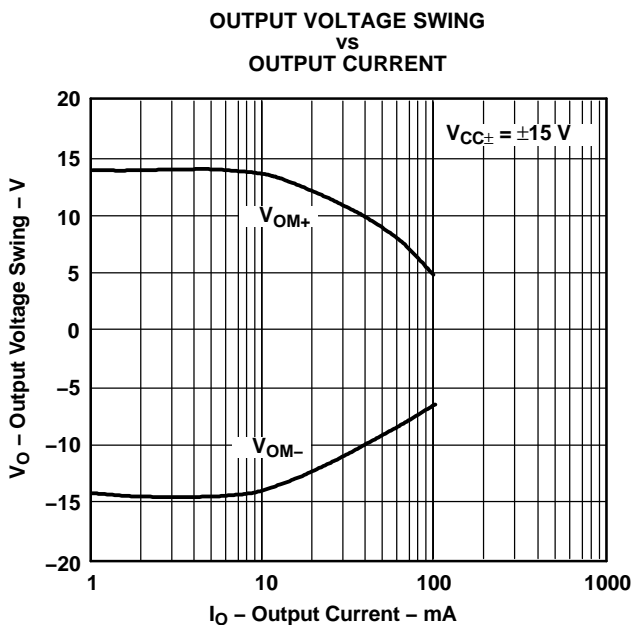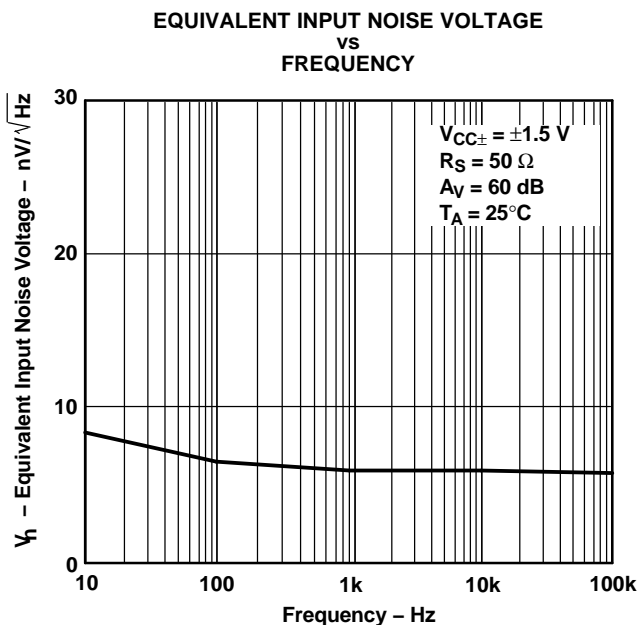
Figure 4.

TYPICAL CHARACTERISTICS (continued)

OPERATING CURRENT
vs
TEMPERATURE

Figure 5.

OUTPUT VOLTAGE SWING
vs
TEMPERATURE

Figure 6.

INPUT OFFSET VOLTAGE
vs
TEMPERATURE

Figure 7.

INPUT BIAS CURRENT
vs
TEMPERATURE
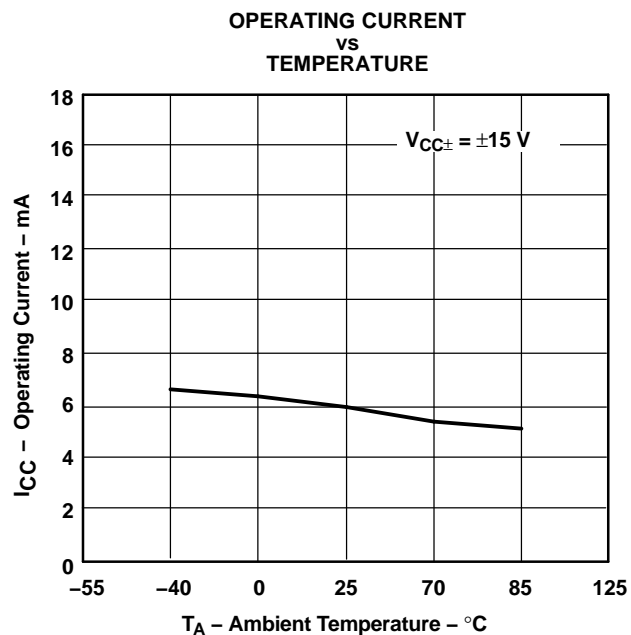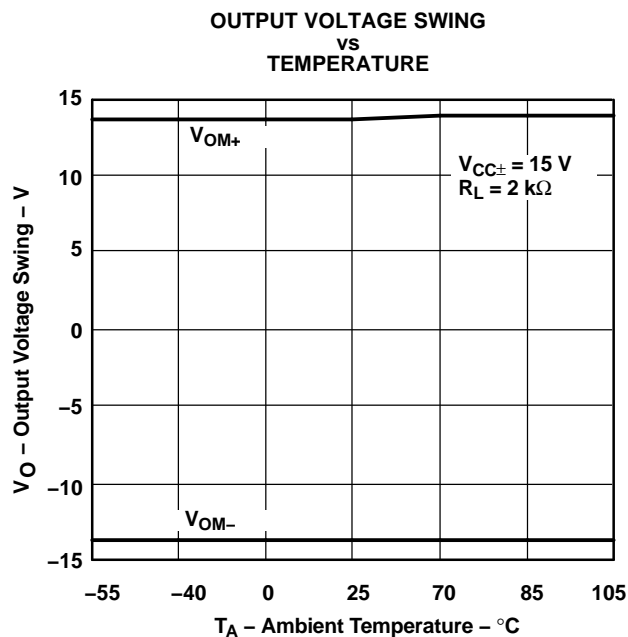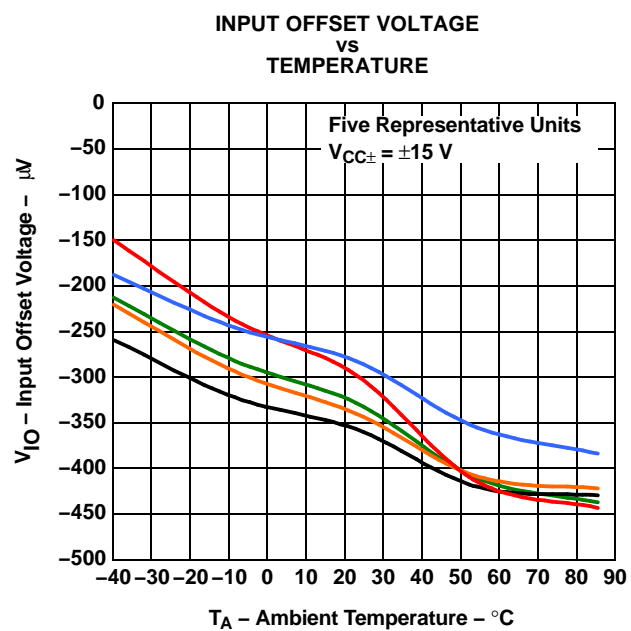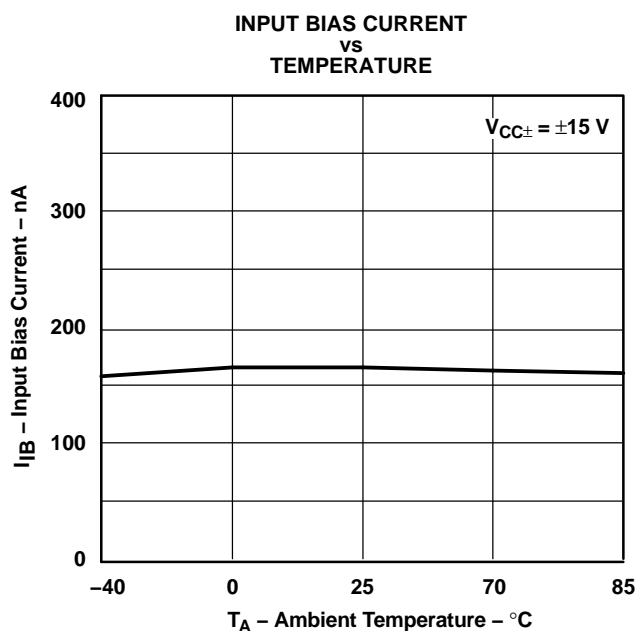
Figure 8.

TYPICAL CHARACTERISTICS (continued)

**MAXIMUM OUTPUT VOLTAGE SWING
vs
OPERATING VOLTAGE**

$T_A = 25°C$
$R_L = 2\ k\Omega$

$+V_{OM}$

$-V_{OM}$

V_O – Maximum Output Voltage Swing – V

V_{CC+}/V_{CC-} – Operating Voltage – V

Figure 9.

**OPERATING CURRENT
vs
OPERATING VOLTAGE**

$T_A = 25°C$

I_{CC} – Operating Current – mA

V_{CC+}/V_{CC-} – Operating Voltage – V

Figure 10.

**TOTAL HARMONIC DISTORTION
vs
OUTPUT VOLTAGE**

$V_{CC\pm} = \pm15\ V$
Gain = 20 dB
$R_L = 2\ k\Omega$

20 kHz

20 Hz

1 kHz

THD – Total Harmonic Distortion – %

V_O – Output Voltage – V

Figure 11.

**VOLTAGE GAIN, PHASE
vs
FREQUENCY**

$V_{CC\pm} = \pm15\ V$
$R_L = 2\ k\Omega$
40-dB Amplification
$T_A = 25°C$

Phase

Gain

Voltage Gain – dB

Phase – Deg

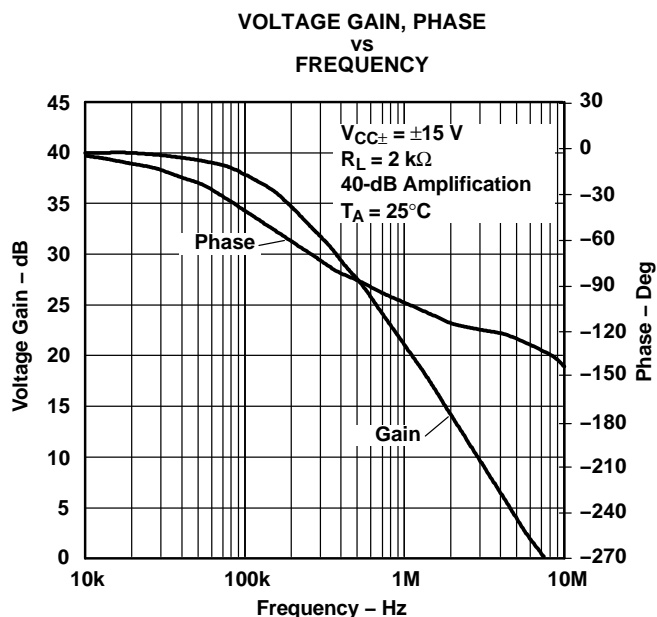Frequency – Hz

Figure 12.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL5580AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	Z5580A	Samples
TL5580AIDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	Z5580A	Samples
TL5580AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	Z5580A	Samples
TL5580AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	Z5580A	Samples
TL5580AIDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	Z5580A	Samples
TL5580AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	Z5580A	Samples
TL5580AIP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TL5580AIP	Samples
TL5580AIPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TL5580AIP	Samples
TL5580AIPWE4	ACTIVE	TSSOP	PW	8		TBD	Call TI	Call TI	-40 to 85	Z5580A	Samples
TL5580AIPWG4	OBSOLETE	TSSOP	PW	8		TBD	Call TI	Call TI	-40 to 85	Z5580A	
TL5580AIPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	Z5580A	Samples
TL5580AIPWRE4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	Z5580A	Samples
TL5580AIPWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	Z5580A	Samples
TL5580IDE4	ACTIVE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 85	Z5580	Samples
TL5580IDG4	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 85	Z5580	
TL5580IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	Z5580	Samples
TL5580IDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	Z5580	Samples
TL5580IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	Z5580	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL5580IP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TL5580IP	Samples
TL5580IPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TL5580IP	Samples
TL5580IPWE4	ACTIVE	TSSOP	PW	8		TBD	Call TI	Call TI	-40 to 85	Z5580	Samples
TL5580IPWG4	OBSOLETE	TSSOP	PW	8		TBD	Call TI	Call TI	-40 to 85	Z5580	
TL5580IPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	Z5580	Samples
TL5580IPWRE4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	Z5580	Samples
TL5580IPWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	Z5580	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL5580AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL5580AIPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TL5580IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL5580IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL5580AIDR	SOIC	D	8	2500	340.5	338.1	20.6
TL5580AIPWR	TSSOP	PW	8	2000	367.0	367.0	35.0
TL5580IDR	SOIC	D	8	2500	340.5	338.1	20.6
TL5580IPWR	TSSOP	PW	8	2000	367.0	367.0	35.0

P (R−PDIP−T8)   PLASTIC DUAL−IN−LINE PACKAGE

0.400 (10,16)
0.355 (9,02)

8   5

0.260 (6,60)
0.240 (6,10)

1   4

0.070 (1,78)
0.045 (1,14)

0.045 (1,14)
0.030 (0,76)

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53)
0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

0.325 (8,26)
0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

0.430 (10,92)
MAX

4040082/E 04/2010

NOTES: A. All linear dimensions are in inches (millimeters).
         B. This drawing is subject to change without notice.
         C. Falls within JEDEC MS−001 variation BA.

D (R−PDSO−G8)   PLASTIC SMALL OUTLINE

0.197 (5,00)
0.189 (4,80)
△C

8   5

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80) △D

Pin 1
Index Area

1   4

0.050 (1,27)   0.020 (0,51)
                      0.012 (0,31)

⊕ 0.010 (0,25) Ⓜ

0.069 (1,75) Max   0.010 (0,25)
                                0.004 (0,10)

0.010 (0,25)
0.005 (0,13)

Gauge Plane   ⌂ 0.004 (0,10)

Seating Plane

0.010 (0,25)   0°−8°

0.050 (1,27)
0.016 (0,40)

4040047−3/M   06/11

NOTES: A.   All linear dimensions are in inches (millimeters).
          B.   This drawing is subject to change without notice.
       △C   Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
               not exceed 0.006 (0,15) each side.
       △D   Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
          E.   Reference JEDEC MS−012 variation AA.

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D (R−PDSO−G8)   PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

6x1,27

5,40

Stencil Openings
(Note D)

8x0,55

8x1,50   6x1,27

5,40

Example
Non Soldermask Defined Pad

Example
Pad Geometry
(See Note C)

0,60

1,55

Example
Solder Mask Opening
(See Note E)

0,07

All Around

4211283−2/E 08/12

NOTES: A. All linear dimensions are in millimeters.
         B. This drawing is subject to change without notice.
         C. Publication IPC−7351 is recommended for alternate designs.
         D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
             contact their board assembly site for stencil design recommendations. Refer to IPC−7525 for other stencil recommendations.
         E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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PW (R−PDSO−G8)   PLASTIC SMALL OUTLINE

0,30
0,19

⊕ | 0,10 Ⓜ

0,65

8   5

⟋D⟍ 4,50   6,60
      4,30   6,20

1   4

3,10
2,90

⟋C⟍

0,15 NOM

Gage Plane

0°−8°

0,25

0,75
0,50

1,20 MAX

0,15
0,05

Seating Plane

⌓ | 0,10
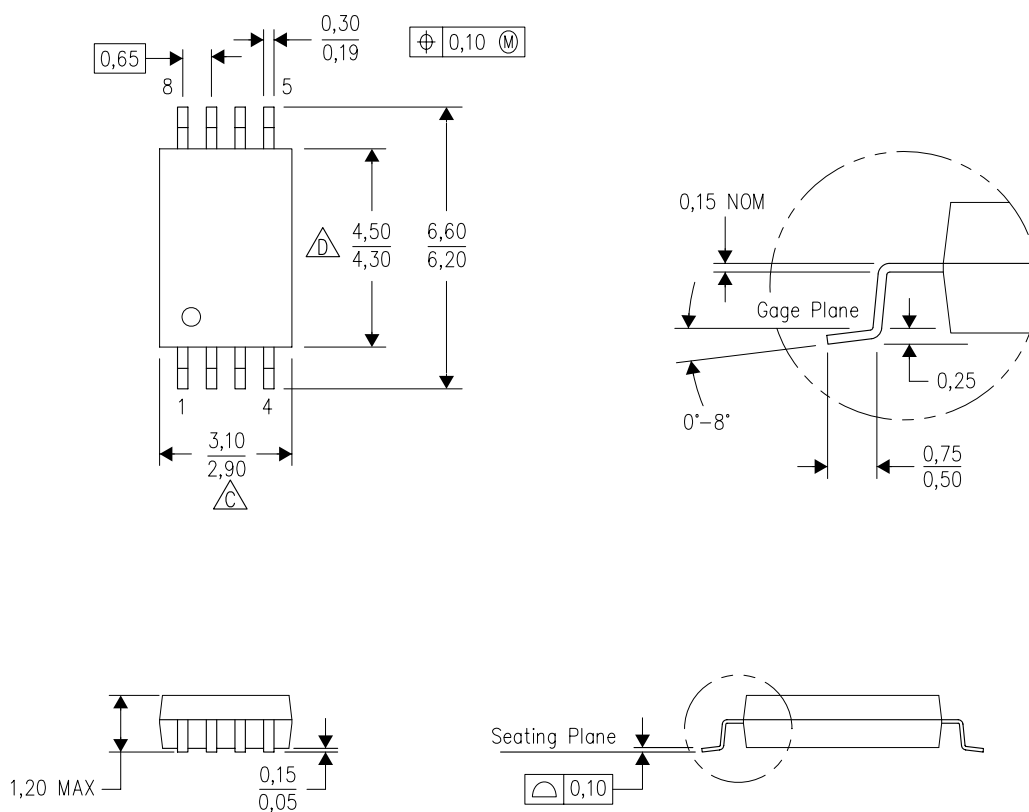
4040064−2/G   02/11

NOTES: A.   All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
          B.   This drawing is subject to change without notice.
          C.   Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
               not exceed 0,15 each side.
          D.   Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
          E.   Falls within JEDEC MO−153

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