ULTRA-SMALL PACKAGE BUILT-IN DELAY CIRCUIT HIGH-PRECISION VOLTAGE DETECTOR

S-801 Series

The S-801 Series is a series of high-precision voltage detectors with a built-in delay time generator of fixed time developed using CMOS process. The detection voltage is fixed internally, with an accuracy of ±2.0 %. Internal oscillator and counter timer can delay the release signal without external parts. Three delay times 50 ms, 100 ms, and 200 ms are available. Two output forms, Nch open-drain and CMOS output, are available.

■ Features

- Ultra-low current consumption 1.3 μA typ. (at V_{DD}=3.5 V)
- High-precision detection voltage ±2.0 %
- Hysteresis characteristics 60 mV typ.
- Detection voltage 2.2 V to 6.0 V (0.1 V step)
- Three delay times A type 50 ms typ.
  B type 100 ms typ.
  C type 200 ms typ.
- ON/OFF switching function of delay time (DS pin)
- Operating voltage range 0.95 V to 10.0 V
- Output forms Nch open-drain output (Active Low)
  CMOS output (Active Low)

■ Applications

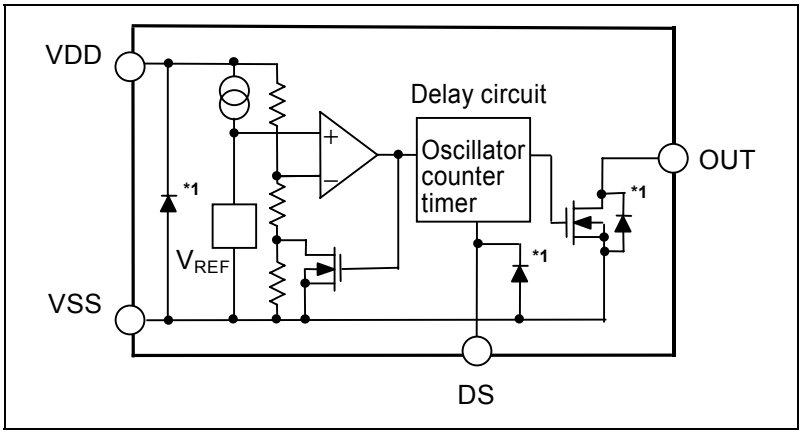
- Power monitor for portable equipment such as notebook computers, digital still cameras, PDA, and cellular phones.
- Constant voltage power monitor for cameras, video equipment and communication devices.
- Power monitor for microcomputers and reset for CPUs.

■ Packages

Package name	Drawing code		
	Package	Tape	Reel
SOT-23-5	MP005-A	MP005-A	MP005-A
SNT-4A	PF004-A	PF004-A	PF004-A

■ Block Diagrams

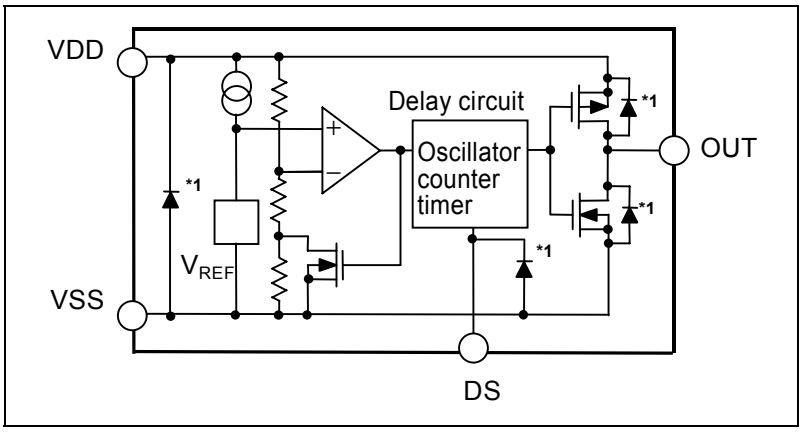
1. Nch Open-drain Output Products



***1.** Parasitic diode

Figure 1

2. CMOS Output Products



***1.** Parasitic diode

Figure 2

■ Product Name Structure

The detection voltage, delay time, output form and packages for S-801 Series can be selected at the user's request. Refer to the "**1. Product name**" for the construction of the product name and "**2. Product Name List**" for the full product names.

1. Product Name

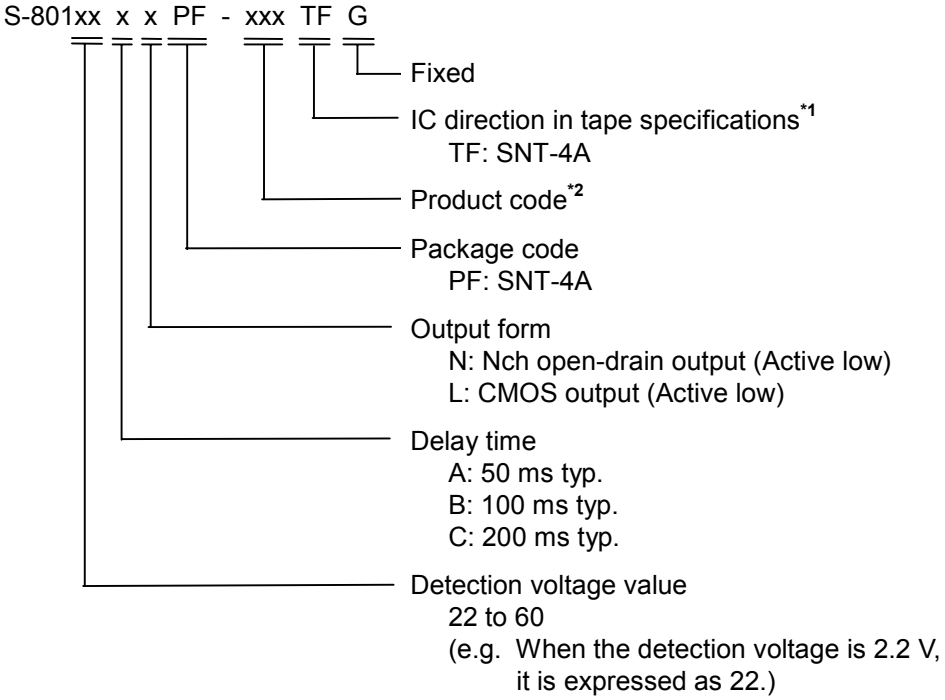
1-1. SOT-23-5 package

S-801xx x x MC - xxx - T2

- IC direction in tape specifications*1
  - T2: SOT-23-5
- Product code*2
- Package code
  - MC: SOT-23-5
- Output form
  - N: Nch open-drain output (Active low)
  - L: CMOS output (Active low)
- Delay time
  - A: 50 ms typ.
  - B: 100 ms typ.
  - C: 200 ms typ.
- Detection voltage value
  - 22 to 60
  - (e.g. When the detection voltage is 2.2 V, it is expressed as 22.)

1. Refer to the taping specifications at the end this book. T2 is the standard.
2. Refer to the **Table 1** in the "**2. Product name list**".

1-2. SNT-4A package



***1**. Refer to the taping specifications at the end this book. TF is the standard.
***2**. Refer to the **Table 2** in the "**2. Product name list**".

2. Product Name List

2-1. SOT-23-5

Table 1 (1/3)

Detection voltage range	Delay time	Nch open-drain output products	CMOS output products
2.2 V ±2.0%	50 ms typ.	S-80122ANMC-JCH-T2	S-80122ALMC-JAH-T2
	100 ms typ.	S-80122BNMC-JGH-T2	S-80122BLMC-JEH-T2
	200 ms typ.	S-80122CNMC-JKH-T2	S-80122CLMC-JIH-T2
2.3 V ±2.0%	50 ms typ.	S-80123ANMC-JCI-T2	S-80123ALMC-JAI-T2
	100 ms typ.	S-80123BNMC-JGI-T2	S-80123BLMC-JEI-T2
	200 ms typ.	S-80123CNMC-JKI-T2	S-80123CLMC-JII-T2
2.4 V ±2.0%	50 ms typ.	S-80124ANMC-JCJ-T2	S-80124ALMC-JAJ-T2
	100 ms typ.	S-80124BNMC-JGJ-T2	S-80124BLMC-JEJ-T2
	200 ms typ.	S-80124CNMC-JKJ-T2	S-80124CLMC-JIJ-T2
2.5 V ±2.0%	50 ms typ.	S-80125ANMC-JCK-T2	S-80125ALMC-JAK-T2
	100 ms typ.	S-80125BNMC-JGK-T2	S-80125BLMC-JEK-T2
	200 ms typ.	S-80125CNMC-JKK-T2	S-80125CLMC-JIK-T2
2.6 V ±2.0%	50 ms typ.	S-80126ANMC-JCL-T2	S-80126ALMC-JAL-T2
	100 ms typ.	S-80126BNMC-JGL-T2	S-80126BLMC-JEL-T2
	200 ms typ.	S-80126CNMC-JKL-T2	S-80126CLMC-JIL-T2
2.7 V ±2.0%	50 ms typ.	S-80127ANMC-JCM-T2	S-80127ALMC-JAM-T2
	100 ms typ.	S-80127BNMC-JGM-T2	S-80127BLMC-JEM-T2
	200 ms typ.	S-80127CNMC-JKM-T2	S-80127CLMC-JIM-T2
2.8 V ±2.0%	50 ms typ.	S-80128ANMC-JCN-T2	S-80128ALMC-JAN-T2
	100 ms typ.	S-80128BNMC-JGN-T2	S-80128BLMC-JEN-T2
	200 ms typ.	S-80128CNMC-JKN-T2	S-80128CLMC-JIN-T2

Table 1 (2/3)

Detection voltage range	Delay time	Nch open-drain output products	CMOS output products
2.9 V ±2.0%	50 ms typ.	S-80129ANMC-JCO-T2	S-80129ALMC-JAO-T2
	100 ms typ.	S-80129BNMC-JGO-T2	S-80129BLMC-JEO-T2
	200 ms typ.	S-80129CNMC-JKO-T2	S-80129CLMC-JIO-T2
3.0 V ±2.0%	50 ms typ.	S-80130ANMC-JCP-T2	S-80130ALMC-JAP-T2
	100 ms typ.	S-80130BNMC-JGP-T2	S-80130BLMC-JEP-T2
	200 ms typ.	S-80130CNMC-JKP-T2	S-80130CLMC-JIP-T2
3.1 V ±2.0%	50 ms typ.	S-80131ANMC-JCQ-T2	S-80131ALMC-JAQ-T2
	100 ms typ.	S-80131BNMC-JGQ-T2	S-80131BLMC-JEQ-T2
	200 ms typ.	S-80131CNMC-JKQ-T2	S-80131CLMC-JIQ-T2
3.2 V ±2.0%	50 ms typ.	S-80132ANMC-JCR-T2	S-80132ALMC-JAR-T2
	100 ms typ.	S-80132BNMC-JGR-T2	S-80132BLMC-JER-T2
	200 ms typ.	S-80132CNMC-JKR-T2	S-80132CLMC-JIR-T2
3.3 V ±2.0%	50 ms typ.	S-80133ANMC-JCS-T2	S-80133ALMC-JAS-T2
	100 ms typ.	S-80133BNMC-JGS-T2	S-80133BLMC-JES-T2
	200 ms typ.	S-80133CNMC-JKS-T2	S-80133CLMC-JIS-T2
3.4 V ±2.0%	50 ms typ.	S-80134ANMC-JCT-T2	S-80134ALMC-JAT-T2
	100 ms typ.	S-80134BNMC-JGT-T2	S-80134BLMC-JET-T2
	200 ms typ.	S-80134CNMC-JKT-T2	S-80134CLMC-JIT-T2
3.5 V ±2.0%	50 ms typ.	S-80135ANMC-JCU-T2	S-80135ALMC-JAU-T2
	100 ms typ.	S-80135BNMC-JGU-T2	S-80135BLMC-JEU-T2
	200 ms typ.	S-80135CNMC-JKU-T2	S-80135CLMC-JIU-T2
3.6 V ±2.0%	50 ms typ.	S-80136ANMC-JCV-T2	S-80136ALMC-JAV-T2
	100 ms typ.	S-80136BNMC-JGV-T2	S-80136BLMC-JEV-T2
	200 ms typ.	S-80136CNMC-JKV-T2	S-80136CLMC-JIV-T2
3.7 V ±2.0%	50 ms typ.	S-80137ANMC-JCW-T2	S-80137ALMC-JAW-T2
	100 ms typ.	S-80137BNMC-JGW-T2	S-80137BLMC-JEW-T2
	200 ms typ.	S-80137CNMC-JKW-T2	S-80137CLMC-JIW-T2
3.8 V ±2.0%	50 ms typ.	S-80138ANMC-JCX-T2	S-80138ALMC-JAX-T2
	100 ms typ.	S-80138BNMC-JGX-T2	S-80138BLMC-JEX-T2
	200 ms typ.	S-80138CNMC-JKX-T2	S-80138CLMC-JIX-T2
3.9 V ±2.0%	50 ms typ.	S-80139ANMC-JCY-T2	S-80139ALMC-JAY-T2
	100 ms typ.	S-80139BNMC-JGY-T2	S-80139BLMC-JEY-T2
	200 ms typ.	S-80139CNMC-JKY-T2	S-80139CLMC-JIY-T2
4.0 V ±2.0%	50 ms typ.	S-80140ANMC-JCZ-T2	S-80140ALMC-JAZ-T2
	100 ms typ.	S-80140BNMC-JGZ-T2	S-80140BLMC-JEZ-T2
	200 ms typ.	S-80140CNMC-JKZ-T2	S-80140CLMC-JIZ-T2
4.1 V ±2.0%	50 ms typ.	S-80141ANMC-JC2-T2	S-80141ALMC-JA2-T2
	100 ms typ.	S-80141BNMC-JG2-T2	S-80141BLMC-JE2-T2
	200 ms typ.	S-80141CNMC-JK2-T2	S-80141CLMC-JI2-T2
4.2 V ±2.0%	50 ms typ.	S-80142ANMC-JC3-T2	S-80142ALMC-JA3-T2
	100 ms typ.	S-80142BNMC-JG3-T2	S-80142BLMC-JE3-T2
	200 ms typ.	S-80142CNMC-JK3-T2	S-80142CLMC-JI3-T2
4.3 V ±2.0%	50 ms typ.	S-80143ANMC-JC4-T2	S-80143ALMC-JA4-T2
	100 ms typ.	S-80143BNMC-JG4-T2	S-80143BLMC-JE4-T2
	200 ms typ.	S-80143CNMC-JK4-T2	S-80143CLMC-JI4-T2
4.4 V ±2.0%	50 ms typ.	S-80144ANMC-JC5-T2	S-80144ALMC-JA5-T2
	100 ms typ.	S-80144BNMC-JG5-T2	S-80144BLMC-JE5-T2
	200 ms typ.	S-80144CNMC-JK5-T2	S-80144CLMC-JI5-T2

Table 1 (3/3)

Detection voltage range	Delay time	Nch open-drain output products	CMOS output products
4.5 V ±2.0%	50 ms typ.	S-80145ANMC-JC6-T2	S-80145ALMC-JA6-T2
	100 ms typ.	S-80145BNMC-JG6-T2	S-80145BLMC-JE6-T2
	200 ms typ.	S-80145CNMC-JK6-T2	S-80145CLMC-JI6-T2
4.6 V ±2.0%	50 ms typ.	S-80146ANMC-JC7-T2	S-80146ALMC-JA7-T2
	100 ms typ.	S-80146BNMC-JG7-T2	S-80146BLMC-JE7-T2
	200 ms typ.	S-80146CNMC-JK7-T2	S-80146CLMC-JI7-T2
4.7 V ±2.0%	50 ms typ.	S-80147ANMC-JC8-T2	S-80147ALMC-JA8-T2
	100 ms typ.	S-80147BNMC-JG8-T2	S-80147BLMC-JE8-T2
	200 ms typ.	S-80147CNMC-JK8-T2	S-80147CLMC-JI8-T2
4.8 V ±2.0%	50 ms typ.	S-80148ANMC-JC9-T2	S-80148ALMC-JA9-T2
	100 ms typ.	S-80148BNMC-JG9-T2	S-80148BLMC-JE9-T2
	200 ms typ.	S-80148CNMC-JK9-T2	S-80148CLMC-JI9-T2
4.9 V ±2.0%	50 ms typ.	S-80149ANMC-JDA-T2	S-80149ALMC-JBA-T2
	100 ms typ.	S-80149BNMC-JHA-T2	S-80149BLMC-JFA-T2
	200 ms typ.	S-80149CNMC-JLA-T2	S-80149CLMC-JJA-T2
5.0 V ±2.0%	50 ms typ.	S-80150ANMC-JDB-T2	S-80150ALMC-JBB-T2
	100 ms typ.	S-80150BNMC-JHB-T2	S-80150BLMC-JFB-T2
	200 ms typ.	S-80150CNMC-JLB-T2	S-80150CLMC-JJB-T2
5.1 V ±2.0%	50 ms typ.	S-80151ANMC-JDC-T2	S-80151ALMC-JBC-T2
	100 ms typ.	S-80151BNMC-JHC-T2	S-80151BLMC-JFC-T2
	200 ms typ.	S-80151CNMC-JLC-T2	S-80151CLMC-JJC-T2
5.2 V ±2.0%	50 ms typ.	S-80152ANMC-JDD-T2	S-80152ALMC-JBD-T2
	100 ms typ.	S-80152BNMC-JHD-T2	S-80152BLMC-JFD-T2
	200 ms typ.	S-80152CNMC-JLD-T2	S-80152CLMC-JJD-T2
5.3 V ±2.0%	50 ms typ.	S-80153ANMC-JDE-T2	S-80153ALMC-JBE-T2
	100 ms typ.	S-80153BNMC-JHE-T2	S-80153BLMC-JFE-T2
	200 ms typ.	S-80153CNMC-JLE-T2	S-80153CLMC-JJE-T2
5.4 V ±2.0%	50 ms typ.	S-80154ANMC-JDF-T2	S-80154ALMC-JBF-T2
	100 ms typ.	S-80154BNMC-JHF-T2	S-80154BLMC-JFF-T2
	200 ms typ.	S-80154CNMC-JLF-T2	S-80154CLMC-JJF-T2
5.5 V ±2.0%	50 ms typ.	S-80155ANMC-JDG-T2	S-80155ALMC-JBG-T2
	100 ms typ.	S-80155BNMC-JHG-T2	S-80155BLMC-JFG-T2
	200 ms typ.	S-80155CNMC-JLG-T2	S-80155CLMC-JJG-T2
5.6 V ±2.0%	50 ms typ.	S-80156ANMC-JDH-T2	S-80156ALMC-JBH-T2
	100 ms typ.	S-80156BNMC-JHH-T2	S-80156BLMC-JFH-T2
	200 ms typ.	S-80156CNMC-JLH-T2	S-80156CLMC-JJH-T2
5.7 V ±2.0%	50 ms typ.	S-80157ANMC-JDI-T2	S-80157ALMC-JBI-T2
	100 ms typ.	S-80157BNMC-JHI-T2	S-80157BLMC-JFI-T2
	200 ms typ.	S-80157CNMC-JLI-T2	S-80157CLMC-JJI-T2
5.8 V ±2.0%	50 ms typ.	S-80158ANMC-JDJ-T2	S-80158ALMC-JBJ-T2
	100 ms typ.	S-80158BNMC-JHJ-T2	S-80158BLMC-JFJ-T2
	200 ms typ.	S-80158CNMC-JLJ-T2	S-80158CLMC-JJJ-T2
5.9 V ±2.0%	50 ms typ.	S-80159ANMC-JDK-T2	S-80159ALMC-JBK-T2
	100 ms typ.	S-80159BNMC-JHK-T2	S-80159BLMC-JFK-T2
	200 ms typ.	S-80159CNMC-JLK-T2	S-80159CLMC-JJK-T2
6.0 V ±2.0%	50 ms typ.	S-80160ANMC-JDL-T2	S-80160ALMC-JBL-T2
	100 ms typ.	S-80160BNMC-JHL-T2	S-80160BLMC-JFL-T2
	200 ms typ.	S-80160CNMC-JLL-T2	S-80160CLMC-JJL-T2

2-2. SNT-4A

Table 2 (1/3)

Detection voltage range	Delay time	Nch open-drain output products	CMOS output products
2.2 V ±2.0%	50 ms typ.	S-80122ANPF-JCHTFG	S-80122ALPF-JAHTFG
	100 ms typ.	S-80122BNPF-JGHTFG	S-80122BLPF-JEHTFG
	200 ms typ.	S-80122CNPF-JKHTFG	S-80122CLPF-JIHTFG
2.3 V ±2.0%	50 ms typ.	S-80123ANPF-JCITFG	S-80123ALPF-JAITFG
	100 ms typ.	S-80123BNPF-JGITFG	S-80123BLPF-JEITFG
	200 ms typ.	S-80123CNPF-JKITFG	S-80123CLPF-JIITFG
2.4 V ±2.0%	50 ms typ.	S-80124ANPF-JCJTFG	S-80124ALPF-JAJTFG
	100 ms typ.	S-80124BNPF-JGJTFG	S-80124BLPF-JEJTFG
	200 ms typ.	S-80124CNPF-JKJTFG	S-80124CLPF-JIJTFG
2.5 V ±2.0%	50 ms typ.	S-80125ANPF-JCKTFG	S-80125ALPF-JAKTFG
	100 ms typ.	S-80125BNPF-JGKTFG	S-80125BLPF-JEKTFG
	200 ms typ.	S-80125CNPF-JKKTFG	S-80125CLPF-JIKTFG
2.6 V ±2.0%	50 ms typ.	S-80126ANPF-JCLTFG	S-80126ALPF-JALTFG
	100 ms typ.	S-80126BNPF-JGLTFG	S-80126BLPF-JELTFG
	200 ms typ.	S-80126CNPF-JKLTFG	S-80126CLPF-JILTFG
2.7 V ±2.0%	50 ms typ.	S-80127ANPF-JCMTFG	S-80127ALPF-JAMTFG
	100 ms typ.	S-80127BNPF-JGMTFG	S-80127BLPF-JEMTFG
	200 ms typ.	S-80127CNPF-JKMTFG	S-80127CLPF-JIMTFG
2.8 V ±2.0%	50 ms typ.	S-80128ANPF-JCNTFG	S-80128ALPF-JANTFG
	100 ms typ.	S-80128BNPF-JGNTFG	S-80128BLPF-JENTFG
	200 ms typ.	S-80128CNPF-JKNTFG	S-80128CLPF-JINTFG
2.9 V ±2.0%	50 ms typ.	S-80129ANPF-JCOTFG	S-80129ALPF-JAOTFG
	100 ms typ.	S-80129BNPF-JGOTFG	S-80129BLPF-JEOTFG
	200 ms typ.	S-80129CNPF-JKOTFG	S-80129CLPF-JIOTFG
3.0 V ±2.0%	50 ms typ.	S-80130ANPF-JCPTFG	S-80130ALPF-JAPTFG
	100 ms typ.	S-80130BNPF-JGPTFG	S-80130BLPF-JEPTFG
	200 ms typ.	S-80130CNPF-JKPTFG	S-80130CLPF-JIPTFG
3.1 V ±2.0%	50 ms typ.	S-80131ANPF-JCQTFG	S-80131ALPF-JAQTFG
	100 ms typ.	S-80131BNPF-JGQTFG	S-80131BLPF-JEQTFG
	200 ms typ.	S-80131CNPF-JKQTFG	S-80131CLPF-JIQTFG
3.2 V ±2.0%	50 ms typ.	S-80132ANPF-JCRTFG	S-80132ALPF-JARTFG
	100 ms typ.	S-80132BNPF-JGRTFG	S-80132BLPF-JERTFG
	200 ms typ.	S-80132CNPF-JKRTFG	S-80132CLPF-JIRTFG
3.3 V ±2.0%	50 ms typ.	S-80133ANPF-JCSTFG	S-80133ALPF-JASTFG
	100 ms typ.	S-80133BNPF-JGSTFG	S-80133BLPF-JESTFG
	200 ms typ.	S-80133CNPF-JKSTFG	S-80133CLPF-JISTFG
3.4 V ±2.0%	50 ms typ.	S-80134ANPF-JCTTFG	S-80134ALPF-JATTFG
	100 ms typ.	S-80134BNPF-JGTTFG	S-80134BLPF-JETTFG
	200 ms typ.	S-80134CNPF-JKTTFG	S-80134CLPF-JITTFG
3.5 V ±2.0%	50 ms typ.	S-80135ANPF-JCUTFG	S-80135ALPF-JAUTFG
	100 ms typ.	S-80135BNPF-JGUTFG	S-80135BLPF-JEUTFG
	200 ms typ.	S-80135CNPF-JKUTFG	S-80135CLPF-JIUTFG
3.6 V ±2.0%	50 ms typ.	S-80136ANPF-JCVTFG	S-80136ALPF-JAVTFG
	100 ms typ.	S-80136BNPF-JGVTFG	S-80136BLPF-JEVTFG
	200 ms typ.	S-80136CNPF-JKVTFG	S-80136CLPF-JIVTFG
3.7 V ±2.0%	50 ms typ.	S-80137ANPF-JCWTFG	S-80137ALPF-JAWTFG
	100 ms typ.	S-80137BNPF-JGWTFG	S-80137BLPF-JEWTFG
	200 ms typ.	S-80137CNPF-JKWTFG	S-80137CLPF-JIWTFG

Table 2 (2/3)

Detection voltage range	Delay time	Nch open-drain output products	CMOS output products
3.8 V ±2.0%	50 ms typ.	S-80138ANPF-JCXTFG	S-80138ALPF-JAXTFG
	100 ms typ.	S-80138BNPF-JGXTFG	S-80138BLPF-JEXTFG
	200 ms typ.	S-80138CNPF-JKXTFG	S-80138CLPF-JIXTFG
3.9 V ±2.0%	50 ms typ.	S-80139ANPF-JCYTFG	S-80139ALPF-JAYTFG
	100 ms typ.	S-80139BNPF-JGYTFG	S-80139BLPF-JEYTFG
	200 ms typ.	S-80139CNPF-JKYTFG	S-80139CLPF-JIYTFG
4.0 V ±2.0%	50 ms typ.	S-80140ANPF-JCZTFG	S-80140ALPF-JAZTFG
	100 ms typ.	S-80140BNPF-JGZTFG	S-80140BLPF-JEZTFG
	200 ms typ.	S-80140CNPF-JKZTFG	S-80140CLPF-JIZTFG
4.1 V ±2.0%	50 ms typ.	S-80141ANPF-JC2TFG	S-80141ALPF-JA2TFG
	100 ms typ.	S-80141BNPF-JG2TFG	S-80141BLPF-JE2TFG
	200 ms typ.	S-80141CNPF-JK2TFG	S-80141CLPF-JI2TFG
4.2 V ±2.0%	50 ms typ.	S-80142ANPF-JC3TFG	S-80142ALPF-JA3TFG
	100 ms typ.	S-80142BNPF-JG3TFG	S-80142BLPF-JE3TFG
	200 ms typ.	S-80142CNPF-JK3TFG	S-80142CLPF-JI3TFG
4.3 V ±2.0%	50 ms typ.	S-80143ANPF-JC4TFG	S-80143ALPF-JA4TFG
	100 ms typ.	S-80143BNPF-JG4TFG	S-80143BLPF-JE4TFG
	200 ms typ.	S-80143CNPF-JK4TFG	S-80143CLPF-JI4TFG
4.4 V ±2.0%	50 ms typ.	S-80144ANPF-JC5TFG	S-80144ALPF-JA5TFG
	100 ms typ.	S-80144BNPF-JG5TFG	S-80144BLPF-JE5TFG
	200 ms typ.	S-80144CNPF-JK5TFG	S-80144CLPF-JI5TFG
4.5 V ±2.0%	50 ms typ.	S-80145ANPF-JC6TFG	S-80145ALPF-JA6TFG
	100 ms typ.	S-80145BNPF-JG6TFG	S-80145BLPF-JE6TFG
	200 ms typ.	S-80145CNPF-JK6TFG	S-80145CLPF-JI6TFG
4.6 V ±2.0%	50 ms typ.	S-80146ANPF-JC7TFG	S-80146ALPF-JA7TFG
	100 ms typ.	S-80146BNPF-JG7TFG	S-80146BLPF-JE7TFG
	200 ms typ.	S-80146CNPF-JK7TFG	S-80146CLPF-JI7TFG
4.7 V ±2.0%	50 ms typ.	S-80147ANPF-JC8TFG	S-80147ALPF-JA8TFG
	100 ms typ.	S-80147BNPF-JG8TFG	S-80147BLPF-JE8TFG
	200 ms typ.	S-80147CNPF-JK8TFG	S-80147CLPF-JI8TFG
4.8 V ±2.0%	50 ms typ.	S-80148ANPF-JC9TFG	S-80148ALPF-JA9TFG
	100 ms typ.	S-80148BNPF-JG9TFG	S-80148BLPF-JE9TFG
	200 ms typ.	S-80148CNPF-JK9TFG	S-80148CLPF-JI9TFG
4.9 V ±2.0%	50 ms typ.	S-80149ANPF-JDATFG	S-80149ALPF-JBATFG
	100 ms typ.	S-80149BNPF-JHATFG	S-80149BLPF-JFATFG
	200 ms typ.	S-80149CNPF-JLATFG	S-80149CLPF-JJATFG
5.0 V ±2.0%	50 ms typ.	S-80150ANPF-JDBTFG	S-80150ALPF-JBBTFG
	100 ms typ.	S-80150BNPF-JHBTFG	S-80150BLPF-JFBTFG
	200 ms typ.	S-80150CNPF-JLBTFG	S-80150CLPF-JJBTFG
5.1 V ±2.0%	50 ms typ.	S-80151ANPF-JDCTFG	S-80151ALPF-JBCTFG
	100 ms typ.	S-80151BNPF-JHCTFG	S-80151BLPF-JFCTFG
	200 ms typ.	S-80151CNPF-JLCTFG	S-80151CLPF-JJCTFG
5.2 V ±2.0%	50 ms typ.	S-80152ANPF-JDDTFG	S-80152ALPF-JBDTFG
	100 ms typ.	S-80152BNPF-JHDTFG	S-80152BLPF-JFDTFG
	200 ms typ.	S-80152CNPF-JLDTFG	S-80152CLPF-JJDTFG
5.3 V ±2.0%	50 ms typ.	S-80153ANPF-JDETFG	S-80153ALPF-JBETFG
	100 ms typ.	S-80153BNPF-JHETFG	S-80153BLPF-JFETFG
	200 ms typ.	S-80153CNPF-JLETFG	S-80153CLPF-JJETFG

Table 2 (3/3)

Detection voltage range	Delay time	Nch open-drain output products	CMOS output products
5.4 V ±2.0%	50 ms typ.	S-80154ANPF-JDFTFG	S-80154ALPF-JBFTFG
	100 ms typ.	S-80154BNPF-JHFTFG	S-80154BLPF-JFFTFG
	200 ms typ.	S-80154CNPF-JLFTFG	S-80154CLPF-JJFTFG
5.5 V ±2.0%	50 ms typ.	S-80155ANPF-JDGTFG	S-80155ALPF-JBGTFG
	100 ms typ.	S-80155BNPF-JHGTFG	S-80155BLPF-JFGTFG
	200 ms typ.	S-80155CNPF-JLGTFG	S-80155CLPF-JJGTFG
5.6 V ±2.0%	50 ms typ.	S-80156ANPF-JDHTFG	S-80156ALPF-JBHTFG
	100 ms typ.	S-80156BNPF-JHHTFG	S-80156BLPF-JFHTFG
	200 ms typ.	S-80156CNPF-JLHTFG	S-80156CLPF-JJHTFG
5.7 V ±2.0%	50 ms typ.	S-80157ANPF-JDITFG	S-80157ALPF-JBITFG
	100 ms typ.	S-80157BNPF-JHITFG	S-80157BLPF-JFITFG
	200 ms typ.	S-80157CNPF-JLITFG	S-80157CLPF-JJITFG
5.8 V ±2.0%	50 ms typ.	S-80158ANPF-JDJTFG	S-80158ALPF-JBJTFG
	100 ms typ.	S-80158BNPF-JHJTFG	S-80158BLPF-JFJTFG
	200 ms typ.	S-80158CNPF-JLJTFG	S-80158CLPF-JJJTFG
5.9 V ±2.0%	50 ms typ.	S-80159ANPF-JDKTFG	S-80159ALPF-JBKTFG
	100 ms typ.	S-80159BNPF-JHKTFG	S-80159BLPF-JFKTFG
	200 ms typ.	S-80159CNPF-JLKTFG	S-80159CLPF-JJKTFG
6.0 V ±2.0%	50 ms typ.	S-80160ANPF-JDLTFG	S-80160ALPF-JBLTFG
	100 ms typ.	S-80160BNPF-JHLTFG	S-80160BLPF-JFLTFG
	200 ms typ.	S-80160CNPF-JLLTFG	S-80160CLPF-JJLTFG

■ Pin Configurations

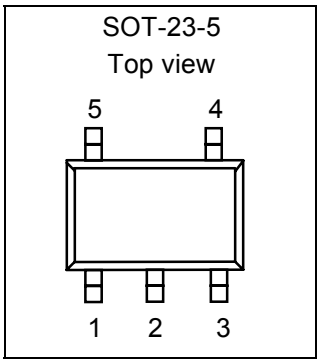


Figure 3

Table 3

Pin No.	Pin name	Pin description
1	DS*1	ON/OFF switch for delay time
2	VSS	GND pin
3	NC*2	No connection
4	OUT	Voltage detection output pin
5	VDD	Voltage input pin

***1.** Refer to "**2. Delay Circuit**" in "■ **Operation**" for operation.
***2.** The NC pin is electrically open.
The NC pin can be connected to VDD or VSS.

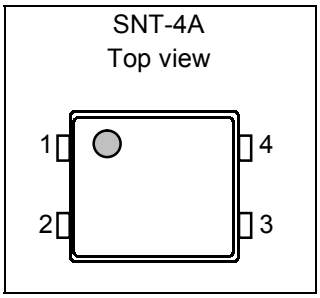


Figure 4

Table 4

Pin No.	Pin name	Pin description
1	VSS	GND pin
2	DS*1	ON/OFF switch for delay time
3	VDD	Voltage input pin
4	OUT	Voltage detection output pin

***1.** Refer to "**2. Delay Circuit**" in "■ **Operation**" for operation.

■ Absolute Maximum Ratings

Table 5

(Ta=25°C unless otherwise specified)

Item		Symbol		Absolute maximum ratings	Unit
Power supply voltage		V_{DD}–V_{SS}		12	V
Output voltage	Nch open-drain output products	V_{OUT}		V_{SS}–0.3 to V_{SS}+12	
	CMOS output products			V_{SS}–0.3 to V_{DD}+0.3	
Output current		I_{OUT}		50	mA
Power dissipation		P_D	SOT-23-5	250	mW
			SNT-4A	140	
Operating ambient temperature		Topr		–40 to +85	°C
Storage temperature		Tstg		–40 to +125	

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

■ Electrical Characteristics

Table 6

(Ta=25 °C Unless otherwise specified)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Test circuit
Detection voltage*1	$-V_{DET}$	—		$-V_{DET(S)}$ ×0.98	$-V_{DET(S)}$	$-V_{DET(S)}$ ×1.02	V	1
Hysteresis width	V_{HYS}	—		30	60	100	mV	
Current consumption	I_{SS}	V_{DD}=3.5 V	S-80122 to 26	—	1.3	3.3	μA	
		V_{DD}=4.5 V	S-80127 to 39	—	1.5	3.5		
		V_{DD}=6.5 V	S-80140 to 60	—	1.8	4.0		
Operating voltage	V_{DD}	—		0.95	—	10.0	V	
Output current	I_{OUT}	Output transistor, Nch, V_{OUT}=0.5 V	V_{DD}=1.2 V S-80122 to 60	0.75	1.5	—	mA	2
			V_{DD}=2.4 V S-80127 to 60	3.0	6.0	—		
		Only for CMOS output products, Output transistor, Pch, $V_{DD}-V_{OUT}$=0.5 V	V_{DD}=4.8 V S-80122 to 39	1.0	2.0	—		
			V_{DD}=6.0 V S-80140 to 54	1.25	2.5	—		
			V_{DD}=8.4 V S-80155 to 60	1.5	3.0	—		
Leakage current	I_{LEAK}	Only for Nch open-drain output products, Output transistor, Nch, V_{DD}=10.0 V, V_{OUT}=10.0 V		—	—	0.1	μA	
Detection voltage temperature coefficient *2	$\frac{\Delta -V_{DET}}{\Delta Ta \bullet -V_{DET}}$	Ta=−40 °C to +85 °C		—	±120	±360	ppm/ °C	1
Delay time 1	t_{D1}	$V_{DD}=-V_{DET}+1$ V, DS pin Low	S-801xxAx	32.5	50	72.5	ms	
			S-801xxBx	65	100	145		
			S-801xxCx	130	200	290		
Delay time 2	t_{D2}	$V_{DD}=-V_{DET}+1$ V, DS pin High		110	220	330	μs	3
Input voltage	V_{SH}	DS pin, V_{DD}=6.0 V		1.0	—	—	V	4
	V_{SL}	DS pin, V_{DD}=6.0 V		—	—	0.3		

***1.** $-V_{DET}$: Actual detection voltage value, $-V_{DET(S)}$: Specified detection voltage value (The center value of the detection voltage range in **Table 1 to 2**.)

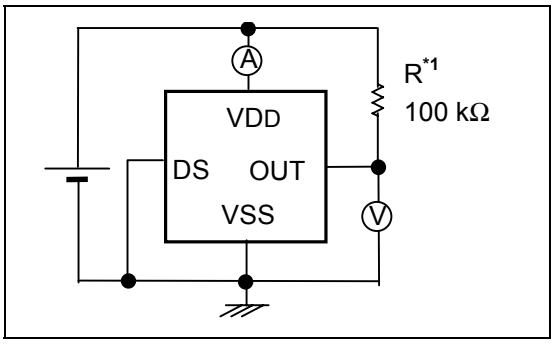
***2.** Temperature change ratio for the detection voltage [mV/°C] is calculated using the following equation.

$$\frac{\Delta -V_{DET}}{\Delta Ta}\left[mV/°C\right]^{*1} = -V_{DET(S)}(Typ.)\left[V\right]^{*2} \times \frac{\Delta -V_{DET}}{\Delta Ta \bullet -V_{DET}}\left[ppm/°C\right]^{*3} \div 1000$$

***1.** Temperature change ratio of the detection voltage
***2.** Specified detection voltage value
***3.** Detection voltage temperature coefficient

■ Test Circuits

1.



1. R is unnecessary for CMOS output products.

Figure 5

2.

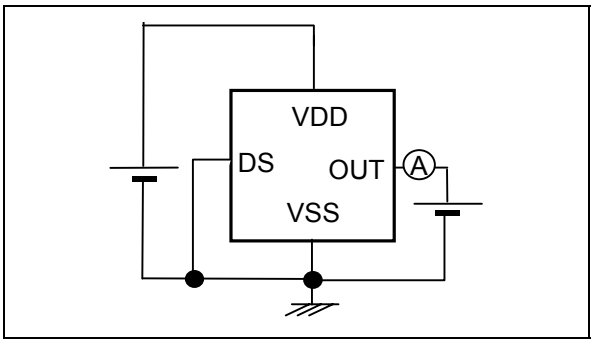
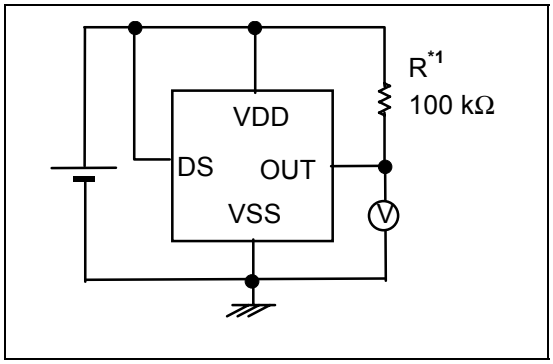


Figure 6

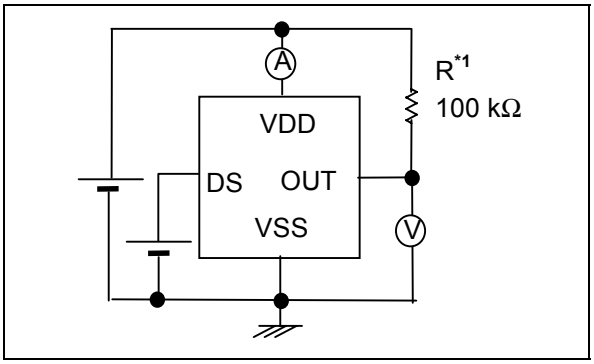
3.



1. R is unnecessary for CMOS output products.

Figure 7

4.



1. R is unnecessary for CMOS output products.

Figure 8

■ Operation

1. Basic Operation: CMOS Output (Active Low)

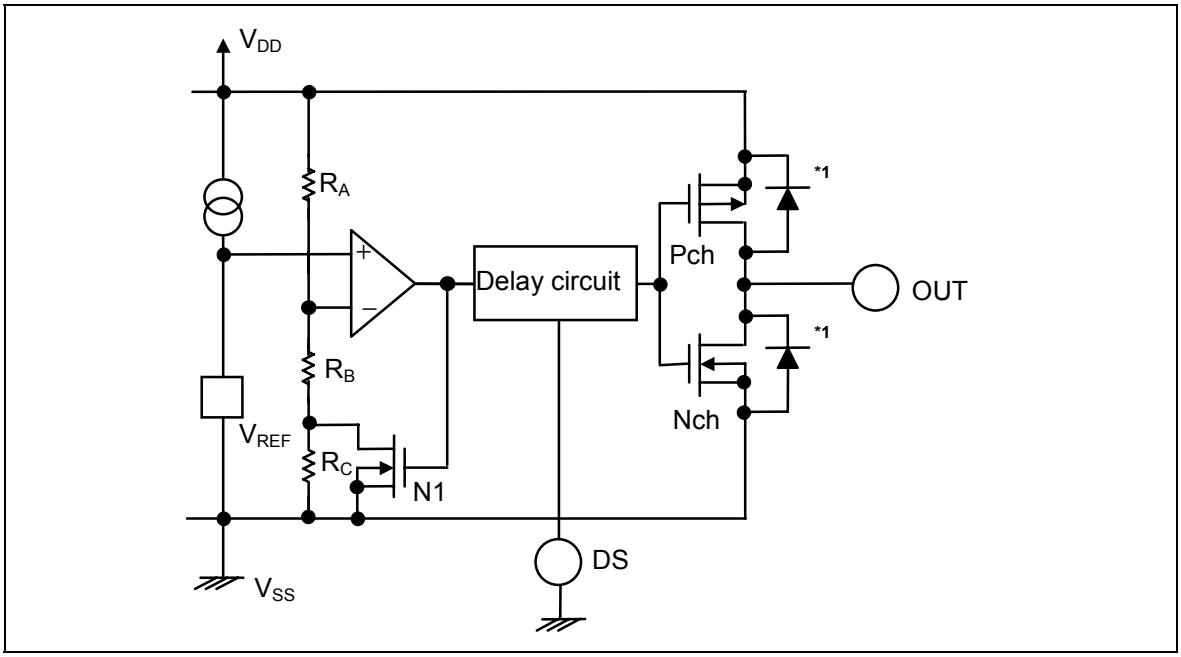
1-1. When the power supply voltage (V_{DD}) is higher than the release voltage ($+V_{DET}$), the Nch transistor is OFF and the Pch transistor is ON to provide V_{DD} (high) at the output. Since the Nch transistor N1 in **Figure 9** is OFF, the comparator input voltage is $\frac{(R_B + R_C) \bullet V_{DD}}{R_A + R_B + R_C}$.

1-2. When the V_{DD} goes below $+V_{DET}$, the output provides the V_{DD} level, as long as V_{DD} remains above the detection voltage ($-V_{DET}$). When the V_{DD} falls below $-V_{DET}$ (point A in **Figure 10**), the Nch transistor becomes ON, the Pch transistor becomes OFF, and the V_{SS} level appears at the output. At this time the Nch transistor N1 in **Figure 9** becomes ON, the comparator input voltage is changed to $\frac{R_B \bullet V_{DD}}{R_A + R_B}$.

1-3. When the V_{DD} falls below the minimum operating voltage, the output becomes undefined, or goes to V_{DD} when the output is pulled up to V_{DD}.

1-4. The V_{SS} level appears when V_{DD} rises above the minimum operating voltage. The V_{SS} level still appears even when V_{DD} surpasses the $-V_{DET}$, as long as it does not exceed the release voltage $+V_{DET}$.

1-5. When V_{DD} rises above $+V_{DET}$ (point B in **Figure 10**), the Nch transistor becomes OFF and the Pch transistor becomes ON to provide V_{DD} at the output. The V_{DD} at the OUT pin is delayed for t_D due to the delay circuit.



***1.** Paracitic diode

Figure 9 Operation 1

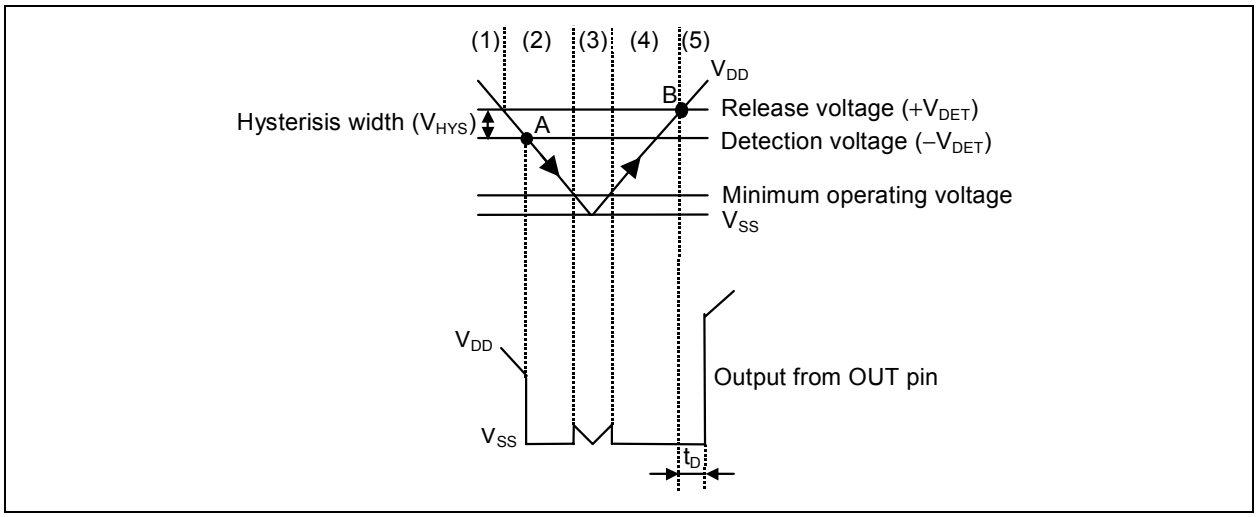


Figure 10 Operation 2

2. Delay Circuit

2-1. Delay Time

The delay circuit delays the output signal from the time at which the power voltage (V_{DD}) exceeds the release voltage ($+V_{DET}$) when V_{DD} is turned on. The output signal is not delayed when the V_{DD} goes below the detection voltage ($-V_{DET}$). (Refer to **Figure 10**.)
The delay time (t_D) is a fixed value that is determined by a built-in oscillation circuit and counter.

2-2. DS Pin (ON/OFF Switch Pin for Delay Time)

The DS pin should be connected to Low or High. When the DS pin is High, the output delay time becomes short since the output signal is taken from the middle of counter circuit (Refer to **Figure 15**).

3. Other Characteristics

3-1. Temperature Characteristics of Detection Voltage

The shaded area in **Figure 11** shows the temperature characteristics of the detection voltage.

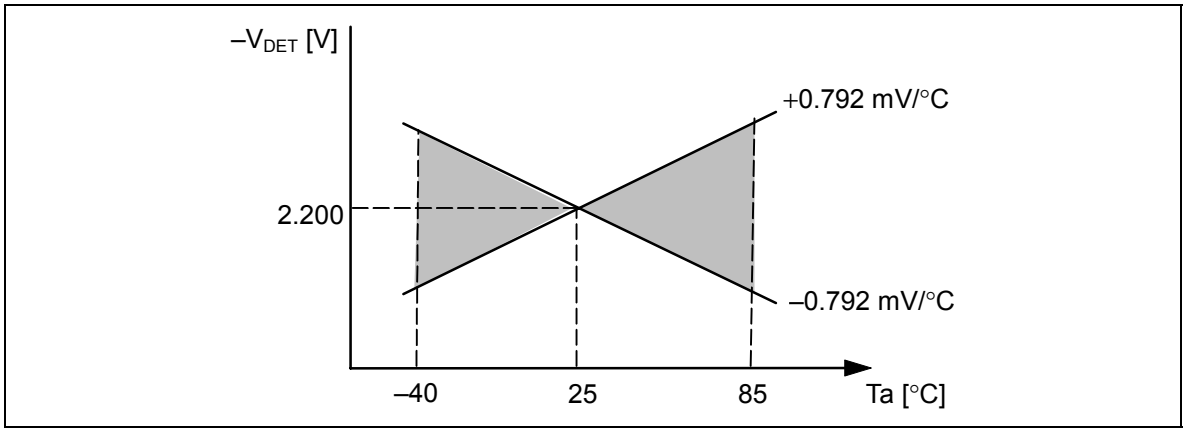


Figure 11 Temperature Characteristics of Detection Voltage (Example for S-80122xxxx)

3-2. Temperature Characteristics of Release Voltage

The temperature coefficient $\frac{\Delta + V_{DET}}{\Delta Ta}$ of the release voltage is calculated by the temperature coefficient $\frac{\Delta - V_{DET}}{\Delta Ta}$ for the detection voltage as follows:

$$\frac{\Delta + V_{DET}}{\Delta Ta} = \frac{+V_{DET}}{-V_{DET}} \times \frac{\Delta - V_{DET}}{\Delta Ta}$$

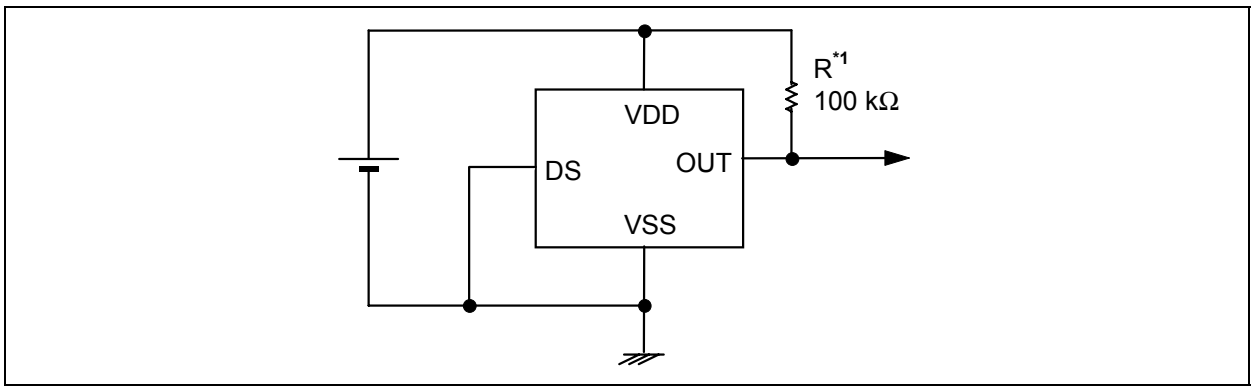
The temperature coefficients for the release voltage and the detection voltage have the same sign consequently.

3-3. Temperature Characteristics of Hysteresis Voltage

The temperature characteristics for the hysteresis voltage is expressed as $\frac{\Delta + V_{DET}}{\Delta Ta} - \frac{\Delta - V_{DET}}{\Delta Ta}$ and is calculated as follows:

$$\frac{\Delta + V_{DET}}{\Delta Ta} - \frac{\Delta - V_{DET}}{\Delta Ta} = \frac{V_{HYS}}{-V_{DET}} \times \frac{\Delta - V_{DET}}{\Delta Ta}$$

■ Standard Circuit



***1.** R is unnecessary for CMOS output products.

Figure 12

Caution The above connection diagram and constant will not guarantees successful operation. Perform through using the actual application to set the constant.

■ Technical Terms

1. Detection Voltage ($-V_{DET}$), Release Voltage ($+V_{DET}$)

The detection voltage ($-V_{DET}$) is a voltage at which the output turns to low. The detection voltage varies slightly among products of the same specification. The variation of detection voltage between the specified minimum ($-V_{DET}$) Min. and the maximum ($-V_{DET}$) Max. is called the detection voltage range (Refer to **Figure 13**).

e.g. For the S-80122AN, the detection voltage lies in the range of $2.156 \leq (-V_{DET}) \leq 2.244$.
This means that some S-80122ANs have 2.156 V for $-V_{DET}$ and some have 2.244 V.

The release voltage ($+V_{DET}$) is a voltage at which the output turns to high. The release voltage varies slightly among products of the same specification. The variation of release voltages between the specified minimum ($+V_{DET}$) Min. and the maximum ($+V_{DET}$) Max. is called the release voltage range (Refer to **Figure 14**).

e.g. For the S-80122AN, the release voltage lies in the range of $2.186 \leq (+V_{DET}) \leq 2.344$.
This means that some S-80122ANs have 2.186 V for $+V_{DET}$ and some have 2.344 V.

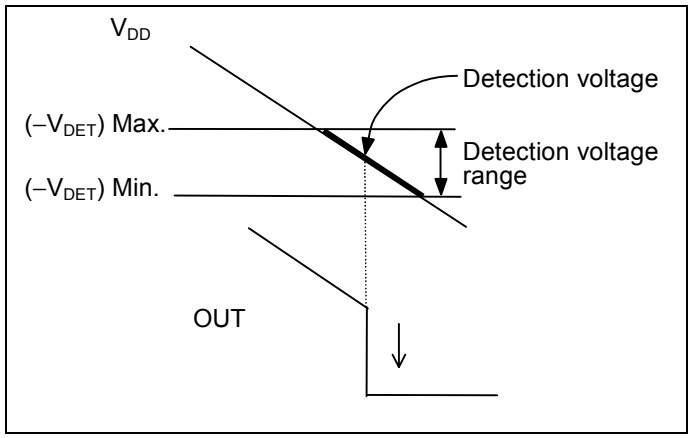


Figure 13 Detection Voltage

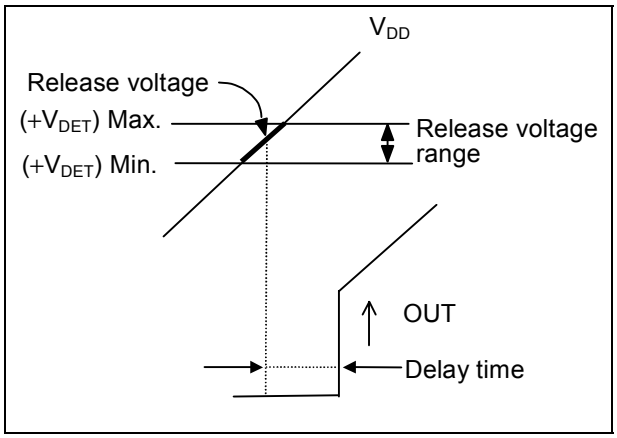


Figure 14 Release Voltage

Remark Although the detection voltage and release voltage overlap in the range of 2.186 V to 2.244 V, $+V_{DET}$ is always larger than $-V_{DET}$.

2. Hysteresis Width (V_{HYS})

Hysteresis width is the voltage difference between the detection voltage and the release voltage (The voltage at point B−The voltage at point A=V_{HYS} in **Figure 10**). The existence of the hysteresis width prevents malfunction caused by noise on input signal.

3. Delay Time (t_D)

Delay time is a time internally measured from the instant at which input voltage to the VDD pin exceeds the release voltage ($+V_{DET}$) to the point at which the output of the OUT pin inverts. The delay time is fixed in each series distinguished by A, B and C.

S-801xxAx series: typ. 50 ms
S-801xxBx series: typ. 100 ms
S-801xxCx series: typ. 200 ms

The output of the OUT pin can be inverted in a short delay time (t_{D2}) by setting the DS pin High (Refer to **Figure 15**).

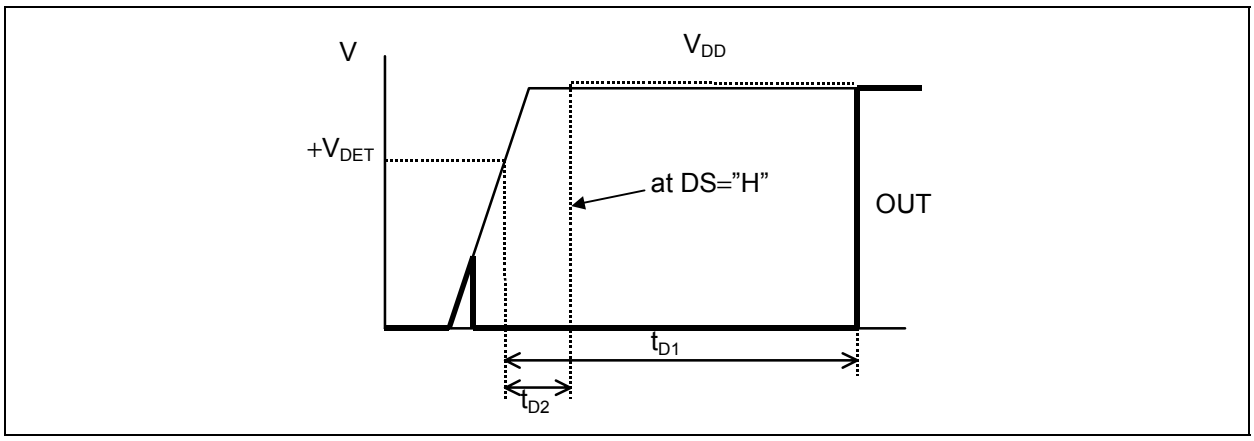


Figure 15

4. Through-type Current

The through-type current refers to the current that flows instantaneously at the time of detection and release of a voltage detector. The through-type current flows at a frequency of 20 kHz during release delay time since the internal logic circuit operates.

5. Oscillation

In applications where a resistor is connected to the voltage detector input (**Figure 16**), taking a CMOS active low products for example, the through-type current which is generated when the output goes from low to high (release) causes a voltage drop equal to [through-type current] × [input resistance] across the resistor. When the input voltage drops below the detection voltage ($-V_{DET}$) as a result, the output voltage goes to low level. In this state, the through-type current stops and its resultant voltage drop disappears, and the output goes from low to high. The through-type current is again generated, a voltage drop appears, and repeating the process finally induces oscillation.

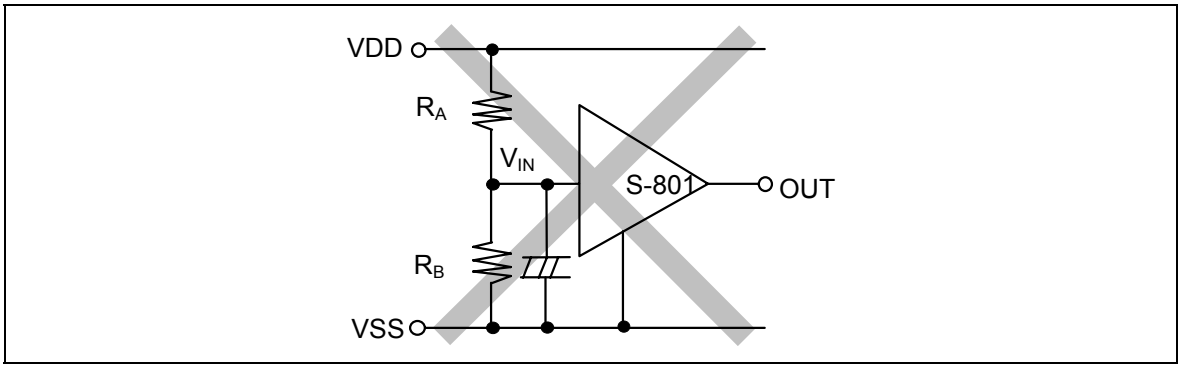


Figure 16 Example for Bad Implementation of Input Voltage Divider

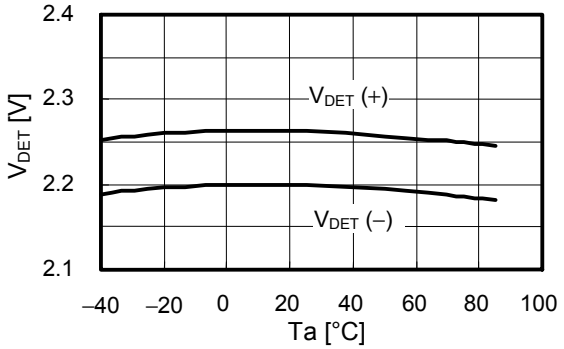
■ Precautions

- In the S-801 series products, the through-type current flows at a frequency of 20 kHz approximately during the delay time since the internal oscillator circuit and counter timer operate at voltage release. High impedance in the input may cause oscillation by the through-type current. When the input impedance is high, insert a capacitor between VDD pin and VSS pin to prevent oscillation.
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- In CMOS output products of the S-801 Series, the through-type current flows at detection and release. If the impedance is high, oscillation may occur due to the voltage drop by the through-type current during releasing.
- When designing for mass production using an application circuit described herein, the product deviation and temperature characteristics should be taken into consideration. SII shall not bear any responsibility for the patents on the circuits described herein.
- SII claims no responsibility for any and all disputes arising out of or in connection with any infringement of the products including this IC upon patents owned a third party.

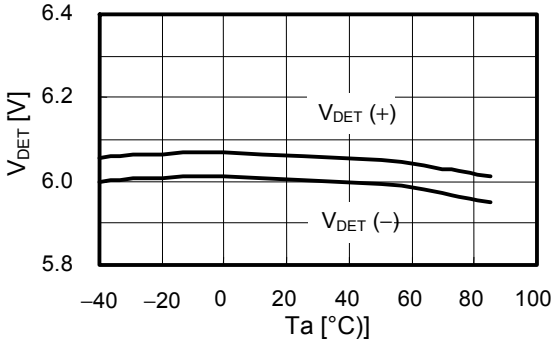
■ Typical Characteristics (Typical Data)

1. Detection Voltage (V_{DET}) - Temperature (Ta)

S-80122AL

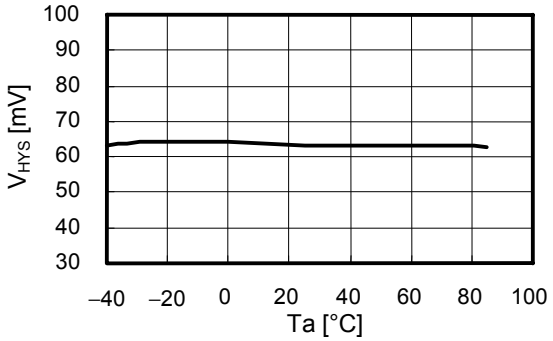


S-80160AL

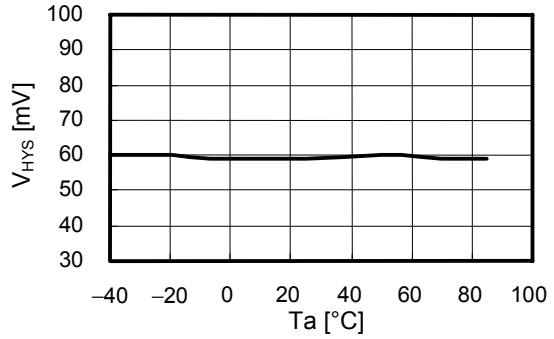


2. Hysteresis Voltage Width (V_{HYS}) - Temperature (Ta)

S-80122AL

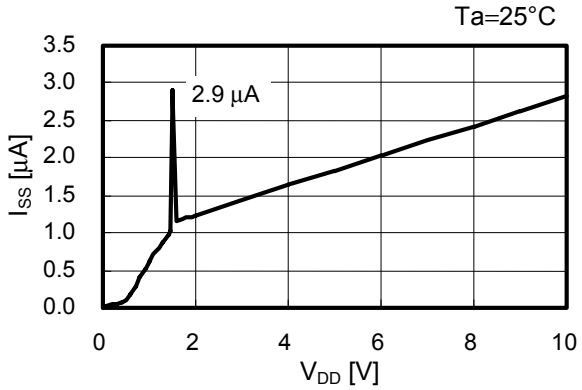


S-80160AL

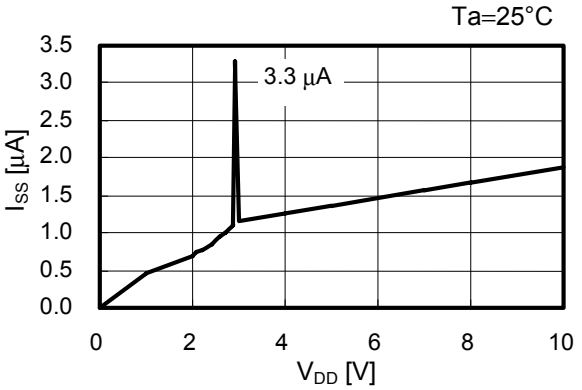


3. Current Consumption (I_{SS}) - Input Voltage (V_{DD})

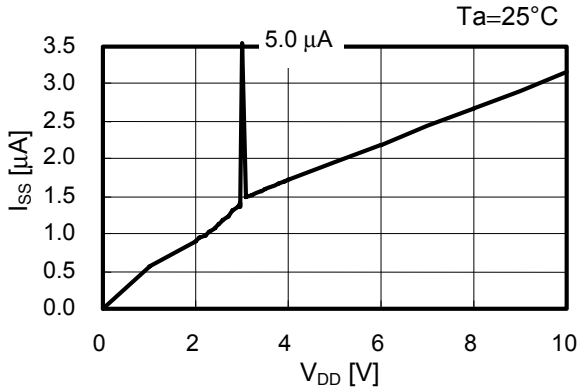
(a) S-80122AL



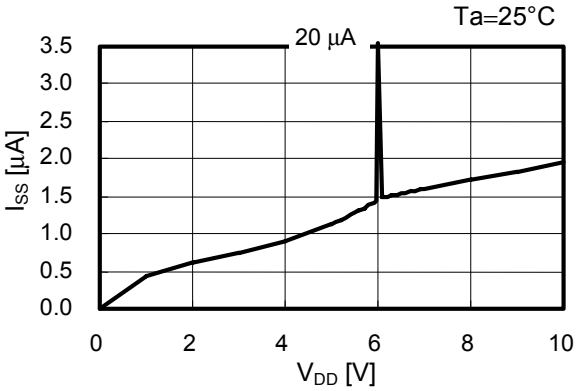
(b) S-80129AL



(c) S-80130AL

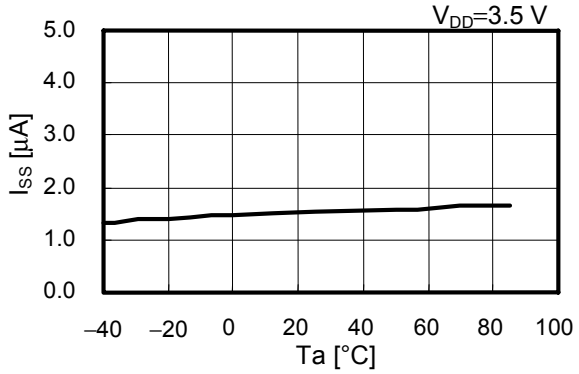


(d) S-80160AL

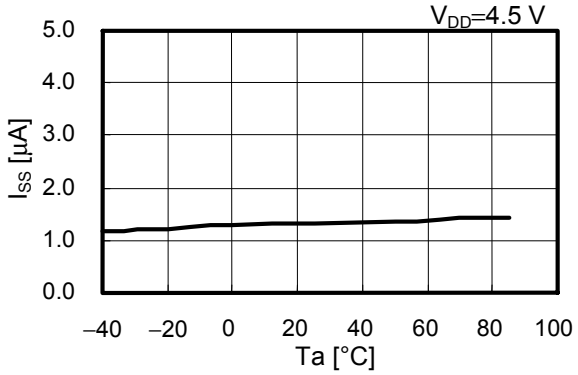


4. Current Consumption (I_{SS}) - Temperature (Ta)

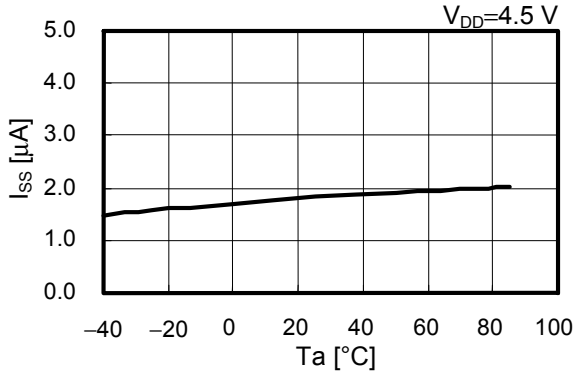
(a) S-80122AL



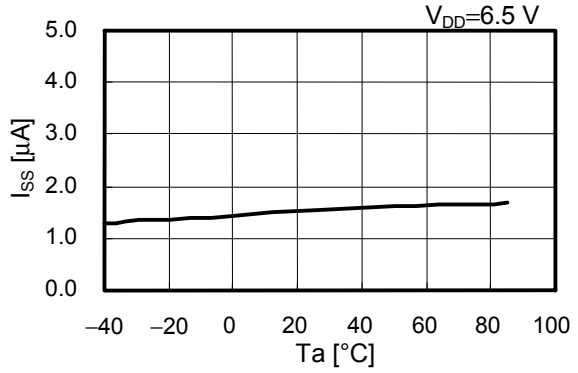
(b) S-80129AL



(c) S-80130AL

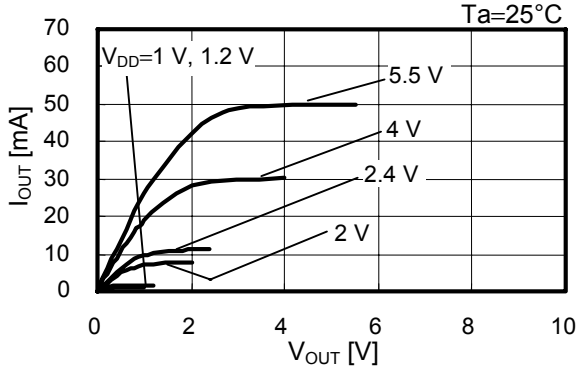


(d) S-80160AL



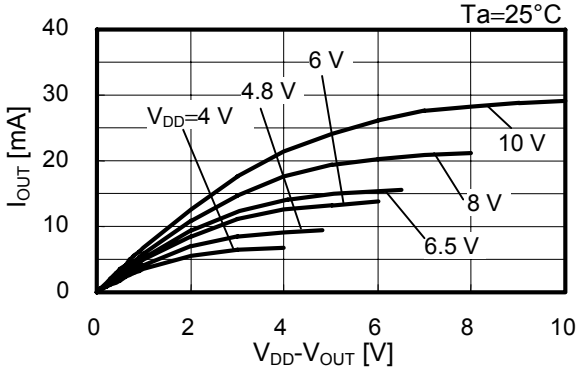
5. Nch Transistor Output Current (I_{OUT}) -V_{OUT}

S-80160AL



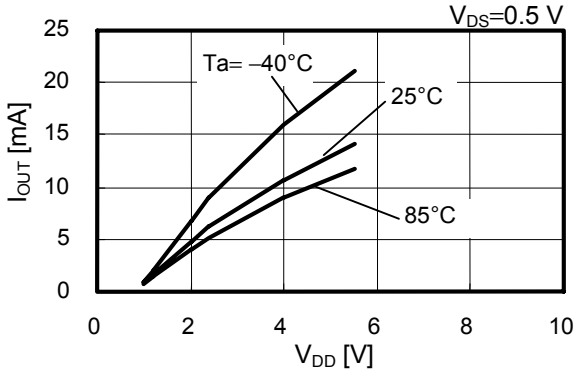
6. Pch Transistor Output Current (I_{OUT}) - (V_{DD}-V_{OUT})

S-80122AL



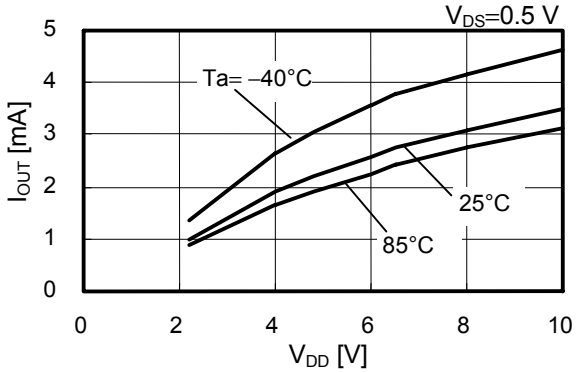
7. Nch Transistor Output Current (I_{OUT}) - Input Voltage (V_{DD})

S-80160AL



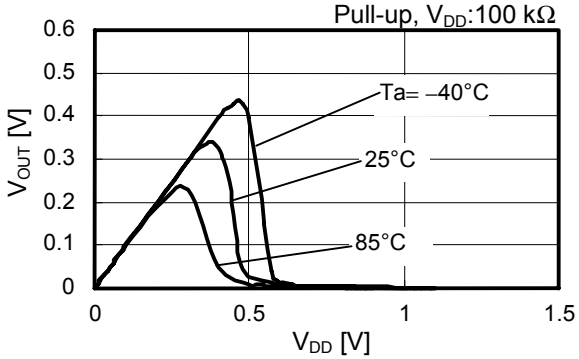
8. Pch transistor Output Current (I_{OUT}) - Input Voltage (V_{DD})

S-80122AL



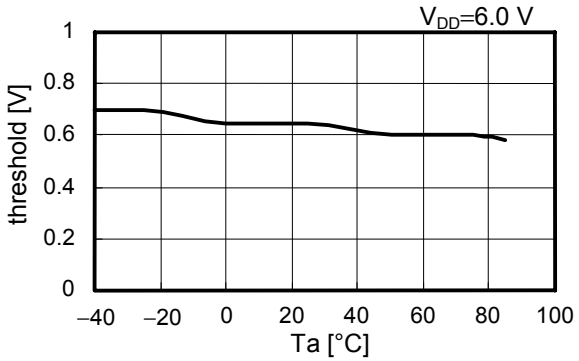
9. Minimum Operating Voltage - Input Voltage (V_{DD})

S-80122AN



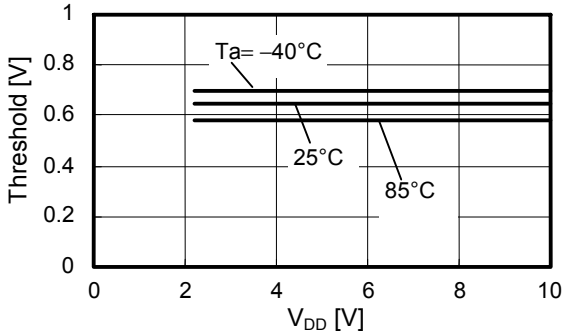
10. Threshold Voltage of DS Pin - Temperature (Ta)

S-80122AL



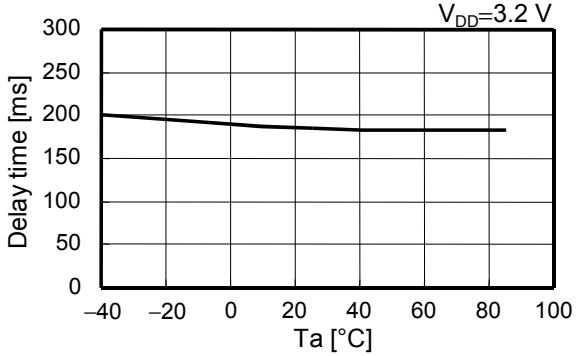
11. Threshold Voltage of DS Pin - Input Voltage (V_{DD})

S-80122AL

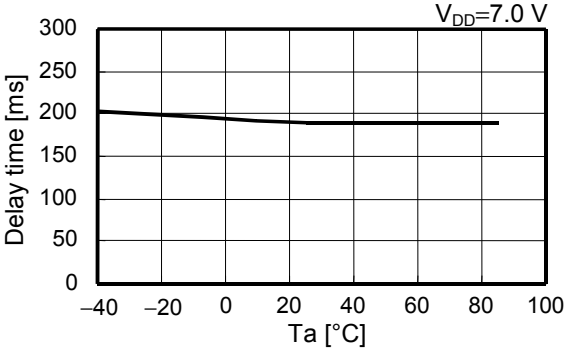


12. Delay Time 1 - Temperature (Ta)

S-80122CL

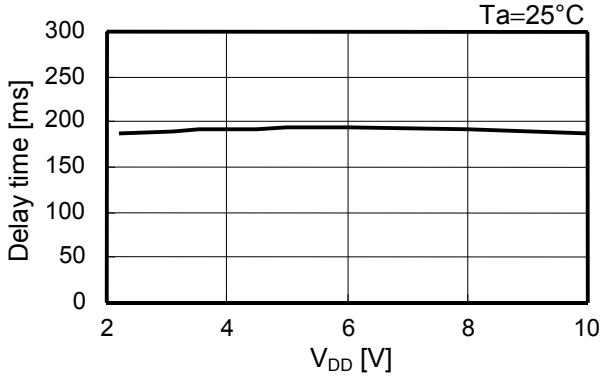


S-80160CL



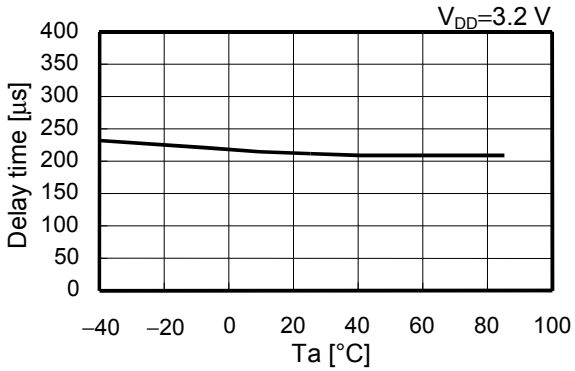
13. Delay Time 1 - Input Voltage (V_{DD})

S-80122CL

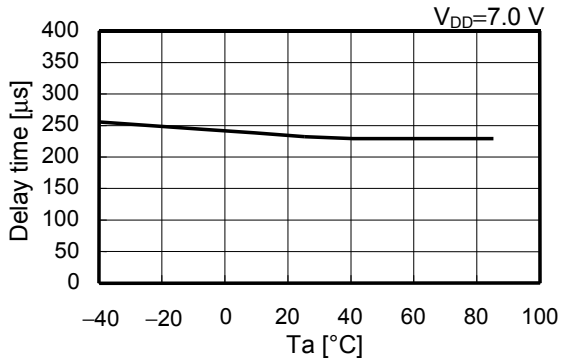


14. Delay Time 2 - Temperature (Ta)

S-80122AL

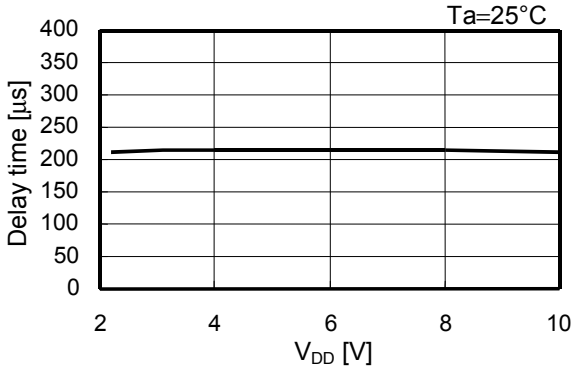


S-80160AL



15. Delay Time 2 - Input Voltage (V_{DD})

S-80122AN



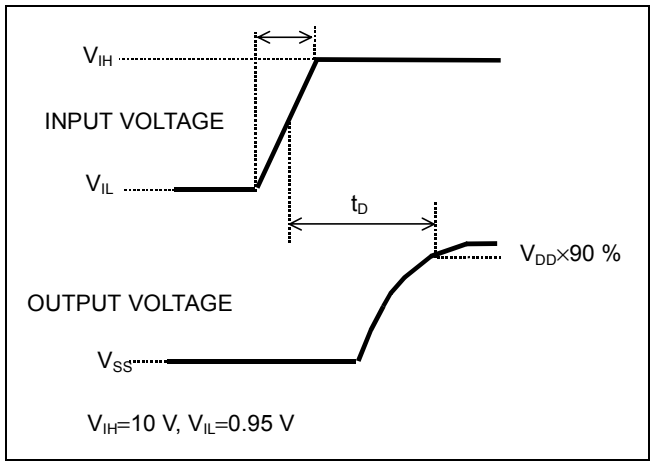
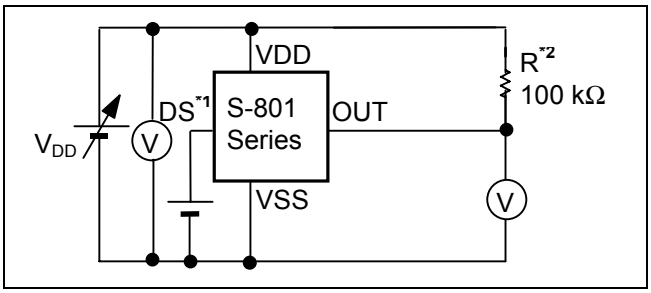


Figure 17 Measurment Condition for Delay Time



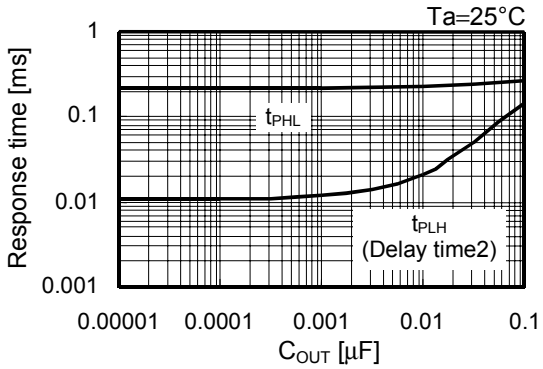
***1.** Set to V_{DD} or V_{SS}.
***2.** R is not necessary for CMOS output products.

Figure 18 Measurment Circuit for Delay Time

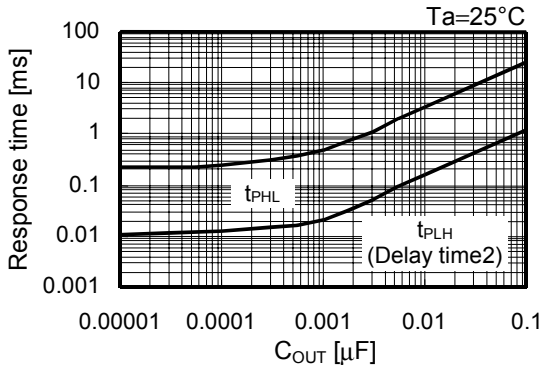
Caution The above connection diagram will not guarantees successful operation. Perform through using the actual application to set the constant.

16. Response Time - Load Capacitor (C_{OUT})

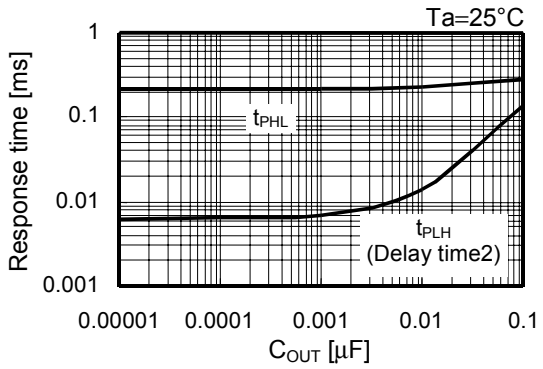
S-80122AL



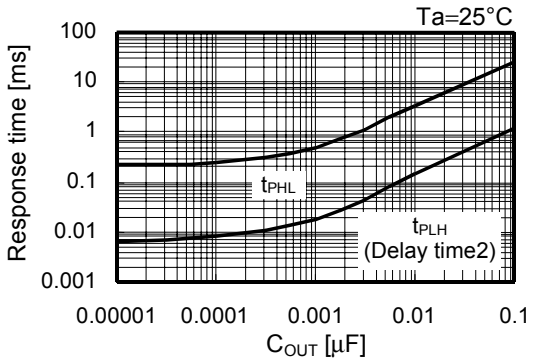
S-80122AN



S-80160AL



S-80160AN



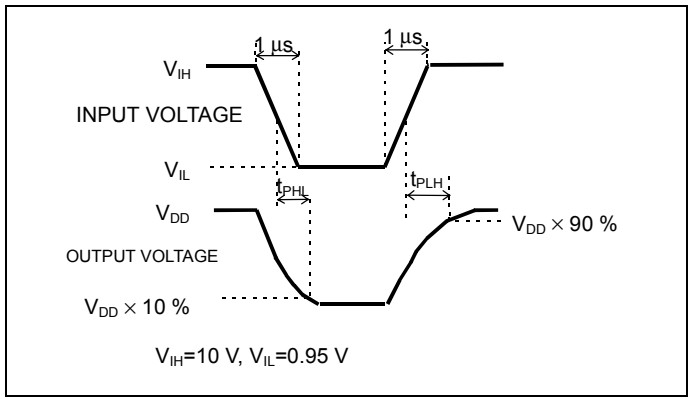
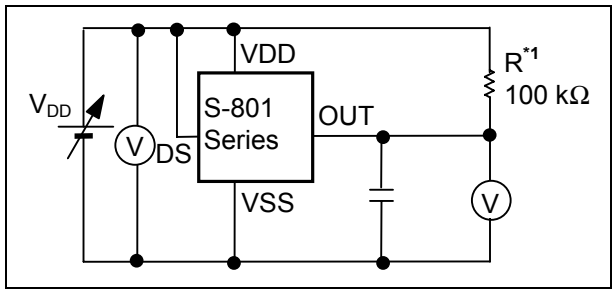


Figure 19 Measurment Condition for Response Time



***1.** R is not necessary for CMOS output products.

Figure 20 Measurment Circuit for Response Time

Caution The above connection diagram will not guarantees successful operation. Perform through using the actual application to set the constant.

■ Application Circuit Examples

Microcomputer Reset Circuits

If the power supply voltage to a microcomputer falls below the specified level, an unspecified operation may be performed or the contents of the memory register may be lost. When power supply voltage returns to normal, the microcomputer needs to be initialized before normal operations can be done. Reset circuits protect microcomputers in the event of current being momentarily switched off or lowered.

Reset circuits shown in **Figures 21 to 22** can be easily constructed with the help of the S-801 series that has low operating voltage, a high-precision detection voltage, hysteresis, and a built-in delay circuit.

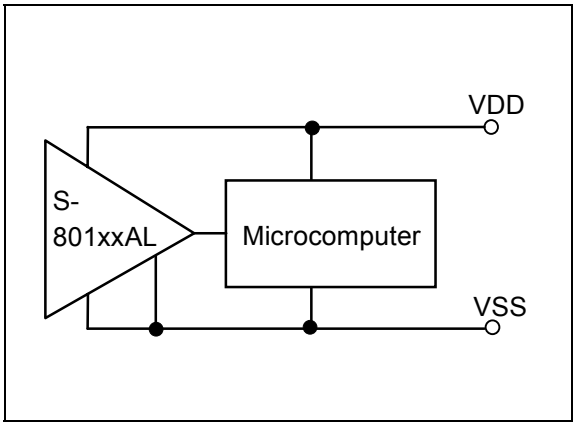


Figure 21 Ret Circuit (S-801xxAL)

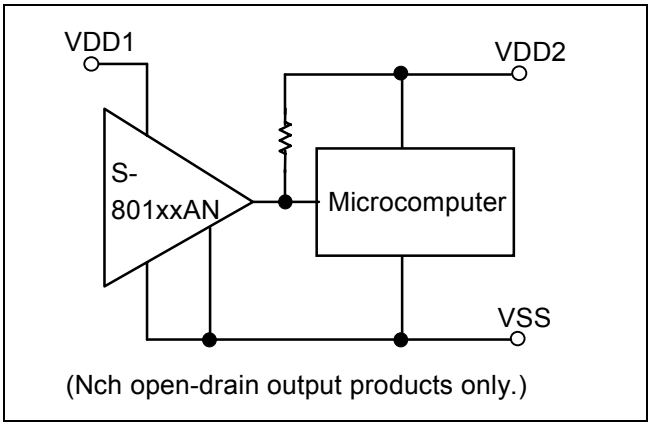
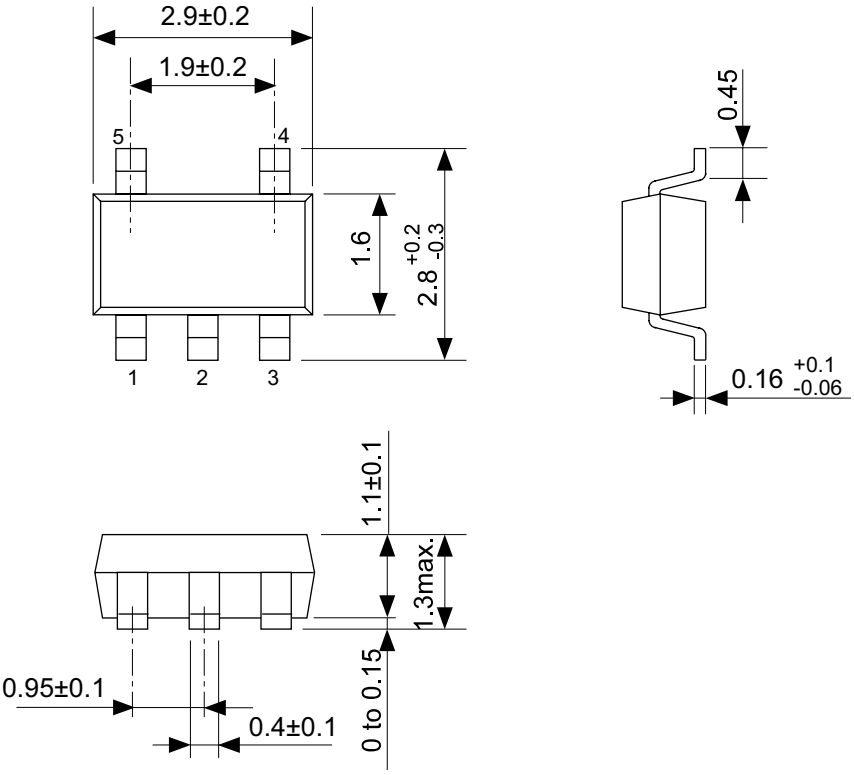


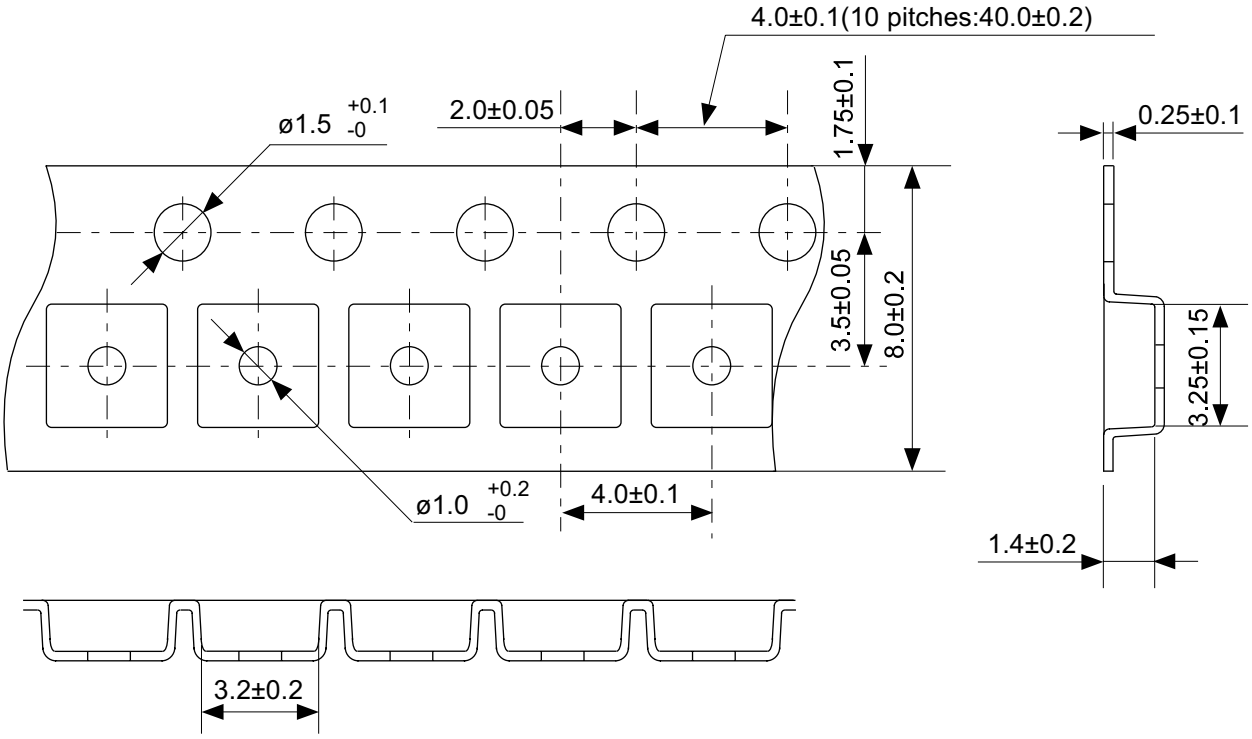
Figure 22 Reset Circuit (S-801xxAN)

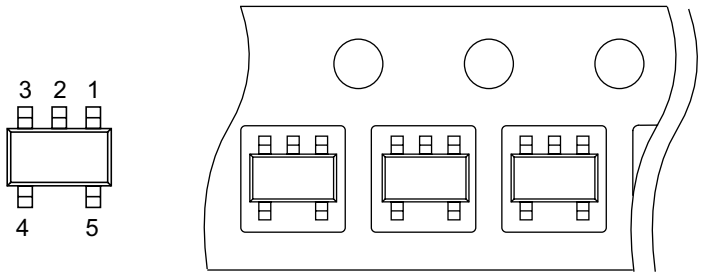
Caution The above connection diagram will not guarantees successful operation. Perform through using the actual application to set the constant.



No. MP005-A-P-SD-1.2

TITLE	SOT235-A-PKG Dimensions
No.	MP005-A-P-SD-1.2
SCALE	
UNIT	mm
Seiko Instruments Inc.	

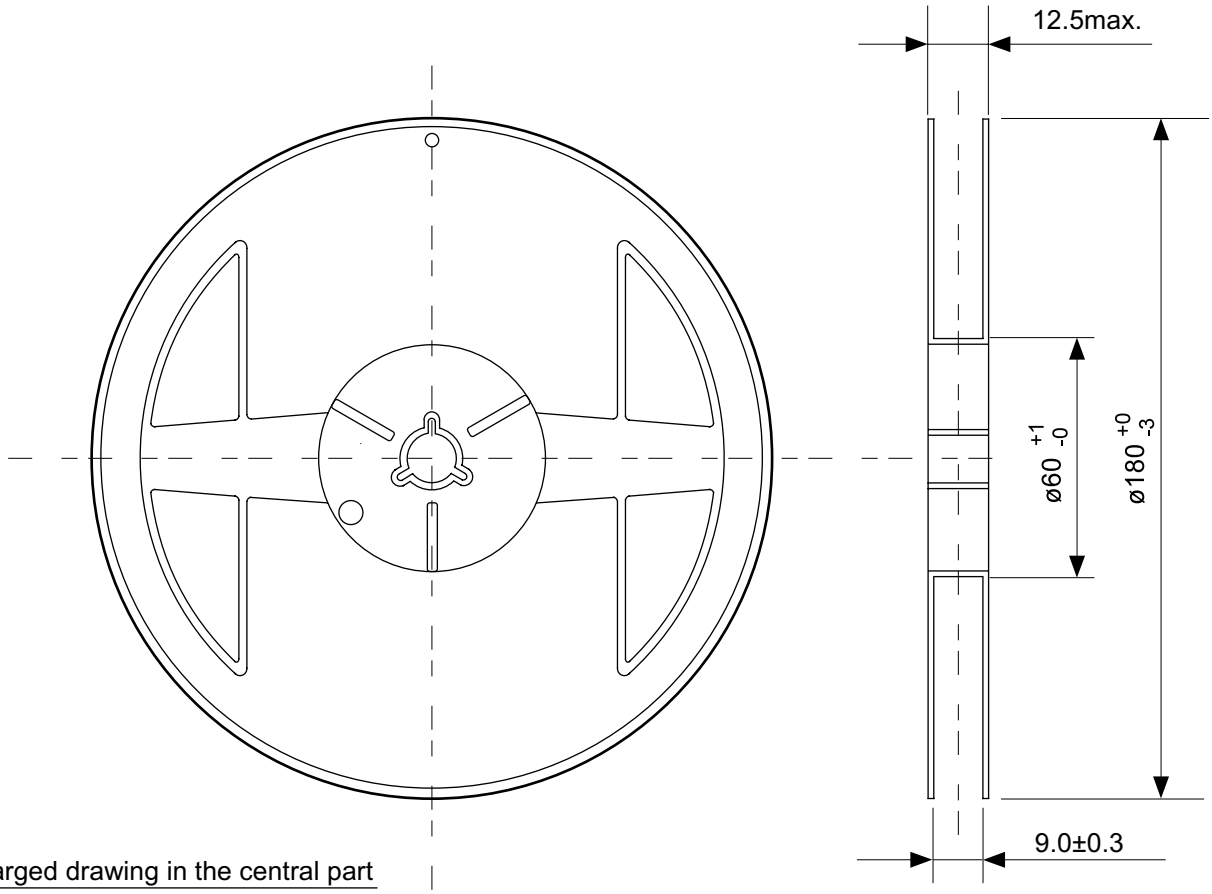




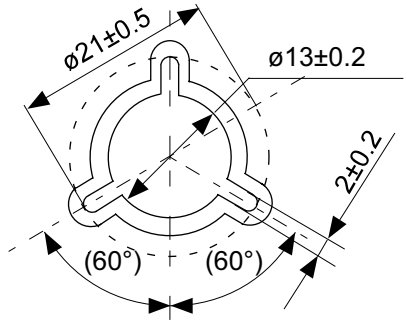
Feed direction

No. MP005-A-C-SD-2.1

TITLE	SOT235-A-Carrier Tape
No.	MP005-A-C-SD-2.1
SCALE	
UNIT	mm
Seiko Instruments Inc.	

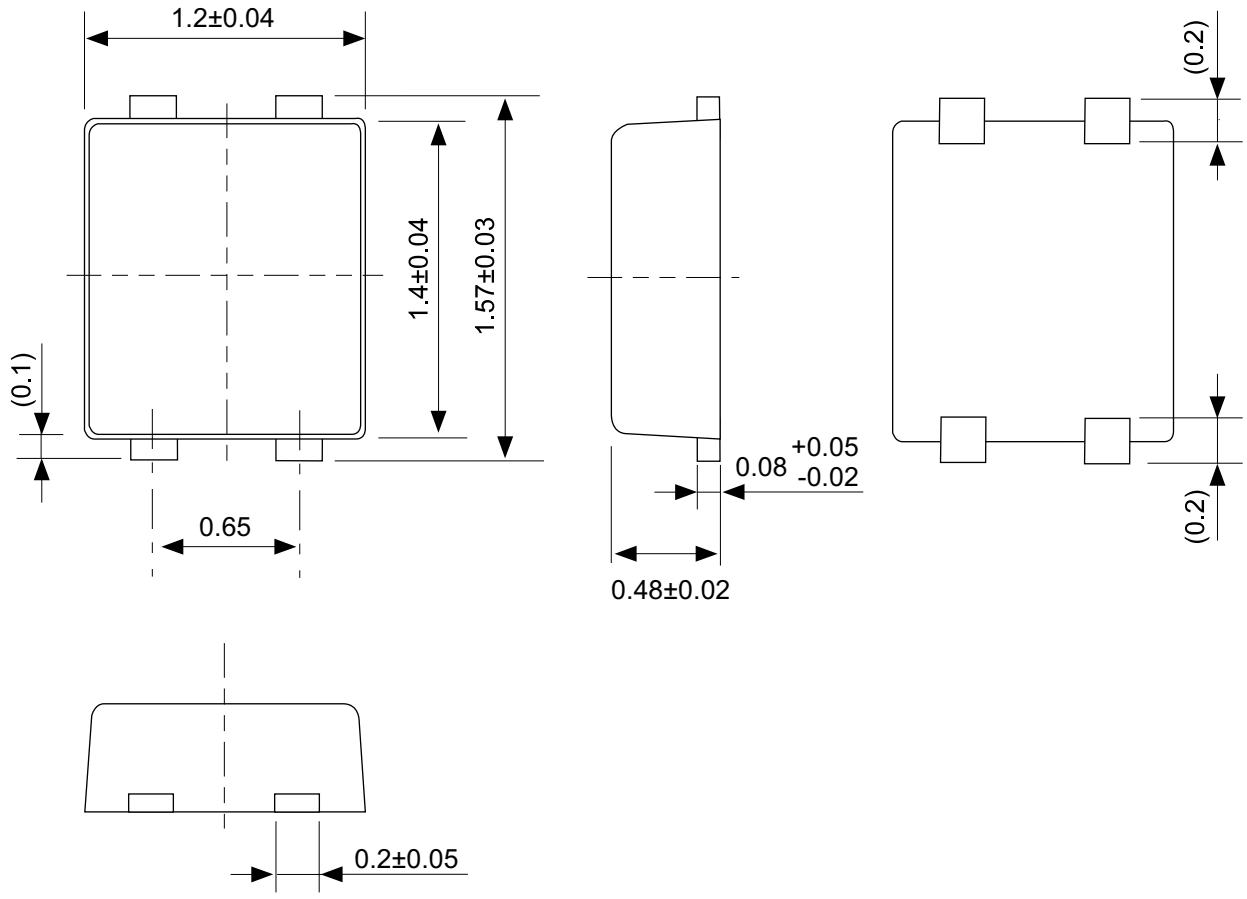


Enlarged drawing in the central part



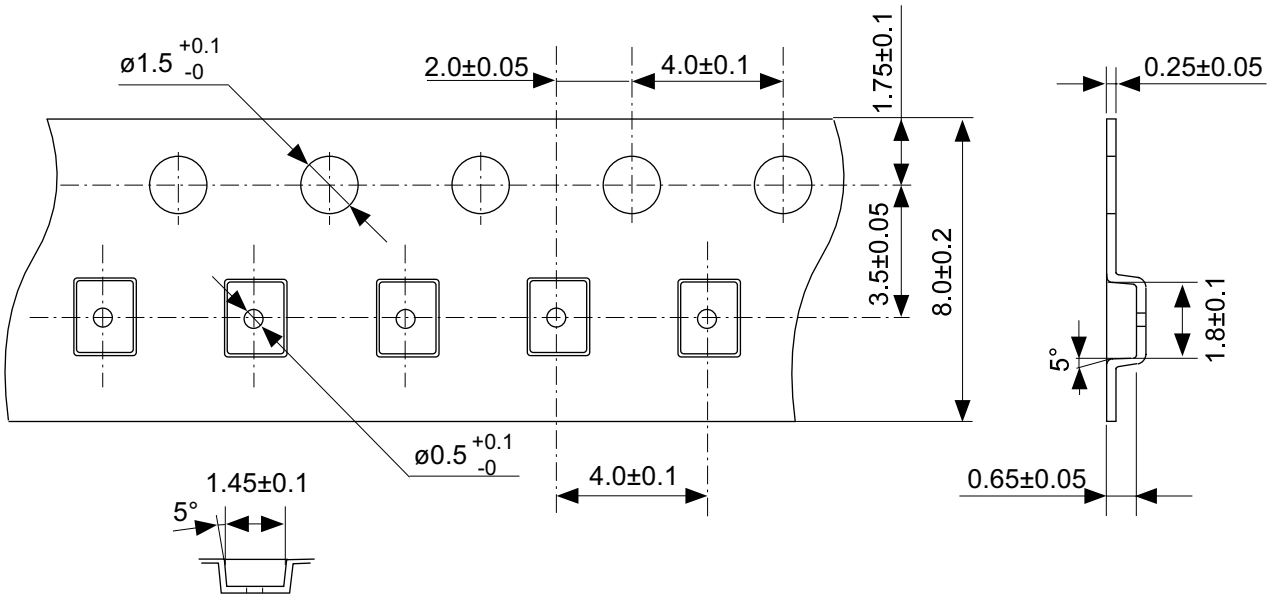
No. MP005-A-R-SD-1.1

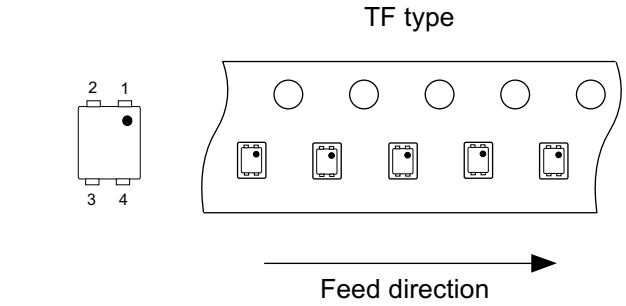
TITLE	SOT235-A-Reel		
No.	MP005-A-R-SD-1.1		
SCALE		QTY.	3,000
UNIT	mm		
Seiko Instruments Inc.			



No. PF004-A-P-SD-3.0

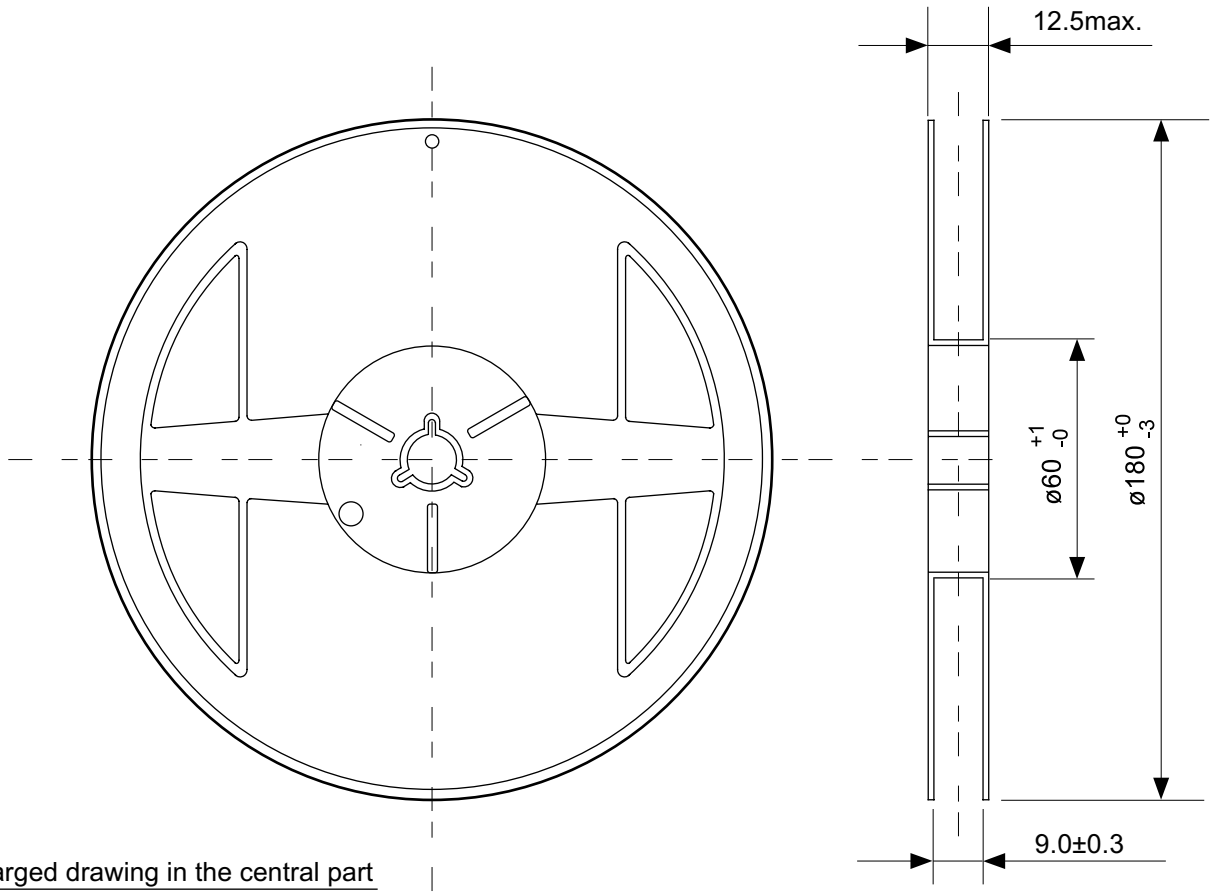
TITLE	SNT-4A-A-PKG Dimensions
No.	PF004-A-P-SD-3.0
SCALE	
UNIT	mm
Seiko Instruments Inc.	



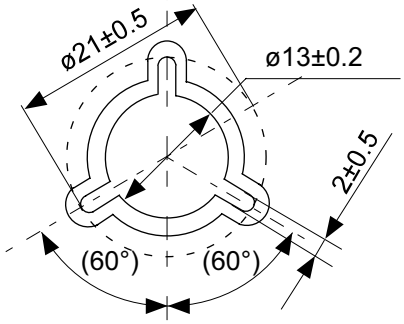


No. PF004-A-C-SD-1.0

TITLE	SNT-4A-A-Carrier Tape
No.	PF004-A-C-SD-1.0
SCALE	
UNIT	mm
Seiko Instruments Inc.	



Enlarged drawing in the central part



No. PF004-A-R-SD-1.0

TITLE	SNT-4A-A-Reel		
No.	PF004-A-R-SD-1.0		
SCALE		QTY.	5,000
UNIT	mm		
Seiko Instruments Inc.			

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