FUJITSU SEMICONDUCTOR
DATA SHEET

DS501-00013-0v02-E

Memory FRAM

64 K (8 K × 8) Bit I²C

MB85RC64V

■ DESCRIPTION

The MB85RC64V is an FRAM (Ferroelectric Random Access Memory) chip in a configuration of 8,192 words × 8 bits, using the ferroelectric process and silicon gate CMOS process technologies for forming the nonvolatile memory cells.

The MB85RC64V adopts the two-wire serial interface.

Unlike SRAM, the MB85RC64V is able to retain data without using a data backup battery.

The read/write endurance of the nonvolatile memory cells used for the MB85RC64V has improved to be at least 10^{12} cycles, significantly outperforming other nonvolatile memory products in the number.

The MB85RC64V provides writing in units of 1 byte because it is unnecessary to take a long time to write data unlike with Flash memories or E²PROM. Therefore, the writing completion wait sequence, for example the write busy state, is not required.

■ FEATURES

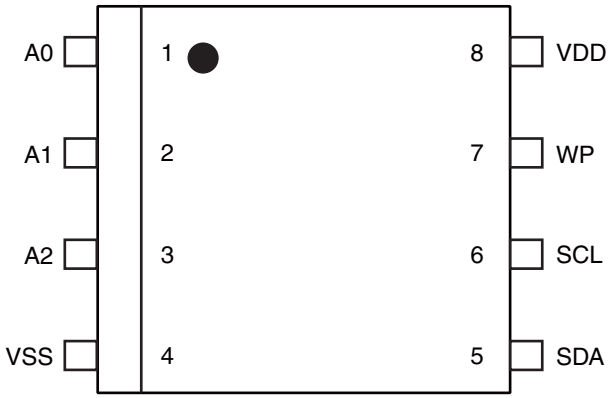
- Bit configuration : 8,192 words × 8 bits
- Two-wire serial interface : I²C-bus specification ver. 2.1 compliant, supports Standard-mode/Fast-mode.
  Fully controllable by two ports: serial clock (SCL) and serial data (SDA).
- Operating frequency : 400 kHz (Max)
- Read/write endurance : 10^{12} times/bit
- Data retention : 10 years (+ 85 °C)
- Operating power supply voltage : 3.0 V to 5.5 V
- Low-power consumption : Operating power supply current 40 µA (Typ: @400 kHz)
  Standby current 10 µA (Typ) [TBD]
- Operation ambient temperature range
  : − 40 °C to + 85 °C
- Package : 8-pin plastic SOP (FPT-8P-M02)
  RoHS compliant

2011.12

FUJITSU

■ PIN ASSIGNMENT

(TOP VIEW)

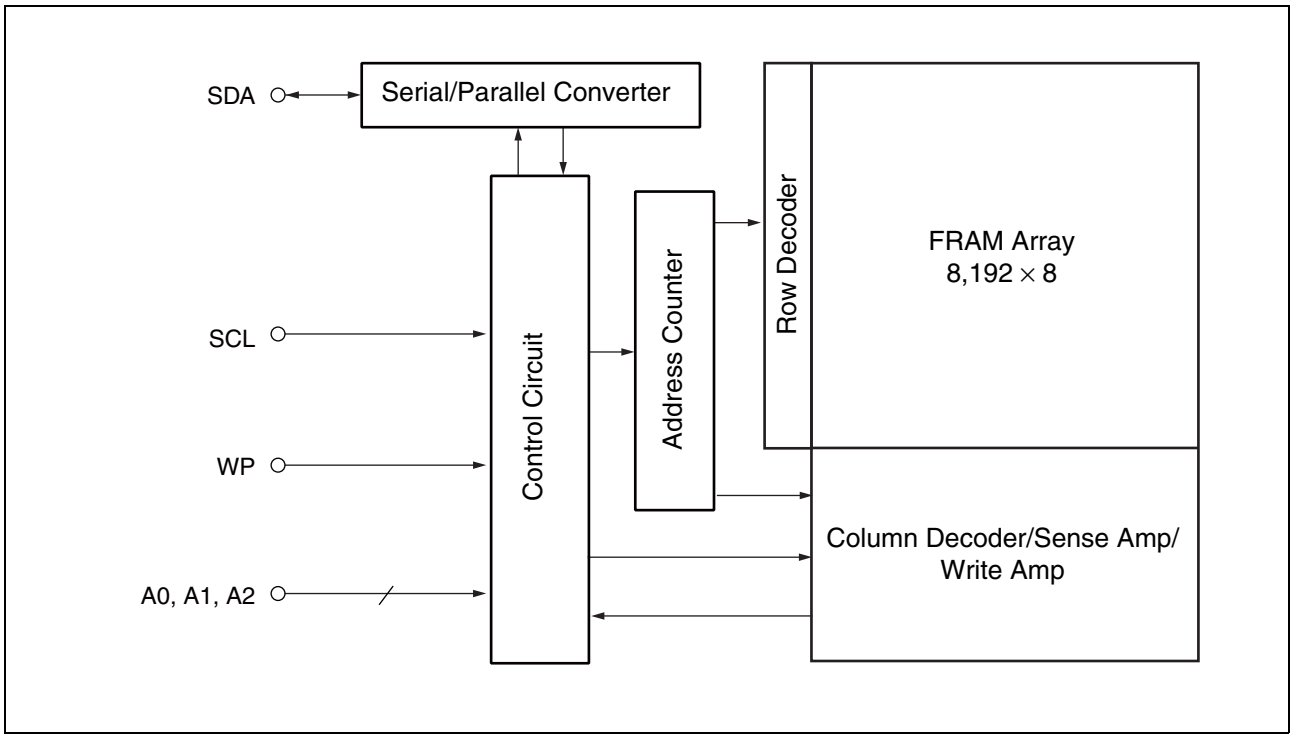


(FPT-8P-M02)

■ PIN FUNCTIONAL DESCRIPTIONS

Pin Number	Pin Name	Functional Description
1 to 3	A0 to A2	Device Address pins The MB85RC64V can be connected to the same data bus up to 8 devices. Device addresses are used in order to identify each of these devices. Connect these pins to VDD pin or VSS pin externally. Only if the combination of VDD and VSS pins matches Device Address Code inputted from the SDA pin, the device operates. In the open pin state, A0, A1, and A2 pins are internally pulled-down and recognized as the "L" level.
4	VSS	Ground pin
5	SDA	Serial Data I/O pin This is an I/O pin which performs bidirectional communication using an address and data. It is possible to connect multiple devices. It is an open drain output, so a pull-up resistor is required to be connected to the external circuit.
6	SCL	Serial Clock pin This is a clock input pin for input/output timing serial data. Data is sampled on the rising edge of the clock and output on the falling edge.
7	WP	Write Protect pin When the Write Protect pin is the “H” level, the writing operation is disabled. When the Write Protect pin is the “L” level, the entire memory region can be overwritten. The reading operation is always enabled regardless of the Write Protect pin condition. In the open pin state, the Write Protect pin is internally pulled-down to the VSS pin and recognized as the “L” level (writing enabled).
8	VDD	Supply Voltage pin

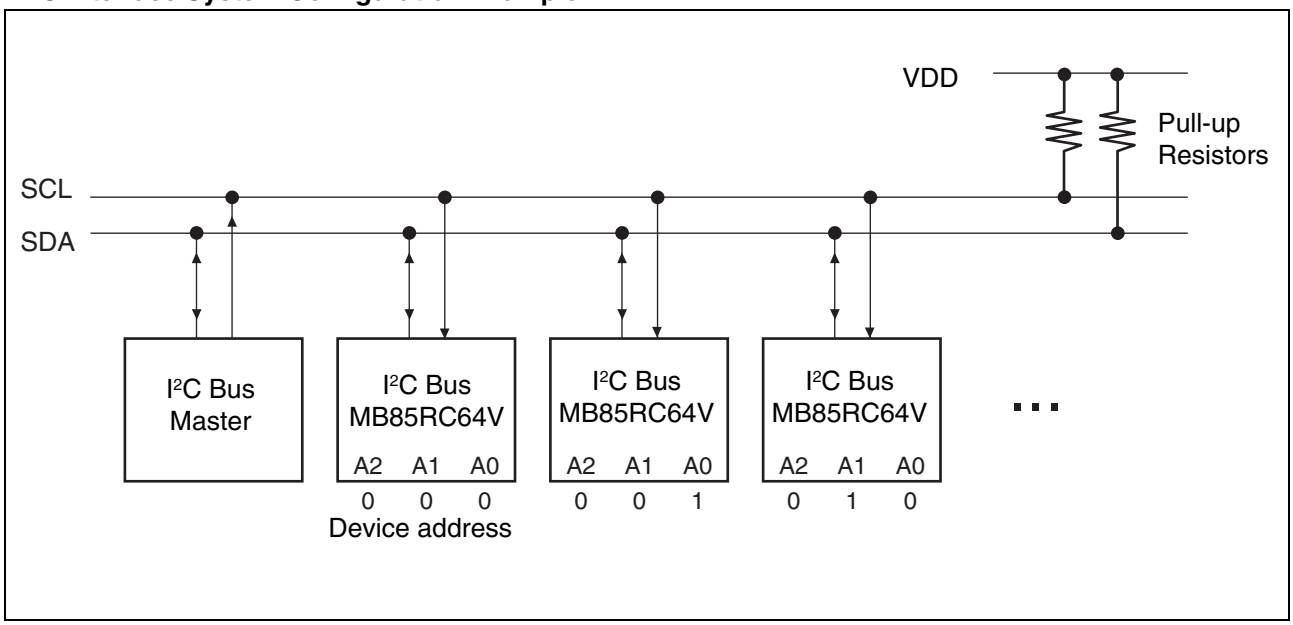
■ BLOCK DIAGRAM



■ I²C (Inter-Integrated Circuit)

The MB85RC64V has the two-wire serial interface; the I²C bus,and operates as a slave device.
The I²C bus defines communication roles of “master” and “slave” devices, with the master side holding the authority to initiate control. Furthermore, the I²C bus connection is possible where a single master device is connected to multiple slave devices in a party-line configuration. In this case, it is necessary to assign a unique device address to the slave device.

• I²C Interface System Configuration Example



■ I²C COMMUNICATION PROTOCOL

The SDA signal should change while SCL is the “L” level because the I²C bus achieves the communication by only two lines. However, as an exception, when starting and stopping communication sequence, SDA is allowed to change while SCL is the “H” level.

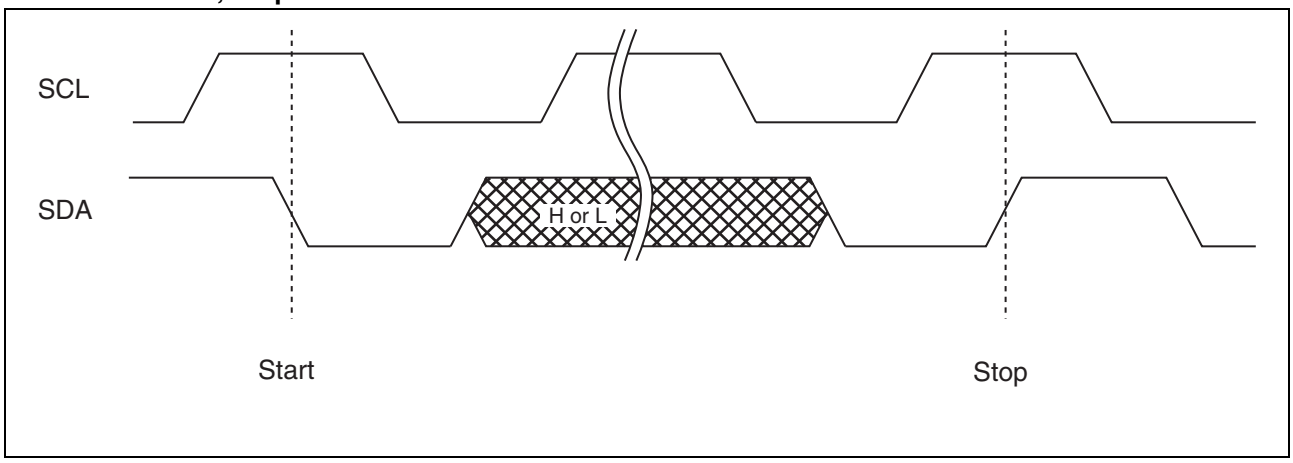
- Start Condition

To start read or write operations by the I²C bus, set the SDA input from the “H” level to the “L” level while the SCL input is in the “H” level.

- Stop Condition

To stop the I²C bus communication, change the SDA input from the “L” level to the “H” level while the SCL input is in the “H” level. In the reading operation, inputting the stop condition finishes reading and enters the standby state. In the writing operation, inputting the stop condition finishes inputting the rewrite data.

• Start Condition, Stop Condition



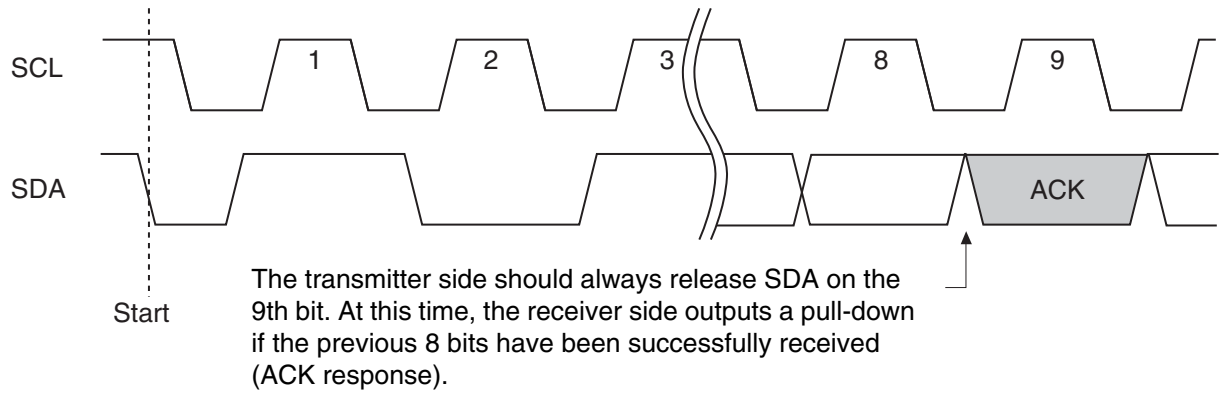
Note : At the write operation, the FRAM device does not need the programming wait time (t_{WC}) after issuing the Stop Condition.

■ ACKNOWLEDGE (ACK)

In the I²C bus, serial data including address or memory information is sent in units of 8 bits. The acknowledge signal indicates that every 8 bits of the data is successfully sent and received. The receiver side usually outputs the “L” level every time on the 9th SCL clock after each 8 bits are successfully transmitted. On the transmitter side, the bus is temporarily released every time on this 9th clock to allow the acknowledge signal to be received and checked. During this released period, the receiver side pulls the SDA line down to indicate that the communication is successfully received.

If the receiver side detects Stop condition before transmitting the acknowledge “L” level, the read operation ends and the I²C bus enters the standby state. If Stop condition is not sent, nor does the transmitter detect the acknowledge “L” level, the bus remains in the released state without doing anything.

• Acknowledge timing overview diagram



■ DEVICE ADDRESS WORD (Slave address)

Following the start condition, the bus master inputs the 8bits device address word. This input makes the device determine the reading/writing operation. The device address word (8bits) consists of a device Type code (4bits), device address code (3bits), and a read/write code (1bit).

- Device Type Code (4bits)

The upper 4 bits of the device address word are a device type code that identifies the device type, and are fixed at “1010” for the MB85RC64V.

- Device Address Code (3bits)

Following the device type code, the 3 bits of the device address code are input in order of A2, A1, and A0. The device address code identifies one device from up to eight devices connected to the bus.
Each MB85RC64V is given a unique 3bits code on the device address pin. The slave only responds if the received device address code is equal to this unique 3 bits code.

- Read/Write Code (1bit)

The 8th bit of the device address word is the R/W (read/write) code. When the R/W code is “0”, a write operation is enabled, and the R/W code is “1”, a read operation is enabled for the MB85RC64V.

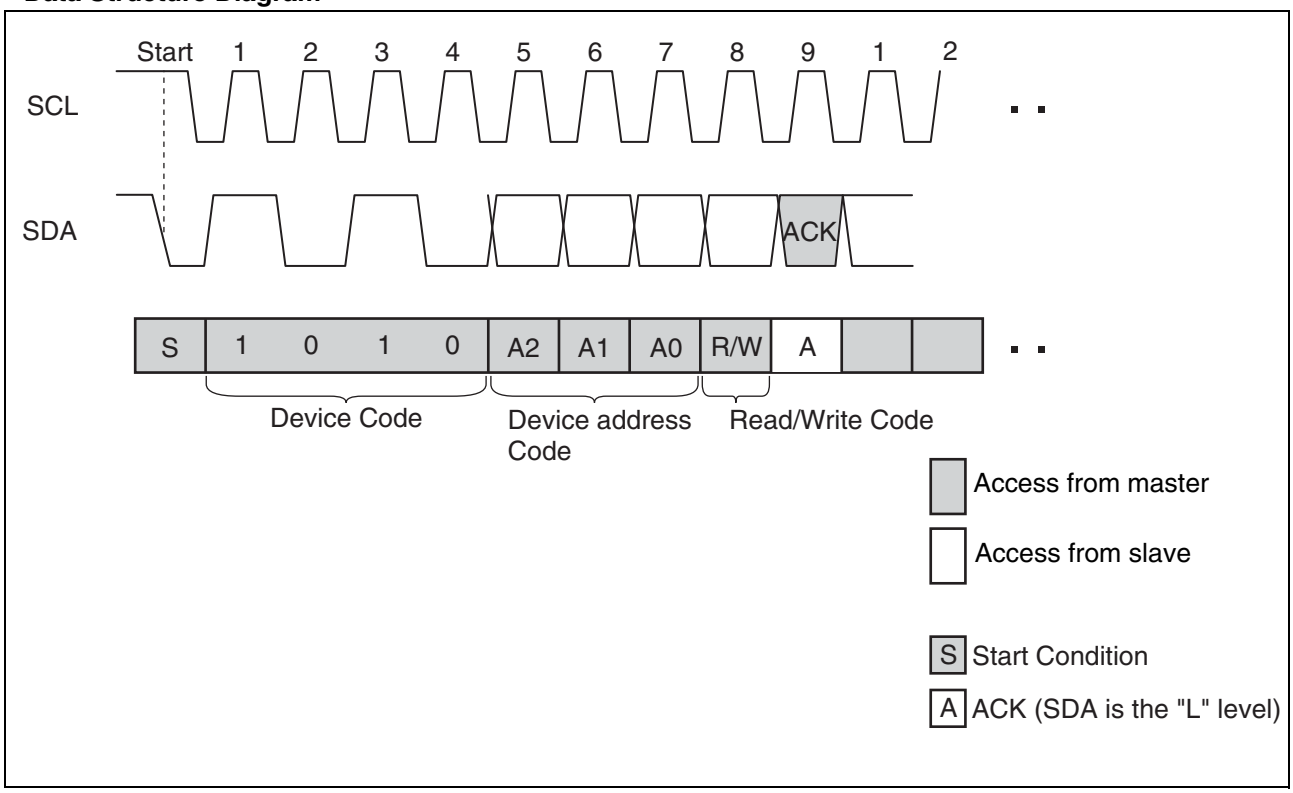
It turns to a stand-by state if the device code is not “1010” or device address code does not equal to pins A2, A1, and A0.

■ DATA STRUCTURE

In the I²C bus, the acknowledge “L” level is output on the 9th bit by a slave, after the 8 bits of the device address word following the start condition are input by a master. After confirming the acknowledge response by the master, the master outputs 8bits × 2 memory address to the slave. When the each memory address input ends, the slave again outputs the acknowledge “L” level. After this operation, the I/O data follows in units of 8 bits, with the acknowledge “L” level output after every 8bits.

It is determined by the R/W code whether the data line is driven by the master or the slave. However, the clock must be driven by the master. The clock becomes the “L” level for the next phase again after turning to the “H” level at the acknowledge bit. If the master finishes communication at this time, after making the condition that the data line, the clock and the data turn to the “L” level, change to the stop condition by turning the clock to the “H” level first and then turning the data to the “H” level (refer to the figure shown below).

• Data Structure Diagram



■ FRAM ACKNOWLEDGE -- POLLING NOT REQUIRED

The MB85RC64V performs the high speed write operations, so any waiting time for an ACK polling* does not occur.

*: In E²PROM, the Acknowledge Polling is performed as a progress check whether rewriting is executed or not. It is normal to judge by the 9th bit of Acknowledge whether rewriting is performed or not after inputting the start condition and then the device address word (8 bits) during rewriting.

■ WRITE PROTECT (WP)

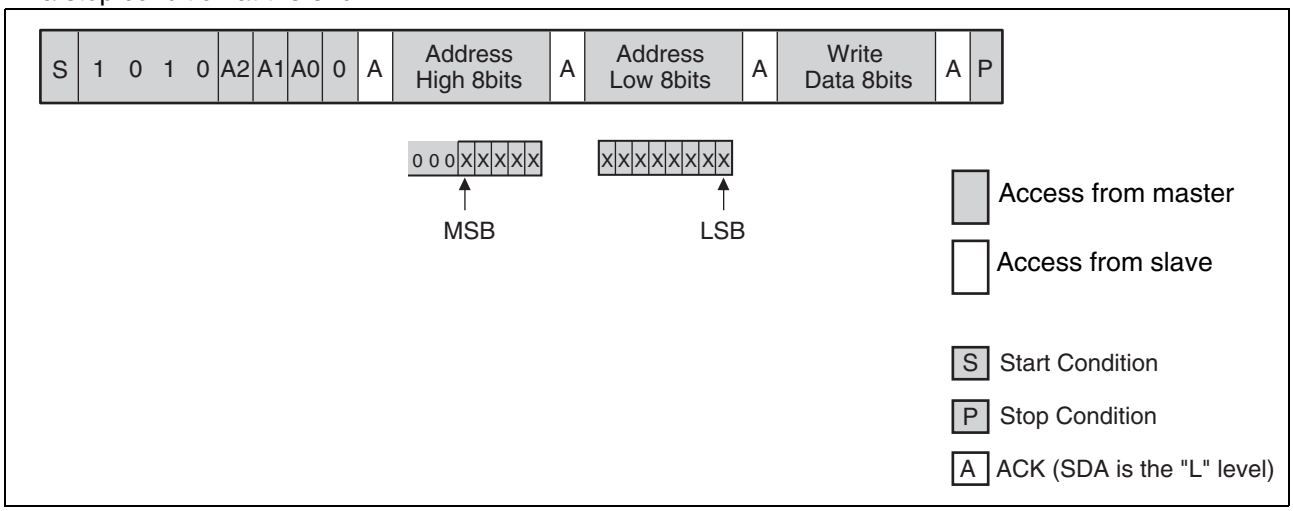
The entire memory array can be write protected using the Write Protect pin. When the Write Protect pin is set to the “H” level, the entire memory array will be write protected. When the Write Protect pin is the “L” level, the entire memory array will be rewritten. Reading is allowed regardless of the WP pin's “H” level or “L” level.

Note : The Write Protect pin is pulled down internally to the VSS pin, therefore if the Write Protect pin is open, the pin status is detected as the “L” level (write enabled).

■ COMMAND

• Byte Write

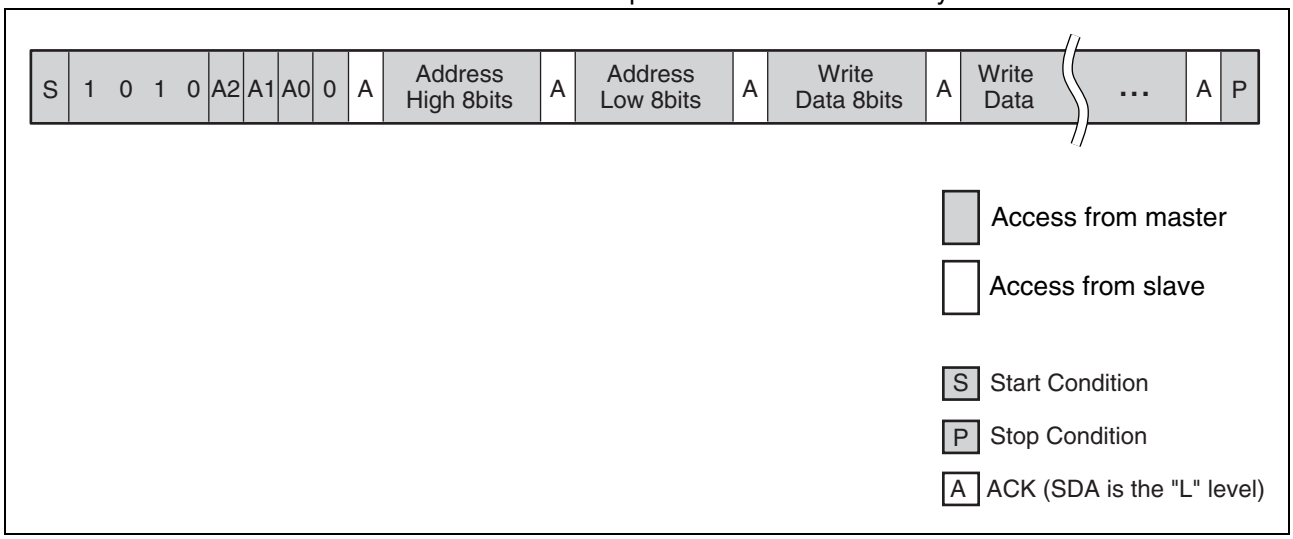
If the device address word (R/W “0” input) is sent following the start condition, the slave responds with an ACK. After this ACK, write addresses and data are sent in the same way, and the write ends by generating a stop condition at the end.



Note : In the MB85RC64V, input “000” to the upper 3 bits of the MSB because the address is expressed with 13 bits.

• Page Write

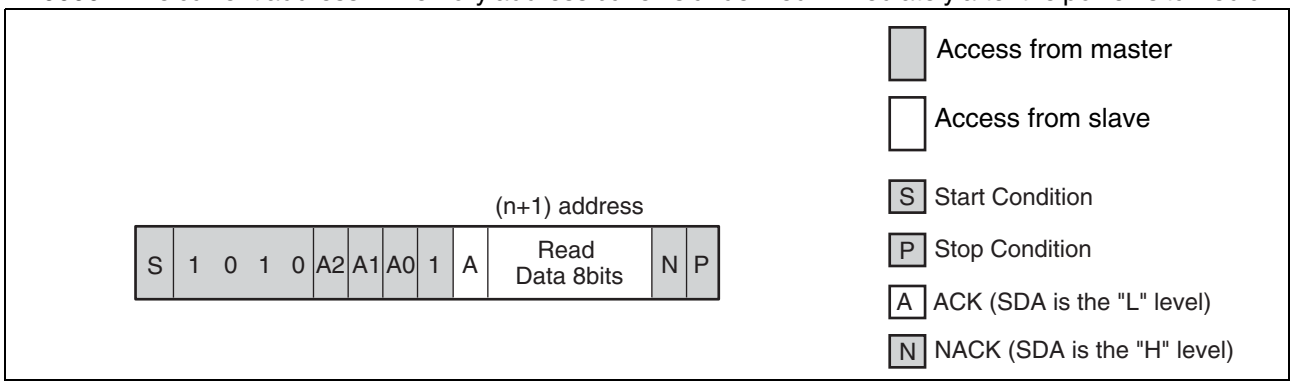
If data is continuously sent after the following address when the same command as Byte Write was sent, a page write is performed. The memory address rolls over to first memory address (0000_H) at the end of the address. Therefore, if more than 8 Kbytes are sent, the data is overwritten in order starting from the start of the FRAM memory address that was written first. Because FRAM performs the high-speed write operations, the data will be written to FRAM after the ACK response finishes immediately.



Note : It is not necessary to take a period for internal write operation cycles from the buffer to the memory after the stop condition is generated.

• Current Address Read

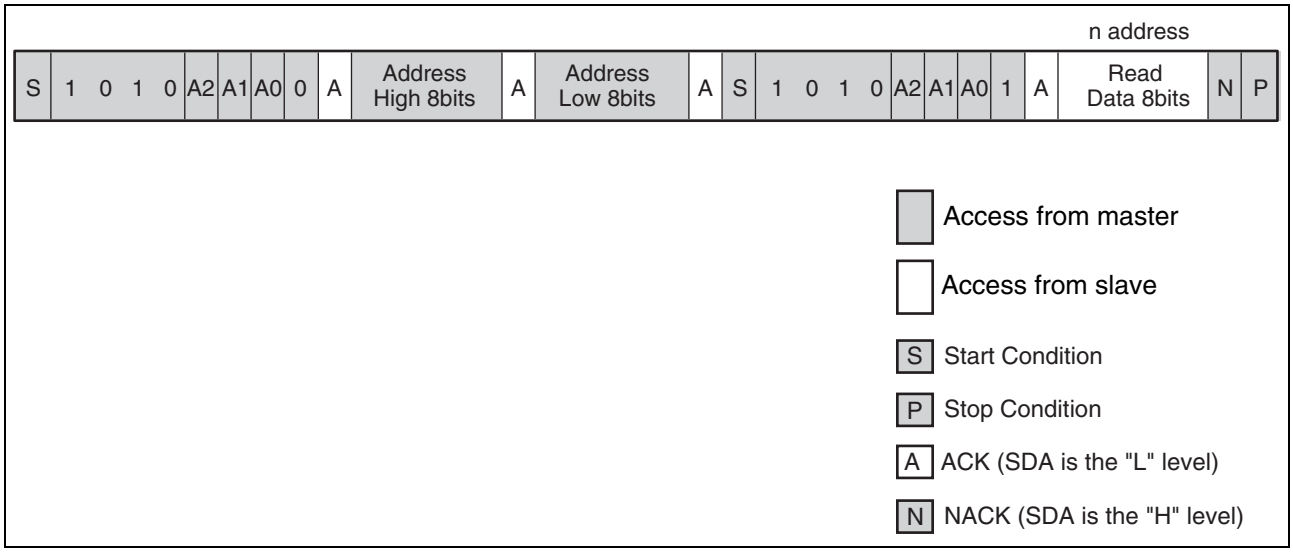
When the previous write or read operation finishes successfully up to the stop condition and if the last accessed address is taken to be “n”, then the address at “n+1” is read by sending the following command unless turning the power off. If the memory address is last address, the address counter will roll over to 0000H. The current address in memory address buffer is undefined immediately after the power is turned on.



• Random Read

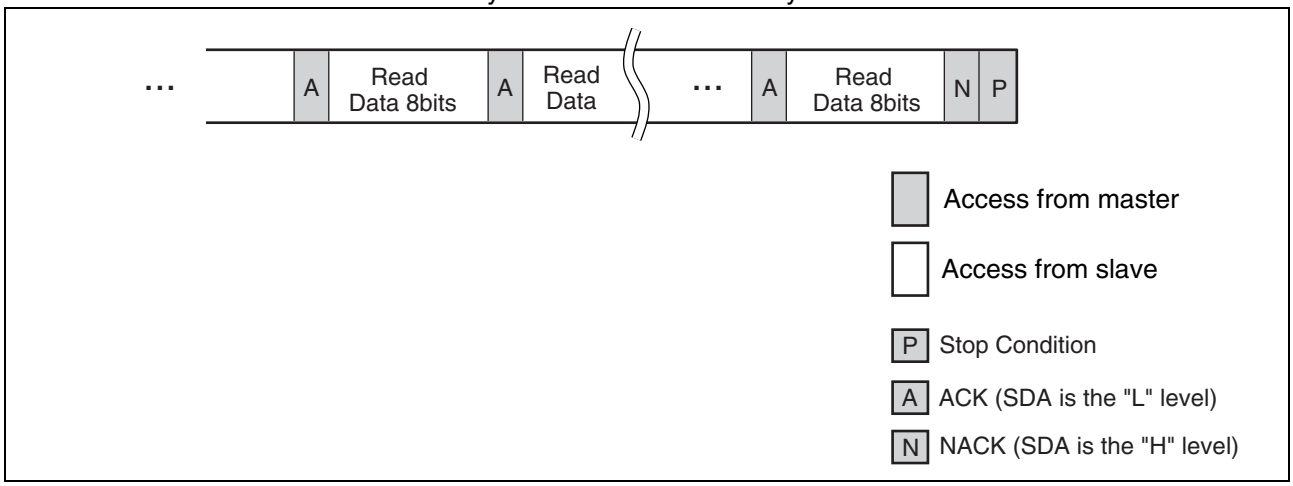
The one byte of data from the memory address as saved in the memory address buffer can be read out synchronously to SCL by specifying the address in the same way as for a write, and then issuing another start condition and sending the Device Address Word (R/W “1” input).

The final NACK is issued by the receiver that receives the data. In this case, this bit is issued by the master side.



• Sequential Read

Data can be received continuously following the Device address word (R/W “1” input) after specifying the address in the same way as for Random Read. If the read reaches the end of address for the MB85RC64V, the internal read address automatically rolls over to first memory address 0000_H.



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Power supply voltage*	V_{DD}	− 0.5	+6.0	V
Input voltage*	V_{IN}	− 0.5	V_{DD} + 0.5 (≤ 6.0)	V
Output voltage*	V_{OUT}	− 0.5	V_{DD} + 0.5 (≤ 6.0)	V
Operation ambient temperature	T_A	− 40	+ 85	°C
Storage temperature	Tstg	− 40	+ 125	°C

*: These parameters are based on the condition that VSS is 0 V.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power supply voltage*	V_{DD}	3.0	—	5.5	V
“H” level input voltage*	V_{IH}	$V_{DD} \times 0.8$	—	5.5	V
“L” level input voltage*	V_{IL}	V_{SS}	—	$V_{DD} \times 0.2$	V
Operation ambient temperature	T_A	− 40	—	+ 85	°C

*: These parameters are based on the condition that VSS is 0 V.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

(within recommended operating conditions)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Input leakage current*1	$\|I_{LI}\|$	V_{IN} = 0 V to V_{DD}	—	—	1	µA
Output leakage current*2	$\|I_{LO}\|$	V_{OUT} = 0 V to V_{DD}	—	—	1	µA
Operating power supply current	I_{DD}	SCL = 400 kHz	—	40	80	µA
Standby current	I_{SB}	SCL, SDA = V_{DD} WP = 0 V or V_{DD} or Open Under Stop Condition T_A = + 25 °C	—	10 (TBD)	15 (TBD)	µA
"L" level output voltage	V_{OL}	I_{OL} = 2 mA	—	—	0.4	V
Input resistance for WP pin	R_{IN}	V_{IN} = V_{IL} (Max)	50	—	—	kΩ
		V_{IN} = V_{IH} (Min)	1	—	—	MΩ

*1: Applicable pin: SCL,SDA

*2: Applicable pin: SDA

2. AC Characteristics

Parameter	Symbol	Value				Unit
		STANDARD MODE		FAST MODE		
		Min	Max	Min	Max	
SCL clock frequency	FSCL	0	100	0	400	kHz
Clock high time	T_{HIGH}	4.0	—	0.6	—	µs
Clock low time	T_{LOW}	4.7	—	1.3	—	µs
SCL/SDA rising time	T_r	—	1000	—	300	ns
SCL/SDA falling time	T_f	—	300	—	300	ns
Start condition hold	$T_{HD:STA}$	4.0	—	0.6	—	µs
Start condition setup	$T_{SU:STA}$	4.7	—	0.6	—	µs
SDA input hold	$T_{HD:DAT}$	0	—	0	—	ns
SDA input setup	$T_{SU:DAT}$	250	—	100	—	ns
SDA output hold	$T_{DH:DAT}$	0	—	0	—	ns
Stop condition setup	$T_{SU:STO}$	4.0	—	0.6	—	µs
SDA output access after SCL falling	T_{AA}	—	3	—	0.9	µs
Pre-charge time	T_{BUF}	4.7	—	1.3	—	µs
Pulse width ignored (Input Filter on SCL and SDA)	T_{SP}	—	50	—	50	ns

AC characteristics were measured under the following measurement conditions.

Power supply voltage : 3.0 V to 5.5 V

Operation ambient temperature: – 40 °C to + 85 °C

Input voltage magnitude : $V_{DD} \times 0.2$ to $V_{DD} \times 0.8$

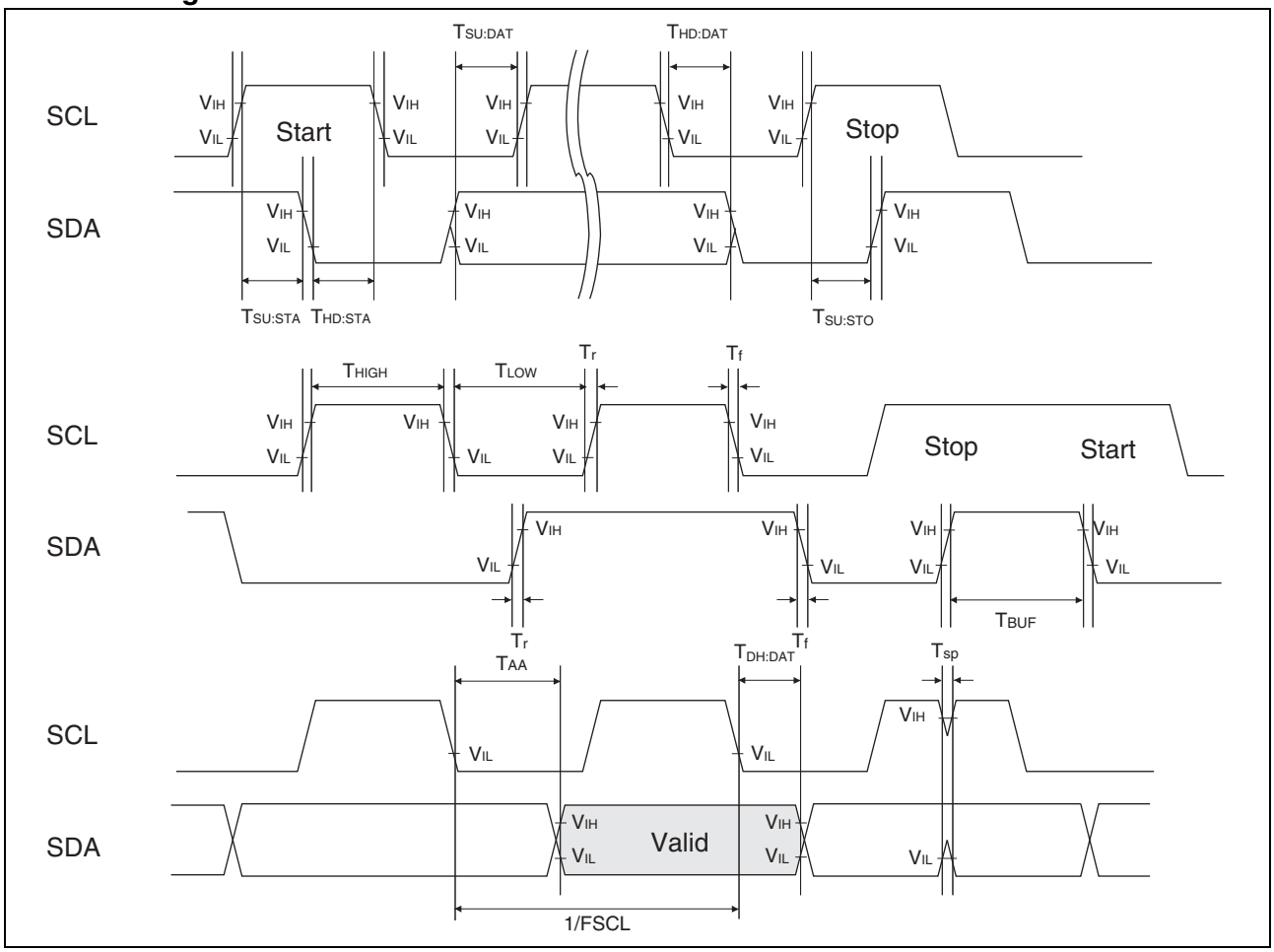
Input rising time : 5 ns

Input falling time : 5 ns

Input judge level : $V_{DD}/2$

Output judge level : $V_{DD}/2$

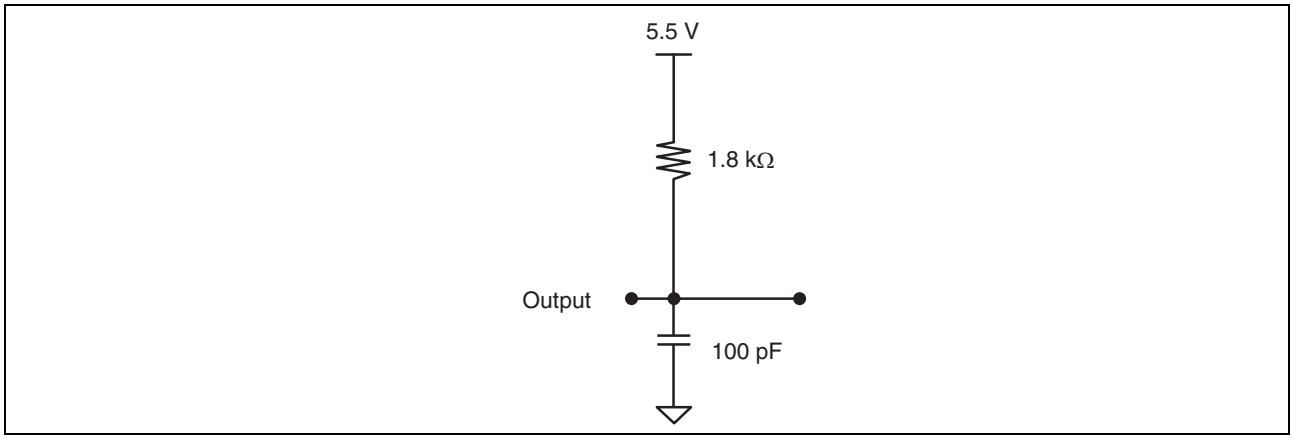
3. AC Timing Definitions



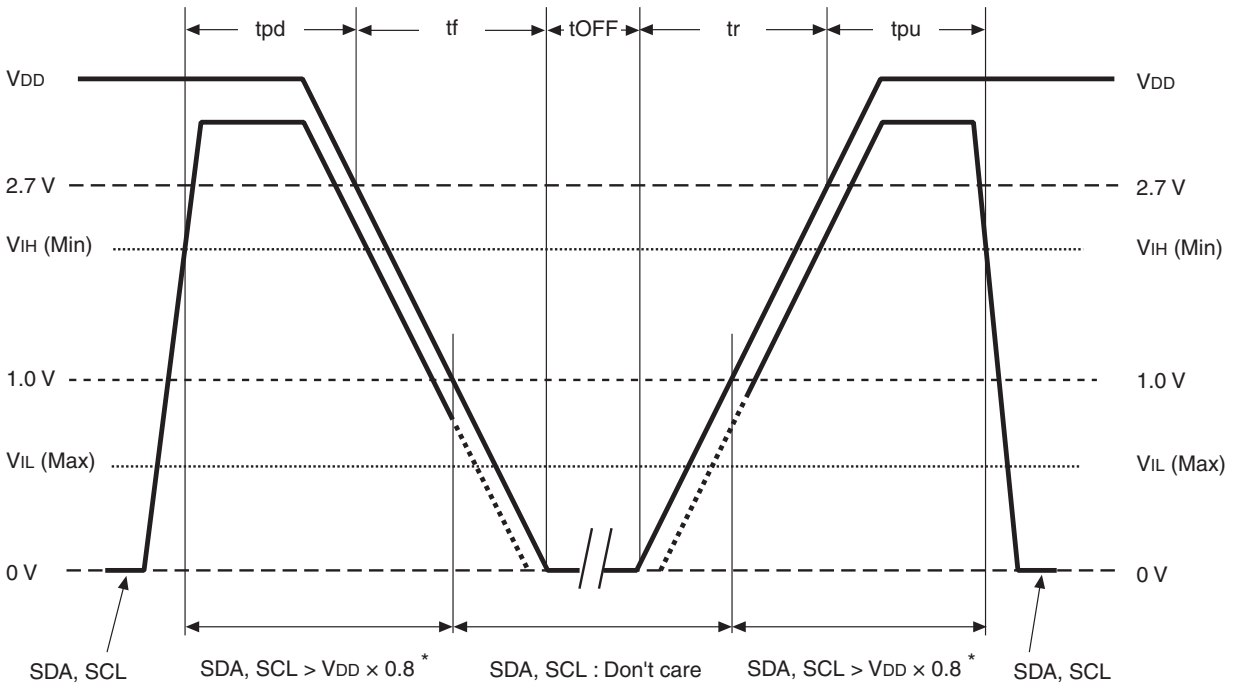
4. Pin Capacitance

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
I/O capacitance	$C_{I/O}$	$V_{DD} = V_{IN} = V_{OUT} = 0$ V, f = 1 MHz, $T_A = +25$ °C	—	—	15	pF
Input capacitance	C_{IN}		—	—	15	pF

5. AC Test Load Circuit



■ POWER ON SEQUENCE



* : SDA, SCL (Max) < V_{DD} + 0.5 V

Note: VDD pin is required to be rising from 0 V because turning the power on from an intermediate level may cause malfunctions, when the power is turned on.

Parameter	Symbol	Value		Unit
		Min	Max	
SDA, SCL level hold time during power down	tpd	85	—	ns
SDA, SCL level hold time during power up	tpu	85	—	ns
Power supply rising time	tr	0.5	50	ms
Power supply falling time	tf	0.5	50	ms
Power off time	tOFF	50	—	ms

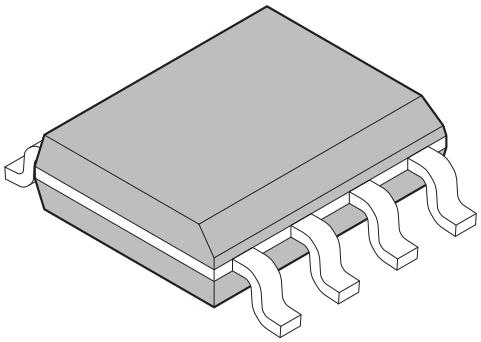
■ NOTES ON USE

- Data written before performing IR reflow is not guaranteed after IR reflow.
- During the access period from the start condition to the stop condition, keep the WP, A0, A1, and A2 signals to the VDD pin level or VSS pin level.

■ ORDERING INFORMATION

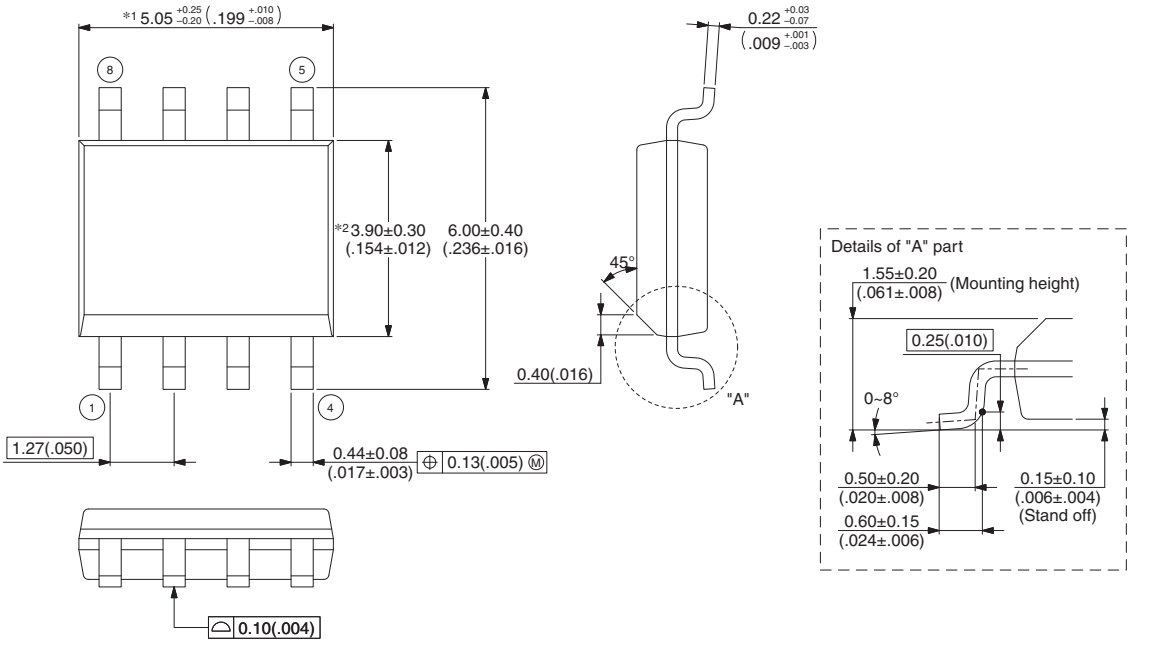
Part number	Package	Shipping form	Minimum shipping quantity
MB85RC64VPNF-G-JNE1	8-pin, plastic SOP (FPT-8P-M02)	Tube	1
MB85RC64VPNF-G-JNERE1	8-pin, plastic SOP (FPT-8P-M02)	Embossed Carrier tape	1500

■ PACKAGE DIMENSION

8-pin plastic SOP		
	Lead pitch	1.27 mm
	Package width × package length	3.9 mm × 5.05 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.75 mm MAX
	Weight	0.06 g
(FPT-8P-M02)		

8-pin plastic SOP
(FPT-8P-M02)

Note 1) *1 : These dimensions include resin protrusion.
Note 2) *2 : These dimensions do not include resin protrusion.
Note 3) Pins width and pins thickness include plating thickness.
Note 4) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please check the latest package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/

■ MAJOR CHANGES IN THIS EDITION

A change on a page is indicated by a vertical line drawn on the left side of that page.

Page	Section	Change Results
1	■ DESCRIPTION	Revised the following description: at least 10^{10} cycles → at least 10^{12} cycles
	■ FEATURES • Read/write endurance	Revised the spec of the read/write endurance: 10^{10} times/bit → 10^{12} time/bit
	• Operating ambient temperature range	Corrected the spec value of temperature range: 40 °C to +85 °C → -40 °C to +85 °C

MEMO

MEMO

FUJITSU SEMICONDUCTOR LIMITED

Nomura Fudosan Shin-yokohama Bldg. 10-23, Shin-yokohama 2-Chome,
Kohoku-ku Yokohama Kanagawa 222-0033, Japan
Tel: +81-45-415-5858
http://jp.fujitsu.com/fsl/en/

For further information please contact:

North and South America
FUJITSU SEMICONDUCTOR AMERICA, INC.
1250 E. Arques Avenue, M/S 333
Sunnyvale, CA 94085-5401, U.S.A.
Tel: +1-408-737-5600 Fax: +1-408-737-5999
http://us.fujitsu.com/micro/

Europe
FUJITSU SEMICONDUCTOR EUROPE GmbH
Pittlerstrasse 47, 63225 Langen, Germany
Tel: +49-6103-690-0 Fax: +49-6103-690-122
http://emea.fujitsu.com/semiconductor/

Korea
FUJITSU SEMICONDUCTOR KOREA LTD.
902 Kosmo Tower Building, 1002 Daechi-Dong,
Gangnam-Gu, Seoul 135-280, Republic of Korea
Tel: +82-2-3484-7100 Fax: +82-2-3484-7111
http://kr.fujitsu.com/fsk/

Asia Pacific
FUJITSU SEMICONDUCTOR ASIA PTE. LTD.
151 Lorong Chuan,
#05-08 New Tech Park 556741 Singapore
Tel : +65-6281-0770 Fax : +65-6281-0220
http://sg.fujitsu.com/semiconductor/

FUJITSU SEMICONDUCTOR SHANGHAI CO., LTD.
30F, Kerry Parkside, 1155 Fang Dian Road, Pudong District,
Shanghai 201204, China
Tel : +86-21-6146-3688 Fax : +86-21-6146-3660
http://cn.fujitsu.com/fss/

FUJITSU SEMICONDUCTOR PACIFIC ASIA LTD.
10/F., World Commerce Centre, 11 Canton Road,
Tsimshatsui, Kowloon, Hong Kong
Tel : +852-2377-0226 Fax : +852-2376-3269
http://cn.fujitsu.com/fsp/

Edited: Sales Promotion Department