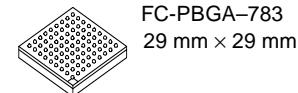


MSC8252

Dual-Core Digital Signal Processor

- Two StarCore SC3850 DSP subsystems, each with an SC3850 DSP core, 32 Kbyte L1 instruction cache, 32 Kbyte L1 data cache, unified 512 Kbyte L2 cache configurable as M2 memory in 64 Kbyte increments, memory management unit (MMU), extended programmable interrupt controller (EPIC), two general-purpose 32-bit timers, debug and profiling support, low-power Wait, Stop, and power-down processing modes, and ECC/EDC support.
- Chip-level arbitration and switching system (CLASS) that provides full fabric non-blocking arbitration between the cores and other initiators and the M2 memory, shared M3 memory, DDR SRAM controllers, device configuration control and status registers, and other targets.
- 1056 Kbyte 128-bit wide M3 memory, 1024 Kbytes of which can be turned off to save power.
- 96 Kbyte boot ROM.
- Three input clocks (one global and two differential).
- Five PLLs (three global and two Serial RapidIO PLLs).
- Two DDR controllers with up to a 400 MHz clock (800 MHz data rate), 64/32 bit data bus, supporting up to a total 2 Gbyte in up to four banks (two per controller) and support for DDR2 and DDR3.
- DMA controller with 32 unidirectional channels supporting 16 memory-to-memory channels with up to 1024 buffer descriptors per channel, and programmable priority, buffer, and multiplexing configuration. It is optimized for DDR SDRAM.
- Up to four independent TDM modules with programmable word size (2, 4, 8, or 16-bit), hardware-base A-law/μ-law conversion, up to 62.5 Mbps data rate for each TDM link, and with glueless interface to E1 or T1 framers that can interface with H-MVIP/H.110 devices, TSI, and codecs such as AC-97.



- High-speed serial interface that supports two Serial RapidIO interfaces, one PCI Express interface, and two SGMII interfaces (multiplexed). The Serial RapidIO interfaces support 1x/4x operation up to 3.125 Gbaud with a single messaging unit and two DMA units. The PCI Express controller supports 32- and 64-bit addressing, x4, x2, and x1 link.
- QUICC Engine technology subsystem with dual RISC processors, 48 Kbyte multi-master RAM, 48 Kbyte instruction RAM, supporting two communication controllers for two Gigabit Ethernet interfaces (RGMII or SGMII), to offload scheduling tasks from the DSP cores, and an SPI.
- I/O Interrupt Concentrator consolidates all chip maskable interrupt and non-maskable interrupt sources and routes them to INT_OUT, NMI_OUT, and the cores.
- UART that permits full-duplex operation with a bit rate of up to 6.25 Mbps.
- Two general-purpose 32-bit timers for RTOS support per SC3850 core, four timer modules with four 16-bit fully programmable timers, and eight software watchdog timers (SWT).
- Eight programmable hardware semaphores.
- Up to 32 virtual interrupts and a virtual NMI asserted by simple write access.
- I²C interface.
- Up to 32 GPIO ports, sixteen of which can be configured as external interrupts.
- Boot interface options include Ethernet, Serial RapidIO interface, I²C, and SPI.
- Supports standard JTAG interface
- Low power CMOS design, with low-power standby and power-down modes, and optimized power-management circuitry.
- 45 nm SOI CMOS technology.

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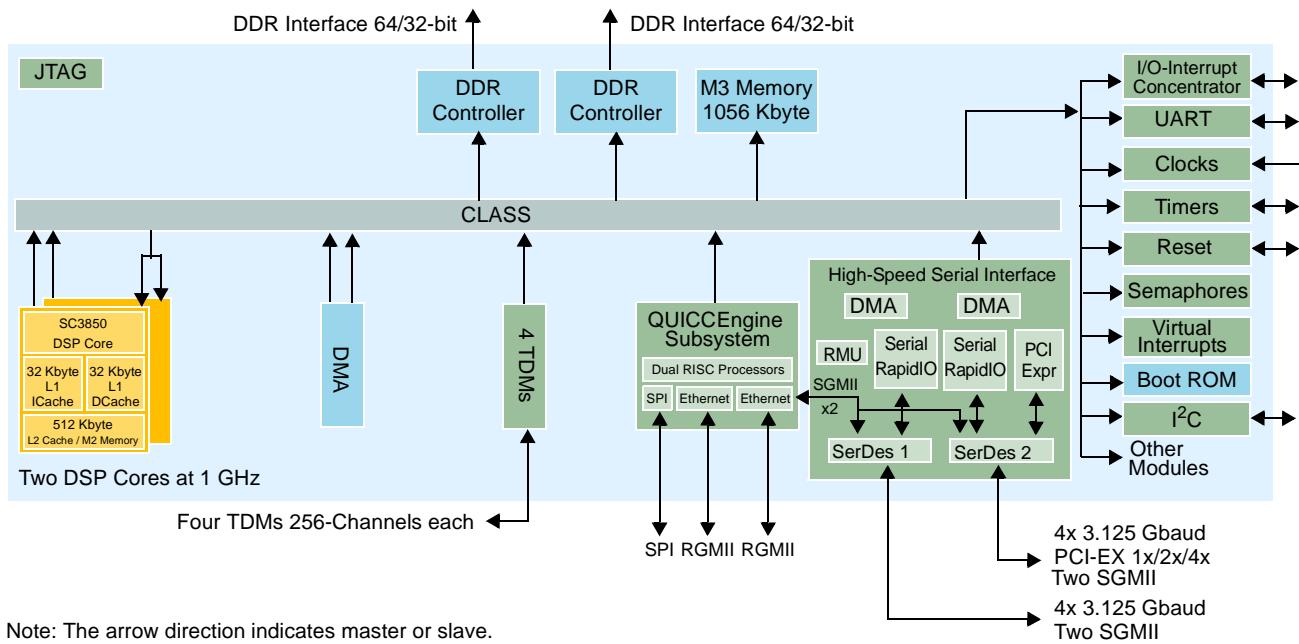


Figure 1. MSC8252 Block Diagram

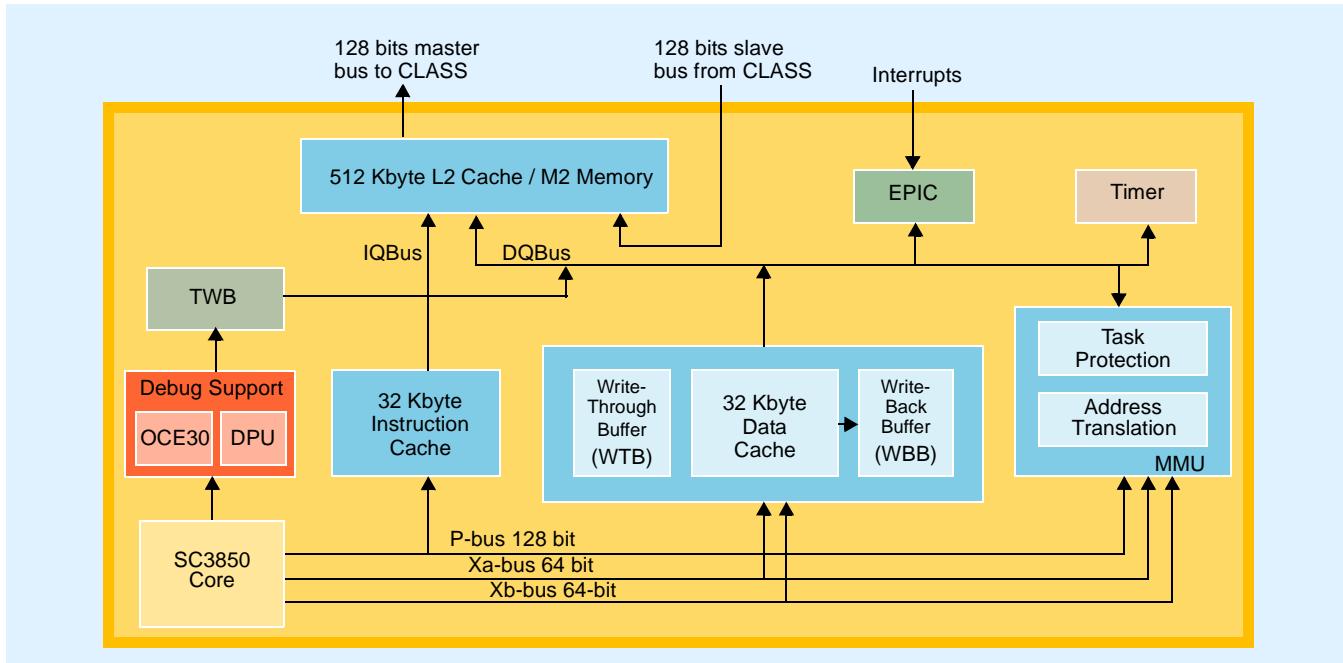


Figure 2. StarCore SC3850 DSP Subsystem Block Diagram

1 Pin Assignment

This section includes diagrams of the MSC8252 package ball grid array layouts and tables showing how the pinouts are allocated for the package.

1.1 FC-PBGA Ball Layout Diagram

The top view of the FC-PBGA package is shown in [Figure 3](#) with the ball location index numbers.

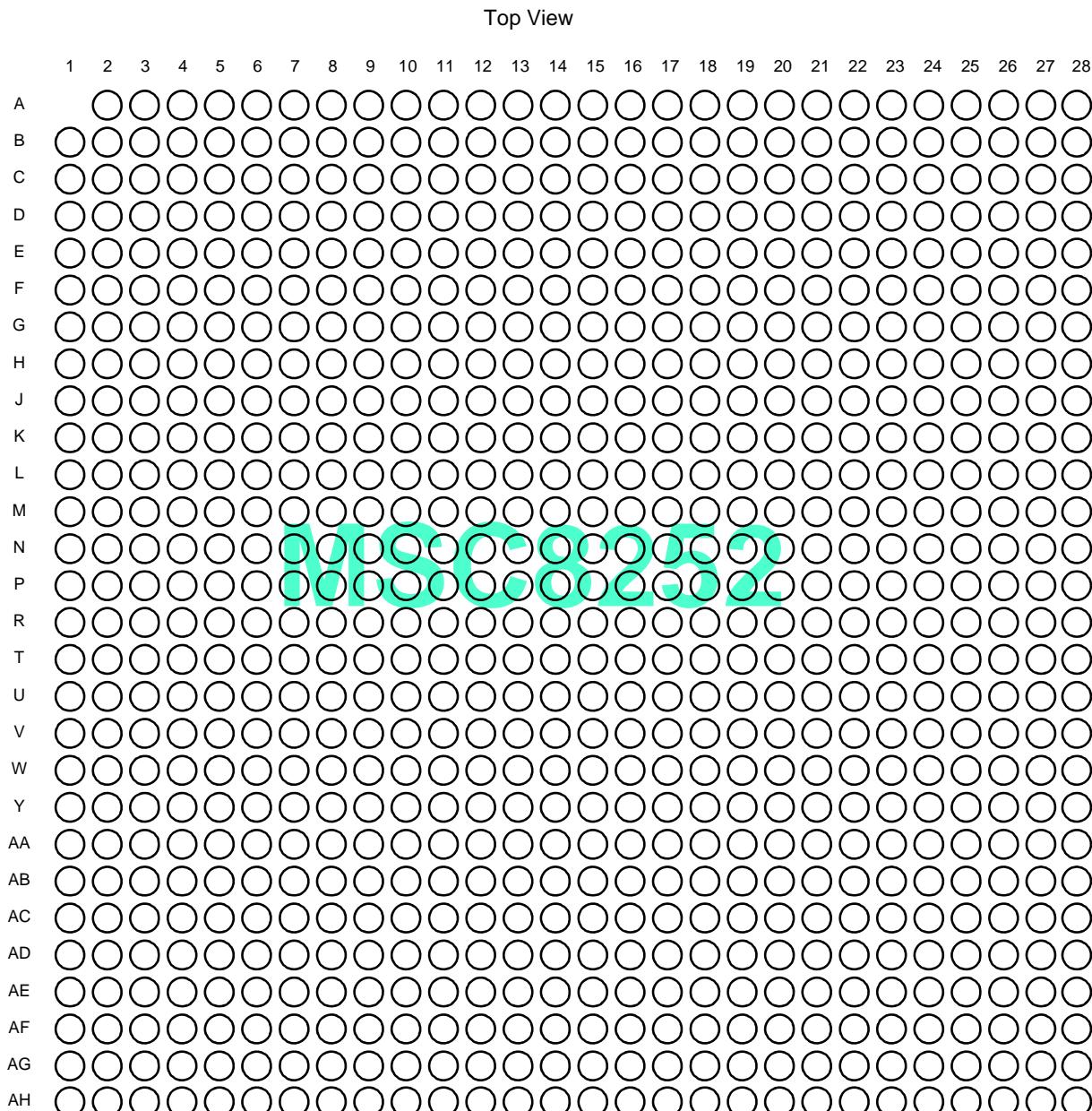


Figure 3. MSC8252 FC-PBGA Package, Top View

1.2 Signal List By Ball Location

Table 1 presents the signal list sorted by ball number. When designing a board, make sure that the power rail for each signal is appropriately considered. The specified power rail must be tied to the voltage level specified in this document if any of the related signal functions are used (active)

Note: The information in Table 1 and Table 2 distinguishes among three concepts. First, the power pins are the balls of the device package used to supply specific power levels for different device subsystems (as opposed to signals). Second, the power rails are the electrical lines on the board that transfer power from the voltage regulators to the device. They are indicated here as the reference power rails for signal lines; therefore, the actual power inputs are listed as N/A with regard to the power rails. Third, symbols used in these tables are the names for the voltage levels (absolute, recommended, and so on) and not the power supplies themselves.

Table 1. Signal List by Ball Number

| Ball Number | Signal Name ^{1,2} | Pin Type ¹⁰ | Power Rail Name |
|-------------|----------------------------|------------------------|-----------------|
| A2 | M2DQS3 | I/O | GVDD2 |
| A3 | M2DQS3 | I/O | GVDD2 |
| A4 | M2ECC0 | I/O | GVDD2 |
| A5 | M2DQS8 | I/O | GVDD2 |
| A6 | M2DQS8 | I/O | GVDD2 |
| A7 | M2A5 | O | GVDD2 |
| A8 | M2CK1 | O | GVDD2 |
| A9 | M2CK1 | O | GVDD2 |
| A10 | M2CS0 | O | GVDD2 |
| A11 | M2BA0 | O | GVDD2 |
| A12 | M2CAS | O | GVDD2 |
| A13 | M2DQ34 | I/O | GVDD2 |
| A14 | M2DQS4 | I/O | GVDD2 |
| A15 | M2DQS4 | I/O | GVDD2 |
| A16 | M2DQ50 | I/O | GVDD2 |
| A17 | M2DQS6 | I/O | GVDD2 |
| A18 | M2DQS6 | I/O | GVDD2 |
| A19 | M2DQ48 | I/O | GVDD2 |
| A20 | M2DQ49 | I/O | GVDD2 |
| A21 | VSS | Ground | N/A |
| A22 | Reserved | NC | — |
| A23 | SXPVDD1 | Power | N/A |
| A24 | SXPVSS1 | Ground | N/A |
| A25 | Reserved | NC | — |
| A26 | Reserved | NC | — |
| A27 | SXCVDD1 | Power | N/A |
| A28 | SXCVSS1 | Ground | N/A |
| B1 | M2DQ24 | I/O | GVDD2 |
| B2 | GVDD2 | Power | N/A |
| B3 | M2DQ25 | I/O | GVDD2 |
| B4 | VSS | Ground | N/A |
| B5 | GVDD2 | Power | N/A |
| B6 | M2ECC1 | I/O | GVDD2 |
| B7 | VSS | Ground | N/A |
| B8 | GVDD2 | Power | N/A |

Table 1. Signal List by Ball Number (continued)

| Ball Number | Signal Name ^{1,2} | Pin Type ¹⁰ | Power Rail Name |
|-------------|----------------------------|------------------------|-----------------|
| B9 | M2A13 | O | GVDD2 |
| B10 | VSS | Ground | N/A |
| B11 | GVDD2 | Power | N/A |
| B12 | M2CS1 | O | GVDD2 |
| B13 | VSS | Ground | N/A |
| B14 | GVDD2 | Power | N/A |
| B15 | M2DQ35 | I/O | GVDD2 |
| B16 | VSS | Ground | N/A |
| B17 | GVDD2 | Power | N/A |
| B18 | M2DQ51 | I/O | GVDD2 |
| B19 | VSS | Ground | N/A |
| B20 | GVDD2 | Power | N/A |
| B21 | Reserved | NC | — |
| B22 | Reserved | NC | — |
| B23 | SR1_TXD0 | O | SXPVDD1 |
| B24 | SR1_RXD0 | O | SXPVDD1 |
| B25 | SXCVDD1 | Power | N/A |
| B26 | SXCVSS1 | Ground | N/A |
| B27 | SR1_RXD0 | I | SXCVDD1 |
| B28 | SR1_RXD0 | I | SXCVDD1 |
| C1 | M2DQ28 | I/O | GVDD2 |
| C2 | M2DM3 | O | GVDD2 |
| C3 | M2DQ26 | I/O | GVDD2 |
| C4 | M2ECC4 | I/O | GVDD2 |
| C5 | M2DM8 | O | GVDD2 |
| C6 | M2ECC2 | I/O | GVDD2 |
| C7 | M2CKE1 | O | GVDD2 |
| C8 | M2CK0 | O | GVDD2 |
| C9 | M2CK0 | O | GVDD2 |
| C10 | M2BA1 | O | GVDD2 |
| C11 | M2A1 | O | GVDD2 |
| C12 | M2WE | O | GVDD2 |
| C13 | M2DQ37 | I/O | GVDD2 |
| C14 | M2DM4 | O | GVDD2 |
| C15 | M2DQ36 | I/O | GVDD2 |
| C16 | M2DQ32 | I/O | GVDD2 |
| C17 | M2DQ55 | I/O | GVDD2 |
| C18 | M2DM6 | O | GVDD2 |
| C19 | M2DQ53 | I/O | GVDD2 |
| C20 | M2DQ52 | I/O | GVDD2 |
| C21 | Reserved | NC | — |
| C22 | SR1_IMP_CAL_RX | I | SXCVDD1 |
| C23 | SXPVSS1 | Ground | N/A |
| C24 | SXPVDD1 | Power | N/A |
| C25 | SR1_REF_CLK | I | SXCVDD1 |
| C26 | SR1_REF_CLK | I | SXCVDD1 |

Table 1. Signal List by Ball Number (continued)

| Ball Number | Signal Name ^{1,2} | Pin Type ¹⁰ | Power Rail Name |
|-------------|----------------------------|------------------------|-----------------|
| C27 | Reserved | NC | — |
| C28 | Reserved | NC | — |
| D1 | GVDD2 | Power | N/A |
| D2 | VSS | Ground | N/A |
| D3 | M2DQ29 | I/O | GVDD2 |
| D4 | GVDD2 | Power | N/A |
| D5 | VSS | Ground | N/A |
| D6 | M2ECC5 | I/O | GVDD2 |
| D7 | GVDD2 | Power | N/A |
| D8 | VSS | Ground | N/A |
| D9 | M2A8 | O | GVDD2 |
| D10 | GVDD2 | Power | N/A |
| D11 | VSS | Ground | N/A |
| D12 | M2A0 | O | GVDD2 |
| D13 | GVDD2 | Power | N/A |
| D14 | VSS | Ground | N/A |
| D15 | M2DQ39 | I/O | GVDD2 |
| D16 | GVDD2 | Power | N/A |
| D17 | VSS | Ground | N/A |
| D18 | M2DQ54 | I/O | GVDD2 |
| D19 | GVDD2 | Power | N/A |
| D20 | VSS | Ground | N/A |
| D21 | SXPVSS1 | Ground | N/A |
| D22 | SXPVDD1 | Power | N/A |
| D23 | SR1_TXD1 | O | SXPVDD1 |
| D24 | SR1_TXD1 | O | SXPVDD1 |
| D25 | SXCVSS1 | Ground | N/A |
| D26 | SXCVDD1 | Power | N/A |
| D27 | SR1_RXD1 | I | SXCVDD1 |
| D28 | SR1_RXD1 | I | SXCVDD1 |
| E1 | M2DQ31 | I/O | GVDD2 |
| E2 | M2DQ30 | I/O | GVDD2 |
| E3 | M2DQ27 | I/O | GVDD2 |
| E4 | M2ECC7 | I/O | GVDD2 |
| E5 | M2ECC6 | I/O | GVDD2 |
| E6 | M2ECC3 | I/O | GVDD2 |
| E7 | M2A9 | O | GVDD2 |
| E8 | M2A6 | O | GVDD2 |
| E9 | M2A3 | O | GVDD2 |
| E10 | M2A10 | O | GVDD2 |
| E11 | M2RAS | O | GVDD2 |
| E12 | M2A2 | O | GVDD2 |
| E13 | M2DQ38 | I/O | GVDD2 |
| E14 | M2DQS5 | I/O | GVDD2 |
| E15 | M2DQS5 | I/O | GVDD2 |
| E16 | M2DQ33 | I/O | GVDD2 |

Table 1. Signal List by Ball Number (continued)

| Ball Number | Signal Name ^{1,2} | Pin Type ¹⁰ | Power Rail Name |
|-------------|------------------------------|------------------------|-----------------|
| E17 | M2DQ56 | I/O | GVDD2 |
| E18 | M2DQ57 | I/O | GVDD2 |
| E19 | <u>M2DQS7</u> | I/O | GVDD2 |
| E20 | Reserved | NC | — |
| E21 | Reserved | NC | — |
| E22 | Reserved | NC | — |
| E23 | SXPVDD1 | Power | N/A |
| E24 | SXPVSS1 | Ground | N/A |
| E25 | SR1_PLL_AGND ⁹ | Ground | SXCVSS1 |
| E26 | SR1_PLL_AVDD ⁹ | Power | SXCVDD1 |
| E27 | SXCVSS1 | Ground | N/A |
| E28 | SXCVDD1 | Power | N/A |
| F1 | VSS | Ground | N/A |
| F2 | GVDD2 | Power | N/A |
| F3 | M2DQ16 | I/O | GVDD2 |
| F4 | VSS | Ground | N/A |
| F5 | GVDD2 | Power | N/A |
| F6 | M2DQ17 | I/O | GVDD2 |
| F7 | VSS | Ground | N/A |
| F8 | GVDD2 | Power | N/A |
| F9 | M2BA2 | O | GVDD2 |
| F10 | VSS | Ground | N/A |
| F11 | GVDD2 | Power | N/A |
| F12 | M2A4 | O | GVDD2 |
| F13 | VSS | Ground | N/A |
| F14 | GVDD2 | Power | N/A |
| F15 | M2DQ42 | I/O | GVDD2 |
| F16 | VSS | Ground | N/A |
| F17 | GVDD2 | Power | N/A |
| F18 | M2DQ58 | I/O | GVDD2 |
| F19 | M2DQS7 | I/O | GVDD2 |
| F20 | GVDD2 | Power | N/A |
| F21 | SXPVDD1 | Power | N/A |
| F22 | SXPVSS1 | Ground | N/A |
| F23 | SR1_TXD2/SG1_TX ⁴ | O | SXPVDD1 |
| F24 | SR1_TXD2/SG1_TX ⁴ | O | SXPVDD1 |
| F25 | SXCVDD1 | Power | N/A |
| F26 | SXCVSS1 | Ground | N/A |
| F27 | SR1_RXD2/SG1_RX ⁴ | I | SXCVDD1 |
| F28 | SR1_RXD2/SG1_RX ⁴ | I | SXCVDD1 |
| G1 | <u>M2DQS2</u> | I/O | GVDD2 |
| G2 | M2DQS2 | I/O | GVDD2 |
| G3 | M2DQ19 | I/O | GVDD2 |
| G4 | M2DM2 | O | GVDD2 |
| G5 | M2DQ21 | I/O | GVDD2 |
| G6 | M2DQ22 | I/O | GVDD2 |

Table 1. Signal List by Ball Number (continued)

| Ball Number | Signal Name ^{1,2} | Pin Type ¹⁰ | Power Rail Name |
|-------------|------------------------------|------------------------|-----------------|
| G7 | M2CKE0 | O | GVDD2 |
| G8 | M2A11 | O | GVDD2 |
| G9 | M2A7 | O | GVDD2 |
| G10 | M2CK2 | O | GVDD2 |
| G11 | M2APAR_OUT | O | GVDD2 |
| G12 | M2ODT1 | O | GVDD2 |
| G13 | M2APAR_IN | I | GVDD2 |
| G14 | M2DQ43 | I/O | GVDD2 |
| G15 | M2DM5 | O | GVDD2 |
| G16 | M2DQ44 | I/O | GVDD2 |
| G17 | M2DQ40 | I/O | GVDD2 |
| G18 | M2DQ59 | I/O | GVDD2 |
| G19 | M2DM7 | O | GVDD2 |
| G20 | M2DQ60 | I/O | GVDD2 |
| G21 | Reserved | NC | — |
| G22 | Reserved | NC | — |
| G23 | SXPVSS1 | Ground | N/A |
| G24 | SXPVDD1 | Power | N/A |
| G25 | SR1_IMP_CAL_TX | I | SXCVDD1 |
| G26 | SXCVSS1 | Ground | N/A |
| G27 | Reserved | NC | — |
| G28 | Reserved | NC | — |
| H1 | GVDD2 | Power | N/A |
| H2 | VSS | Ground | N/A |
| H3 | M2DQ18 | I/O | GVDD2 |
| H4 | GVDD2 | Power | N/A |
| H5 | VSS | Ground | N/A |
| H6 | M2DQ20 | I/O | GVDD2 |
| H7 | GVDD2 | Power | N/A |
| H8 | VSS | Ground | N/A |
| H9 | M2A15 | O | GVDD2 |
| H10 | M2CK2 | O | GVDD2 |
| H11 | M2MDIC0 | I/O | GVDD2 |
| H12 | M2VREF | I | GVDD2 |
| H13 | M2MDIC1 | I/O | GVDD2 |
| H14 | M2DQ46 | I/O | GVDD2 |
| H15 | M2DQ47 | I/O | GVDD2 |
| H16 | M2DQ45 | I/O | GVDD2 |
| H17 | M2DQ41 | I/O | GVDD2 |
| H18 | M2DQ62 | I/O | GVDD2 |
| H19 | M2DQ63 | I/O | GVDD2 |
| H20 | M2DQ61 | I/O | GVDD2 |
| H21 | Reserved | NC | — |
| H22 | Reserved | NC | — |
| H23 | SR1_TXD3/SG2_TX ⁴ | O | SXPVDD1 |
| H24 | SR1_TXD3/SG2_TX ⁴ | O | SXPVDD1 |

Table 1. Signal List by Ball Number (continued)

| Ball Number | Signal Name ^{1,2} | Pin Type ¹⁰ | Power Rail Name |
|-------------|------------------------------|------------------------|-----------------|
| H25 | SXCVSS1 | Ground | N/A |
| H26 | SXCVDD1 | Power | N/A |
| H27 | SR1_RXD3/SG2_RX ⁴ | I | SXCVDD1 |
| H28 | SR1_RXD3/SG2_RX ⁴ | I | SXCVDD1 |
| J1 | M2DQS1 | I/O | GVDD2 |
| J2 | M2DQS1 | I/O | GVDD2 |
| J3 | M2DQ10 | I/O | GVDD2 |
| J4 | M2DQ11 | I/O | GVDD2 |
| J5 | M2DQ14 | I/O | GVDD2 |
| J6 | M2DQ23 | I/O | GVDD2 |
| J7 | M2ODT0 | O | GVDD2 |
| J8 | M2A12 | O | GVDD2 |
| J9 | M2A14 | O | GVDD2 |
| J10 | VSS | Ground | N/A |
| J11 | GVDD2 | Power | N/A |
| J12 | VSS | Ground | N/A |
| J13 | GVDD2 | Power | N/A |
| J14 | VSS | Ground | N/A |
| J15 | GVDD2 | Power | N/A |
| J16 | VSS | Ground | N/A |
| J17 | GVDD2 | Power | N/A |
| J18 | VSS | Ground | N/A |
| J19 | GVDD2 | Power | N/A |
| J20 | Reserved | NC | — |
| J21 | Reserved | NC | — |
| J22 | Reserved | NC | — |
| J23 | SXPVDD1 | Power | N/A |
| J24 | SXPVSS1 | Ground | N/A |
| J25 | SXCVDD1 | Power | N/A |
| J26 | SXCVSS1 | Ground | N/A |
| J27 | SXCVDD1 | Power | N/A |
| J28 | SXCVSS1 | Ground | N/A |
| K1 | VSS | Ground | N/A |
| K2 | GVDD2 | Power | N/A |
| K3 | M2DM1 | O | GVDD2 |
| K4 | VSS | Ground | N/A |
| K5 | GVDD2 | Power | N/A |
| K6 | M2DQ0 | I/O | GVDD2 |
| K7 | VSS | Ground | N/A |
| K8 | GVDD2 | Power | N/A |
| K9 | M2DQ5 | I/O | GVDD2 |
| K10 | VSS | Ground | N/A |
| K11 | VDD | Power | N/A |
| K12 | VSS | Ground | N/A |
| K13 | VDD | Power | N/A |
| K14 | VSS | Ground | N/A |

Table 1. Signal List by Ball Number (continued)

| Ball Number | Signal Name ^{1,2} | Pin Type ¹⁰ | Power Rail Name |
|-------------|--------------------------------------|------------------------|-----------------|
| K15 | VDD | Power | N/A |
| K16 | VSS | Ground | N/A |
| K17 | VSS | Ground | N/A |
| K18 | VSS | Ground | N/A |
| K19 | VDD | Power | N/A |
| K20 | Reserved | NC | — |
| K21 | Reserved | NC | — |
| K22 | Reserved | NC | — |
| K23 | SXPVDD2 | Power | N/A |
| K24 | SXPVSS2 | Ground | N/A |
| K25 | SXCVDD2 | Power | N/A |
| K26 | SXCVSS2 | Ground | N/A |
| K27 | SXCVDD2 | Power | N/A |
| K28 | SXCVSS2 | Ground | N/A |
| L1 | M2DQ9 | I/O | GVDD2 |
| L2 | M2DQ12 | I/O | GVDD2 |
| L3 | M2DQ13 | I/O | GVDD2 |
| L4 | M2DQS0 | I/O | GVDD2 |
| L5 | M2DQS0 | I/O | GVDD2 |
| L6 | M2DM0 | O | GVDD2 |
| L7 | M2DQ3 | I/O | GVDD2 |
| L8 | M2DQ2 | I/O | GVDD2 |
| L9 | M2DQ4 | I/O | GVDD2 |
| L10 | VDD | Power | N/A |
| L11 | VSS | Ground | N/A |
| L12 | M3VDD | Power | N/A |
| L13 | VSS | Ground | N/A |
| L14 | VSS | Ground | N/A |
| L15 | VSS | Ground | N/A |
| L16 | VSS | Ground | N/A |
| L17 | VSS | Ground | N/A |
| L18 | VDD | Power | N/A |
| L19 | VSS | Ground | N/A |
| L20 | Reserved | NC | — |
| L21 | Reserved | NC | — |
| L22 | Reserved | NC | — |
| L23 | SR2_RXD3/PE_RXD3/SG2_RX ⁴ | O | SXPVDD2 |
| L24 | SR2_RXD3/PE_RXD3/SG2_RX ⁴ | O | SXPVDD2 |
| L25 | SXCVSS2 | Ground | N/A |
| L26 | SXCVDD2 | Power | N/A |
| L27 | SR2_RXD3/PE_RXD3/SG2_RX ⁴ | I | SXCVDD2 |
| L28 | SR2_RXD3/PE_RXD3/SG2_RX ⁴ | I | SXCVDD2 |
| M1 | M2DQ8 | I/O | GVDD2 |
| M2 | VSS | Ground | N/A |
| M3 | GVDD2 | Power | N/A |
| M4 | M2DQ15 | I/O | GVDD2 |

Table 1. Signal List by Ball Number (continued)

| Ball Number | Signal Name ^{1,2} | Pin Type ¹⁰ | Power Rail Name |
|-------------|----------------------------|------------------------|-----------------|
| M5 | M2DQ1 | I/O | GVDD2 |
| M6 | VSS | Ground | N/A |
| M7 | GVDD2 | Power | N/A |
| M8 | M2DQ7 | I/O | GVDD2 |
| M9 | M2DQ6 | I/O | GVDD2 |
| M10 | VSS | Ground | N/A |
| M11 | VDD | Power | N/A |
| M12 | VSS | Ground | N/A |
| M13 | VDD | Power | N/A |
| M14 | VSS | Ground | N/A |
| M15 | VSS | Ground | N/A |
| M16 | VSS | Ground | N/A |
| M17 | VSS | Ground | N/A |
| M18 | VSS | Ground | N/A |
| M19 | VDD | Power | N/A |
| M20 | Reserved | NC | — |
| M21 | Reserved | NC | — |
| M22 | Reserved | NC | — |
| M23 | SXPVSS2 | Ground | N/A |
| M24 | SXPVDD2 | Power | N/A |
| M25 | SR2_IMP_CAL_TX | I | SXCVDD2 |
| M26 | SXCVSS2 | Ground | N/A |
| M27 | Reserved | NC | — |
| M28 | Reserved | NC | — |
| N1 | VSS | Ground | N/A |
| N2 | TRST ⁷ | I | QVDD |
| N3 | PORESET ⁷ | I | QVDD |
| N4 | VSS | Ground | N/A |
| N5 | TMS ⁷ | I | QVDD |
| N6 | CLKOUT | O | QVDD |
| N7 | VSS | Ground | N/A |
| N8 | VSS | Ground | N/A |
| N9 | VSS | Ground | N/A |
| N10 | VDD | Power | N/A |
| N11 | VSS | Ground | N/A |
| N12 | M3VDD | Power | N/A |
| N13 | VSS | Ground | N/A |
| N14 | VSS | Ground | N/A |
| N15 | VSS | Ground | N/A |
| N16 | VDD | Power | N/A |
| N17 | VSS | Ground | N/A |
| N18 | VDD | Power | N/A |
| N19 | VSS | Ground | N/A |
| N20 | Reserved | NC | — |
| N21 | SXPVDD2 | Power | N/A |
| N22 | SXPVSS2 | Ground | N/A |

Table 1. Signal List by Ball Number (continued)

| Ball Number | Signal Name ^{1,2} | Pin Type ¹⁰ | Power Rail Name |
|-------------|--------------------------------------|------------------------|-----------------|
| N23 | SR2_TXD2/PE_TXD2/SG1_TX ⁴ | O | SXPVDD2 |
| N24 | SR2_TXD2/PE_TXD2/SG1_TX ⁴ | O | SXPVDD2 |
| N25 | SXCVDD2 | Power | N/A |
| N26 | SXCVSS2 | Ground | N/A |
| N27 | SR2_RXD2/PE_RXD2/SG1_RX ⁴ | I | SXCVDD2 |
| N28 | SR2_RXD2/PE_RXD2/SG1_RX ⁴ | I | SXCVDD2 |
| P1 | CLKIN | I | QVDD |
| P2 | EE0 | I | QVDD |
| P3 | QVDD | Power | N/A |
| P4 | VSS | Ground | N/A |
| P5 | STOP_BS | I | QVDD |
| P6 | QVDD | Power | N/A |
| P7 | VSS | Ground | N/A |
| P8 | PLL0_AVDD ⁹ | Power | VDD |
| P9 | PLL2_AVDD ⁹ | Power | VDD |
| P10 | VSS | Ground | N/A |
| P11 | VDD | Power | N/A |
| P12 | VSS | Ground | N/A |
| P13 | VDD | Power | N/A |
| P14 | VSS | Ground | N/A |
| P15 | VSS | Ground | N/A |
| P16 | VSS | Ground | N/A |
| P17 | VSS | Ground | N/A |
| P18 | VSS | Ground | N/A |
| P19 | VDD | Power | N/A |
| P20 | Reserved | NC | — |
| P21 | Reserved | NC | — |
| P22 | Reserved | NC | — |
| P23 | SXPVDD2 | Power | N/A |
| P24 | SXPVSS2 | Ground | N/A |
| P25 | SR2_PLL_AGND ⁹ | Ground | SXCVSS2 |
| P26 | SR2_PLL_AVDD ⁹ | Power | SXCVDD2 |
| P27 | SXCVSS2 | Ground | N/A |
| P28 | SXCVDD2 | Power | N/A |
| R1 | VSS | Ground | N/A |
| R2 | NMI | I | QVDD |
| R3 | NMI_OUT ⁶ | O | QVDD |
| R4 | HRESET ^{6,7} | I/O | QVDD |
| R5 | INT_OUT ⁶ | O | QVDD |
| R6 | EE1 | O | QVDD |
| R7 | VSS | Ground | N/A |
| R8 | PLL1_AVDD ⁹ | Power | VDD |
| R9 | VSS | Ground | N/A |
| R10 | VDD | Power | N/A |
| R11 | VSS | Non-user | N/A |
| R12 | VDD | Power | N/A |

Table 1. Signal List by Ball Number (continued)

| Ball Number | Signal Name ^{1,2} | Pin Type ¹⁰ | Power Rail Name |
|-------------|-------------------------------|------------------------|-----------------|
| R13 | VSS | Ground | N/A |
| R14 | VDD | Power | N/A |
| R15 | VSS | Ground | N/A |
| R16 | VSS | Ground | N/A |
| R17 | VSS | Ground | N/A |
| R18 | VDD | Power | N/A |
| R19 | VSS | Ground | N/A |
| R20 | VSS | Non-user | N/A |
| R21 | SXPVSS2 | Ground | N/A |
| R22 | SXPVDD2 | Power | N/A |
| R23 | SR2_TXD1/PE_TXD1 ⁴ | O | SXPVDD2 |
| R24 | SR2_TXD1/PE_TXD1 ⁴ | O | SXPVDD2 |
| R25 | SXCVSS2 | Ground | N/A |
| R26 | SXCVDD2 | Power | N/A |
| R27 | SR2_RXD1/PE_RXD1 ⁴ | I | SXCVDD2 |
| R28 | SR2_RXD1/PE_RXD1 ⁴ | I | SXCVDD2 |
| T1 | VSS | Ground | N/A |
| T2 | TCK | I | QVDD |
| T3 | SRESET ^{6,7} | I/O | QVDD |
| T4 | TDI | I | QVDD |
| T5 | VSS | Ground | N/A |
| T6 | TDO | O | QVDD |
| T7 | VSS | Ground | N/A |
| T8 | VSS | Ground | N/A |
| T9 | QVDD | Power | N/A |
| T10 | VSS | Ground | N/A |
| T11 | VDD | Power | N/A |
| T12 | VSS | Ground | N/A |
| T13 | M3VDD | Power | N/A |
| T14 | VSS | Ground | N/A |
| T15 | VDD | Power | N/A |
| T16 | VSS | Ground | N/A |
| T17 | VSS | Ground | N/A |
| T18 | VSS | Ground | N/A |
| T19 | VDD | Power | N/A |
| T20 | VSS | Ground | N/A |
| T21 | VSS | Non-user | N/A |
| T22 | SR2_IMP_CAL_RX | I | SXCVDD2 |
| T23 | SXPVSS2 | Ground | N/A |
| T24 | SXPVDD2 | Power | N/A |
| T25 | SR2_REF_CLK | I | SXCVDD2 |
| T26 | SR2_REF_CLK | I | SXCVDD2 |
| T27 | Reserved | NC | — |
| T28 | Reserved | NC | — |
| U1 | M1DQ8 | I/O | GVDD1 |
| U2 | VSS | Ground | N/A |

Table 1. Signal List by Ball Number (continued)

| Ball Number | Signal Name ^{1,2} | Pin Type ¹⁰ | Power Rail Name |
|-------------|-------------------------------|------------------------|-----------------|
| U3 | GVDD1 | Power | N/A |
| U4 | M1DQ15 | I/O | GVDD1 |
| U5 | M1DQ1 | I/O | GVDD1 |
| U6 | VSS | Ground | N/A |
| U7 | GVDD1 | Power | N/A |
| U8 | M1DQ7 | I/O | GVDD1 |
| U9 | M1DQ6 | I/O | GVDD1 |
| U10 | VDD | Power | N/A |
| U11 | VSS | Ground | N/A |
| U12 | M3VDD | Power | N/A |
| U13 | VSS | Ground | N/A |
| U14 | VDD | Power | N/A |
| U15 | VSS | Ground | N/A |
| U16 | VDD | Power | N/A |
| U17 | VSS | Ground | N/A |
| U18 | VDD | Power | N/A |
| U19 | VSS | Ground | N/A |
| U20 | VSS | Ground | N/A |
| U21 | VSS | Ground | N/A |
| U22 | VSS | Non-user | N/A |
| U23 | SR2_RXD0/PE_RXD0 ⁴ | O | SXPVDD2 |
| U24 | SR2_RXD0/PE_RXD0 ⁴ | O | SXPVDD2 |
| U25 | SXCVDD2 | Power | N/A |
| U26 | SXCVSS2 | Ground | N/A |
| U27 | SR2_RXD0/PE_RXD0 ⁴ | I | SXCVDD2 |
| U28 | SR2_RXD0/PE_RXD0 ⁴ | I | SXCVDD2 |
| V1 | M1DQ9 | I/O | GVDD1 |
| V2 | M1DQ12 | I/O | GVDD1 |
| V3 | M1DQ13 | I/O | GVDD1 |
| V4 | M1DQS0 | I/O | GVDD1 |
| V5 | M1DQS0 | I/O | GVDD1 |
| V6 | M1DM0 | O | GVDD1 |
| V7 | M1DQ3 | I/O | GVDD1 |
| V8 | M1DQ2 | I/O | GVDD1 |
| V9 | M1DQ4 | I/O | GVDD1 |
| V10 | VSS | Ground | N/A |
| V11 | VDD | Power | N/A |
| V12 | VSS | Ground | N/A |
| V13 | VDD | Power | N/A |
| V14 | VSS | Ground | N/A |
| V15 | VDD | Power | N/A |
| V16 | VSS | Ground | N/A |
| V17 | VDD | Power | N/A |
| V18 | VSS | Ground | N/A |
| V19 | VDD | Power | N/A |
| V20 | NVDD | Power | N/A |

Table 1. Signal List by Ball Number (continued)

| Ball Number | Signal Name ^{1,2} | Pin Type ¹⁰ | Power Rail Name |
|-------------|------------------------------------|------------------------|-----------------|
| V21 | RCW_LSEL_3/RC20 | I/O | NVDD |
| V22 | RCW_LSEL_2/RC19 | I/O | NVDD |
| V23 | SXPVDD2 | Power | N/A |
| V24 | SXPVSS2 | Ground | N/A |
| V25 | RCW_LSEL_1/RC18 | I/O | NVDD |
| V26 | RC21 | I | NVDD |
| V27 | SXCVDD2 | Power | N/A |
| V28 | SXCVSS2 | Ground | N/A |
| W1 | VSS | Ground | N/A |
| W2 | GVDD1 | Power | N/A |
| W3 | M1DM1 | O | GVDD1 |
| W4 | VSS | Ground | N/A |
| W5 | GVDD1 | Power | N/A |
| W6 | M1DQ0 | I/O | GVDD1 |
| W7 | VSS | Ground | N/A |
| W8 | GVDD1 | Power | N/A |
| W9 | M1DQ5 | I/O | GVDD1 |
| W10 | VDD | Power | N/A |
| W11 | VSS | Ground | N/A |
| W12 | VDD | Power | N/A |
| W13 | VSS | Ground | N/A |
| W14 | VDD | Power | N/A |
| W15 | VSS | Ground | N/A |
| W16 | VDD | Power | N/A |
| W17 | VSS | Ground | N/A |
| W18 | VDD | Power | N/A |
| W19 | VSS | Ground | N/A |
| W20 | VSS | Ground | N/A |
| W21 | RCW_LSEL0/RC17 | I/O | NVDD |
| W22 | GPIO19/SPI_MISO ^{5,8} | I/O | NVDD |
| W23 | VSS | Ground | N/A |
| W24 | NVDD | Power | N/A |
| W25 | GPIO11/IRQ11/RC11 ^{5,8} | I/O | NVDD |
| W26 | GPIO3/DRQ1/IRQ3/RC3 ^{5,8} | I/O | NVDD |
| W27 | GPIO7/IRQ7/RC7 ^{5,8} | I/O | NVDD |
| W28 | GPIO2/IRQ2/RC2 ^{5,8} | I/O | NVDD |
| Y1 | M1DQS1 | I/O | GVDD1 |
| Y2 | M1DQS1 | I/O | GVDD1 |
| Y3 | M1DQ10 | I/O | GVDD1 |
| Y4 | M1DQ11 | I/O | GVDD1 |
| Y5 | M1DQ14 | I/O | GVDD1 |
| Y6 | M1DQ23 | I/O | GVDD1 |
| Y7 | M1ODT0 | O | GVDD1 |
| Y8 | M1A12 | O | GVDD1 |
| Y9 | M1A14 | O | GVDD1 |
| Y10 | VSS | Ground | N/A |

Table 1. Signal List by Ball Number (continued)

| Ball Number | Signal Name ^{1,2} | Pin Type ¹⁰ | Power Rail Name |
|-------------|---------------------------------------|------------------------|-----------------|
| Y11 | GVDD1 | Power | N/A |
| Y12 | VSS | Ground | N/A |
| Y13 | GVDD1 | Power | N/A |
| Y14 | VSS | Ground | N/A |
| Y15 | GVDD1 | Power | N/A |
| Y16 | VSS | Ground | N/A |
| Y17 | GVDD1 | Power | N/A |
| Y18 | VSS | Ground | N/A |
| Y19 | GVDD1 | Power | N/A |
| Y20 | VSS | Ground | N/A |
| Y21 | NVDD | Power | N/A |
| Y22 | GPIO20/SPI_SL ^{5,8} | I/O | NVDD |
| Y23 | GPIO17/SPI_SCK ^{5,8} | I/O | NVDD |
| Y24 | GPIO14/DRQ0/IRQ14/RC14 ^{5,8} | I/O | NVDD |
| Y25 | GPIO12/IRQ12/RC12 ^{5,8} | I/O | NVDD |
| Y26 | GPIO8/IRQ8/RC8 ^{5,8} | I/O | NVDD |
| Y27 | NVDD | Power | N/A |
| Y28 | VSS | Ground | N/A |
| AA1 | GVDD1 | Power | N/A |
| AA2 | VSS | Ground | N/A |
| AA3 | M1DQ18 | I/O | GVDD1 |
| AA4 | GVDD1 | Power | N/A |
| AA5 | VSS | Ground | N/A |
| AA6 | M1DQ20 | I/O | GVDD1 |
| AA7 | GVDD1 | Power | N/A |
| AA8 | VSS | Ground | N/A |
| AA9 | M1A15 | O | GVDD1 |
| AA10 | M1CK2 | O | GVDD1 |
| AA11 | M1MDIC0 | I/O | GVDD1 |
| AA12 | M1VREF | I | GVDD1 |
| AA13 | M1MDIC1 | I/O | GVDD1 |
| AA14 | M1DQ46 | I/O | GVDD1 |
| AA15 | M1DQ47 | I/O | GVDD1 |
| AA16 | M1DQ45 | I/O | GVDD1 |
| AA17 | M1DQ41 | I/O | GVDD1 |
| AA18 | M1DQ62 | I/O | GVDD1 |
| AA19 | M1DQ63 | I/O | GVDD1 |
| AA20 | M1DQ61 | I/O | GVDD1 |
| AA21 | VSS | Ground | N/A |
| AA22 | GPIO21 ^{5,8} | I/O | NVDD |
| AA23 | GPIO18/SPI_MOSI ^{5,8} | I/O | NVDD |
| AA24 | GPIO16/RC16 ^{5,8} | I/O | NVDD |
| AA25 | GPIO4/DDN1/IRQ4/RC4 ^{5,8} | I/O | NVDD |
| AA26 | GPIO9/IRQ9/RC9 ^{5,8} | I/O | NVDD |
| AA27 | GPIO6/IRQ6/RC6 ^{5,8} | I/O | NVDD |
| AA28 | GPIO1/IRQ1/RC1 ^{5,8} | I/O | NVDD |

Table 1. Signal List by Ball Number (continued)

| Ball Number | Signal Name ^{1,2} | Pin Type ¹⁰ | Power Rail Name |
|-------------|-------------------------------------|------------------------|-----------------|
| AB1 | M1DQS2 | I/O | GVDD1 |
| AB2 | M1DQS2 | I/O | GVDD1 |
| AB3 | M1DQ19 | I/O | GVDD1 |
| AB4 | M1DM2 | O | GVDD1 |
| AB5 | M1DQ21 | I/O | GVDD1 |
| AB6 | M1DQ22 | I/O | GVDD1 |
| AB7 | M1CKE0 | O | GVDD1 |
| AB8 | M1A11 | O | GVDD1 |
| AB9 | M1A7 | O | GVDD1 |
| AB10 | M1CK2 | O | GVDD1 |
| AB11 | M1APAR_OUT | O | GVDD1 |
| AB12 | M1ODT1 | O | GVDD1 |
| AB13 | M1APAR_IN | I | GVDD1 |
| AB14 | M1DQ43 | I/O | GVDD1 |
| AB15 | M1DM5 | O | GVDD1 |
| AB16 | M1DQ44 | I/O | GVDD1 |
| AB17 | M1DQ40 | I/O | GVDD1 |
| AB18 | M1DQ59 | I/O | GVDD1 |
| AB19 | M1DM7 | O | GVDD1 |
| AB20 | M1DQ60 | I/O | GVDD1 |
| AB21 | VSS | Ground | N/A |
| AB22 | GPIO31/I2C_SDA ^{5,8} | I/O | NVDD |
| AB23 | GPIO27/TMR4/RCW_SRC0 ^{5,8} | I/O | NVDD |
| AB24 | GPIO25/TMR2/RCW_SRC1 ^{5,8} | I/O | NVDD |
| AB25 | GPIO24/TMR1/RCW_SRC2 ^{5,8} | I/O | NVDD |
| AB26 | GPIO10/IRQ10/RC10 ^{5,8} | I/O | NVDD |
| AB27 | GPIO5/IRQ5/RC5 ^{5,8} | I/O | NVDD |
| AB28 | GPIO0/IRQ0/RC0 ^{5,8} | I/O | NVDD |
| AC1 | VSS | Ground | N/A |
| AC2 | GVDD1 | Power | N/A |
| AC3 | M1DQ16 | I/O | GVDD1 |
| AC4 | VSS | Ground | N/A |
| AC5 | GVDD1 | Power | N/A |
| AC6 | M1DQ17 | I/O | GVDD1 |
| AC7 | VSS | Ground | N/A |
| AC8 | GVDD1 | Power | N/A |
| AC9 | M1BA2 | O | GVDD1 |
| AC10 | VSS | Ground | N/A |
| AC11 | GVDD1 | Power | N/A |
| AC12 | M1A4 | O | GVDD1 |
| AC13 | VSS | Ground | N/A |
| AC14 | GVDD1 | Power | N/A |
| AC15 | M1DQ42 | I/O | GVDD1 |
| AC16 | VSS | Ground | N/A |
| AC17 | GVDD1 | Power | N/A |
| AC18 | M1DQ58 | I/O | GVDD1 |

Table 1. Signal List by Ball Number (continued)

| Ball Number | Signal Name ^{1,2} | Pin Type ¹⁰ | Power Rail Name |
|-------------|---------------------------------------|------------------------|-----------------|
| AC19 | VSS | Ground | N/A |
| AC20 | GVDD1 | Power | N/A |
| AC21 | VSS | Ground | N/A |
| AC22 | NVDD | Power | N/A |
| AC23 | GPIO30/I2C_SCL ^{5,8} | I/O | NVDD |
| AC24 | GPIO26/TMR3 ^{5,8} | I/O | NVDD |
| AC25 | VSS | Ground | N/A |
| AC26 | NVDD | Power | N/A |
| AC27 | GPIO23/TMR0 ^{5,8} | I/O | NVDD |
| AC28 | GPIO22 ^{5,8} | I/O | NVDD |
| AD1 | M1DQ31 | I/O | GVDD1 |
| AD2 | M1DQ30 | I/O | GVDD1 |
| AD3 | M1DQ27 | I/O | GVDD1 |
| AD4 | M1ECC7 | I/O | GVDD1 |
| AD5 | M1ECC6 | I/O | GVDD1 |
| AD6 | M1ECC3 | I/O | GVDD1 |
| AD7 | M1A9 | O | GVDD1 |
| AD8 | M1A6 | O | GVDD1 |
| AD9 | M1A3 | O | GVDD1 |
| AD10 | M1A10 | O | GVDD1 |
| AD11 | <u>M1RAS</u> | O | GVDD1 |
| AD12 | M1A2 | O | GVDD1 |
| AD13 | M1DQ38 | I/O | GVDD1 |
| AD14 | <u>M1DQS5</u> | I/O | GVDD1 |
| AD15 | M1DQS5 | I/O | GVDD1 |
| AD16 | M1DQ33 | I/O | GVDD1 |
| AD17 | M1DQ56 | I/O | GVDD1 |
| AD18 | M1DQ57 | I/O | GVDD1 |
| AD19 | <u>M1DQS7</u> | I/O | GVDD1 |
| AD20 | M1DQS7 | I/O | GVDD1 |
| AD21 | VSS | Ground | N/A |
| AD22 | GE2_TX_CTL | O | NVDD |
| AD23 | GPIO15/DDN0/IRQ15/RC15 ^{5,8} | I/O | NVDD |
| AD24 | GPIO13/IRQ13/RC13 ^{5,8} | I/O | NVDD |
| AD25 | GE_MDC | O | NVDD |
| AD26 | GE_MDIO | I/O | NVDD |
| AD27 | TDM2TCK/GE1_TD3 ³ | I/O | NVDD |
| AD28 | TDM2RCK/GE1_TD0 ³ | I/O | NVDD |
| AE1 | GVDD1 | Power | N/A |
| AE2 | VSS | Ground | N/A |
| AE3 | M1DQ29 | I/O | GVDD1 |
| AE4 | GVDD1 | Power | N/A |
| AE5 | VSS | Ground | N/A |
| AE6 | M1ECC5 | I/O | GVDD1 |
| AE7 | GVDD1 | Power | N/A |
| AE8 | VSS | Ground | N/A |

Table 1. Signal List by Ball Number (continued)

| Ball Number | Signal Name ^{1,2} | Pin Type ¹⁰ | Power Rail Name |
|-------------|----------------------------------|------------------------|-----------------|
| AE9 | M1A8 | O | GVDD1 |
| AE10 | GVDD1 | Power | N/A |
| AE11 | VSS | Ground | N/A |
| AE12 | M1A0 | O | GVDD1 |
| AE13 | GVDD1 | Power | N/A |
| AE14 | VSS | Ground | N/A |
| AE15 | M1DQ39 | I/O | GVDD1 |
| AE16 | GVDD1 | Power | N/A |
| AE17 | VSS | Ground | N/A |
| AE18 | M1DQ54 | I/O | GVDD1 |
| AE19 | GVDD1 | Power | N/A |
| AE20 | VSS | Ground | N/A |
| AE21 | GPIO29/UART_TXD ^{5,8} | I/O | NVDD |
| AE22 | TDM1TCK/GE2_RX_CLK ³ | I | NVDD |
| AE23 | TDM1RSN/GE2_RX_CTL ³ | I/O | NVDD |
| AE24 | VSS | Ground | N/A |
| AE25 | TDM3RCK/GE1_GTX_CLK ³ | I/O | NVDD |
| AE26 | TDM3TSN/GE1_RX_CLK ³ | I/O | NVDD |
| AE27 | TDM2RSN/GE1_TD2 ³ | I/O | NVDD |
| AE28 | TDM2RDT/GE1_TD1 ³ | I/O | NVDD |
| AF1 | M1DQ28 | I/O | GVDD1 |
| AF2 | M1DM3 | O | GVDD1 |
| AF3 | M1DQ26 | I/O | GVDD1 |
| AF4 | M1ECC4 | I/O | GVDD1 |
| AF5 | M1DM8 | O | GVDD1 |
| AF6 | M1ECC2 | I/O | GVDD1 |
| AF7 | M1CKE1 | O | GVDD1 |
| AF8 | M1CK0 | O | GVDD1 |
| AF9 | M1CK0 | O | GVDD1 |
| AF10 | M1BA1 | O | GVDD1 |
| AF11 | M1A1 | O | GVDD1 |
| AF12 | M1WE | O | GVDD1 |
| AF13 | M1DQ37 | I/O | GVDD1 |
| AF14 | M1DM4 | O | GVDD1 |
| AF15 | M1DQ36 | I/O | GVDD1 |
| AF16 | M1DQ32 | I/O | GVDD1 |
| AF17 | M1DQ55 | I/O | GVDD1 |
| AF18 | M1DM6 | O | GVDD1 |
| AF19 | M1DQ53 | I/O | GVDD1 |
| AF20 | M1DQ52 | I/O | GVDD1 |
| AF21 | GPIO28/UART_RXD ^{5,8} | I/O | NVDD |
| AF22 | TDM0RSN/GE2_TD2 ³ | I/O | NVDD |
| AF23 | TDM0TDT/GE2_TD3 ³ | I/O | NVDD |
| AF24 | NVDD | Power | N/A |
| AF25 | TDM2TSN/GE1_TX_CTL ³ | I/O | NVDD |
| AF26 | GE1_RX_CTL | I | NVDD |

Table 1. Signal List by Ball Number (continued)

| Ball Number | Signal Name ^{1,2} | Pin Type ¹⁰ | Power Rail Name |
|-------------|----------------------------------|------------------------|-----------------|
| AF27 | TDM2TDT/GE1_TX_CLK ³ | I/O | NVDD |
| AF28 | TDM3RSN/GE1_RD1 ³ | I/O | NVDD |
| AG1 | M1DQ24 | I/O | GVDD1 |
| AG2 | GVDD1 | Power | N/A |
| AG3 | M1DQ25 | I/O | GVDD1 |
| AG4 | VSS | Ground | N/A |
| AG5 | GVDD1 | Power | N/A |
| AG6 | M1ECC1 | I/O | GVDD1 |
| AG7 | VSS | Ground | N/A |
| AG8 | GVDD1 | Power | N/A |
| AG9 | M1A13 | O | GVDD1 |
| AG10 | VSS | Ground | N/A |
| AG11 | GVDD1 | Power | N/A |
| AG12 | M1CS1 | O | GVDD1 |
| AG13 | VSS | Ground | N/A |
| AG14 | GVDD1 | Power | N/A |
| AG15 | M1DQ35 | I/O | GVDD1 |
| AG16 | VSS | Ground | N/A |
| AG17 | GVDD1 | Power | N/A |
| AG18 | M1DQ51 | I/O | GVDD1 |
| AG19 | VSS | Ground | N/A |
| AG20 | GVDD1 | Power | N/A |
| AG21 | NVDD | Power | N/A |
| AG22 | TDM1TSN/GE2_TD1 ³ | I/O | NVDD |
| AG23 | TDM1RDT/GE2_TX_CLK ³ | I/O | NVDD |
| AG24 | TDM0TCK/GE2_GTX_CLK ³ | I/O | NVDD |
| AG25 | TDM1TDT/GE2_TD0 ³ | I/O | NVDD |
| AG26 | VSS | Ground | N/A |
| AG27 | NVDD | Power | N/A |
| AG28 | TDM3RDT/GE1_RD0 ³ | I/O | NVDD |
| AH1 | Reserved. | NC | — |
| AH2 | M1DQS3 | I/O | GVDD1 |
| AH3 | M1DQS3 | I/O | GVDD1 |
| AH4 | M1ECC0 | I/O | GVDD1 |
| AH5 | M1DQS8 | I/O | GVDD1 |
| AH6 | M1DQS8 | I/O | GVDD1 |
| AH7 | M1A5 | O | GVDD1 |
| AH8 | M1CK1 | O | GVDD1 |
| AH9 | M1CK1 | O | GVDD1 |
| AH10 | M1CS0 | O | GVDD1 |
| AH11 | M1BA0 | O | GVDD1 |
| AH12 | M1CAS | O | GVDD1 |
| AH13 | M1DQ34 | I/O | GVDD1 |
| AH14 | M1DQS4 | I/O | GVDD1 |
| AH15 | M1DQS4 | I/O | GVDD1 |
| AH16 | M1DQ50 | I/O | GVDD1 |

Table 1. Signal List by Ball Number (continued)

| Ball Number | Signal Name ^{1,2} | Pin Type ¹⁰ | Power Rail Name |
|-------------|------------------------------|------------------------|-----------------|
| AH17 | M1DQS6 | I/O | GVDD1 |
| AH18 | M1DQS6 | I/O | GVDD1 |
| AH19 | M1DQ48 | I/O | GVDD1 |
| AH20 | M1DQ49 | I/O | GVDD1 |
| AH21 | VSS | Ground | N/A |
| AH22 | TDM0RCK/GE2_RD2 ³ | I/O | NVDD |
| AH23 | TDM0RDT/GE2_RD3 ³ | I/O | NVDD |
| AH24 | TDM0TSN/GE2_RDO ³ | I/O | NVDD |
| AH25 | TDM1RCK/GE2_RD1 ³ | I/O | NVDD |
| AH26 | TDM3TDT/GE1_RD3 ³ | I/O | NVDD |
| AH27 | TDM3TCK/GE1_RD2 ³ | I | NVDD |
| AH28 | VSS | Ground | N/A |

Notes:

1. Reserved signals should be disconnected for compatibility with future revisions of the device. Non-user signals are reserved for manufacturing and test purposes only. The assigned signal name is used to indicate whether the signal must be unconnected (Reserved), pulled down (VSS), or pulled up (VDD).
2. Signal function during power-on reset is determined by the RCW source type.
3. Selection of TDM versus RGMII functionality is determined by the RCW bit values.
4. Selection of RapidIO, SGMII, and PCI Express functionality is determined by the RCW bit values.
5. Selection of the GPIO function and other functions is done by GPIO register setup. For configuration details, see the *GPIO* chapter in the *MSC8252 Reference Manual*.
6. Open-drain signal.
7. Internal 20 KΩ pull-up resistor.
8. For signals with GPIO functionality, the open-drain and internal 20 KΩ pull-up resistor can be configured by GPIO register programming. See the *GPIO* chapter of the *MSC8252 Reference Manual* for configuration details.
9. Connect to power supply via external filter. See **Section 3.2, PLL Power Supply Design Considerations** for details.
10. Pin types are: Ground = all VSS connections; Power = all VDD connections; I = Input; O = Output; I/O = Input/Output; NC = not connected.

2 Electrical Characteristics

This document contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications. For additional information, see the *MSC8252 Reference Manual*.

2.1 Maximum Ratings

In calculating timing requirements, adding a maximum value of one specification to a minimum value of another specification does not yield a reasonable sum. A maximum specification is calculated using a worst case variation of process parameter values in one direction. The minimum specification is calculated using the worst case for the same parameters in the opposite direction. Therefore, a “maximum” value for a specification never occurs in the same device with a “minimum” value for another specification; adding a maximum to a minimum represents a condition that can never exist.

Table 2 describes the maximum electrical ratings for the MSC8252.

Table 2. Absolute Maximum Ratings

| Rating | Power Rail Name | Symbol | Value | Unit |
|---|--|--|---|-------------|
| Core supply voltage • Cores 0–3 | VDD | V_{DD} | –0.3 to 1.1 | V |
| PLL supply voltage ³ | | V_{DDPLL0} V_{DDPLL1} V_{DDPLL2} | –0.3 to 1.1 –0.3 to 1.1 –0.3 to 1.1 | V V V |
| M3 memory supply voltage | M3VDD | V_{DDM3} | –0.3 to 1.1 | V |
| DDR memory supply voltage • DDR2 mode • DDR3 mode | GVDD1, GVDD2 | V_{DDDDR} | –0.3 to 1.98 –0.3 to 1.65 | V V |
| DDR reference voltage | MVREF | MV_{REF} | –0.3 to $0.51 \times V_{DDDDR}$ | V |
| Input DDR voltage | | V_{INDDR} | –0.3 to $V_{DDDDR} + 0.3$ | V |
| I/O voltage excluding DDR and RapidIO lines | NVDD, QVDD | V_{DDIO} | –0.3 to 2.625 | V |
| Input I/O voltage | | V_{INIO} | –0.3 to $V_{DDIO} + 0.3$ | V |
| RapidIO pad voltage | SXPVDD1, SXPVDD2 | V_{DDSXP} | –0.3 to 1.26 | V |
| Rapid I/O core voltage | SXCVDD1, SXCVDD2 | V_{DDSXC} | –0.3 to 1.21 | V |
| Rapid I/O PLL voltage ³ | | $V_{DDRIOPLL}$ | –0.3 to 1.21 | V |
| Input RapidIO I/O voltage | | V_{INRIO} | –0.3 to $V_{DDSXC} + 0.3$ | V |
| Operating temperature | | T_J | –40 to 105 | °C |
| Storage temperature range | | T_{STG} | –55 to +150 | °C |
| Notes: | <ol style="list-style-type: none"> Functional operating conditions are given in Table 3. Absolute maximum ratings are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond the listed limits may affect device reliability or cause permanent damage. PLL supply voltage is specified at input of the filter and not at pin of the MSC8252 (see Figure 37 and Figure 38) | | | |

2.2 Recommended Operating Conditions

Table 3 lists recommended operating conditions. Proper device operation outside of these conditions is not guaranteed.

Table 3. Recommended Operating Conditions

| Rating | Symbol | Min | Nominal | Max | Unit |
|---|--|-------------------------|------------------------|-------------------------|------|
| Core supply voltage | V_{DD} | 0.97 | 1.0 | 1.05 | V |
| M3 memory supply voltage | V_{DDM3} | 0.97 | 1.0 | 1.05 | V |
| DDR memory supply voltage | V_{DDDDR} | | | | |
| • DDR2 mode | | 1.7 | 1.8 | 1.9 | V |
| • DDR3 mode | | 1.425 | 1.5 | 1.575 | V |
| DDR reference voltage | MV_{REF} | $0.49 \times V_{DDDDR}$ | $0.5 \times V_{DDDDR}$ | $0.51 \times V_{DDDDR}$ | V |
| I/O voltage excluding DDR and RapidIO lines | V_{DDIO} | 2.375 | 2.5 | 2.625 | V |
| Rapid I/O pad voltage | V_{DDSP} | 0.97 | 1.0 | 1.05 | V |
| Rapid I/O core voltage | V_{DDXC} | 0.97 | 1.0 | 1.05 | V |
| Operating temperature range: | | | | | |
| • Standard | T_J | 0 | | 90 | °C |
| • Higher | T_J | 0 | | 105 | °C |
| • Extended | T_A | -40 | | — | °C |
| | T_J | — | | 105 | °C |
| Typical power: 1 GHz at 1.0 V ¹ | P | — | 3.54 | — | W |
| Notes: | 1. The typical power values are derived for a device running under the following conditions. <ul style="list-style-type: none"> Two cores running at 1 GHz, Core voltage at 1V, 75% utilization (50% control/50% DSP). A single 64 bit DDR3 running at 800 MHz, 50% utilization (50% reads/50% writes). M3 Memory 50% utilized, PCI Express controller disabled, TDM enabled 20% loading, Serial RapidIO controller disabled, 1 RGMII at 1 Gbps 50% loading. A junction temperature of 60°C. | | | | |

2.3 Thermal Characteristics

Table 4 describes thermal characteristics of the MSC8252 for the FC-PBGA packages.

Table 4. Thermal Characteristics for the MSC8252

| Characteristic | Symbol | FC-PBGA 29 × 29 mm ² | | Unit |
|---|---|------------------------------------|-------------------------------|------|
| | | Natural Convection | 200 ft/min (1 m/s) airflow | |
| Junction-to-ambient ^{1, 2} | $R_{\theta JA}$ | 18 | 12 | °C/W |
| Junction-to-ambient, four-layer board ^{1, 2} | $R_{\theta JA}$ | 13 | 9 | °C/W |
| Junction-to-board (bottom) ³ | $R_{\theta JB}$ | 5 | | °C/W |
| Junction-to-case ⁴ | $R_{\theta JC}$ | 0.6 | | °C/W |
| Notes: | 1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance. 2. Junction-to-ambient thermal resistance determined per JEDEC JESD51-3 and JESDC51-6. Thermal test board meets JEDEC specification for the specified package. 3. Junction-to-board thermal resistance determined per JEDEC JESD 51-8. Thermal test board meets JEDEC specification for the specified package. 4. Junction-to-case at the top of the package determined using MIL- STD-883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer | | | |

2.4 CLKIN Requirements

Table 5 summarizes the required characteristics for the CLKIN signal.

Table 5. CLKIN Requirements

| Parameter/Condition ¹ | Symbol | Min | Typ | Max | Unit | Notes |
|-------------------------------------|-----------------|-----|-----|------|------|-------|
| CLKIN duty cycle | — | 40 | — | 60 | % | 2 |
| CLKIN slew rate | — | 1 | — | 4 | V/ns | 3 |
| CLKIN peak period jitter | — | — | — | ±150 | ps | — |
| CLKIN jitter phase noise at -56 dBc | — | — | — | 500 | KHz | 4 |
| AC input swing limits | ΔV_{AC} | 1.5 | — | — | V | — |
| Input capacitance | C_{IN} | — | — | 15 | pf | — |

Notes:

1. For clock frequencies, see the *Clock* chapter in the *MSC8252 Reference Manual*.
2. Measured at the rising edge and/or the falling edge at $V_{DDIO}/2$.
3. Slew rate as measured from ±20% to 80% of voltage swing at clock input.
4. Phase noise is calculated as FFT of TIE jitter.

2.5 DC Electrical Characteristics

This section describes the DC electrical characteristics for the MSC8252.

2.5.1 DDR SDRAM DC Electrical Characteristics

This section describes the DC electrical specifications for the DDR SDRAM interface of the MSC8252.

Note: DDR2 SDRAM uses $V_{DDDDR}(\text{typ}) = 1.8$ V and DDR3 SDRAM uses $V_{DDDDR}(\text{typ}) = 1.5$ V.

2.5.1.1 DDR2 (1.8 V) SDRAM DC Electrical Characteristics

Table 6 provides the recommended operating conditions for the DDR SDRAM controller when interfacing to DDR2 SDRAM.

Note: At recommended operating conditions (see Table 3) with $V_{DDDDR} = 1.8$ V.

Table 6. DDR2 SDRAM Interface DC Electrical Characteristics

| Parameter/Condition | Symbol | Min | Max | Unit | Notes |
|---|------------|-------------------------|-------------------------|---------|---------|
| I/O reference voltage | MV_{REF} | $0.49 \times V_{DDDDR}$ | $0.51 \times V_{DDDDR}$ | V | 2, 3, 4 |
| Input high voltage | V_{IH} | $MV_{REF} + 0.125$ | $V_{DDDDR} + 0.3$ | V | 5 |
| Input low voltage | V_{IL} | -0.3 | $MV_{REF} - 0.125$ | V | 5 |
| I/O leakage current | I_{OZ} | -50 | 50 | μA | 6 |
| Output high current (V_{OUT} (VOH) = 1.37 V) | I_{OH} | -13.4 | — | mA | 7 |
| Output low current (V_{OUT} (VOL) = 0.33 V) | I_{OL} | 13.4 | — | mA | 7 |

Notes:

1. V_{DDDDR} is expected to be within 50 mV of the DRAM V_{DD} supply voltage at all times. The DRAM and memory controller can use the same or different sources.
2. MV_{REF} is expected to be equal to $0.5 \times V_{DDDDR}$, and to track V_{DDDDR} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF} with a minimum value of $MV_{REF} - 0.4$ and a maximum value of $MV_{REF} + 0.04$ V. V_{TT} should track variations in the DC-level of MV_{REF} .
4. The voltage regulator for MV_{REF} must be able to supply up to 300 μA .
5. Input capacitance load for DQ, DQS, and DQS signals are available in the IBIS models.
6. Output leakage is measured with all outputs are disabled, 0 V $\leq V_{OUT} \leq V_{DDDDR}$.
7. Refer to the IBIS model for the complete output IV curve characteristics.

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2.5.1.2 DDR3 (1.5V) SDRAM DC Electrical Characteristics

Table 7 provides the recommended operating conditions for the DDR SDRAM controller when interfacing to DDR3 SDRAM.

Note: At recommended operating conditions (see Table 3) with $V_{DDDDR} = 1.5$ V.

Table 7. DDR3 SDRAM Interface DC Electrical Characteristics

| Parameter/Condition | Symbol | Min | Max | Unit | Notes |
|-----------------------|--|-------------------------|-------------------------|---------|-------|
| I/O reference voltage | MV_{REF} | $0.49 \times V_{DDDDR}$ | $0.51 \times V_{DDDDR}$ | V | 2,3,4 |
| Input high voltage | V_{IH} | $MV_{REF} + 0.100$ | V_{DDDDR} | V | 5 |
| Input low voltage | V_{IL} | GND | $MV_{REF} - 0.100$ | V | 5 |
| I/O leakage current | I_{OZ} | -50 | 50 | μA | 6 |
| Notes: | <ol style="list-style-type: none"> V_{DDDDR} is expected to be within 50 mV of the DRAM V_{DD} at all times. The DRAM and memory controller can use the same or different sources. MV_{REF} is expected to be equal to $0.5 \times V_{DDDDR}$ and to track V_{DDDDR} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed $\pm 1\%$ of the DC value. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF} with a minimum value of $MV_{REF} - 0.4$ and a maximum value of $MV_{REF} + 0.04$ V. V_{TT} should track variations in the DC-level of MV_{REF}. The voltage regulator for MV_{REF} must be able to supply up to 250 μA. Input capacitance load for DQ, DQS, and \overline{DQS} signals are available in the IBIS models. Output leakage is measured with all outputs are disabled, $0 V \leq V_{OUT} \leq V_{DDDDR}$. | | | | |

2.5.1.3 DDR2/DDR3 SDRAM Capacitance

Table 8 provides the DDR controller interface capacitance for DDR2 and DDR3 memory.

Note: At recommended operating conditions (see Table 3) with $V_{DDDDR} = 1.8$ V for DDR2 memory or $V_{DDDDR} = 1.5$ V for DDR3 memory.

Table 8. DDR2/DDR3 SDRAM Capacitance

| Parameter | Symbol | Min | Max | Unit |
|--|-----------|-----|-----|------|
| I/O capacitance: DQ, DQS, \overline{DQS} | C_{IO} | 6 | 8 | pF |
| Delta I/O capacitance: DQ, DQS, \overline{DQS} | C_{DIO} | — | 0.5 | pF |
| Note: Guaranteed by FAB process and micro-construction. | | | | |

2.5.1.4 DDR Reference Current Draw

Table 9 lists the current draw characteristics for MV_{REF} .

Note: Values when used at recommended operating conditions (see Table 3).

Table 9. Current Draw Characteristics for MV_{REF}

| Parameter / Condition | Symbol | Min | Max | Unit |
|--|--------------|-----|------------|---------|
| Current draw for MV_{REFn} • DDR2 SDRAM • DDR3 SDRAM | I_{MVREFn} | — | 300 250 | μA |

2.5.2 High-Speed Serial Interface (HSSI) DC Electrical Characteristics

The MSC8252 features an HSSI that includes two 4-channel SerDes ports used for high-speed serial interface applications (PCI Express, Serial RapidIO interfaces, and SGMII). This section and its subsections describe the common portion of the SerDes DC, including the DC requirements for the SerDes reference clocks and the SerDes data lane transmitter (Tx) and receiver (Rx) reference circuits. The data lane circuit specifications are specific for each supported interface, and they have individual subsections by protocol. The selection of individual data channel functionality is done via the Reset Configuration Word High Register (RCWHR) SerDes Protocol selection fields (S1P and S2P). Specific AC electrical characteristics are defined in Section 2.6.2, “HSSI AC Timing Specifications.”

2.5.2.1 Signal Term Definitions

The SerDes interface uses differential signalling to transfer data across the serial link. This section defines terms used in the description and specification of differential signals. Figure 4 shows how the signals are defined. For illustration purposes only, one SerDes lane is used in the description. Figure 4 shows the waveform for either a transmitter output (SR[1–2]_TX and $\overline{SR[1-2]_TX}$) or a receiver input (SR[1–2]_RX and $\overline{SR[1-2]_RX}$). Each signal swings between A volts and B volts where $A > B$.

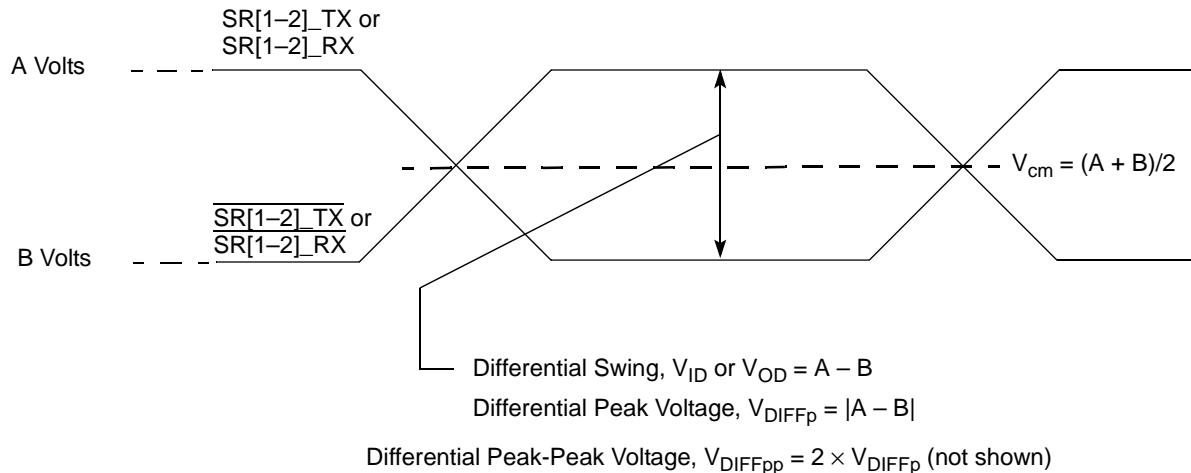


Figure 4. Differential Voltage Definitions for Transmitter or Receiver

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Using this waveform, the definitions are listed in [Table 10](#). To simplify the illustration, the definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signalling environment.

Table 10. Differential Signal Definitions

| Term | Definition |
|---|---|
| Single-Ended Swing | The transmitter output signals and the receiver input signals SR[1-2]_TX, $\overline{\text{SR[1-2]_TX}}$, SR[1-2]_RX and $\overline{\text{SR[1-2]_RX}}$ each have a peak-to-peak swing of A – B volts. This is also referred to as each signal wire's single-ended swing. |
| Differential Output Voltage, V_{OD} (or Differential Output Swing): | The differential output voltage (or swing) of the transmitter, V_{OD} , is defined as the difference of the two complimentary output voltages: $V_{SR[1-2]_TX} - V_{\overline{SR[1-2]_TX}}$. The V_{OD} value can be either positive or negative. |
| Differential Input Voltage, V_{ID} (or Differential Input Swing) | The differential input voltage (or swing) of the receiver, V_{ID} , is defined as the difference of the two complimentary input voltages: $V_{SR[1-2]_RX} - V_{\overline{SR[1-2]_RX}}$. The V_{ID} value can be either positive or negative. |
| Differential Peak Voltage, V_{DIFFp} | The peak value of the differential transmitter output signal or the differential receiver input signal is defined as the differential peak voltage, $V_{DIFFp} = A - B $ volts. |
| Differential Peak-to-Peak, $V_{DIFFp-p}$ | Since the differential output signal of the transmitter and the differential input signal of the receiver each range from A – B to $-(A - B)$ volts, the peak-to-peak value of the differential transmitter output signal or the differential receiver input signal is defined as differential peak-to-peak voltage, $V_{DIFFp-p} = 2 \times V_{DIFFp} = 2 \times (A - B) $ volts, which is twice the differential swing in amplitude, or twice of the differential peak. For example, the output differential peak-peak voltage can also be calculated as $V_{TX-DIFFp-p} = 2 \times V_{OD} $. |
| Differential Waveform | The differential waveform is constructed by subtracting the inverting signal ($\overline{\text{SR[1-2]_TX}}$, for example) from the non-inverting signal (SR[1-2]_TX , for example) within a differential pair. There is only one signal trace curve in a differential waveform. The voltage represented in the differential waveform is not referenced to ground. Refer to Figure 16 as an example for differential waveform. |
| Common Mode Voltage, V_{cm} | The common mode voltage is equal to half of the sum of the voltages between each conductor of a balanced interchange circuit and ground. In this example, for SerDes output, $V_{cm_out} = (V_{SR[1-2]_TX} + V_{\overline{SR[1-2]_TX}}) / 2 = (A + B) / 2$, which is the arithmetic mean of the two complimentary output voltages within a differential pair. In a system, the common mode voltage may often differ from one component's output to the other's input. It may be different between the receiver input and driver output circuits within the same component. It is also referred to as the DC offset on some occasions. |

To illustrate these definitions using real values, consider the example of a current mode logic (CML) transmitter that has a common mode voltage of 2.25 V and outputs, TD and $\overline{\text{TD}}$. If these outputs have a swing from 2.0 V to 2.5 V, the peak-to-peak voltage swing of each signal (TD or $\overline{\text{TD}}$) is 500 mV p-p, which is referred to as the single-ended swing for each signal. Because the differential signaling environment is fully symmetrical in this example, the transmitter output differential swing (V_{OD}) has the same amplitude as each signal single-ended swing. The differential output signal ranges between 500 mV and –500 mV. In other words, V_{OD} is 500 mV in one phase and –500 mV in the other phase. The peak differential voltage (V_{DIFFp}) is 500 mV. The peak-to-peak differential voltage ($V_{DIFFp-p}$) is 1000 mV p-p.

2.5.2.2 SerDes Reference Clock Receiver Characteristics

The SerDes reference clock inputs are applied to an internal PLL whose output creates the clock used by the corresponding SerDes lanes. The SerDes reference clock inputs are SR1_REF_CLK/SR1_REF_CLK or SR2_REF_CLK/SR2_REF_CLK. Figure 5 shows a receiver reference diagram of the SerDes reference clocks.

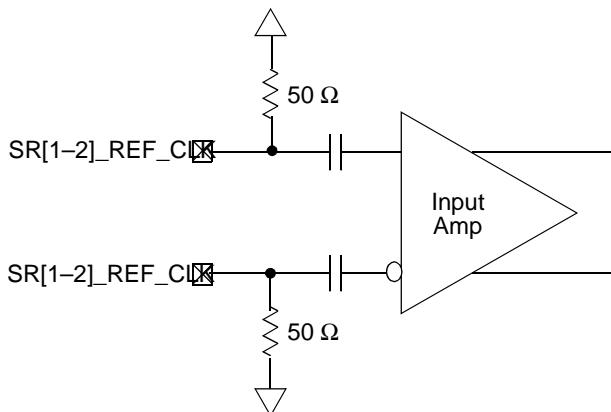


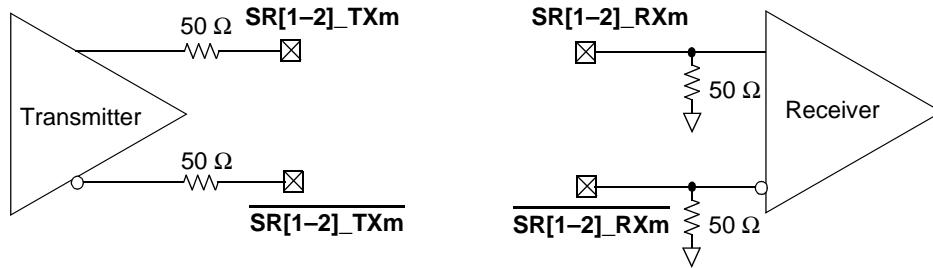
Figure 5. Receiver of SerDes Reference Clocks

The characteristics of the clock signals are as follows:

- The supply voltage requirements for $V_{DD_{SXC}}$ are as specified in [Table 3](#).
- The SerDes reference clock receiver reference circuit structure is as follows:
 - The SR[1-2]_REF_CLK and SR[1-2]_REF_CLK are internally AC-coupled differential inputs as shown in [Figure 5](#). Each differential clock input (SR[1-2]_REF_CLK or SR[1-2]_REF_CLK) has on-chip 50- Ω termination to GND_{SXC} followed by on-chip AC-coupling.
 - The external reference clock driver must be able to drive this termination.
 - The SerDes reference clock input can be either differential or single-ended. Refer to the differential mode and single-ended mode descriptions below for detailed requirements.
- The maximum average current requirement also determines the common mode voltage range.
 - When the SerDes reference clock differential inputs are DC coupled externally with the clock driver chip, the maximum average current allowed for each input pin is 8 mA. In this case, the exact common mode input voltage is not critical as long as it is within the range allowed by the maximum average current of 8 mA because the input is AC-coupled on-chip.
 - This current limitation sets the maximum common mode input voltage to be less than 0.4 V ($0.4 \text{ V} / 50 = 8 \text{ mA}$) while the minimum common mode input level is 0.1 V above GND_{SXC}. For example, a clock with a 50/50 duty cycle can be produced by a clock driver with output driven by its current source from 0 mA to 16 mA (0–0.8 V), such that each phase of the differential input has a single-ended swing from 0 V to 800 mV with the common mode voltage at 400 mV.
 - If the device driving the SR[1-2]_REF_CLK and SR[1-2]_REF_CLK inputs cannot drive 50 Ω to GND_{SXC} DC or the drive strength of the clock driver chip exceeds the maximum input current limitations, it must be AC-coupled externally.
- The input amplitude requirement is described in detail in the following sections.

2.5.2.3 SerDes Transmitter and Receiver Reference Circuits

Figure 6 shows the reference circuits for SerDes data lane transmitter and receiver.



Note: The [1-2] indicates the specific SerDes Interface (1 or 2) and the m indicates the specific channel within that interface (0,1,2,3). Actual signals are assigned by the HRCW assignments at reset (see **Chapter 5, Reset** in the reference manual for details)

Figure 6. SerDes Transmitter and Receiver Reference Circuits

2.5.3 DC-Level Requirements for SerDes Interfaces

The following subsections define the DC-level requirements for the SerDes reference clocks, the PCI Express data lines, the Serial RapidIO data lines, and the SGMII data lines.

2.5.3.1 DC-Level Requirements for SerDes Reference Clocks

The DC-level requirement for the SerDes reference clock inputs is different depending on the signaling mode used to connect the clock driver chip and SerDes reference clock inputs, as described below:

- Differential Mode
 - The input amplitude of the differential clock must be between 400 mV and 1600 mV differential peak-peak (or between 200 mV and 800 mV differential peak). In other words, each signal wire of the differential pair must have a single-ended swing of less than 800 mV and greater than 200 mV. This requirement is the same for both external DC-coupled or AC-coupled connection.
 - For an external DC-coupled connection, the maximum average current requirements sets the requirement for average voltage (common mode voltage) as between 100 mV and 400 mV. **Figure 7** shows the SerDes reference clock input requirement for DC-coupled connection scheme.

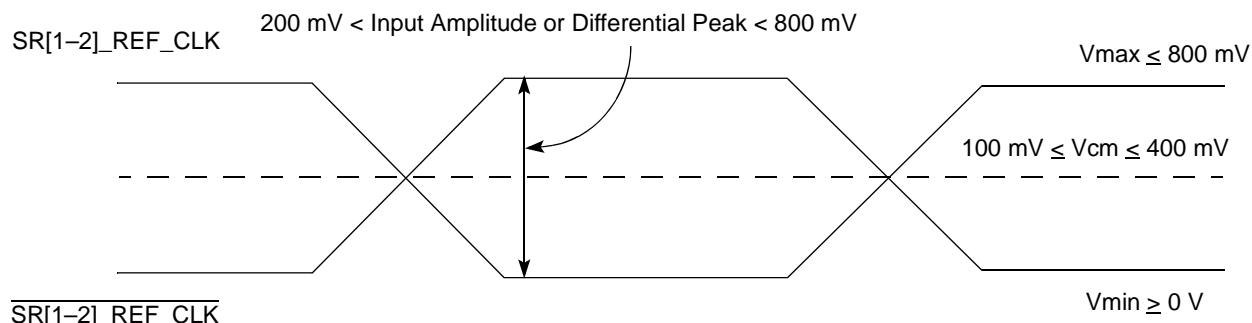


Figure 7. Differential Reference Clock Input DC Requirements (External DC-Coupled)

- For an external AC-coupled connection, there is no common mode voltage requirement for the clock driver. Because the external AC-coupling capacitor blocks the DC-level, the clock driver and the SerDes reference clock receiver operate in different command mode voltages. The SerDes reference clock receiver in this connection scheme has its common mode voltage set to GND_{SXC} . Each signal wire of the differential inputs is allowed to swing below and above the command mode voltage GND_{SXC} . Figure 8 shows the SerDes reference clock input requirement for AC-coupled connection scheme.

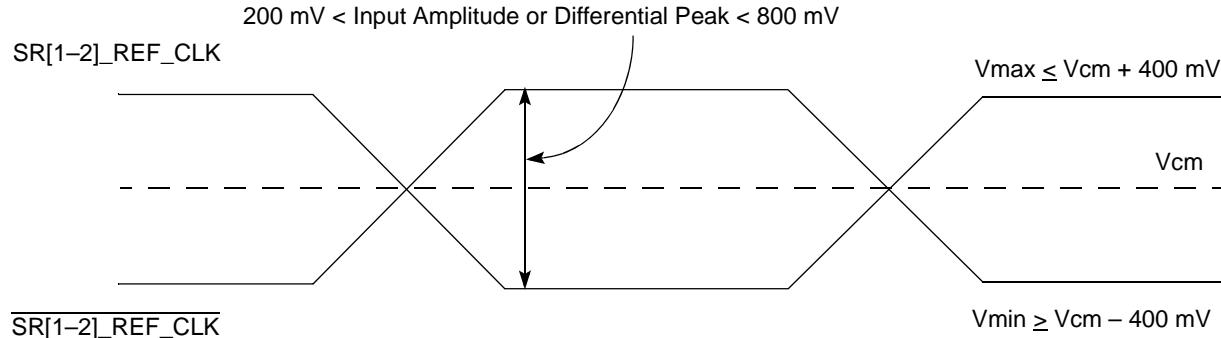


Figure 8. Differential Reference Clock Input DC Requirements (External AC-Coupled)

- Single-Ended Mode
 - The reference clock can also be single-ended. The SR[1-2]_REF_CLK input amplitude (single-ended swing) must be between 400 mV and 800 mV peak-peak (from V_{MIN} to V_{MAX}) with $\overline{SR[1-2]_REF_CLK}$ either left unconnected or tied to ground.
 - The SR[1-2]_REF_CLK input average voltage must be between 200 and 400 mV. Figure 9 shows the SerDes reference clock input requirement for single-ended signalling mode.
 - To meet the input amplitude requirement, the reference clock inputs may need to be DC- or AC-coupled externally. For the best noise performance, the reference of the clock could be DC- or AC-coupled into the unused phase ($\overline{SR[1-2]_REF_CLK}$) through the same source impedance as the clock input (SR[1-2]_REF_CLK) in use.

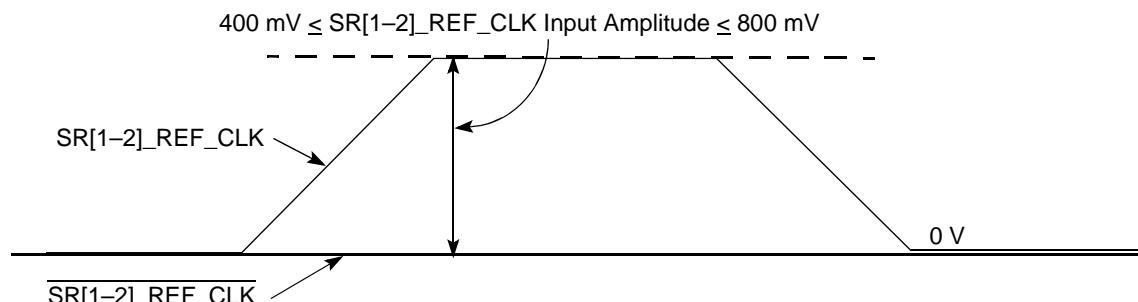


Figure 9. Single-Ended Reference Clock Input DC Requirements

2.5.3.2 DC-Level Requirements for PCI Express Configurations

The DC-level requirements for PCI Express implementations have separate requirements for the Tx and Rx lines. The MSC8252 supports a 2.5 Gbps PCI Express interface defined by the *PCI Express Base Specification, Revision 1.0a*. The transmitter specifications are defined in Table 11 and the receiver specifications are defined in Table 12.

Electrical Characteristics

Note: Specifications are valid at the recommended operating conditions listed in [Table 3](#).

Table 11. PCI Express (2.5 Gbps) Differential Transmitter (Tx) Output DC Specifications

| Parameter | Symbol | Min | Typical | Max | Units | Notes |
|---|---|-----|---------|------|----------|-------|
| Differential peak-to-peak output voltage | $V_{TX-DIFFp-p}$ | 800 | 1000 | 1200 | mV | 1 |
| De-emphasized differential output voltage (ratio) | $V_{TX-DE-RATIO}$ | 3.0 | 3.5 | 4.0 | dB | 2 |
| DC differential Tx impedance | $Z_{TX-DIFF-DC}$ | 80 | 100 | 120 | Ω | 3 |
| Transmitter DC impedance | Z_{TX-DC} | 40 | 50 | 60 | Ω | 4 |
| Notes: | 1. $V_{TX-DIFFp-p} = 2 \times V_{TX-D+} - V_{TX-D-} $ Measured at the package pins with a test load of 50Ω to GND on each pin. 2. Ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition. Measured at the package pins with a test load of 50Ω to GND on each pin. 3. Tx DC differential mode low impedance 4. Required Tx D+ as well as D- DC Impedance during all states | | | | | |

Table 12. PCI Express (2.5 Gbps) Differential Receiver (Rx) Input DC Specifications

| Parameter | Symbol | Min | Typical | Max | Units | Notes |
|---|--|-----|---------|------|-----------|-------|
| Differential input peak-to-peak voltage | $V_{RX-DIFFp-p}$ | 120 | 1000 | 1200 | mV | 1 |
| DC differential Input Impedance | $Z_{RX-DIFF-DC}$ | 80 | 100 | 120 | Ω | 2 |
| DC input impedance | Z_{RX-DC} | 40 | 50 | 60 | Ω | 3 |
| Powered down DC input impedance | $Z_{RX-HIGH-IMP-DC}$ | 50 | — | — | $K\Omega$ | 4 |
| Electrical idle detect threshold | $V_{RX-IDLE-DET-DIFFp-p}$ | 65 | — | 175 | mV | 5 |
| Notes: | 1. $V_{RX-DIFFp-p} = 2 \times V_{RX-D+} - V_{RX-D-} $ Measured at the package pins with a test load of 50Ω to GND on each pin. 2. Rx DC differential mode impedance. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM), there is a 5 ms transition time before the receiver termination values must be met on all unconfigured lanes of a port. 3. Required Rx D+ as well as D- DC Impedance ($50 \pm 20\%$ tolerance). Measured at the package pins with a test load of 50Ω to GND on each pin. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM), there is a 5 ms transition time before the receiver termination values must be met on all unconfigured lanes of a port. 4. Required Rx D+ as well as D- DC Impedance when the receiver terminations do not have power. The Rx DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the Rx ground. 5. $V_{RX-IDLE-DET-DIFFp-p} = 2 \times V_{RX-D+} - V_{RX-D-} $. Measured at the package pins of the receiver | | | | | |

2.5.3.3 DC-Level Requirements for Serial RapidIO Configurations

This sections provided various DC-level requirements for Serial RapidIO Configurations.

Note: Specifications are valid at the recommended operating conditions listed in [Table 3](#).

Table 13. Serial RapidIO Transmitter DC Specifications

| Parameter | Symbol | Min | Typical | Max | Units | Notes |
|---------------------------------------|---|-------|---------|------|-------|-------|
| Output voltage | V_O | -0.40 | — | 2.30 | V | 1 |
| Long run differential output voltage | V_{DIFFPP} | 800 | — | 1600 | mVp-p | — |
| Short run differential output voltage | V_{DIFFPP} | 500 | — | 1000 | mVp-p | — |
| Note: | Voltage relative to COMMON of either signal comprising a differential pair. | | | | | |

Table 14. Serial RapidIO Receiver DC Specifications

| Parameter | Symbol | Min | Typical | Max | Units | Notes |
|--|----------|-----|---------|------|-------|-------|
| Differential input voltage | V_{IN} | 200 | — | 1600 | mVp-p | 1 |
| Notes: 1. Measured at receiver. | | | | | | |

2.5.3.4 DC-Level Requirements for SGMII Configurations

Note: Specifications are valid at the recommended operating conditions listed in [Table 3](#)

[Table 15](#) describes the SGMII SerDes transmitter AC-coupled DC electrical characteristics. Transmitter DC characteristics are measured at the transmitter outputs ($SR[1-2]_TX[n]$ and $\bar{SR}[1-2]_TX[n]$) as shown in [Figure 10](#).

Table 15. SGMII DC Transmitter Electrical Characteristics

| Parameter | Symbol | Min | Typ | Max | Unit | Notes |
|---|-------------|--|-----|--|----------|--------|
| Output high voltage | V_{OH} | — | — | $XV_{DD_SRDS-Typ}/2 + V_{ODL_max} /2$ | mV | 1 |
| Output low voltage | V_{OL} | $XV_{DD_SRDS-Typ}/2 - V_{ODL_max} /2$ | — | — | mV | 1 |
| Output differential voltage (XV_{DD-Typ} at 1.0 V) | $ V_{ODL} $ | 323 | 500 | 725 | mV | 2,3,4 |
| | | 296 | 459 | 665 | | 2,3,5 |
| | | 269 | 417 | 604 | | 2,3,6 |
| | | 243 | 376 | 545 | | 2,3,7 |
| | | 215 | 333 | 483 | | 2,3,8 |
| | | 189 | 292 | 424 | | 2,3,9 |
| | | 162 | 250 | 362 | | 2,3,10 |
| Output impedance (single-ended) | R_O | 40 | 50 | 60 | Ω | — |
| Notes: 1. This does not align to DC-coupled SGMII. $XV_{DD_SRDS2-Typ} = 1.1$ V. 2. The $ V_{ODL} $ value shown in the table assumes full multitude by setting srd_smi_lvl as 000 and the following transmit equalization setting in the XMITEQAB (for lanes A and B) or XMITEQEF (for lanes E and F) bit field of Control Register: • The MSB (bit 0) of the above bit field is set to zero (selecting the full $V_{DD-DIFF-p-p}$ amplitude which is power up default); • The LSB (bit [1-3]) of the above bit field is set based on the equalization settings listed in notes 4 through 10. 3. The $ V_{ODL} $ value shown in the Typ column is based on the condition of $XV_{DD_SRDS2-Typ} = 1.0$ V, no common mode offset variation ($V_{OS} = 500$ mV), SerDes transmitter is terminated with 100Ω differential load between 4. Equalization setting: 1.0x: 0000. 5. Equalization setting: 1.09x: 1000. 6. Equalization setting: 1.2x: 0100. 7. Equalization setting: 1.33x: 1100. 8. Equalization setting: 1.5x: 0010. 9. Equalization setting: 1.71x: 1010. 10. Equalization setting: 2.0x: 0110. 11. $ V_{ODL} = V_{SR[1-2]_TXn} - V_{\bar{SR}[1-2]_TXn} $. $ V_{ODL} $ is also referred to as output differential peak voltage. $V_{TX-DIFFp-p} = 2* V_{ODL} $. | | | | | | |

Electrical Characteristics

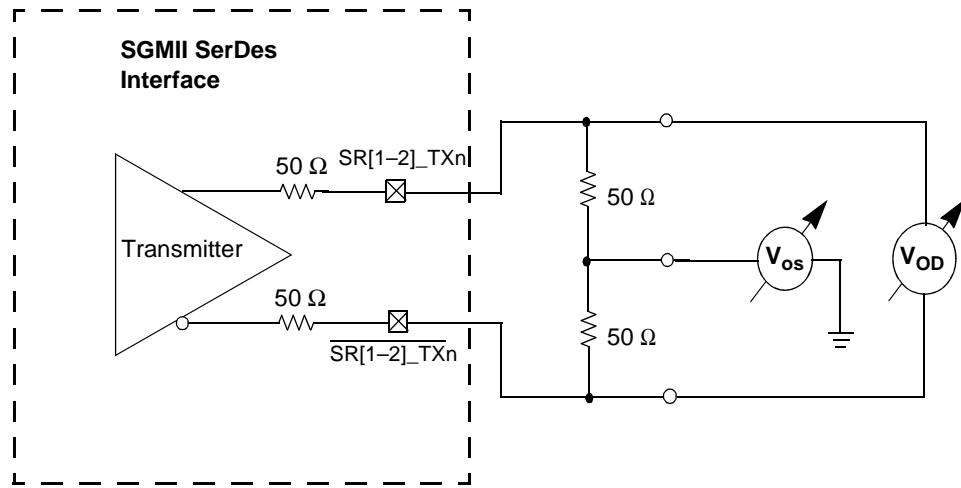


Figure 10. SGMII Transmitter DC Measurement Circuit

Table 16 describes the SGMII SerDes receiver AC-coupled DC electrical characteristics.

Table 16. SGMII DC Receiver Electrical Characteristics⁵

| Parameter | | Symbol | Min | Typ | Max | Unit | Notes |
|---|--|-------------------------|-----|-----|------|------|-------|
| DC Input voltage range | | — | N/A | | | — | 1 |
| Input differential voltage | SRDSnCR4[EICE{12:10}] = 0b001 for SGMII1 SRDSnCR4[EICF{4:2}] = 0b001 for SGMII2 | V _{RX_DIFFp-p} | 100 | — | 1200 | mV | 2, 4 |
| | SRDSnCR4[EICE{12:10}] = 0b100 for SGMII1 SRDSnCR4[EICF{4:2}] = 0b100 for SGMII2 | | 175 | — | | | |
| Loss of signal threshold | SRDSnCR4[EICE{12:10}] = 0b001 for SGMII1 SRDSnCR4[EICF{4:2}] = 0b001 for SGMII2 | V _{LOS} | 30 | — | 100 | mV | 3, 4 |
| | SRDSnCR4[EICE{12:10}] = 0b100 for SGMII1 SRDSnCR4[EICF{4:2}] = 0b100 for SGMII2 | | 65 | — | 175 | | |
| Receiver differential input impedance | | Z _{RX_DIFF} | 80 | — | 120 | W | — |
| Notes: <ol style="list-style-type: none"> 1. Input must be externally AC-coupled. 2. V_{RX_DIFFp-p} is also referred to as peak-to-peak input differential voltage. 3. The concept of this parameter is equivalent to the Electrical Idle Detect Threshold parameter in the PCI Express interface. Refer to the PCI Express Differential Receiver (RX) Input Specifications section of the <i>PCI Express Specification</i> document for details. 4. The values for SGMII1 and SGMII2 are selected in the SRDS control registers. 5. The supply voltage is 1.0 V. | | | | | | | |

2.5.4 RGMII and Other Interface DC Electrical Characteristics

Table 17 describes the DC electrical characteristics for the following interfaces:

- RGMII Ethernet
- SPI
- TDM
- GPIO
- UART
- TIMER
- EE
- I²C
- Interrupts ($\overline{\text{IRQn}}$, $\overline{\text{NMI_OUT}}$, $\overline{\text{INT_OUT}}$)
- Clock and resets ($\overline{\text{CLKIN}}$, $\overline{\text{PORESET}}$, $\overline{\text{HRESET}}$, $\overline{\text{SRESET}}$)
- DMA External Request
- JTAG signals

Table 17. 2.5 V I/O DC Electrical Characteristics

| Characteristic | Symbol | Min | Max | Unit | Notes |
|--|----------|-------------|------------------|---------------|-------|
| Input high voltage | V_{IH} | 1.7 | — | V | 1 |
| Input low voltage | V_{IL} | — | 0.7 | V | 1 |
| Input high current ($V_{IN} = V_{DDIO}$) | I_{IN} | — | 30 | μA | 2 |
| Output high voltage ($V_{DDIO} = \text{min}$, $I_{OH} = -1.0 \text{ mA}$) | V_{OH} | 2.0 | $V_{DDIO} + 0.3$ | V | 1 |
| Output low voltage ($V_{DDIO} = \text{min}$, $I_{OL} = 1.0 \text{ mA}$) | V_{OL} | $GND - 0.3$ | 0.40 | V | 1 |

Notes:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max V_{IN} values listed in Table 3.
2. The symbol V_{IN} represents the input voltage of the supply. It is referenced in Table 3.

2.6 AC Timing Characteristics

This section describes the AC timing characteristics for the MSC8252.

2.6.1 DDR SDRAM AC Timing Specifications

This section describes the AC electrical characteristics for the DDR SDRAM interface.

2.6.1.1 DDR SDRAM Input AC Timing Specifications

Table 18 provides the input AC timing specifications for the DDR SDRAM when V_{DDDDR} (typ) = 1.8 V.

Table 18. DDR2 SDRAM Input AC Timing Specifications for 1.8 V Interface

| Parameter | Symbol | Min | Max | Unit |
|-----------------------|----------|-------------------|-------------------|------|
| AC input low voltage | V_{IL} | — | $MV_{REF} - 0.20$ | V |
| AC input high voltage | V_{IH} | $MV_{REF} + 0.20$ | — | V |

Note: At recommended operating conditions with V_{DDDDR} of $1.8 \pm 5\%$.

Table 19 provides the input AC timing specifications for the DDR SDRAM when V_{DDDDR} (typ) = 1.5 V.

Table 19. DDR3 SDRAM Input AC Timing Specifications for 1.5 V Interface

| Parameter | Symbol | Min | Max | Unit |
|-----------------------|----------|--------------------|--------------------|------|
| AC input low voltage | V_{IL} | — | $MV_{REF} - 0.175$ | V |
| AC input high voltage | V_{IH} | $MV_{REF} + 0.175$ | — | V |

Note: At recommended operating conditions with V_{DDDDR} of $1.5 \pm 5\%$.

Table 20 provides the input AC timing specifications for the DDR SDRAM interface.

Table 20. DDR SDRAM Input AC Timing Specifications

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|--------------|--------------|------------|----------|-------|
| Controller Skew for MDQS—MDQ/MECC/MDM • 800 MHz data rate • 667 MHz data rate | t_{CISKEW} | -200 -240 | 200 240 | ps ps | 1, 2 |
| Tolerated Skew for MDQS—MDQ/MECC/MDM • 800 MHz data rate • 667 MHz data rate | t_{DISKEW} | -425 -510 | 425 510 | ps ps | 2, 3 |

Notes:

1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that is captured with MDQS[n]. Subtract this value from the total timing budget.
2. At recommended operating conditions with V_{DDDDR} (1.8 V or 1.5 V) $\pm 5\%$
3. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW} . This can be determined by the following equation: $t_{DISKEW} = \pm(T \div 4 - \text{abs}(t_{CISKEW}))$ where T is the clock period and $\text{abs}(t_{CISKEW})$ is the absolute value of t_{CISKEW} .

Figure 11 shows the DDR2 and DDR3 SDRAM interface input timing diagram.

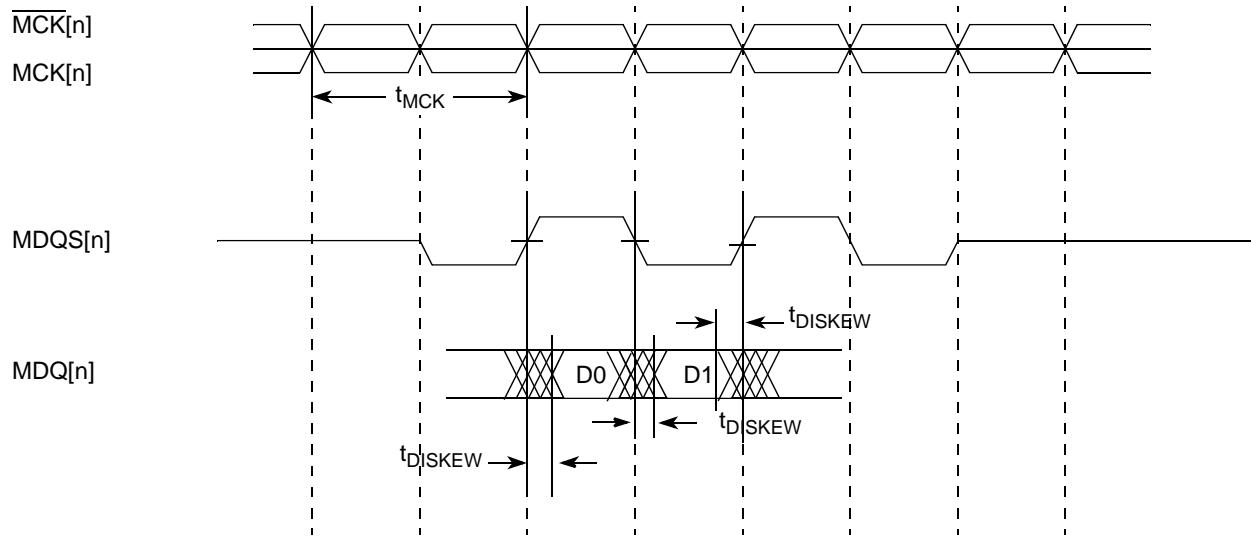


Figure 11. DDR2 and DDR3 SDRAM Interface Input Timing Diagram

2.6.1.2 DDR SDRAM Output AC Timing Specifications

Table 21 provides the output AC timing specifications for the DDR SDRAM interface.

Table 21. DDR SDRAM Output AC Timing Specifications

| Parameter | Symbol ¹ | Min | Max | Unit | Notes |
|--|--------------------------------|-----------------------|-----------------------|----------|-------|
| MCK[n] cycle time | t_{MCK} | 2.5 | 5 | ns | 2 |
| ADDR/CMD output setup with respect to MCK | t_{DDKHAS} | | | | 3 |
| • 800 MHz data rate | 0.917 | — | | ns | |
| • 667 MHz data rate | 1.10 | — | | ns | |
| ADDR/CMD output hold with respect to MCK | t_{DDKHAX} | 0.767 | — | ns | 3 |
| • 800 MHz data rate | 1.02 | — | | ns | |
| MCSn output setup with respect to MCK | t_{DDKHCS} | 0.917 | — | ns | 3 |
| • 800 MHz data rate | 1.10 | — | | ns | |
| MCSn output hold with respect to MCK | t_{DDKHCX} | 0.767 | — | ns | 3 |
| • 800 MHz data rate | 1.02 | — | | ns | |
| MCK to MDQS Skew | t_{DDKHMH} | -0.4 -0.6 | 0.375 0.6 | ns | 4 |
| MDQ/MECC/MDM output setup with respect to MDQS | t_{DDKHDS} , t_{DDKLDS} | 300 375 | — | ps ps | 5 |
| MDQ/MECC/MDM output hold with respect to MDQS | t_{DDKHDX} , t_{DDKLDX} | 300 375 | — | ps ps | 5 |
| MDQS preamble | t_{DDKHMP} | $-0.9 \times t_{MCK}$ | — | ns | — |
| MDQS postamble | t_{DDKHME} | $-0.4 \times t_{MCK}$ | $-0.6 \times t_{MCK}$ | ns | — |

Electrical Characteristics

Table 21. DDR SDRAM Output AC Timing Specifications (continued)

| Parameter | Symbol ¹ | Min | Max | Unit | Notes |
|---------------|---------------------|-----|-----|------|--|
| Notes: | | | | | |
| 1. | t_{DDKHAS} | | | | The symbols used for timing specifications follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)\ (reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time. |
| 2. | | | | | All MCK/MCK referenced measurements are made from the crossing of the two signals. |
| 3. | | | | | ADDR/CMD includes all DDR SDRAM output signals except MCK/MCK, MCS, and MDQ/MECC/MDM/MDQS. |
| 4. | | | | | Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK(n) clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. This will typically be set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these two parameters have been set to the same adjustment value. See the <i>MSC8252 Reference Manual</i> for a description and understanding of the timing modifications enabled by use of these bits. |
| 5. | | | | | Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the MSC8252. |
| 6. | | | | | At recommended operating conditions with V_{DDDDR} (1.5 V or 1.8 V) $\pm 5\%$. |

Note: For the ADDR/CMD setup and hold specifications in [Table 21](#), it is assumed that the clock control register is set to adjust the memory clocks by $\frac{1}{2}$ applied cycle.

[Figure 12](#) shows the DDR SDRAM output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).

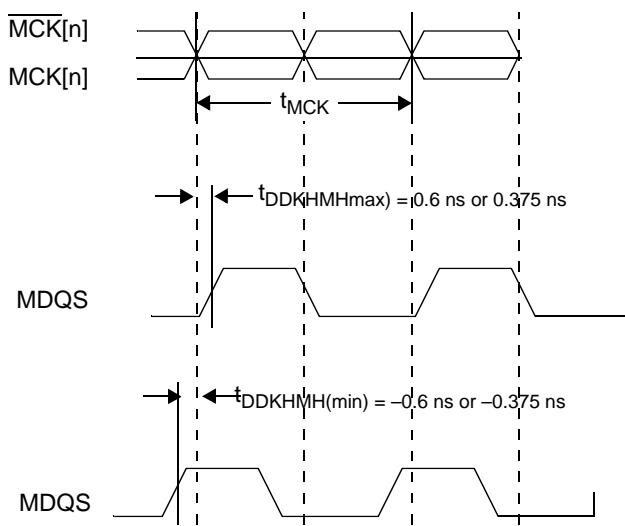


Figure 12. MCK to MDQS Timing

Figure 13 shows the DDR SDRAM output timing diagram.

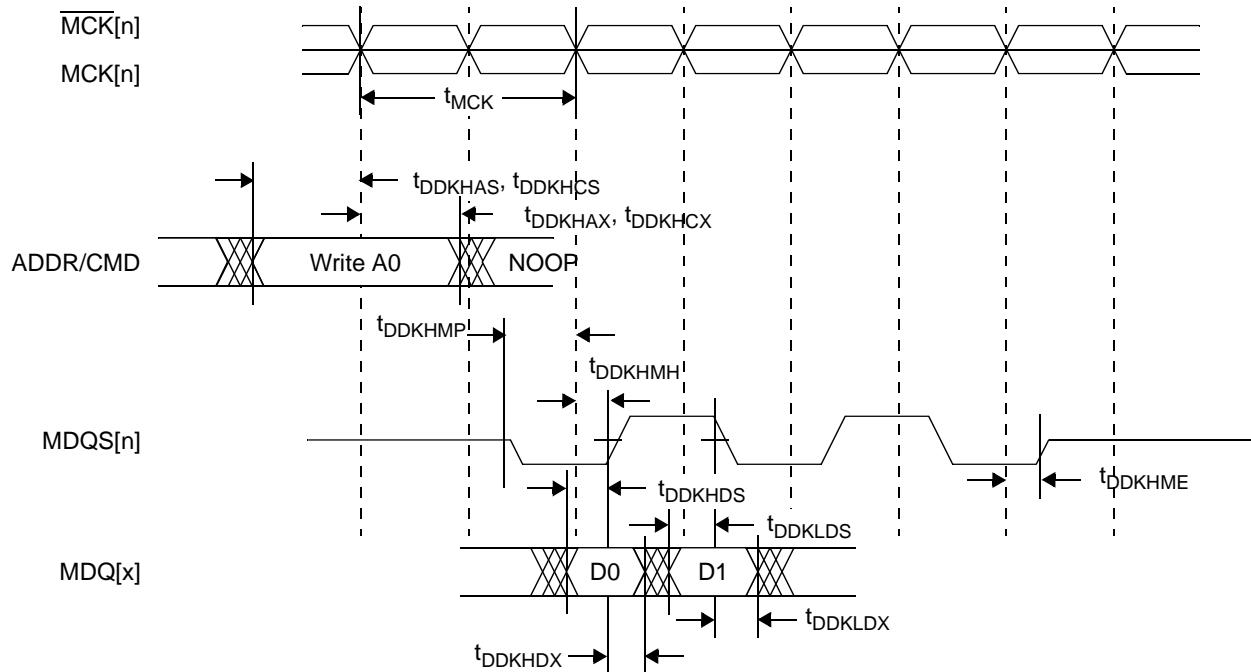


Figure 13. DDR SDRAM Output Timing

Figure 14 provides the AC test load for the DDR2 and DDR3 controller bus.

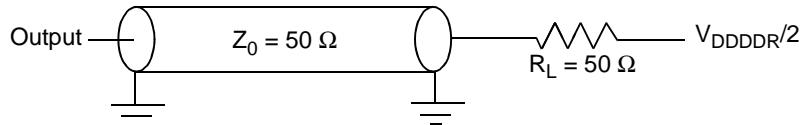


Figure 14. DDR2 and DDR3 Controller Bus AC Test Load

2.6.1.3 DDR2 and DDR3 SDRAM Differential Timing Specifications

This section describes the DC and AC differential timing specifications for the DDR2 and DDR3 SDRAM controller interface. Figure 15 shows the differential timing specification.

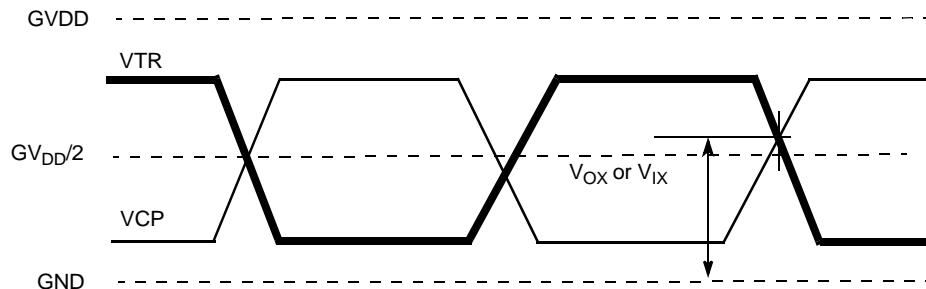


Figure 15. DDR2 and DDR3 SDRAM Differential Timing Specifications

Note: VTR specifies the true input signal (such as MCK or MDQS) and VCP is the complementary input signal (such as MCK or MDQS).

Electrical Characteristics

Table 22 provides the DDR2 differential specifications for the differential signals MDQS/MDQS and MCK/MCK.

Table 22. DDR2 SDRAM Differential Electrical Characteristics

| Parameter | Symbol | Min | Max | Unit |
|--|------------|---------------------------|---------------------------|------|
| Input AC differential cross-point voltage | V_{IXAC} | $0.5 \times GVDD - 0.175$ | $0.5 \times GVDD + 0.175$ | V |
| Output AC differential cross-point voltage | V_{OXAC} | $0.5 \times GVDD - 0.125$ | $0.5 \times GVDD + 0.125$ | V |

Table 23 provides the DDR3 differential specifications for the differential signals MDQS/MDQS and MCK/MCK.

Table 23. DDR3 SDRAM Differential Electrical Characteristics

| Parameter | Symbol | Min | Max | Unit |
|--|------------|---------------------------|---------------------------|------|
| Input AC differential cross-point voltage | V_{IXAC} | $0.5 \times GVDD - 0.150$ | $0.5 \times GVDD + 0.150$ | V |
| Output AC differential cross-point voltage | V_{OXAC} | $0.5 \times GVDD - 0.115$ | $0.5 \times GVDD + 0.115$ | V |

2.6.2 HSSI AC Timing Specifications

The following subsections define the AC timing requirements for the SerDes reference clocks, the PCI Express data lines, the Serial RapidIO data lines, and the SGMII data lines.

2.6.2.1 AC Requirements for SerDes Reference Clock

Table 24 lists AC requirements for the SerDes reference clocks.

Note: Specifications are valid at the recommended operating conditions listed in Table 3.

Table 24. SR[1-2]_REF_CLK and SR[1-2]_REF_CLK Input Clock Requirements

| Parameter | Symbol | Min | Typical | Max | Units | Notes |
|--|-----------------------|------|---------|------|-------|-------|
| SR[1-2]_REF_CLK/SR[1-2]_REF_CLK frequency range | t_{CLK_REF} | — | 100/125 | — | MHz | 1 |
| SR[1-2]_REF_CLK/SR[1-2]_REF_CLK clock frequency tolerance | t_{CLK_TOL} | -350 | — | 350 | ppm | — |
| SR[1-2]_REF_CLK/SR[1-2]_REF_CLK reference clock duty cycle (measured at 1.6 V) | t_{CLK_DUTY} | 40 | 50 | 60 | % | — |
| SR[1-2]_REF_CLK/SR[1-2]_REF_CLK max deterministic peak-peak jitter at 10^{-6} BER | t_{CLK_DJ} | — | — | 42 | ps | — |
| SR[1-2]_REF_CLK/SR[1-2]_REF_CLK total reference clock jitter at 10^{-6} BER (peak-to-peak jitter at ref_clk input) | t_{CLK_TJ} | — | — | 86 | ps | 2 |
| SR[1-2]_REF_CLK/SR[1-2]_REF_CLK rising/falling edge rate | t_{CLKRR}/t_{CLKFR} | 1 | — | 4 | V/ns | 3 |
| Differential input high voltage | V_{IH} | 200 | — | — | mV | 4 |
| Differential input low voltage | V_{IL} | — | — | -200 | mV | 4 |
| Rising edge rate (SR[1-2]_REF_CLK) to falling edge rate (SR[1-2]_REF_CLK) matching | Rise-Fall Matching | — | — | 20 | % | 5, 6 |

Table 24. SR[1-2]_REF_CLK and SR[1-2]_REF_CLK Input Clock Requirements (continued)

| Parameter | Symbol | Min | Typical | Max | Units | Notes |
|---------------|--|-----|---------|-----|-------|-------|
| Notes: | | | | | | |
| 1. | Caution: Only 100 and 125 have been tested. Other values will not work correctly with the rest of the system. | | | | | |
| 2. | Limits from PCI Express CEM Rev 1.0a | | | | | |
| 3. | Measured from -200 mV to +200 mV on the differential waveform (derived from SR[1-2]_REF_CLK minus SR[1-2]_REF_CLK). The signal must be monotonic through the measurement region for rise and fall time. The 400 mV measurement window is centered on the differential zero crossing. See Figure 16 . | | | | | |
| 4. | Measurement taken from differential waveform | | | | | |
| 5. | Measurement taken from single-ended waveform | | | | | |
| 6. | Matching applies to rising edge for SR[1-2]_REF_CLK and falling edge rate for SR[1-2]_REF_CLK. It is measured using a 200 mV window centered on the median cross point where SR[1-2]_REF_CLK rising meets SR[1-2]_REF_CLK falling. The median cross point is used to calculate the voltage thresholds that the oscilloscope uses for the edge rate calculations. The rise edge rate of SR[1-2]_REF_CLK should be compared to the fall edge rate of SR[1-2]_REF_CLK; the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 17 . | | | | | |

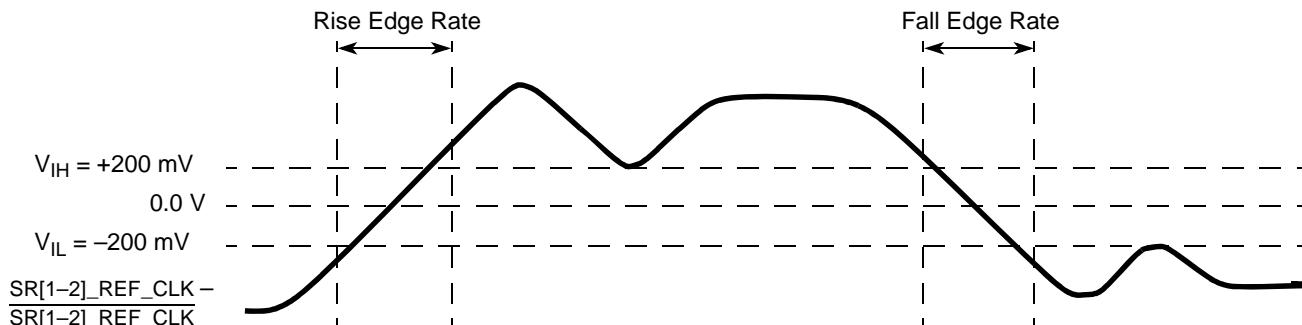


Figure 16. Differential Measurement Points for Rise and Fall Time

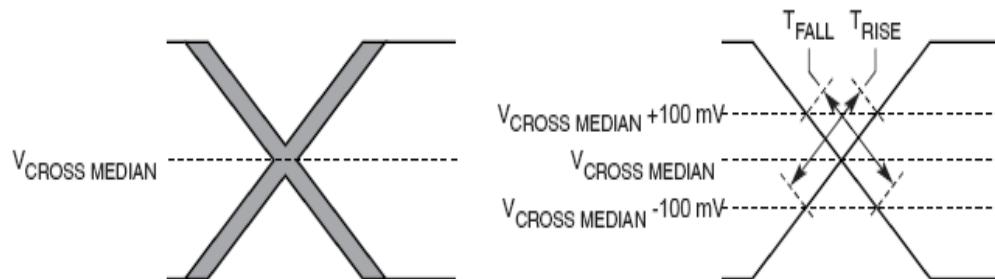


Figure 17. Single-Ended Measurement Points for Rise and Fall Time Matching

2.6.2.2 PCI Express AC Physical Layer Specifications

The AC requirements for PCI Express implementations have separate requirements for the Tx and Rx lines. The MSC8252 supports a 2.5 Gbps PCI Express interface defined by the *PCI Express Base Specification, Revision 1.0a*. The transmitter specifications are defined in [Table 25](#) and the receiver specifications are defined in [Table 26](#). The parameters are specified at the component pins. the AC timing specifications do not include REF_CLK jitter.

Note: Specifications are valid at the recommended operating conditions listed in [Table 3](#).

Table 25. PCI Express (2.5 Gbps) Differential Transmitter (Tx) Output AC Specifications

| Parameter | Symbol | Min | Typical | Max | Units | Notes |
|---|--|--------|---------|--------|-------|-------|
| Unit interval | UI | 399.88 | 400.00 | 400.12 | ps | 1 |
| Minimum Tx eye width | T_{TX-EYE} | 0.70 | — | — | UI | 2, 3 |
| Maximum time between the jitter median and maximum deviation from the median. | $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ | — | — | 0.15 | UI | 3, 4 |
| AC coupling capacitor | C_{TX} | 75 | — | 200 | nF | 5 |
| Notes: | <ol style="list-style-type: none"> 1. Each UI is $400 \text{ ps} \pm 300 \text{ ppm}$. UI does not account for spread spectrum clock dictated variations. No test load is necessarily associated with this value. 2. The maximum transmitter jitter can be derived as $T_{TX-MAX-JITTER} = 1 - T_{TX-EYE} = 0.3 \text{ UI}$. 3. Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 8 and measured over any 250 consecutive Tx UIs. A $T_{TX-EYE} = 0.70 \text{ UI}$ provides for a total sum of deterministic and random jitter budget of $T_{TX-JITTER-MAX} = 0.30 \text{ UI}$ for the transmitter collected over any 250 consecutive Tx UIs. The $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ median is less than half of the total Tx jitter budget collected over any 250 consecutive Tx UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. Jitter is defined as the measurement variation of the crossing points ($V_{TX-DIFFp-p} = 0 \text{ V}$) in relation to a recovered Tx UI. A recovered Tx UI is calculated over 3500 consecutive unit intervals of sample data. 4. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the Tx UI. 5. All transmitters shall be AC-coupled. The AC coupling is required either within the media or within the transmitting component itself. The SerDes transmitter does not have built-in Tx capacitance. An external AC coupling capacitor is required. | | | | | |

Table 26. PCI Express (2.5 Gbps) Differential Receiver (Rx) Input AC Specifications

| Parameter | Symbol | Min | Typical | Max | Units | Notes |
|---|---|--------|---------|--------|-------|---------|
| Unit Interval | UI | 399.88 | 400.00 | 400.12 | ps | 1 |
| Minimum receiver eye width | T_{RX-EYE} | 0.4 | — | — | UI | 2, 3, 4 |
| Maximum time between the jitter median and maximum deviation from the median. | $T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ | — | — | 0.3 | UI | 3, 4, 5 |
| Notes: | <ol style="list-style-type: none"> 1. Each UI is $400 \text{ ps} \pm 300 \text{ ppm}$. UI does not account for spread spectrum clock dictated variations. No test load is necessarily associated with this value. 2. The maximum interconnect media and transmitter jitter that can be tolerated by the receiver can be derived as $T_{RX-MAX-JITTER} = 1 - T_{RX-EYE} = 0.6 \text{ UI}$. 3. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 8 should be used as the Rx device when taking measurements. If the clocks to the Rx and Tx are not derived from the same reference clock, the Tx UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram. 4. A $T_{RX-EYE} = 0.40 \text{ UI}$ provides for a total sum of 0.60 UI deterministic and random jitter budget for the transmitter and interconnect collected any 250 consecutive UIs. The $T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive Tx UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the Rx and Tx are not derived from the same reference clock, the Tx UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram. 5. Jitter is defined as the measurement variation of the crossing points ($V_{RX-DIFFp-p} = 0 \text{ V}$) in relation to a recovered Tx UI. A recovered Tx UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the Tx UI. It is recommended that the recovered Tx UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data. | | | | | |

2.6.2.3 Serial RapidIO AC Timing Specifications

Note: Specifications are valid at the recommended operating conditions listed in [Table 3](#).

[Table 27](#) defines the transmitter AC specifications for the Serial RapidIO interface. The AC timing specifications do not include REF_CLK jitter.

Table 27. Serial RapidIO Transmitter AC Timing Specifications

| Characteristic | Symbol | Min | Typical | Max | Unit |
|----------------------------|--------|--------------|---------|--------------|--------|
| Deterministic Jitter | J_D | — | — | 0.17 | UI p-p |
| Total Jitter | J_T | — | — | 0.35 | UI p-p |
| Unit Interval: 1.25 GBaud | UI | 800 – 100ppm | 800 | 800 + 100ppm | ps |
| Unit Interval: 2.5 GBaud | UI | 400 – 100ppm | 400 | 400 + 100ppm | ps |
| Unit Interval: 3.125 GBaud | UI | 320 – 100ppm | 320 | 320 + 100ppm | ps |

[Table 28](#) defines the Receiver AC specifications for the Serial RapidIO interface. The AC timing specifications do not include REF_CLK jitter.

Table 28. Serial RapidIO Receiver AC Timing Specifications

| Characteristic | Symbol | Min | Typical | Max | Unit | Notes |
|--|----------|--------------|---------|--------------|--------|-------|
| Deterministic Jitter Tolerance | J_D | 0.37 | — | — | UI p-p | 1 |
| Combined Deterministic and Random Jitter Tolerance | J_{DR} | 0.55 | — | — | UI p-p | 1 |
| Total Jitter Tolerance | J_T | 0.65 | — | — | UI p-p | 1, 2 |
| Bit Error Rate | BER | — | — | 10^{-12} | — | — |
| Unit Interval: 1.25 GBaud | UI | 800 – 100ppm | 800 | 800 + 100ppm | ps | — |
| Unit Interval: 2.5 GBaud | UI | 400 – 100ppm | 400 | 400 + 100ppm | ps | — |
| Unit Interval: 3.125 GBaud | UI | 320 – 100ppm | 320 | 320 + 100ppm | ps | — |

Notes:

1. Measured at receiver.
2. Total jitter is composed of three components, deterministic jitter, random jitter, and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of [Figure 18](#). The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk, and other variable system effects.

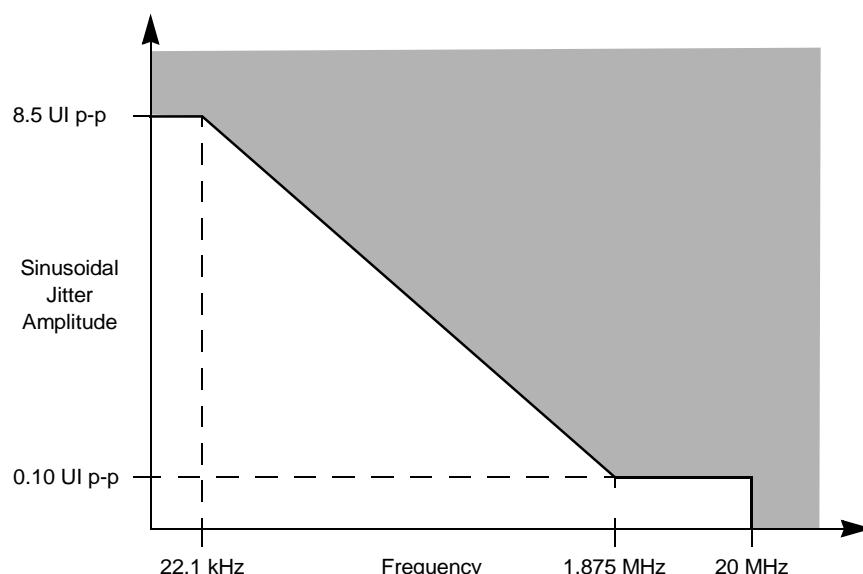


Figure 18. Single Frequency Sinusoidal Jitter Limits

2.6.2.4 SGMII AC Timing Specifications

Note: Specifications are valid at the recommended operating conditions listed in [Table 3](#).

Transmitter and receiver AC characteristics are measured at the transmitter outputs ($SR[1-2]_{TX}[n]$ and $\overline{SR[1-2]_{TX}[n]}$) or at the receiver inputs ($SR[1-2]_{RX}[n]$ and $SR[1-2]_{RX}[n]$) as depicted in [Figure 19](#), respectively.

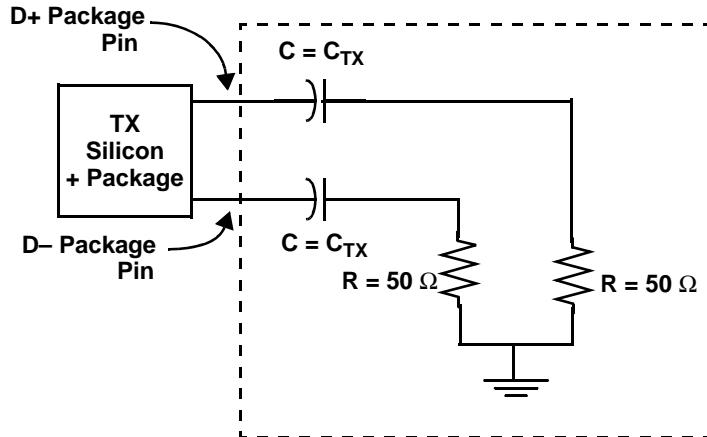


Figure 19. SGMII AC Test/Measurement Load

[Table 29](#) provides the SGMII transmit AC timing specifications. A source synchronous clock is not supported. The AC timing specifications do not include REF_CLK jitter.

Table 29. SGMII Transmit AC Timing Specifications

| Parameter | Symbol | Min | Typ | Max | Unit | Notes |
|--|--------|--------|-----|--------|--------|-------|
| Deterministic Jitter | JD | — | — | 0.17 | UI p-p | — |
| Total Jitter | JT | — | — | 0.35 | UI p-p | 2 |
| Unit Interval | UI | 799.92 | 800 | 800.08 | ps | 1 |
| Notes: | | | | | | |
| 1. See Figure 18 for single frequency sinusoidal jitter limits | | | | | | |
| 2. Each UI is 800 ps \pm 100 ppm. | | | | | | |

[Table 30](#) provides the SGMII receiver AC timing specifications. The AC timing specifications do not include REF_CLK jitter.

Table 30. SGMII Receive AC Timing Specifications

| Parameter | Symbol | Min | Typ | Max | Unit | Notes |
|---|--------|--------|--------|------------|--------|-------|
| Deterministic Jitter Tolerance | JD | 0.37 | — | — | UI p-p | 1, 2 |
| Combined Deterministic and Random Jitter Tolerance | JDR | 0.55 | — | — | UI p-p | 1, 2 |
| Total Jitter Tolerance | JT | 0.65 | — | — | UI p-p | 1, 2 |
| Bit Error Ratio | BER | — | — | 10^{-12} | — | — |
| Unit Interval | UI | 799.92 | 800.00 | 800.08 | ps | 3 |
| Notes: | | | | | | |
| 1. Measured at receiver. | | | | | | |
| 2. Refer to RapidIO™ 1x/4x LP Serial Physical Layer Specification for interpretation of jitter specifications. Also see Figure 18 . | | | | | | |
| 3. Each UI is 800 ps \pm 100 ppm. | | | | | | |

2.6.3 TDM Timing

Table 31 provides the input and output AC timing specifications for the TDM interface.

Table 31. TDM AC Timing Specifications for 62.5 MHz¹

| Parameter | Symbol ² | Min | Max | Unit |
|--|---------------------|------|------|------|
| TDMxRCK/TDMxTCK | t_{DM} | 16.0 | — | ns |
| TDMxRCK/TDMxTCK high pulse width | t_{DM_HIGH} | 7.0 | — | ns |
| TDMxRCK/TDMxTCK low pulse width | t_{DM_LOW} | 7.0 | — | ns |
| TDM all input setup time | t_{DMIVKH} | 3.6 | — | ns |
| TDMxRD hold time | $t_{DMRDIXKH}$ | 1.9 | — | ns |
| TDMxTFS/TDMxRFS input hold time | $t_{DMFSIXKH}$ | 1.9 | — | ns |
| TDMxTCK High to TDMxTD output active | t_{DM_OUTAC} | 2.5 | — | ns |
| TDMxTCK High to TDMxTD output valid | $t_{DMTKHOV}$ | — | 9.8 | ns |
| TDMxTD hold time | $t_{DMTKHOX}$ | 2.5 | — | ns |
| TDMxTCK High to TDMxTD output high impedance | t_{DM_OUTHI} | — | 9.8 | ns |
| TDMxTFS/TDMxRFS output valid | $t_{DMFSKHOV}$ | — | 9.25 | ns |
| TDMxTFS/TDMxRFS output hold time | $t_{DMFSKHOX}$ | 2.0 | — | ns |

Notes:

1. The symbols used for timing specifications follow the pattern $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)(reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{HIKHOX} symbolizes the output internal timing (HI) for the time t_{serial} memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).
2. Output values are based on 30 pF capacitive load.
3. Inputs are referenced to the sampling that the TDM is programmed to use. Outputs are referenced to the programming edge they are programmed to use. Use of the rising edge or falling edge as a reference is programmable. T_{DMxTCK} and T_{DMxRCK} are shown using the rising edge.
4. All values are based on a maximum TDM interface frequency of 62.5 MHz.

Figure 20 shows the TDM receive signal timing.

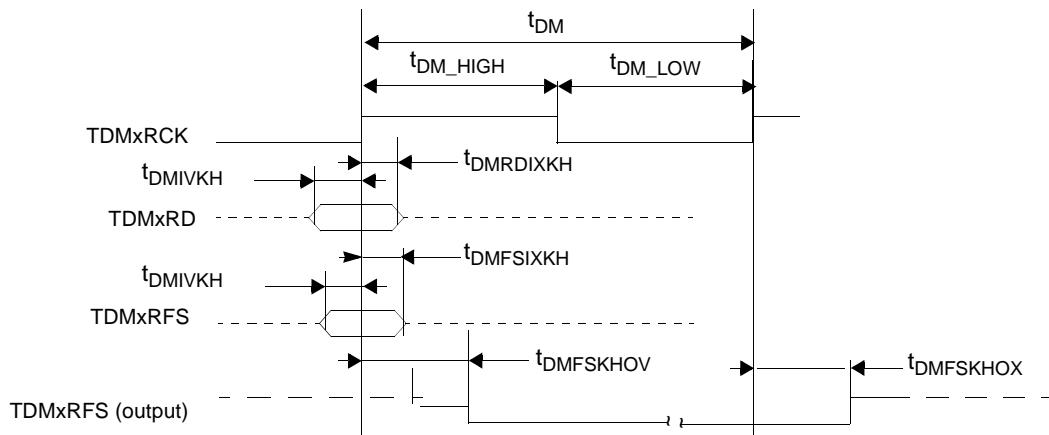


Figure 20. TDM Receive Signals

Electrical Characteristics

Figure 21 shows the TDM transmit signal timing.

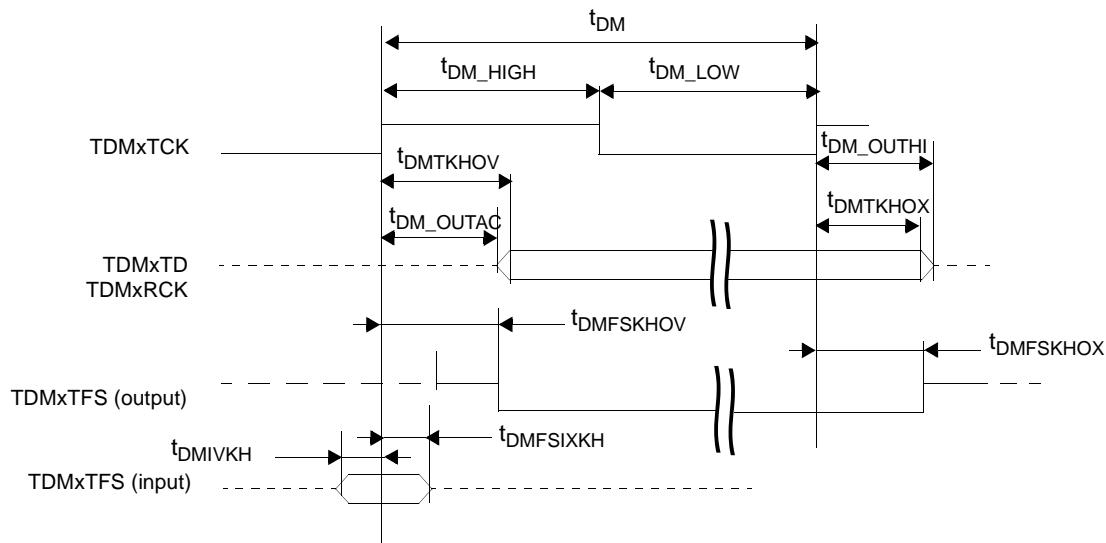


Figure 21. TDM Transmit Signals

Figure 22 provides the AC test load for the TDM/SI.

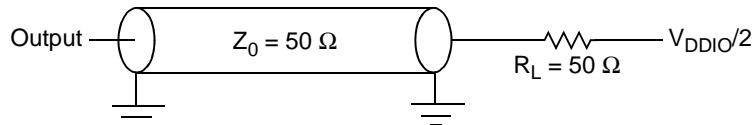


Figure 22. TDM AC Test Load

2.6.4 Timers AC Timing Specifications

Table 32 lists the timer input AC timing specifications.

Table 32. Timers Input AC Timing Specifications

| Characteristics | Symbol | Minimum | Unit | Notes |
|---|-------------|---------|------|-------|
| Timers inputs—minimum pulse width | t_{TIWID} | 8 | ns | 1, 2 |
| Notes: 1. The maximum allowed frequency of timer outputs is 125 MHz. Configure the timer modules appropriately. 2. Timer inputs and outputs are asynchronous to any visible clock. Timer outputs should be synchronized before use by any external synchronous logic. Timer inputs are required to be valid for at least t_{TIWID} ns to ensure proper operation. | | | | |

Note: For recommended operating conditions, see Table 3.

Figure 23 shows the AC test load for the timers.

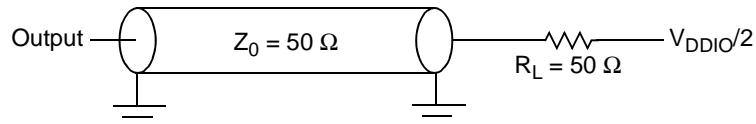


Figure 23. Timer AC Test Load

2.6.5 Ethernet Timing

This section describes the AC electrical characteristics for the Ethernet interface.

There are programmable delay units (PDU) that should be programmed differently for each interface to meet timing. There is a general configuration register 4 (GCR4) used to configure the timing. For additional information, see the *MSC8252 Reference Manual*.

2.6.5.1 Management Interface Timing

Table 33 lists the timer input Ethernet controller management interface timing specifications shown in Figure 24.

Table 33. Ethernet Controller Management Interface Timing

| Characteristics | Symbol | Min | Max | Unit |
|--|--------------|-----|-----|------|
| GE_MDC frequency | f_{MDC} | — | 2.5 | MHz |
| GE_MDC period | t_{MDC} | 400 | — | ns |
| GE_MDC clock pulse width high | t_{MDC_H} | 160 | — | ns |
| GE_MDC clock pulse width low | t_{MDC_L} | 160 | — | ns |
| GE_MDC to GE_MDIO delay ² | t_{MDKHD} | 10 | 70 | ns |
| GE_MDIO to GE_MDC rising edge setup time | t_{MDDVKH} | 20 | — | ns |
| GE_MDC rising edge to GE_MDIO hold time | t_{MDDXKH} | 0 | — | ns |

Notes:

1. Program the GE_MDC frequency (f_{MDC}) to a maximum value of 2.5 MHz (400 ns period for t_{MDC}). The value depends on the source clock and configuration of MIIMCFG[MCS] and UPSMR[MDCP]. For example, for a source clock of 400 MHz to achieve $f_{MDC} = 2.5$ MHz, program MIIMCFG[MCS] = 0x4 and UPSMR[MDCP] = 0. See the *MSC8252 Reference Manual* for configuration details.
2. The value depends on the source clock. For example, for a source clock of 267 MHz, the delay is 70 ns. For a source clock of 333 MHz, the delay is 58 ns.

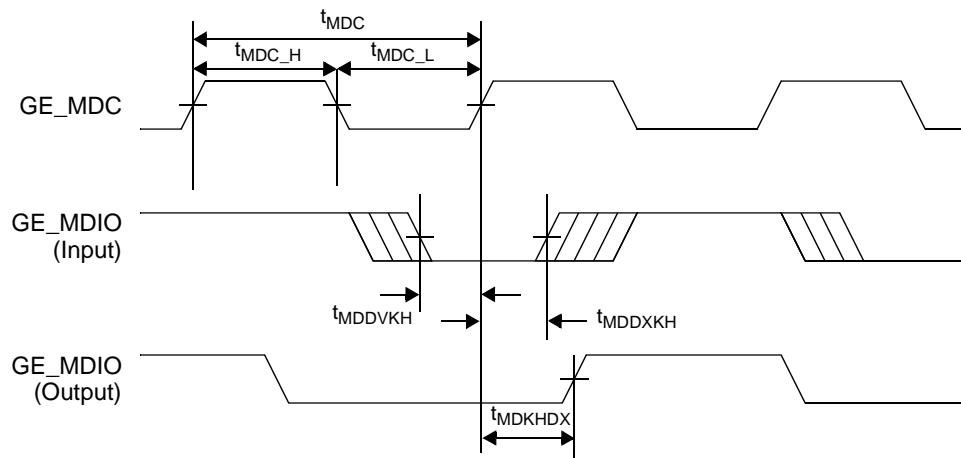


Figure 24. MII Management Interface Timing

2.6.5.2 RGMII AC Timing Specifications

Table 34 presents the RGMII AC timing specifications for applications requiring an on-board delayed clock.

Table 34. RGMII at 1 Gbps² with On-Board Delay³ AC Timing Specifications

| Parameter/Condition | Symbol | Min | Typ | Max | Unit |
|--|-------------|------|-----|-----|------|
| Data to clock output skew (at transmitter) ⁴ | t_{SKEWT} | -0.5 | — | 0.5 | ns |
| Data to clock input skew (at receiver) ⁴ | t_{SKEWR} | 1 | — | 2.6 | ns |
| Notes: | | | | | |
| 1. At recommended operating conditions with V_{DDIO} of 2.5 V \pm 5%. | | | | | |
| 2. RGMII at 100 Mbps support is guaranteed by design. | | | | | |
| 3. Program GCR4 as 0x00000000. | | | | | |
| 4. This implies that PC board design requires clocks to be routed such that an additional trace delay of greater than 1.5 ns and less than 2.0 ns is added to the associated clock signal. | | | | | |

Table 35 presents the RGMII AC timing specification for applications required non-delayed clock on board.

Table 35. RGMII at 1 Gbps² with No On-Board Delay³ AC Timing Specifications

| Parameter/Condition | Symbol | Min | Typ | Max | Unit |
|--|-------------|------|-----|------|------|
| Data to clock output skew (at transmitter) ⁴ | t_{SKEWT} | -2.6 | — | -1.0 | ns |
| Data to clock input skew (at receiver) ⁴ | t_{SKEWR} | -0.5 | — | 0.5 | ns |
| Notes: | | | | | |
| 1. At recommended operating conditions with V_{DDIO} of 2.5 V \pm 5%. | | | | | |
| 2. RGMII at 100 Mbps support is guaranteed by design. | | | | | |
| 3. GCR4 should be programmed as 0x000CC330. | | | | | |
| 4. This implies that PC board design requires clocks to be routed with no additional trace delay | | | | | |

Figure 25 shows the RGMII AC timing and multiplexing diagrams.

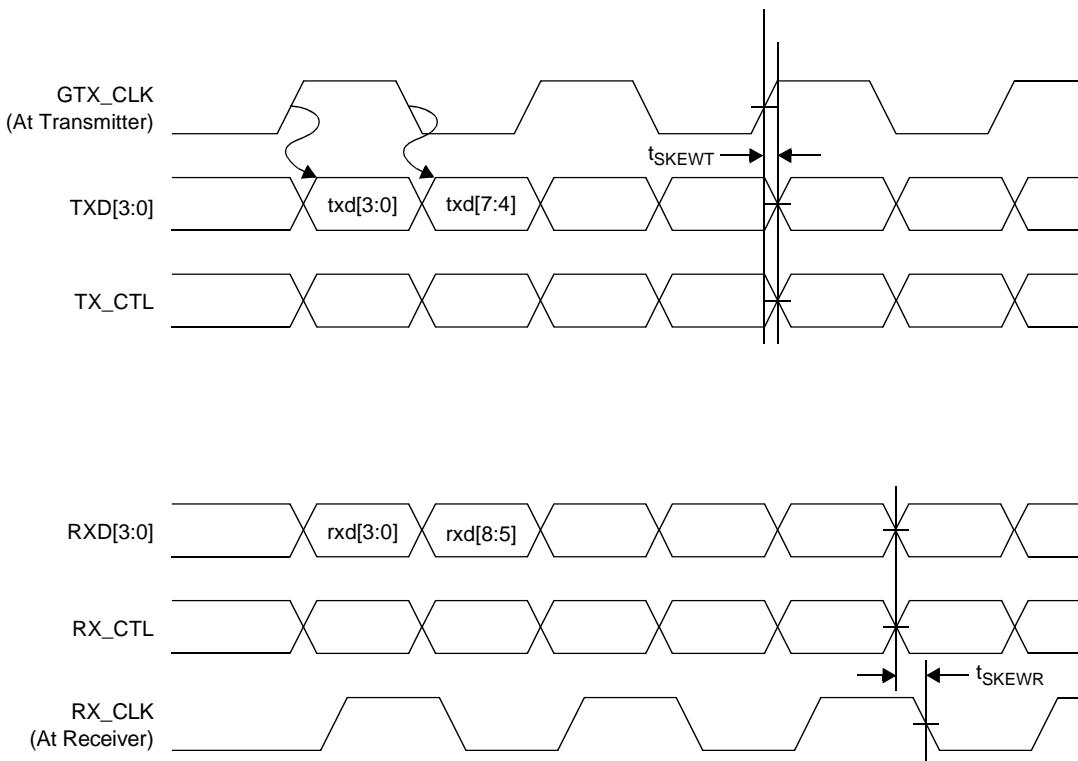


Figure 25. RGMII AC Timing and Multiplexing

2.6.6 SPI Timing

Table 36 lists the SPI input and output AC timing specifications.

Table 36. SPI AC Timing Specifications

| Parameter | Symbol ¹ | Min | Max | Unit | Note |
|--|---------------------|-----|-----|------|------|
| SPI outputs valid—Master mode (internal clock) delay | t_{NIKHOV} | — | 6 | ns | 2 |
| SPI outputs hold—Master mode (internal clock) delay | t_{NIKHOX} | 0.5 | — | ns | 2 |
| SPI outputs valid—Slave mode (external clock) delay | t_{NEKHOV} | — | 12 | ns | 2 |
| SPI outputs hold—Slave mode (external clock) delay | t_{NEKHOX} | 2 | — | ns | 2 |
| SPI inputs—Master mode (internal clock) input setup time | t_{NIIVKH} | 12 | — | ns | — |
| SPI inputs—Master mode (internal clock) input hold time | t_{NIIXKH} | 0 | — | ns | — |
| SPI inputs—Slave mode (external clock) input setup time | t_{NEIVKH} | 4 | — | ns | — |
| SPI inputs—Slave mode (external clock) input hold time | t_{NEIXKH} | 2 | — | ns | — |
| Notes: | | | | | |
| 1. The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})}$ (reference)(state) for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{NIKHOX} symbolizes the internal timing (NI) for the time SPICLK clock reference (K) goes to the high state (H) until outputs (O) are invalid (X). | | | | | |
| 2. Output specifications are measured from the 50% level of the rising edge of SPICLK to the 50% level of the signal. Timings are measured at the pin. | | | | | |

Figure 26 provides the AC test load for the SPI.

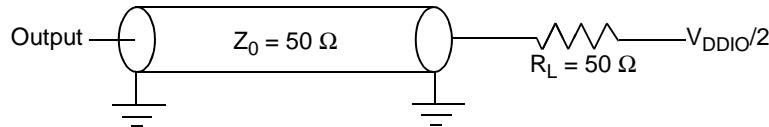
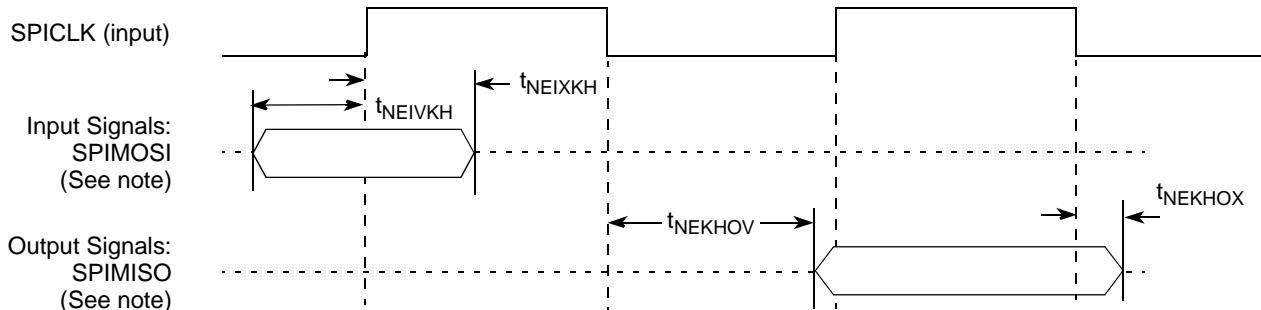


Figure 26. SPI AC Test Load

Figure 27 and Figure 28 represent the AC timings from Table 36. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

Figure 27 shows the SPI timings in slave mode (external clock).

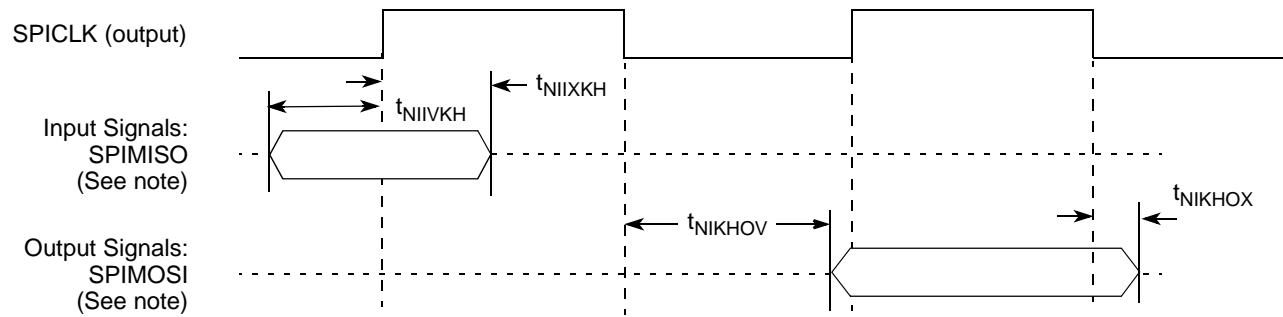


Note: measured with SPMODE[CI] = 0, SPMODE[CP] = 0

Figure 27. SPI AC Timing in Slave Mode (External Clock)

Figure 28 shows the SPI timings in master mode (internal clock).

Electrical Characteristics



Note: measured with SPMODE[CI] = 0, SPMODE[CP] = 0

Figure 28. SPI AC Timing in Master Mode (Internal Clock)

2.6.7 Asynchronous Signal Timing

Table 35 lists the asynchronous signal timing specifications.

Table 37. Signal Timing

| Characteristics | Symbol | Type | Min |
|--|-----------|--------------|-----------------------|
| Input | t_{IN} | Asynchronous | One CLKIN cycle |
| Output | t_{OUT} | Asynchronous | Application dependent |
| Note: Input value relevant for EE0, $\overline{IRQ[15-0]}$, and \overline{NMI} only. | | | |

The following interfaces use the specified asynchronous signals:

- *GPIO*. Signals GPIO[31–0], when used as GPIO signals, that is, when the alternate multiplexed special functions are not selected.

Note: When used as a general purpose input (GPI), the input signal should be driven until it is acknowledged by the MSC8252 device, that is, when the expected input value is read from the GPIO data register.

- *EE port*. Signals EE0, EE1.
- *Boot function*. Signal $STOP_BS$.
- *I^2C interface*. Signals $I2C_SCL$ and $I2C_SDA$.
- *Interrupt inputs*. Signals $\overline{IRQ[15-0]}$ and \overline{NMI} .
- *Interrupt outputs*. Signals $\overline{INT_OUT}$ and $\overline{NMI_OUT}$ (minimum pulse width is 32 ns).

2.6.8 JTAG Signals

Table 38 lists the JTAG timing specifications shown in Figure 29 through Figure 32.

Table 38. JTAG Timing

| Characteristics | Symbol | All frequencies | | Unit |
|---|--------------|-----------------|------|------|
| | | Min | Max | |
| TCK cycle time | t_{TCKX} | 36.0 | — | ns |
| TCK clock high phase measured at $V_M = V_{DDIO}/2$ | t_{TCKH} | 15.0 | — | ns |
| Boundary scan input data setup time | t_{BSVKH} | 0.0 | — | ns |
| Boundary scan input data hold time | t_{BSXKH} | 15.0 | — | ns |
| TCK fall to output data valid | t_{TCKHOV} | — | 20.0 | ns |
| TCK fall to output high impedance | t_{TCKHOZ} | — | 24.0 | ns |
| TMS, TDI data setup time | t_{TDIVKH} | 0.0 | — | ns |
| TMS, TDI data hold time | t_{TDIXKH} | 5.0 | — | ns |
| TCK fall to TDO data valid | t_{TDOHOV} | — | 10.0 | ns |
| TCK fall to TDO high impedance | t_{TDOHOZ} | — | 12.0 | ns |
| TRST assert time | t_{TRST} | 100.0 | — | ns |

Note: All timings apply to OnCE module data transfers as well as any other transfers via the JTAG port.

Figure 29 shows the test clock input timing diagram

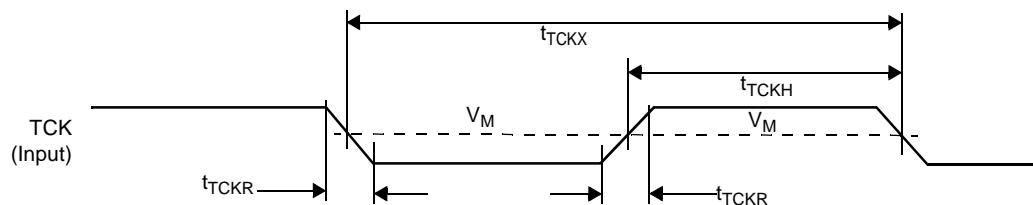


Figure 29. Test Clock Input Timing

Figure 30 shows the boundary scan (JTAG) timing diagram.

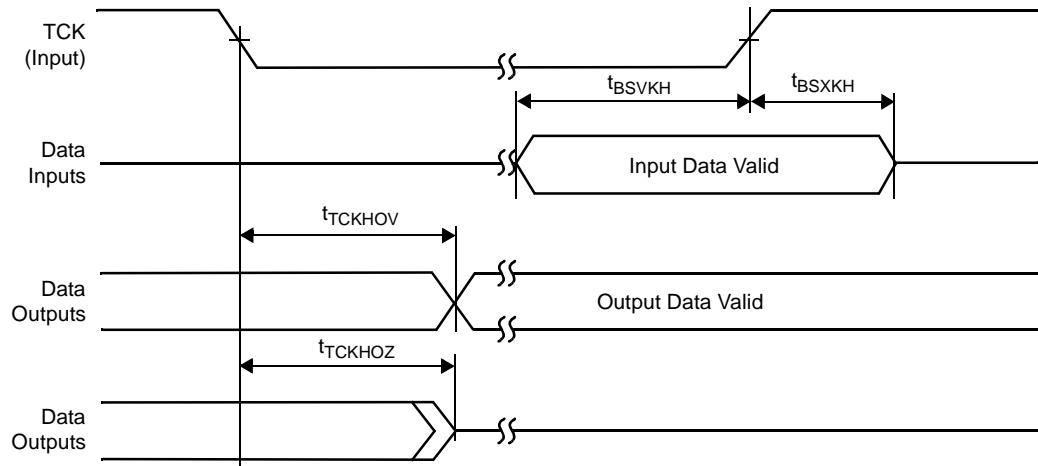


Figure 30. Boundary Scan (JTAG) Timing

Figure 31 shows the test access port timing diagram.

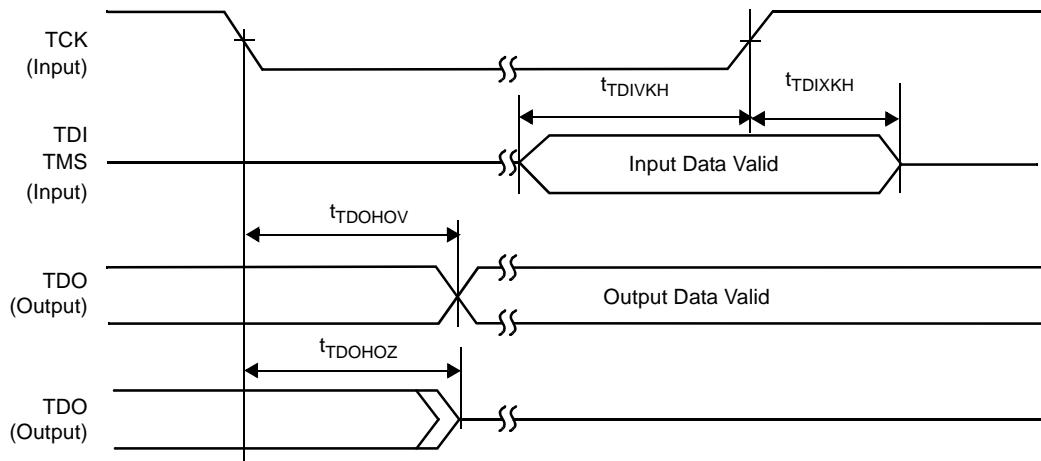


Figure 31. Test Access Port Timing

Figure 32 shows the $\overline{\text{TRST}}$ timing diagram.



Figure 32. $\overline{\text{TRST}}$ Timing

3 Hardware Design Considerations

The following sections discuss areas to consider when the MSC8252 device is designed into a system.

3.1 Power Supply Ramp-Up Sequence

The following subsections describe the required device initialization sequence.

3.1.1 Clock, Reset, and Supply Coordination

Starting the device requires coordination between several inputs including: clock, reset, and power supplies. Follow this guidelines when starting up an MSC8252 device:

- $\overline{\text{PORESET}}$ and $\overline{\text{TRST}}$ must be asserted externally for the duration of the supply ramp-up, using the V_{DDIO} supply. $\overline{\text{TRST}}$ deassertion does not have to be synchronized with $\overline{\text{PORESET}}$ deassertion. However, $\overline{\text{TRST}}$ must be deasserted before normal operation begins to ensure correct functionality of the device.
- CLKIN should toggle at least 32 cycles before $\overline{\text{PORESET}}$ deassertion to guarantee correct device operation. The 32 cycles should only be counted from the time after V_{DDIO} reaches its nominal value (see timing 1 in Figure 33).
- CLKIN should either be stable low during ramp-up of V_{DDIO} supply (and start its swings after ramp-up) or should swing within V_{DDIO} range during V_{DDIO} ramp-up, so its amplitude grows as V_{DDIO} grows during ramp-up.

Figure 33 shows a sequence in which V_{DDIO} ramps-up after V_{DD} and CLKIN begins to toggle with the raise of V_{DDIO} supply.

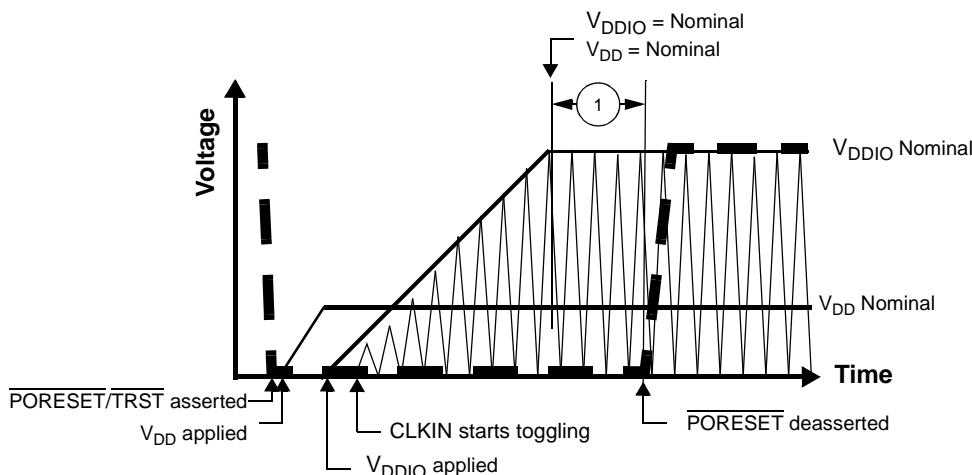


Figure 33. Supply Ramp-Up Sequence with V_{DD} Ramping Before V_{DDIO} and CLKIN Starting With V_{DDIO}

Note: For details on power-on reset flow and duration, see the *Reset* chapter in the *MSC8252 Reference Manual*.

3.1.2 Power-On Ramp Time

This section describes the AC electrical specification for the power-on ramp rate requirements for all voltage supplies (including GVDD/SXPVDD/SXCVDD/QVDD/GVDD/NVDD, all VDD supplies, MVREF, and all AVDD supplies). Controlling the power-on ramp time is required to avoid falsely triggering the ESD circuitry. [Table 39](#) defines the power supply ramp time specification.

Table 39. Power Supply Ramp Rate

| Parameter | Min | Max | Unit |
|---------------------|-----|-------|------|
| Required ramp rate. | — | 36000 | V/s |

Notes:

1. Ramp time is specified as a linear ramp from 10% to 90% of nominal voltage of the specific voltage supply. If the ramp is non-linear (for example, exponential), the maximum rate of change from 200 to 500 mV is the most critical because this range might falsely trigger the ESD circuitry.
2. Required over the full recommended operating temperature range (see [Table 3](#)).
3. All supplies must be at their stable values within 50 ms.
4. The GVDD pins can be held low on the application board at powerup. If GVDD is not held low, then GVDD will rise to a voltage level that depends on the board-level impedance-to-ground. If the impedance is high (that is, infinite), then theoretically, GVDD can rise up close to the VDD levels.

3.1.3 Power Supply Guidelines

Use the following guidelines for power-up sequencing:

- Couple M3VDD with the VDD power rail using an extremely low impedance path.
- Couple inputs PLL1_AVDD, PLL2_AVDD and PLL3_AVDD with the VDD power rail using an RC filter (see [Figure 37](#)).
- There is no dependency in power-on/power-off sequence between the GVDD1, GVDD2, NVDD, and QVDD power rails.
- Couple inputs M1VREF and M2VREF with the GVDD1 and GVDD2 power rails, respectively. They should rise at the same time as or after their respective power rail.
- There is no dependency between RapidIO supplies: SXCVDD1, SXCVDD2, SXPVDD1 and SXPVDD2 and other MSC8252 supplies in the power-on/power-off sequence
- Couple inputs SR1_PLL_AVDD and SR2_PLL_AVDD with SXCVDD1 and SXCVDD2 power rails, respectively, using an RC filter (see [Figure 38](#)).

External voltage applied to any input line must not exceed the I/O supply voltage related to this line by more than 0.6 V at any time, including during power-up. Some designs require pull-up voltages applied to selected input lines during power-up for configuration purposes. This is an acceptable exception to the rule during start-up. However, each such input can draw up to 80 mA per input pin per MSC8252 device in the system during power-up. An assertion of the inputs to the high voltage level before power-up should be with slew rate less than 4 V/ns.

The device power rails should rise in the following sequence:

1. VDD (and all coupled supplies)

2. After the above rails rise to 90% of their nominal voltage, the following I/O power rails may rise in any sequence (see [Figure 34](#)): QVDD, NVDD, GVDD1, and GVDD2.

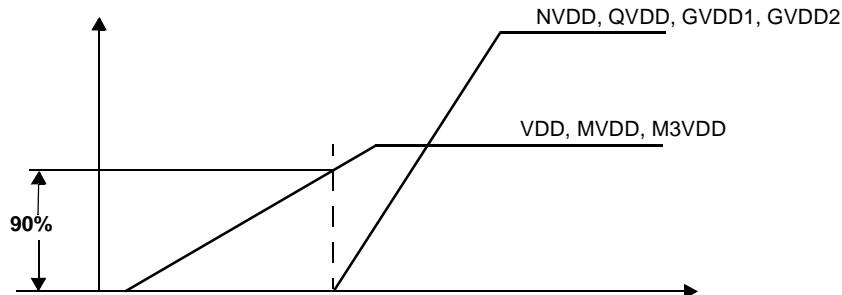


Figure 34. Supply Ramp-Up Sequence

Notes:

1. If the M3 memory is not used, M3VDD can be tied to GND.
2. If the HSSI port1 is not used, SXCVDD1 and SXPVDD1 must be connected to the designated power supplies.
3. If the HSSI port2 is not used, SXCVDD2 and SXPVDD2 must be connected to the designated power supplies.
4. If the DDR port 1 interface is not used, it is recommended that GVDD1 be left unconnected.
5. If the DDR port 2 interface is not used, it is recommended that GVDD2 be left unconnected.

3.1.4 Reset Guidelines

When a debugger is not used, implement the connection scheme shown in [Figure 35](#).



Figure 35. Reset Connection in Functional Application

When a debugger is used, implement the connection scheme shown in [Figure 36](#).

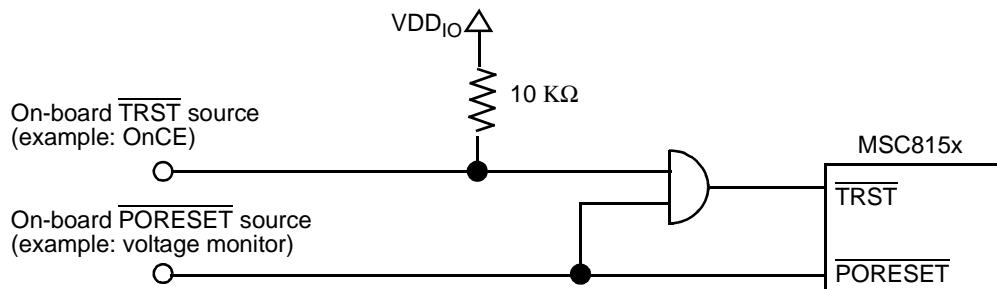


Figure 36. Reset Connection in Debugger Application

3.2 PLL Power Supply Design Considerations

Each global PLL power supply must have an external RC filter for the $\text{PLL}_n\text{_AVDD}$ input (see [Figure 37](#)) in which the following components are defined as listed:

- $R = 5 \Omega \pm 5\%$
- $C1 = 10 \mu\text{F} \pm 10\%$, 0603, X5R, with $\text{ESL} \leq 0.5 \text{ nH}$, low ESL Surface Mount Capacitor.
- $C2 = 1.0 \mu\text{F} \pm 10\%$, 0402, X5R, with $\text{ESL} \leq 0.5 \text{ nH}$, low ESL Surface Mount Capacitor.

Note: A higher capacitance value for $C2$ may be used to improve the filter as long as the other $C2$ parameters do not change.

All three PLLs can connect to a single supply voltage source (such as a voltage regulator) as long as the external RC filter is applied to each PLL separately. For optimal noise filtering, place the circuit as close as possible to its $\text{PLL}_n\text{_AVDD}$ inputs.

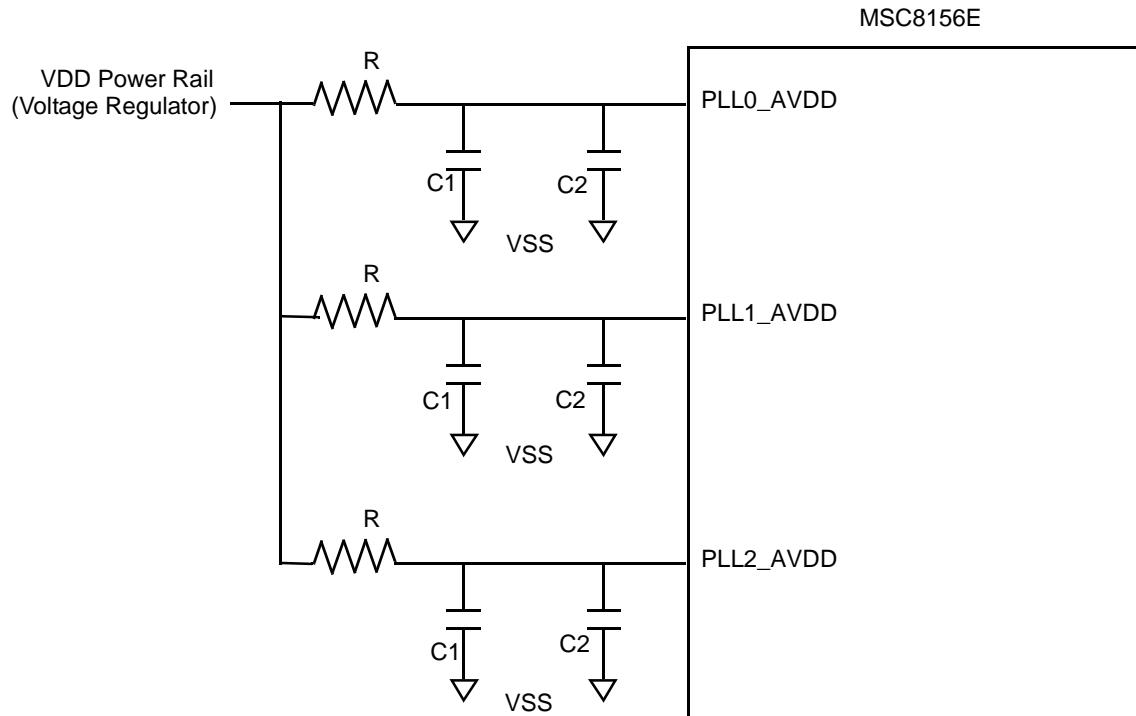


Figure 37. PLL Supplies

Each SerDes PLL power supply must be filtered using a circuit similar to the one shown in [Figure 38](#), to ensure stability of the internal clock. For maximum effectiveness, the filter circuit should be placed as closely as possible to the $\text{SR}_n\text{_PLL_AVDD}$ ball to ensure it filters out as much noise as possible. The ground connection should be near the $\text{SR}_n\text{_PLL_AVDD}$ ball. The $0.003 \mu\text{F}$ capacitor is closest to the ball, followed by the two $2.2 \mu\text{F}$ capacitors, and finally the 1Ω resistor to the board supply plane. The capacitors are connected from $\text{SR}_n\text{_PLL_AVDD}$ to the ground plane. Use ceramic chip capacitors with the highest possible self-resonant frequency. All trances should be kept short, wide, and direct.

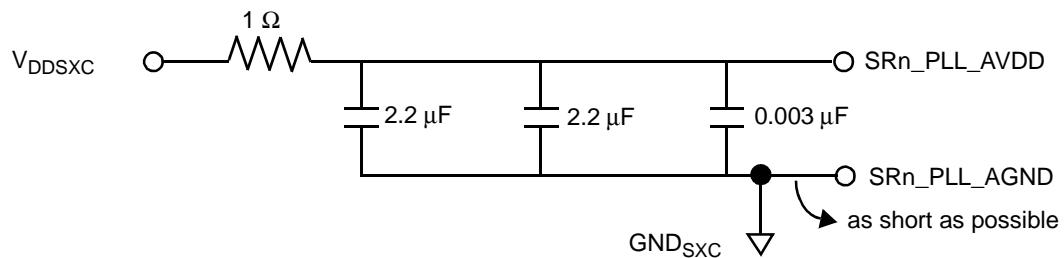


Figure 38. SerDes PLL Supplies

3.3 Clock and Timing Signal Board Layout Considerations

When laying out the system board, use the following guidelines:

- Keep clock and timing signal paths as short as possible and route with $50\ \Omega$ impedance.
- Use a serial termination resistor placed close to the clock buffer to minimize signal reflection. Use the following equation to compute the resistor value:

$$R_{\text{term}} = R_{\text{im}} - R_{\text{buf}}$$

where R_{im} = trace characteristic impedance

R_{buf} = clock buffer internal impedance.

3.4 SGMII AC-Coupled Serial Link Connection Example

Figure 39 shows an example of a 4-wire AC-coupled serial link connection. For additional layout suggestions, see *AN3556 MSC815x High Speed Serial Interface Hardware Design Considerations*, available on the Freescale website or from your local sales office or representative.

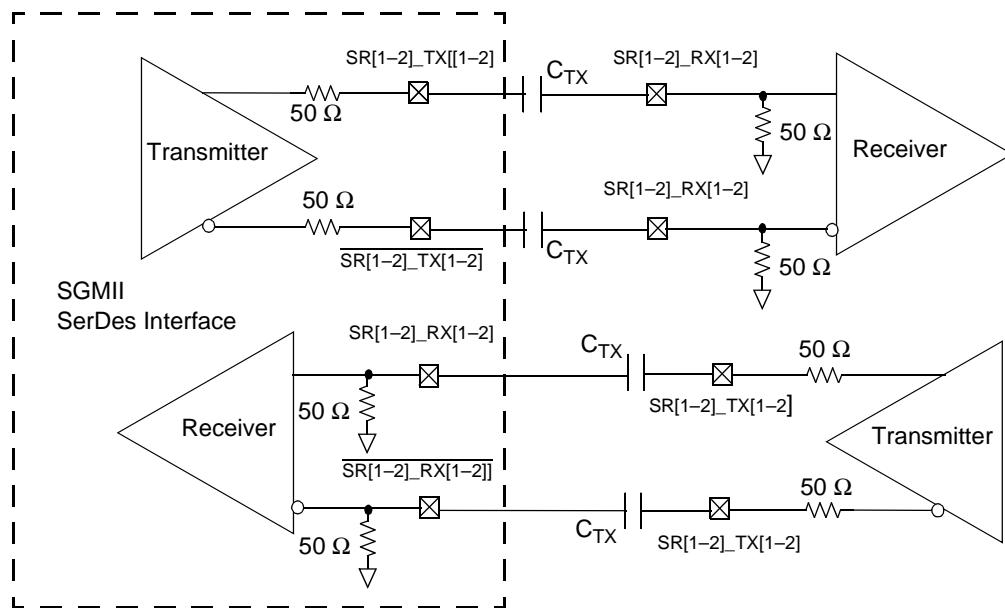


Figure 39. 4-Wire AC-Coupled SGMII Serial Link Connection Example

3.5 Connectivity Guidelines

Note: Although the package actually uses a ball grid array, the more conventional term pin is used to denote signal connections in this discussion.

First, select the pin multiplexing mode to allocate the required I/O signals. Then use the guidelines presented in the following subsections for board design and connections. The following conventions are used in describing the connectivity requirements:

1. GND indicates using a $10\text{ k}\Omega$ pull-down resistor (recommended) or a direct connection to the ground plane. Direct connections to the ground plane may yield DC current up to 50 mA through the I/O supply that adds to overall power consumption.
2. V_{DD} indicates using a $10\text{ k}\Omega$ pull-up resistor (recommended) or a direct connection to the appropriate power supply. Direct connections to the supply may yield DC current up to 50 mA through the I/O supply that adds to overall power consumption.
3. Mandatory use of a pull-up or pull-down resistor is clearly indicated as “pull-up/pull-down.” For buses, each pin on the bus should have its own resistor.
4. NC indicates “not connected” and means do not connect anything to the pin.
5. The phrase “in use” indicates a typical pin connection for the required function.

Note: Please see recommendations #1 and #2 as mandatory pull-down or pull-up connection for unused pins in case of subset interface connection.

3.5.1 DDR Memory Related Pins

This section discusses the various scenarios that can be used with either of the MSC8252 DDR ports.

Note: The signal names in [Table 40](#), [Table 41](#) and [Table 42](#) are generic names for a DDR SDRAM interface. For actual pin names refer to [Table 1](#).

3.5.1.1 DDR Interface Is Not Used

Table 40. Connectivity of DDR Related Pins When the DDR Interface Is Not Used

| Signal Name | Pin Connection |
|--------------------------|----------------|
| MDQ[0–63] | NC |
| MDQS[7–0] | NC |
| MDQS[7–0] | NC |
| MA[15–0] | NC |
| MCK[0–2] | NC |
| MCK[0–2] | NC |
| MCS[1–0] | NC |
| MDM[7–0] | NC |
| MBA[2–0] | NC |
| MCAS | NC |
| MCKE[1–0] | NC |
| MODT[1–0] | NC |
| MMDIC[1–0] | NC |
| MRAS | NC |
| MWE | NC |
| MECC[7–0] | NC |
| MDM8 | NC |
| MDQS8 | NC |
| MDQS8 | NC |
| MAPAR_OUT | NC |
| MAPAR_IN | NC |
| MVREF ³ | NC |
| GVDD1/GVDD2 ³ | NC |

Notes:

1. For the signals listed in this table, the initial M stands for M1 or M2 depending on which DDR controller is not used.
2. If the DDR controller is not used, disable the internal DDR clock by setting the appropriate bit in the System Clock Control Register (SCCR) and put all DDR I/O in sleep mode by setting DRx_GCR[DDRx_DOZE] (for DDR controller x). See the *Clocks and General Configuration Registers* chapters in the [MSC8252 Reference Manual](#) for details.
3. For MSC8252 Revision 1 silicon, these pins were connected to GND. For newer revisions of the MSC8252, connecting these pins to GND increases device power consumption.

3.5.1.2 DDR Interface Is Used With 32-Bit DDR Memory Only

Table 41 lists unused pin connection when using 32-bit DDR memory. The 32 most significant data lines are not used.

Table 41. Connectivity of DDR Related Pins When Using 32-bit DDR Memory Only

| Signal Name | Pin Connection |
|--|----------------|
| MDQ[31–0] | in use |
| MDQ[63–32] | NC |
| MDQS[3–0] | in use |
| MDQS[7–4] | NC |
| MDQS[3–0] | in use |
| MDQS[7–4] | NC |
| MA[15–0] | in use |
| MCK[2–0] | in use |
| MCK[2–0] | in use |
| MCS[1–0] | in use |
| MDM[3–0] | in use |
| MDM[7–4] | NC |
| MBA[2–0] | in use |
| MCAS | in use |
| MCKE[1–0] | in use |
| MODT[1–0] | in use |
| MMDIC[1–0] | in use |
| MRAS | in use |
| MWE | in use |
| MVREF | in use |
| GVDD1/GVDD2 | in use |
| Notes: | |
| 1. For the signals listed in this table, the initial M stands for M1 or M2 depending on which DDR controller is not used. | |
| 2. For MSC8252 Revision 1 silicon, these pins were connected to GND (or VDD). For newer revisions of the MSC8252, connecting these pins to GND increases device power consumption. | |

3.5.1.3 ECC Unused Pin Connections

When the error code correction mechanism is not used in any 32- or 64-bit DDR configuration, refer to Table 42 to determine the correct pin connections.

Table 42. Connectivity of Unused ECC Mechanism Pins

| Signal Name | Pin connection |
|--|----------------|
| MECC[7–0] | NC |
| MDM8 | NC |
| MDQS8 | NC |
| MDQS8 | NC |
| Notes: | |
| 1. For the signals listed in this table, the initial M stands for M1 or M2 depending on which DDR controller is not used. | |
| 2. For MSC8252 Revision 1 silicon, these pins were connected to GND (or VDD). For newer revisions of the MSC8252, connecting these pins to GND increases device power consumption. | |

3.5.1.4 DDR2 Unused MAPAR Pin Connections

When the MAPAR signals are not used, refer to [Table 43](#) to determine the correct pin connections.

Table 43. Connectivity of MAPAR Pins for DDR2

| Signal Name | Pin connection |
|-------------|----------------|
| MAPAR_OUT | NC |
| MAPAR_IN | NC |

Notes:

1. For the signals listed in this table, the initial M stands for M1 or M2 depending on which DDR controller is used for DDR2.
2. For MSC8252 Revision 1 silicon, these pins were connected to GND. For newer revisions of the MSC8252, connecting these pins to GND increases device power consumption.

3.5.2 HSSI-Related Pins

3.5.2.1 HSSI Port Is Not Used

The signal names in [Table 44](#) and [Table 45](#) are generic names for a RapidIO interface. For actual pin names refer to [Table 1](#).

Table 44. Connectivity of Serial RapidIO Interface Related Pins When the RapidIO Interface Is Not Used

| Signal Name | Pin Connection |
|------------------|----------------|
| SR_IMP_CAL_RX | NC |
| SR_IMP_CAL_TX | NC |
| SR[1-2]_REF_CLK | SXCVSS |
| SR[1-2]_REF_CLK | SXCVSS |
| SR[1-2]_RXD[3-0] | SXCVSS |
| SR[1-2]_RXD[3-0] | SXCVSS |
| SR[1-2]_TXD[3-0] | NC |
| SR[1-2]_TXD[3-0] | NC |
| SR[1-2]_PLL_AVDD | In use |
| SR[1-2]_PLL_AGND | In use |
| SXPVSS | In use |
| SXCVSS | In use |
| SXPVDD | In use |
| SXCVDD | In use |

Note: All lanes in the HSSI SerDes should be powered down. Refer to the *MSC8252 Reference Manual* for details.

3.5.2.2 HSSI Specific Lane Is Not Used

Table 45. Connectivity of HSSI Related Pins When Specific Lane Is Not Used

| Signal Name | Pin Connection |
|-----------------|----------------|
| SR_IMP_CAL_RX | In use |
| SR_IMP_CAL_TX | In use |
| SR[1-2]_REF_CLK | In use |
| SR[1-2]_REF_CLK | In use |

Table 45. Connectivity of HSSI Related Pins When Specific Lane Is Not Used (continued)

| Signal Name | Pin Connection |
|--|----------------|
| SR[1-2]_RXD n | SXCVSS |
| SR[1-2]_RXD n | SXCVSS |
| SR[1-2]_TXD n | NC |
| SR[1-2]_TXD n | NC |
| SR[1-2]_PLL_AVDD | in use |
| SR[1-2]_PLL_AGND | in use |
| SXPVSS | in use |
| SXCVSS | in use |
| SXPVDD | in use |
| SXCVD n | in use |
| Note: The n indicates the lane number {0,1,2,3} for all unused lanes. | |

3.5.3 RGMII Ethernet Related Pins

Note: [Table 46](#) and [Table 47](#) assume that the alternate function of the specified pin is not used. If the alternate function is used, connect the pin as required to support that function.

Table 46. Connectivity of RGMII Related Pins When the RGMII Interface Is Not Used

| Signal Name | Pin Connection |
|---|----------------|
| GE1_RX_CTL | GND |
| GE2_TX_CTL | NC |
| Note: Assuming GE1 and GE2 are disabled in the reset configuration word. | |

GE_MDC and GE_MDIO pins should be connected as required by the specified protocol. If neither GE1 nor GE2 is used, [Table 47](#) lists the recommended management pin connections.

Table 47. Connectivity of GE Management Pins When GE1 and GE2 Are Not Used

| Signal Name | Pin Connection |
|-------------|----------------|
| GE_MDC | NC |
| GE_MDIO | NC |

3.5.4 TDM Interface Related Pins

[Table 48](#) lists the board connections of the TDM pins when an entire specific TDM is not used. For multiplexing options that select a subset of a TDM interface, use the connections described in [Table 48](#) for those signals that are not selected. [Table 48](#) assumes that the alternate function of the specified pin is not used. If the alternate function is used, connect that pin as required to support the selected function.

Table 48. Connectivity of TDM Related Pins When TDM Interface Is Not Used

| Signal Name | Pin Connection |
|--------------|----------------|
| TDM n RCLK | GND |
| TDM n RDAT | GND |
| TDM n RSYN | GND |

Table 48. Connectivity of TDM Related Pins When TDM Interface Is Not Used

| Signal Name | Pin Connection |
|-------------------|--|
| TDM n TCLK | GND |
| TDM n TDAT | GND |
| TDM n TSYN | GND |
| V _{DDIO} | 2.5 V |
| Notes: | <ol style="list-style-type: none"> 1. $n = \{0, 1, 2, 3\}$ 2. In case of subset of TDM interface usage please make sure to disable unused TDM modules. See <i>TDM</i> chapter in the <i>MSC8252 Reference Manual</i> for details. |

3.5.5 Miscellaneous Pins

Table 49 lists the board connections for the pins not required by the system design. Table 49 assumes that the alternate function of the specified pin is not used. If the alternate function is used, connect that pin as required to support the selected function.

Table 49. Connectivity of Individual Pins When They Are Not Required

| Signal Name | Pin Connection |
|-------------------|---|
| CLKOUT | NC |
| EE0 | GND |
| EE1 | NC |
| GPIO[31–0] | NC |
| SCL | See the GPIO connectivity guidelines in this table. |
| SDA | See the GPIO connectivity guidelines in this table. |
| INT_OUT | NC |
| IRQ[15–0] | See the GPIO connectivity guidelines in this table. |
| NMI | V _{DDIO} |
| NMI_OUT | NC |
| RC[21–0] | GND |
| STOP_BS | GND |
| TCK | GND |
| TDI | GND |
| TDO | NC |
| TMR[4–0] | See the GPIO connectivity guidelines in this table. |
| TMS | GND |
| TRST | See Section 3.1 for guidelines. |
| URXD | See the GPIO connectivity guidelines in this table. |
| UTXD | See the GPIO connectivity guidelines in this table. |
| DDN[1–0] | See the GPIO connectivity guidelines in this table. |
| DRQ[1–0] | See the GPIO connectivity guidelines in this table. |
| RCW_LSEL_0 | GND |
| RCW_LSEL_1 | GND |
| RCW_LSEL_2 | GND |
| RCW_LSEL_3 | GND |
| V _{DDIO} | 2.5 V |

Note: For details on configuration, see the *MSC8252 Reference Manual*. For additional information, refer to the *MSC815x* and *MSC825x DSP Family Design Checklist*.

3.6 Guide to Selecting Connections for Remote Power Supply Sensing

To assure consistency of input power levels, some applications use a practice of connecting the remote sense signal input of an on-board power supply to one of power supply pins of the IC device. The advantage of using this connection is the ability to compensate for the slow components of the IR drop caused by resistive supply current path from on-board power supply to the pins layer on the package. However, because of specific device requirements, not every ball connection can be selected as the remote sense pin. Some of these pins must be connected to the appropriate power supply or ground to ensure correct device functionality. Some connections supply critical power to a specific high usage area of the IC die; using such a connection as a non-supply pin could impact necessary supply current during high current events. The following balls can be used as the board supply remote sense output without degrading the power and ground supply quality:

- *VDD*: W10, T19
- *VSS*: J18, Y10
- *M3VDD*: None

Do not use any other connections for remote sensing. Use of any other connections for this purpose can result in application and device failure.

4 Ordering Information

Consult a Freescale Semiconductor sales office or authorized distributor to determine product availability and place an order.

| Part | Package Type | Spheres | Core Voltage | Operating Temperature | Core Frequency (MHz) | Order Number |
|---------|---|-----------|--------------|-----------------------|----------------------|-----------------|
| MSC8252 | Flip Chip Plastic Ball Grid Array (FC-PBGA) | Lead-free | 1.0 V | 0° C to 105°C | 1000 | MSC8252SVT1000B |
| | | | | –40° C to 105°C | 1000 | MSC8252TBT1000B |



5 Package Information

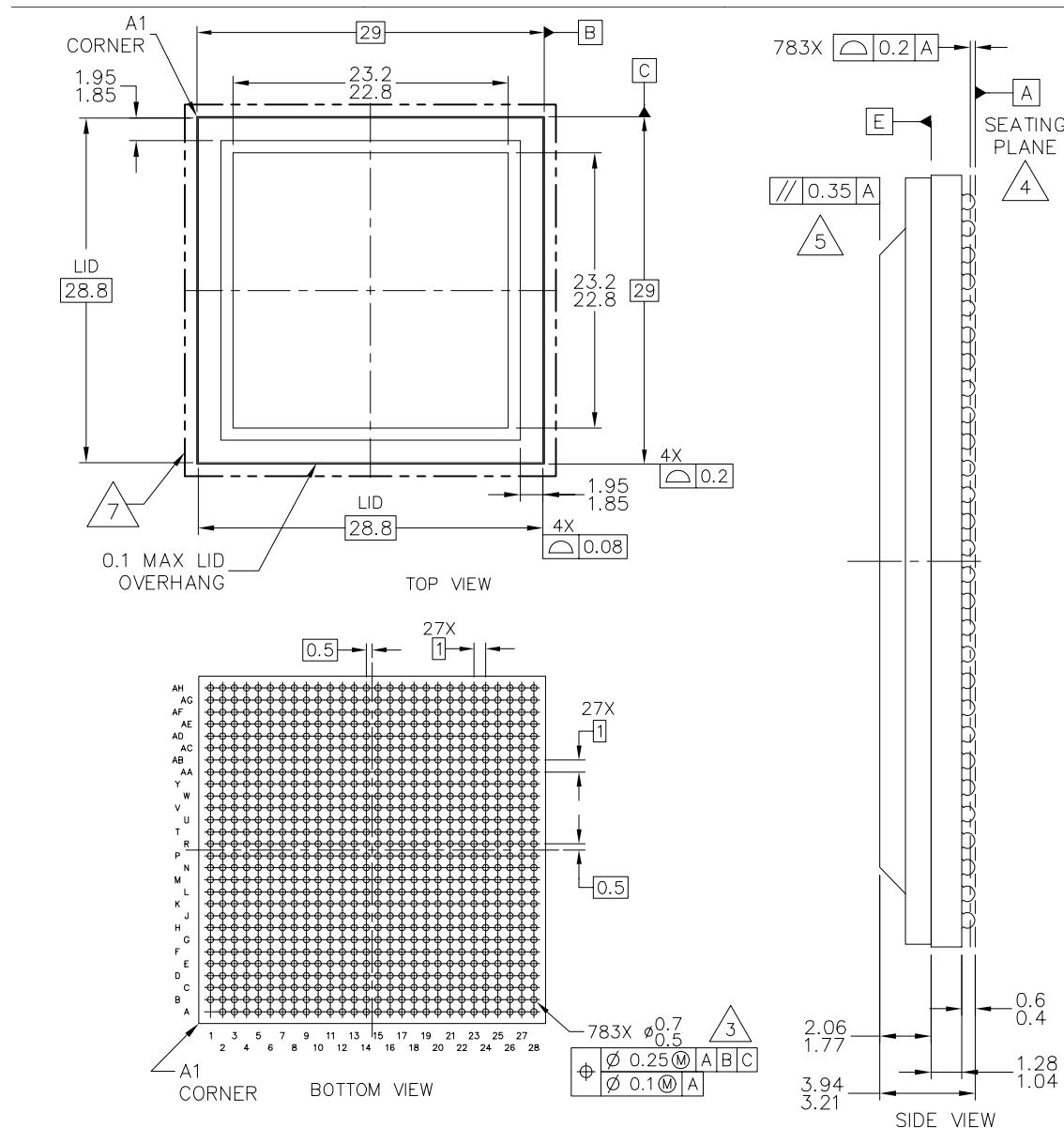


Figure 40. MSC8252 Mechanical Information, 783-ball FC-PBGA Package

6 Product Documentation

Following is a general list of supporting documentation:

- *MSC8252 Technical Data Sheet* (MSC8252). Details the signals, AC/DC characteristics, clock signal characteristics, package and pinout, and electrical design considerations of the MSC8252 device.
- *MSC8252 Reference Manual* (MSC8252RM). Includes functional descriptions of the extended cores and all the internal subsystems including configuration and programming information.
- *Application Notes*. Cover various programming topics related to the StarCore DSP core and the MSC8252 device.
- *QUICC Engine Block Reference Manual with Protocol Interworking* (QEIWRM). Provides detailed information regarding the QUICC Engine technology including functional description, registers, and programming information.
- *SC3850 DSP Core Reference Manual*. Covers the SC3850 core architecture, control registers, clock registers, program control, and instruction set.
- *MSC8156SC3850 DSP Core Subsystem Reference Manual*. Covers core subsystem architecture, functionality, and registers.

7 Revision History

[Table 50](#) provides a revision history for this data sheet.

Table 50. Document Revision History

| Rev. | Date | Description |
|------|-----------|---|
| 0 | Apr. 2010 | <ul style="list-style-type: none"> Initial public release. |
| 1 | May 2010 | <ul style="list-style-type: none"> Changed connection for pins K17, L14, L16, M15, M17, and N14 from VDD to VSS in Table 1. Updated Section 3.1.2, Power-On Ramp Time. |
| 2 | Jun 2010 | <ul style="list-style-type: none"> Changed the number of cores in the first bullet on the first page from four to two. The correction to the L16 connection was not made in Rev. 1. Fixed the entry to change from VDD to VSS in Table 1. |
| 3 | Dec 2010 | <ul style="list-style-type: none"> Updated Table 16. Updated Section 3.1.2, Power-On Ramp Time. Updated Section 4, Ordering Information. |
| 4 | Mar 2011 | <ul style="list-style-type: none"> Updated Table 8. Updated Table 15. Updated Table 17. Updated Table 33. Updated Table 35. Updated Table 39. |
| 5 | May 2011 | <ul style="list-style-type: none"> Updated Table 1. Changed the pin types for the following: <ul style="list-style-type: none"> – F25 from ground to power. – F26 from power to ground. – T6 from power to O. |
| 6 | Oct 2011 | <ul style="list-style-type: none"> Updated Table 34 and Table 35 to reflect 1 Gbps and 100 Mbps data rate instead of 1 GHz and 100 MHz. |
| 7 | Dec 2011 | <ul style="list-style-type: none"> Added note 4 to Table 39. |

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