

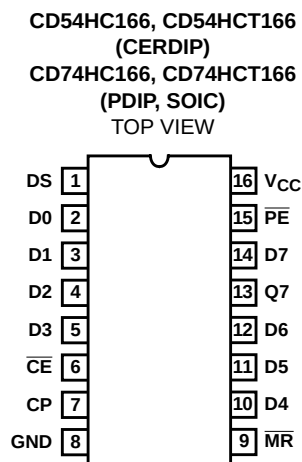
# CD54HC166, CD74HC166, CD54HCT166, CD74HCT166

## High-Speed CMOS Logic 8-Bit Parallel-In/Serial-Out Shift Register

### Features

- Buffered Inputs
- Fanout (Over Temperature Range)
  - Standard Outputs . . . . . 10 LSTTL Loads
  - Bus Driver Outputs . . . . . 15 LSTTL Loads
- Wide Operating Temperature Range . . . -55°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
  - 2V to 6V Operation
  - High Noise Immunity:  $N_{IL} = 30\%$ ,  $N_{IH} = 30\%$  of  $V_{CC}$  at  $V_{CC} = 5V$
- HCT Types
  - 4.5V to 5.5V Operation
  - Direct LSTTL Input Logic Compatibility,  $V_{IL} = 0.8V$  (Max),  $V_{IH} = 2V$  (Min)

### Pinout



### Description

The 'HC166 and 'HCT166 8-bit shift register is fabricated with silicon gate CMOS technology. It possesses the low power consumption of standard CMOS integrated circuits, and can operate at speeds comparable to the equivalent low power Schottky device.

The 'HCT166 is functionally and pin compatible with the standard 'LS166.

The 166 is an 8-bit shift register that has fully synchronous serial or parallel data entry selected by an active LOW Parallel Enable (PE) input. When the PE is LOW one setup time before the LOW-to-HIGH clock transition, parallel data is entered into the register. When  $\overline{PE}$  is HIGH, data is entered into the internal bit position Q0 from Serial Data Input (DS), and the remaining bits are shifted one place to the right ( $Q0 \rightarrow Q1 \rightarrow Q2$ , etc.) with each positive-going clock transition. For expansion of the register in parallel to serial converters, the Q7 output is connected to the DS input of the succeeding stage.

The clock input is a gated OR structure which allows one input to be used as an active LOW Clock Enable ( $\overline{CE}$ ) input. The pin assignment for the CP and  $\overline{CE}$  inputs is arbitrary and can be reversed for layout convenience. The LOW-to-HIGH transition of CE input should only take place while the CP is HIGH for predictable operation.

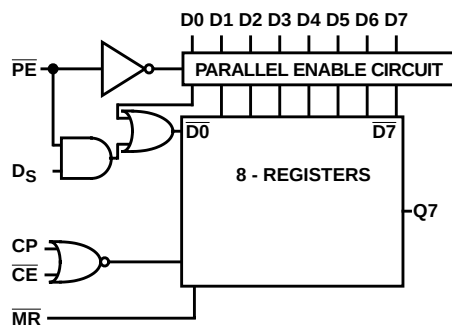
A LOW on the Master Reset ( $\overline{MR}$ ) input overrides all other inputs and clears the register asynchronously, forcing all bit positions to a LOW state.

### Ordering Information

| PART NUMBER   | TEMP. RANGE (°C) | PACKAGE      |
|---------------|------------------|--------------|
| CD54HC166F3A  | -55 to 125       | 16 Ld CERDIP |
| CD54HCT166F3A | -55 to 125       | 16 Ld CERDIP |
| CD74HC166E    | -55 to 125       | 16 Ld PDIP   |
| CD74HC166M    | -55 to 125       | 16 Ld SOIC   |
| CD74HC166MT   | -55 to 125       | 16 Ld SOIC   |
| CD74HC166M96  | -55 to 125       | 16 Ld SOIC   |
| CD74HCT166E   | -55 to 125       | 16 Ld PDIP   |
| CD74HCT166M   | -55 to 125       | 16 Ld SOIC   |
| CD74HCT166MT  | -55 to 125       | 16 Ld SOIC   |
| CD74HCT166M96 | -55 to 125       | 16 Ld SOIC   |

NOTE: When ordering, use the entire part number. The suffix 96 denotes tape and reel. The suffix T denotes a small-quantity reel of 250.

## Functional Diagram



TRUTH TABLE

| INPUTS       |                 |              |       |        |                | INTERNAL Q STATES |     | OUTPUT Q7 |
|--------------|-----------------|--------------|-------|--------|----------------|-------------------|-----|-----------|
| MASTER RESET | PARALLEL ENABLE | CLOCK ENABLE | CLOCK | SERIAL | PARALLEL D0 D7 | Q0                | Q1  |           |
| L            | X               | X            | X     | X      | X              | L                 | L   | L         |
| H            | X               | L            | L     | X      | X              | Q00               | Q10 | Q0        |
| H            | L               | L            | ↑     | X      | a...h          | a                 | b   | h         |
| H            | H               | L            | ↑     | H      | X              | H                 | Q0n | Q6n       |
| H            | H               | L            | ↑     | L      | X              | L                 | Q0n | Q6n       |
| H            | X               | H            | ↑     | X      | X              | Q00               | Q10 | Q70       |

H= High Voltage Level

L= Low Voltage Level

X= Don't Care

↑= Transition from Low to High Level

a...h = The level of steady-state input at inputs D0 thru D7, respectively.

Q00, Q10, Q70 = The level of Q0, Q1, or Q7, respectively, before the indicated steady-state input conditions were established.

Q0n, Q6n = The level of Q0 or Q6, respectively, before the most recent ↑ transition of the clock.

# CD54HC166, CD74HC166, CD54HCT166, CD74HCT166

## Absolute Maximum Ratings

DC Supply Voltage,  $V_{CC}$  ..... -0.5V to 7V  
 DC Input Diode Current,  $I_{IK}$   
 For  $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$  .....  $\pm 20mA$   
 DC Output Diode Current,  $I_{OK}$   
 For  $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$  .....  $\pm 20mA$   
 DC Drain Current, per Output,  $I_O$   
 For  $-0.5V < V_O < V_{CC} + 0.5V$  .....  $\pm 25mA$   
 DC Output Source or Sink Current per Output Pin,  $I_O$   
 For  $V_O > -0.5V$  or  $V_O < V_{CC} + 0.5V$  .....  $\pm 25mA$   
 DC  $V_{CC}$  or Ground Current,  $I_{CC}$  or  $I_{GND}$  .....  $\pm 50mA$

## Thermal Information

Thermal Resistance (Typical, Note 1)  $\theta_{JA}$  ( $^{\circ}C/W$ )  
 E (PDIP) Package ..... 67  
 M (SOIC) Package ..... 73  
 Maximum Junction Temperature .....  $150^{\circ}C$   
 Maximum Storage Temperature Range .....  $-65^{\circ}C$  to  $150^{\circ}C$   
 Maximum Lead Temperature (Soldering 10s) .....  $300^{\circ}C$   
 (SOIC - Lead Tips Only)

## Operating Conditions

Temperature Range ( $T_A$ ) .....  $-55^{\circ}C$  to  $125^{\circ}C$   
 Supply Voltage Range,  $V_{CC}$   
 HC Types ..... 2V to 6V  
 HCT Types ..... 4.5V to 5.5V  
 DC Input or Output Voltage,  $V_I$ ,  $V_O$  ..... 0V to  $V_{CC}$   
 Input Rise and Fall Time  
 2V ..... 1000ns (Max)  
 4.5V ..... 500ns (Max)  
 6V ..... 400ns (Max)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

### NOTE:

1. The package thermal impedance is calculated in accordance with JESD 51-7.

## DC Electrical Specifications

| PARAMETER                               | SYMBOL          | TEST CONDITIONS                       |                     | V <sub>CC</sub> (V) | 25°C |     |      | -40°C TO 85°C |      | -55°C TO 125°C |      | UNITS |
|-----------------------------------------|-----------------|---------------------------------------|---------------------|---------------------|------|-----|------|---------------|------|----------------|------|-------|
|                                         |                 | V <sub>I</sub> (V)                    | I <sub>O</sub> (mA) |                     | MIN  | TYP | MAX  | MIN           | MAX  | MIN            | MAX  |       |
| HC TYPES                                |                 |                                       |                     |                     |      |     |      |               |      |                |      |       |
| High Level Input Voltage                | V <sub>IH</sub> | -                                     | -                   | 2                   | 1.5  | -   | -    | 1.5           | -    | 1.5            | -    | V     |
|                                         |                 |                                       |                     | 4.5                 | 3.15 | -   | -    | 3.15          | -    | 3.15           | -    | V     |
|                                         |                 |                                       |                     | 6                   | 4.2  | -   | -    | 4.2           | -    | 4.2            | -    | V     |
| Low Level Input Voltage                 | V <sub>IL</sub> | -                                     | -                   | 2                   | -    | -   | 0.5  | -             | 0.5  | -              | 0.5  | V     |
|                                         |                 |                                       |                     | 4.5                 | -    | -   | 1.35 | -             | 1.35 | -              | 1.35 | V     |
|                                         |                 |                                       |                     | 6                   | -    | -   | 1.8  | -             | 1.8  | -              | 1.8  | V     |
| High Level Output Voltage<br>CMOS Loads | V <sub>OH</sub> | V <sub>IH</sub> or<br>V <sub>IL</sub> | -0.02               | 2                   | 1.9  | -   | -    | 1.9           | -    | 1.9            | -    | V     |
|                                         |                 |                                       | -0.02               | 4.5                 | 4.4  | -   | -    | 4.4           | -    | 4.4            | -    | V     |
|                                         |                 |                                       | -0.02               | 6                   | 5.9  | -   | -    | 5.9           | -    | 5.9            | -    | V     |
| High Level Output Voltage<br>TTL Loads  | V <sub>OH</sub> | V <sub>IH</sub> or<br>V <sub>IL</sub> | -4                  | 4.5                 | 3.98 | -   | -    | 3.84          | -    | 3.7            | -    | V     |
| -5.2                                    |                 |                                       | 6                   | 5.48                | -    | -   | 5.34 | -             | 5.2  | -              | V    |       |
| Low Level Output Voltage<br>CMOS Loads  | V <sub>OL</sub> | V <sub>IH</sub> or<br>V <sub>IL</sub> | 0.02                | 2                   | -    | -   | 0.1  | -             | 0.1  | -              | 0.1  | V     |
|                                         |                 |                                       | 0.02                | 4.5                 | -    | -   | 0.1  | -             | 0.1  | -              | 0.1  | V     |
|                                         |                 |                                       | 0.02                | 6                   | -    | -   | 0.1  | -             | 0.1  | -              | 0.1  | V     |
| Low Level Output Voltage<br>TTL Loads   | V <sub>OL</sub> | V <sub>IH</sub> or<br>V <sub>IL</sub> | 4                   | 4.5                 | -    | -   | 0.26 | -             | 0.33 | -              | 0.4  | V     |
|                                         |                 |                                       | 5.2                 | 6                   | -    | -   | 0.26 | -             | 0.33 | -              | 0.4  | V     |
| Input Leakage Current                   | I <sub>I</sub>  | V <sub>CC</sub> or<br>GND             | -                   | 6                   | -    | -   | ±0.1 | -             | ±1   | -              | ±1   | μA    |

# **CD54HC166, CD74HC166, CD54HCT166, CD74HCT166**

## **DC Electrical Specifications (Continued)**

| PARAMETER                                                      | SYMBOL                   | TEST CONDITIONS      |            | $V_{CC}$ (V) | 25°C |     |           | -40°C TO 85°C |         | -55°C TO 125°C |         | UNITS   |
|----------------------------------------------------------------|--------------------------|----------------------|------------|--------------|------|-----|-----------|---------------|---------|----------------|---------|---------|
|                                                                |                          | $V_I$ (V)            | $I_O$ (mA) |              | MIN  | TYP | MAX       | MIN           | MAX     | MIN            | MAX     |         |
| Quiescent Device Current                                       | $I_{CC}$                 | $V_{CC}$ or GND      | 0          | 6            | -    | -   | 8         | -             | 80      | -              | 160     | $\mu A$ |
| <b>HCT TYPES</b>                                               |                          |                      |            |              |      |     |           |               |         |                |         |         |
| High Level Input Voltage                                       | $V_{IH}$                 | -                    | -          | 4.5 to 5.5   | 2    | -   | -         | 2             | -       | 2              | -       | V       |
| Low Level Input Voltage                                        | $V_{IL}$                 | -                    | -          | 4.5 to 5.5   | -    | -   | 0.8       | -             | 0.8     | -              | 0.8     | V       |
| High Level Output Voltage<br>CMOS Loads                        | $V_{OH}$                 | $V_{IH}$ or $V_{IL}$ | -0.02      | 4.5          | 4.4  | -   | -         | 4.4           | -       | 4.4            | -       | V       |
| High Level Output Voltage<br>TTL Loads                         |                          |                      | -4         | 4.5          | 3.98 | -   | -         | 3.84          | -       | 3.7            | -       | V       |
| Low Level Output Voltage<br>CMOS Loads                         | $V_{OL}$                 | $V_{IH}$ or $V_{IL}$ | 0.02       | 4.5          | -    | -   | 0.1       | -             | 0.1     | -              | 0.1     | V       |
| Low Level Output Voltage<br>TTL Loads                          |                          |                      | 4          | 4.5          | -    | -   | 0.26      | -             | 0.33    | -              | 0.4     | V       |
| Input Leakage Current                                          | $I_I$                    | $V_{CC}$ to GND      | 0          | 5.5          | -    | -   | $\pm 0.1$ | -             | $\pm 1$ | -              | $\pm 1$ | $\mu A$ |
| Quiescent Device Current                                       | $I_{CC}$                 | $V_{CC}$ or GND      | 0          | 5.5          | -    | -   | 8         | -             | 80      | -              | 160     | $\mu A$ |
| Additional Quiescent Device Current Per Input Pin: 1 Unit Load | $\Delta I_{CC}$ (Note 2) | $V_{CC}$ -2.1        | -          | 4.5 to 5.5   | -    | 100 | 360       | -             | 450     | -              | 490     | $\mu A$ |

NOTE:

- For dual-supply systems theoretical worst case ( $V_I = 2.4V$ ,  $V_{CC} = 5.5V$ ) specification is 1.8mA.

## **HCT Input Loading Table**

| INPUT               | UNIT LOADS |
|---------------------|------------|
| DS, D0-D7           | 0.2        |
| PE                  | 0.35       |
| CP, $\overline{CE}$ | 0.5        |
| $\overline{MR}$     | 0.2        |

NOTE: Unit Load is  $\Delta I_{CC}$  limit specified in DC Electrical Specifications table, e.g., 360 $\mu A$  max at 25°C.

## **Prerequisite For Switching Specifications**

| PARAMETER                     | SYMBOL           | V <sub>CC</sub> (V) | 25°C |     | -40°C TO 85°C |     | -55°C TO 125°C |     | UNITS |
|-------------------------------|------------------|---------------------|------|-----|---------------|-----|----------------|-----|-------|
|                               |                  |                     | MIN  | MAX | MIN           | MAX | MIN            | MAX |       |
| HC TYPES                      |                  |                     |      |     |               |     |                |     |       |
| Clock Frequency<br>(Figure 1) | f <sub>MAX</sub> | 2                   | 6    | -   | 5             | -   | 4              | -   | MHz   |
|                               |                  | 4.5                 | 30   | -   | 25            | -   | 20             | -   | MHz   |
|                               |                  | 6                   | 35   | -   | 29            | -   | 23             | -   | MHz   |

**CD54HC166, CD74HC166, CD54HCT166, CD74HCT166**

**Prerequisite For Switching Specifications (Continued)**

| PARAMETER                                                      | SYMBOL           | V <sub>CC</sub> (V) | 25°C |     | -40°C TO 85°C |     | -55°C TO 125°C |     | UNITS |
|----------------------------------------------------------------|------------------|---------------------|------|-----|---------------|-----|----------------|-----|-------|
|                                                                |                  |                     | MIN  | MAX | MIN           | MAX | MIN            | MAX |       |
| MR Pulse Width<br>(Figure 1)                                   | t <sub>w</sub>   | 2                   | 100  | -   | 125           | -   | 150            | -   | ns    |
|                                                                |                  | 4.5                 | 20   | -   | 25            | -   | 30             | -   | ns    |
|                                                                |                  | 6                   | 17   | -   | 21            | -   | 26             | -   | ns    |
| Clock Pulse Width<br>(Figure 1)                                | t <sub>w</sub>   | 2                   | 80   | -   | 100           | -   | 120            | -   | ns    |
|                                                                |                  | 4.5                 | 16   | -   | 20            | -   | 24             | -   | ns    |
|                                                                |                  | 6                   | 14   | -   | 17            | -   | 20             | -   | ns    |
| Set-up Time<br>Data and $\overline{CE}$ to Clock<br>(Figure 5) | t <sub>SU</sub>  | 2                   | 80   | -   | 100           | -   | 120            | -   | ns    |
|                                                                |                  | 4.5                 | 16   | -   | 20            | -   | 24             | -   | ns    |
|                                                                |                  | 6                   | 14   | -   | 17            | -   | 20             | -   | ns    |
| Hold Time<br>Data to Clock<br>(Figure 5)                       | t <sub>H</sub>   | 2                   | 1    | -   | 1             | -   | 1              | -   | ns    |
|                                                                |                  | 4.5                 | 1    | -   | 1             | -   | 1              | -   | ns    |
|                                                                |                  | 6                   | 1    | -   | 1             | -   | 1              | -   | ns    |
| Removal Time<br>MR to Clock<br>(Figure 5)                      | t <sub>REM</sub> | 2                   | 0    | -   | 0             | -   | 0              | -   | ns    |
|                                                                |                  | 4.5                 | 0    | -   | 0             | -   | 0              | -   | ns    |
|                                                                |                  | 6                   | 0    | -   | 0             | -   | 0              | -   | ns    |
| Set-up Time<br>PE to CP<br>(Figure 5)                          | t <sub>SU</sub>  | 2                   | 145  | -   | 180           | -   | 220            | -   | ns    |
|                                                                |                  | 4.5                 | 29   | -   | 36            | -   | 44             | -   | ns    |
|                                                                |                  | 6                   | 25   | -   | 31            | -   | 38             | -   | ns    |
| Hold Time<br>PE to CP or $\overline{CE}$<br>(Figure 5)         | t <sub>H</sub>   | 2                   | 0    | -   | 0             | -   | 0              | -   | ns    |
|                                                                |                  | 4.5                 | 0    | -   | 0             | -   | 0              | -   | ns    |
|                                                                |                  | 6                   | 0    | -   | 0             | -   | 0              | -   | ns    |
| HCT TYPES                                                      |                  |                     |      |     |               |     |                |     |       |
| Clock Frequency (Figure 2)                                     | f <sub>MAX</sub> | 4.5                 | 25   | -   | 20            | -   | 16             | -   | MHz   |
| MR Pulse Width (Figure 2)                                      | t <sub>w</sub>   | 4.5                 | 35   | -   | 44            | -   | 53             | -   | ns    |
| Clock Pulse Width (Figure 2)                                   | t <sub>w</sub>   | 4.5                 | 20   | -   | 25            | -   | 30             | -   | ns    |
| Set-up Time Data and $\overline{CE}$ to Clock (Figure 6)       | t <sub>SU</sub>  | 4.5                 | 16   | -   | 20            | -   | 24             | -   | ns    |
| Hold Time Data to Clock (Figure 6)                             | t <sub>H</sub>   | 4.5                 | 0    | -   | 0             | -   | 0              | -   | ns    |
| Removal Time $\overline{MR}$ to Clock (Figure 6)               | t <sub>REM</sub> | 4.5                 | 0    | -   | 0             | -   | 0              | -   | ns    |
| Set-up Time $\overline{PE}$ to CP (Figure 6)                   | t <sub>SU</sub>  | 4.5                 | 30   | -   | 38            | -   | 45             | -   | ns    |
| Hold Time $\overline{PE}$ to CP or $\overline{CE}$ (Figure 6)  | t <sub>H</sub>   | 4.5                 | 0    | -   | 0             | -   | 0              | -   | ns    |

**Switching Specifications** Input  $t_r$ ,  $t_f$  = 6ns

| PARAMETER                                        | SYMBOL                              | TEST CONDITIONS       | V <sub>CC</sub> (V) | 25°C |     | -40°C TO 85°C | -55°C TO 125°C | UNITS |
|--------------------------------------------------|-------------------------------------|-----------------------|---------------------|------|-----|---------------|----------------|-------|
|                                                  |                                     |                       |                     | TYP  | MAX | MAX           | MAX            |       |
| HC TYPES                                         |                                     |                       |                     |      |     |               |                |       |
| Propagation Delay,<br>Clock to Output (Figure 3) | t <sub>PLH</sub> , t <sub>PHL</sub> | C <sub>L</sub> = 50pF | 2                   | -    | 160 | 200           | 240            | ns    |
|                                                  |                                     |                       | 4.5                 | -    | 32  | 40            | 48             | ns    |
|                                                  |                                     | C <sub>L</sub> = 15pF | 5                   | 13   | -   | -             | -              | ns    |
|                                                  |                                     | CL = 50pF             | 6                   | -    | 27  | 34            | 41             | ns    |

# CD54HC166, CD74HC166, CD54HCT166, CD74HCT166

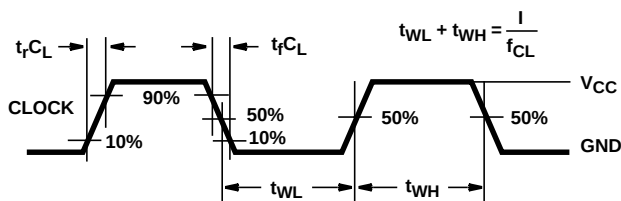
## Switching Specifications Input $t_r, t_f = 6\text{ns}$ (Continued)

| PARAMETER                                           | SYMBOL             | TEST CONDITIONS     | $V_{CC}$ (V) | 25°C |     | -40°C TO 85°C | -55°C TO 125°C | UNITS |
|-----------------------------------------------------|--------------------|---------------------|--------------|------|-----|---------------|----------------|-------|
|                                                     |                    |                     |              | TYP  | MAX | MAX           | MAX            |       |
| Output Transition Time<br>(Figure 3)                | $t_{TLH}, t_{THL}$ | $C_L = 50\text{pF}$ | 2            | -    | 75  | 95            | 110            | ns    |
|                                                     |                    |                     | 4.5          | -    | 15  | 19            | 22             | ns    |
|                                                     |                    |                     | 6            | -    | 13  | 16            | 19             | ns    |
| Propagation Delay<br>MR to Output<br>(Figure 3)     | $t_{PHL}$          | $C_L = 50\text{pF}$ | 2            | -    | 160 | 200           | 240            | ns    |
|                                                     |                    |                     | 4.5          | -    | 32  | 40            | 48             | ns    |
|                                                     |                    |                     | 6            | -    | 27  | 34            | 41             | ns    |
| Input Capacitance                                   | $C_I$              | -                   | -            | -    | 10  | 10            | 10             | pF    |
| Power Dissipation<br>Capacitance<br>(Notes 3, 4)    | $C_{PD}$           | -                   | 5            | 41   | -   | -             | -              | pF    |
| <b>HCT TYPES</b>                                    |                    |                     |              |      |     |               |                |       |
| Propagation Delay,<br>Clock to Output<br>(Figure 4) | $t_{PLH}, t_{PHL}$ | $C_L = 50\text{pF}$ | 4.5          | -    | 40  | 50            | 60             | ns    |
| Output Transition Time<br>(Figure 4)                | $t_{TLH}, t_{THL}$ | $C_L = 50\text{pF}$ | 4.5          | -    | 15  | 19            | 22             | ns    |
| Propagation Delay<br>MR to Output (Figure 4)        | $t_{PHL}$          | $C_L = 50\text{pF}$ | 4.5          | -    | 40  | 50            | 60             | ns    |
| Input Capacitance                                   | $C_I$              | -                   | -            | -    | 10  | 10            | 10             | pF    |

### NOTES:

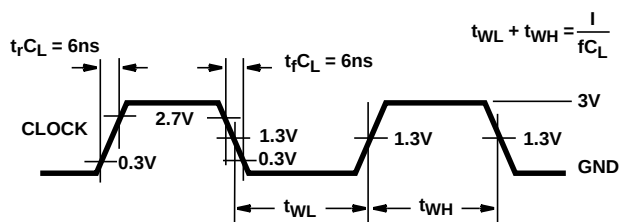
- $C_{PD}$  is used to determine the dynamic power consumption, per gate.
- $P_D = C_{PD} V_{CC}^2 f_i + \sum (C_L V_{CC}^2 + f_O)$  where  $f_i$  = Input Frequency,  $f_O$  = Output Frequency,  $C_L$  = Output Load Capacitance,  $V_{CC}$  = Supply Voltage.

## Test Circuits and Waveforms



NOTE: Outputs should be switching from 10%  $V_{CC}$  to 90%  $V_{CC}$  in accordance with device truth table. For  $f_{MAX}$ , input duty cycle = 50%.

**FIGURE 1. HC CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH**



NOTE: Outputs should be switching from 10%  $V_{CC}$  to 90%  $V_{CC}$  in accordance with device truth table. For  $f_{MAX}$ , input duty cycle = 50%.

**FIGURE 2. HCT CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH**

Test Circuits and Waveforms (Continued)

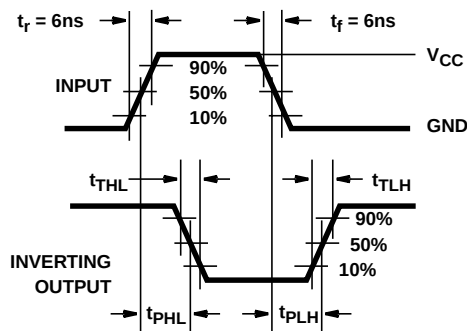


FIGURE 3. HC AND HCU TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

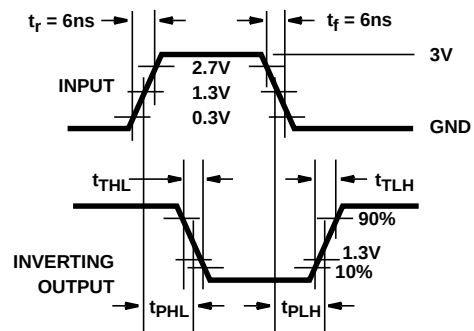


FIGURE 4. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

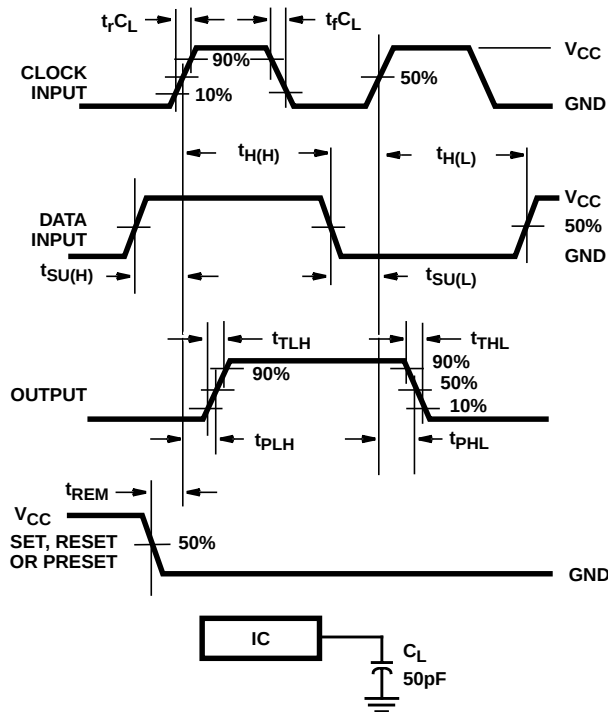


FIGURE 5. HC SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

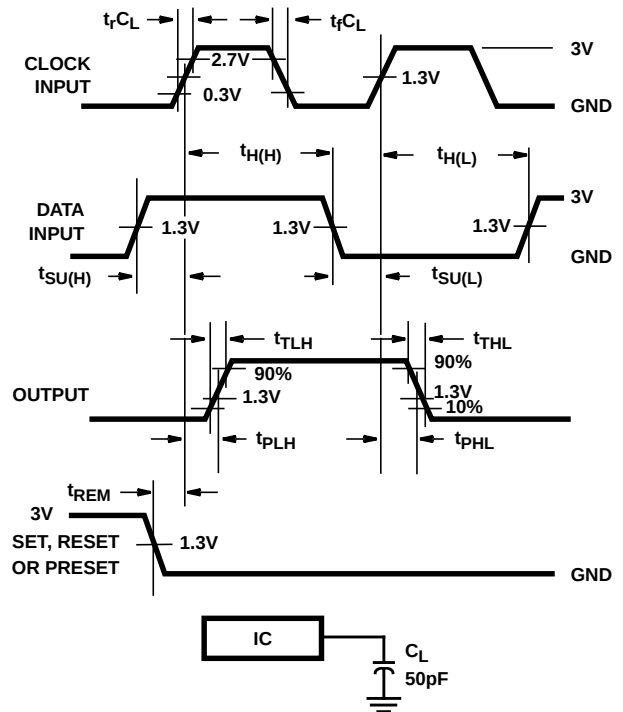


FIGURE 6. HCT SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)            | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| CD54HC166F3A     | ACTIVE        | CDIP         | J                  | 16   | 1              | TBD                        | A42                     | N / A for Pkg Type   | -55 to 125   | CD54HC166F3A            | <a href="#">Samples</a> |
| CD54HCT166F3A    | ACTIVE        | CDIP         | J                  | 16   | 1              | TBD                        | A42                     | N / A for Pkg Type   | -55 to 125   | CD54HCT166F3A           | <a href="#">Samples</a> |
| CD74HC166E       | ACTIVE        | PDIP         | N                  | 16   | 25             | Pb-Free<br>(RoHS)          | CU NIPDAU               | N / A for Pkg Type   | -55 to 125   | CD74HC166E              | <a href="#">Samples</a> |
| CD74HC166M       | ACTIVE        | SOIC         | D                  | 16   | 40             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -55 to 125   | HC166M                  | <a href="#">Samples</a> |
| CD74HC166M96     | ACTIVE        | SOIC         | D                  | 16   | 2500           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -55 to 125   | HC166M                  | <a href="#">Samples</a> |
| CD74HC166MG4     | ACTIVE        | SOIC         | D                  | 16   | 40             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -55 to 125   | HC166M                  | <a href="#">Samples</a> |
| CD74HC166MT      | ACTIVE        | SOIC         | D                  | 16   | 250            | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -55 to 125   | HC166M                  | <a href="#">Samples</a> |
| CD74HCT166E      | ACTIVE        | PDIP         | N                  | 16   | 25             | Pb-Free<br>(RoHS)          | CU NIPDAU               | N / A for Pkg Type   | -55 to 125   | CD74HCT166E             | <a href="#">Samples</a> |
| CD74HCT166EE4    | ACTIVE        | PDIP         | N                  | 16   | 25             | Pb-Free<br>(RoHS)          | CU NIPDAU               | N / A for Pkg Type   | -55 to 125   | CD74HCT166E             | <a href="#">Samples</a> |
| CD74HCT166M      | ACTIVE        | SOIC         | D                  | 16   | 40             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -55 to 125   | HCT166M                 | <a href="#">Samples</a> |
| CD74HCT166M96    | ACTIVE        | SOIC         | D                  | 16   | 2500           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -55 to 125   | HCT166M                 | <a href="#">Samples</a> |
| CD74HCT166M96G4  | ACTIVE        | SOIC         | D                  | 16   | 2500           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -55 to 125   | HCT166M                 | <a href="#">Samples</a> |
| CD74HCT166MG4    | ACTIVE        | SOIC         | D                  | 16   | 40             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -55 to 125   | HCT166M                 | <a href="#">Samples</a> |
| CD74HCT166MT     | ACTIVE        | SOIC         | D                  | 16   | 250            | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -55 to 125   | HCT166M                 | <a href="#">Samples</a> |
| CD74HCT166TM96Q1 | OBSOLETE      | SOIC         | D                  | 16   |                | TBD                        | Call TI                 | Call TI              | -40 to 125   |                         |                         |

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.



<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF CD54HC166, CD54HCT166, CD74HC166, CD74HCT166 :**

● Catalog: [CD74HC166](#), [CD74HCT166](#)

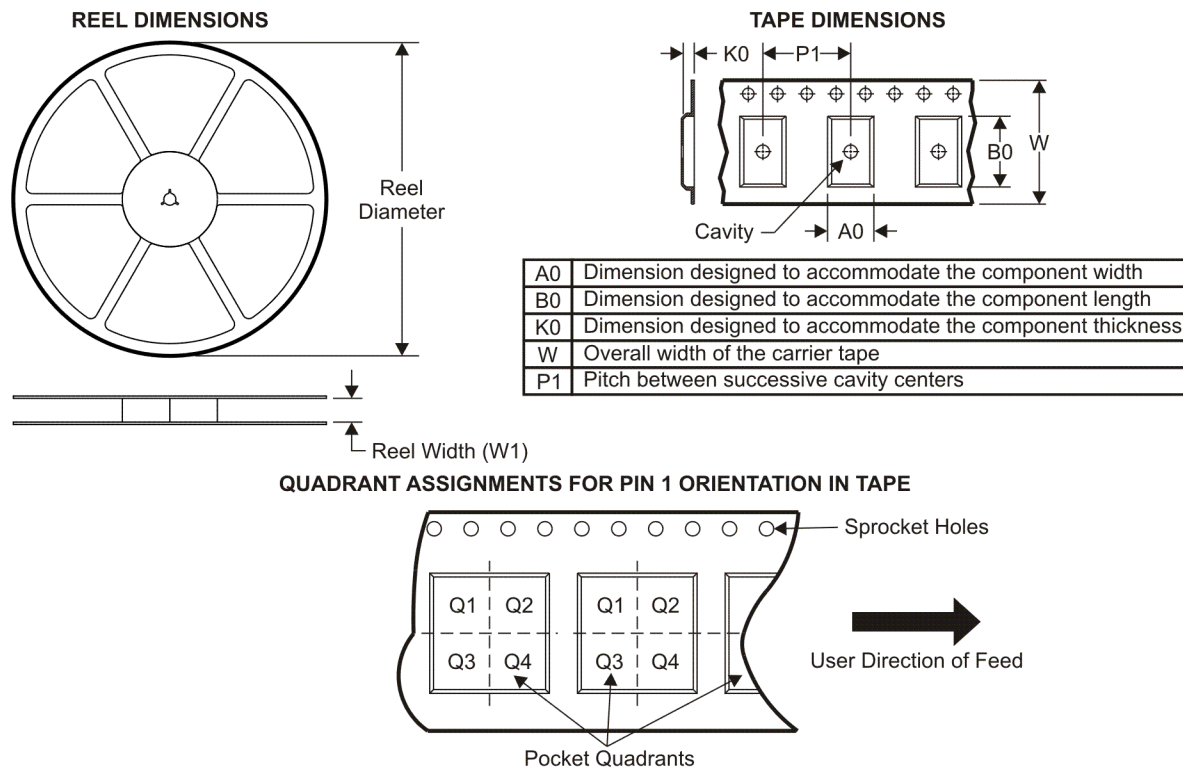
● Military: [CD54HC166](#), [CD54HCT166](#)

NOTE: Qualified Version Definitions:

● Catalog - TI's standard catalog product

- 
- Military - QML certified for Military and Defense Applications

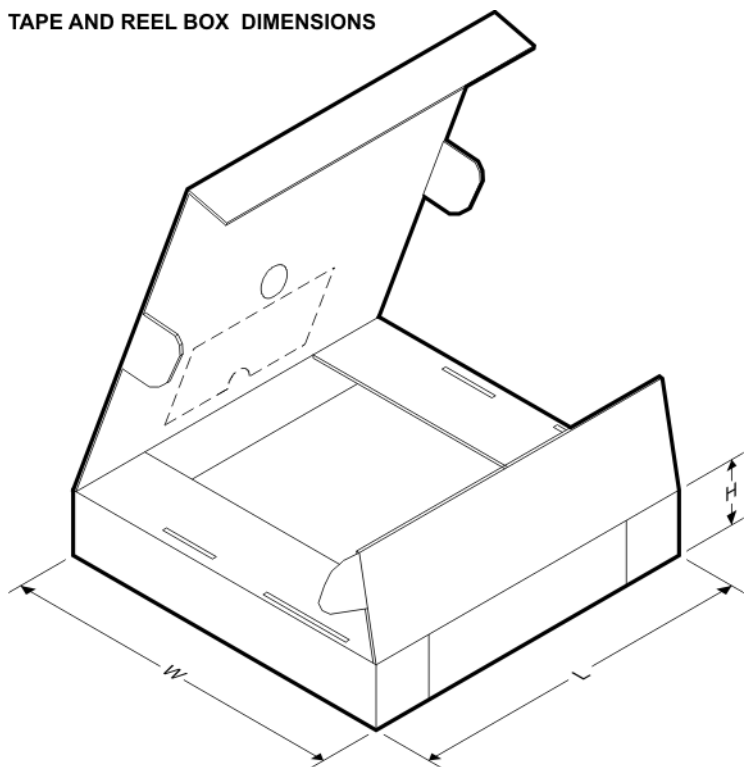
**TAPE AND REEL INFORMATION**



\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CD74HC166M96  | SOIC         | D               | 16   | 2500 | 330.0              | 16.4               | 6.5     | 10.3    | 2.1     | 8.0     | 16.0   | Q1            |
| CD74HCT166M96 | SOIC         | D               | 16   | 2500 | 330.0              | 16.4               | 6.5     | 10.3    | 2.1     | 8.0     | 16.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



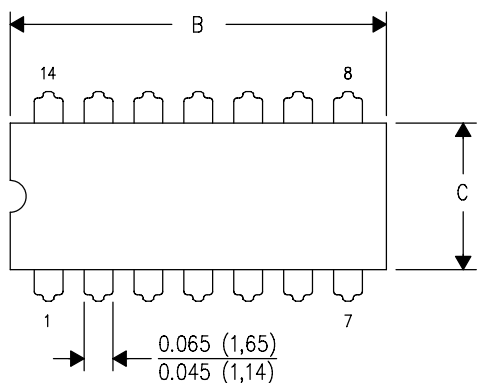
\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CD74HC166M96  | SOIC         | D               | 16   | 2500 | 333.2       | 345.9      | 28.6        |
| CD74HCT166M96 | SOIC         | D               | 16   | 2500 | 333.2       | 345.9      | 28.6        |

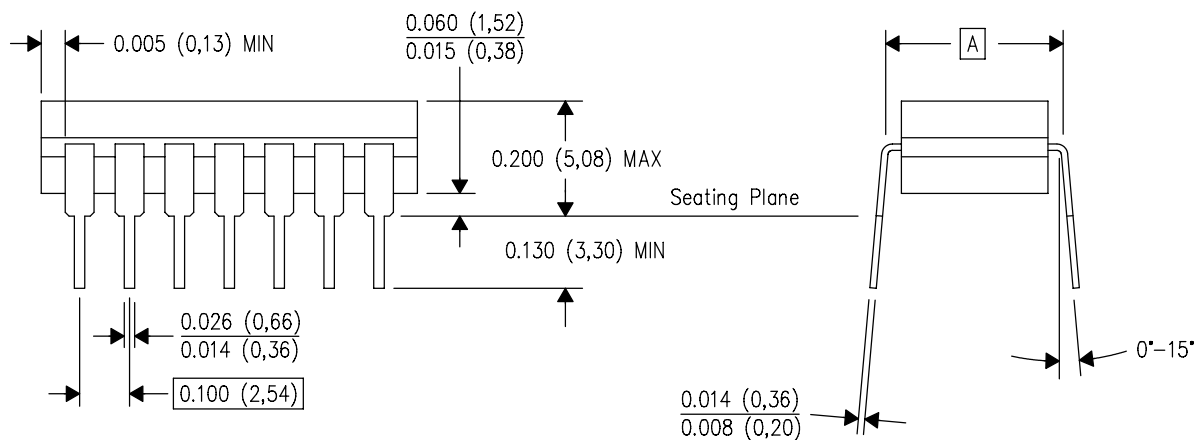
J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



| PINS **<br>DIM | 14                     | 16                     | 18                     | 20                     |
|----------------|------------------------|------------------------|------------------------|------------------------|
| A              | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC |
| B MAX          | 0.785<br>(19,94)       | .840<br>(21,34)        | 0.960<br>(24,38)       | 1.060<br>(26,92)       |
| B MIN          | —                      | —                      | —                      | —                      |
| C MAX          | 0.300<br>(7,62)        | 0.300<br>(7,62)        | 0.310<br>(7,87)        | 0.300<br>(7,62)        |
| C MIN          | 0.245<br>(6,22)        | 0.245<br>(6,22)        | 0.220<br>(5,59)        | 0.245<br>(6,22)        |



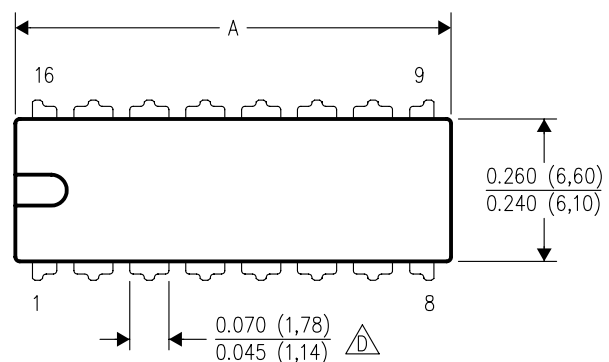
4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

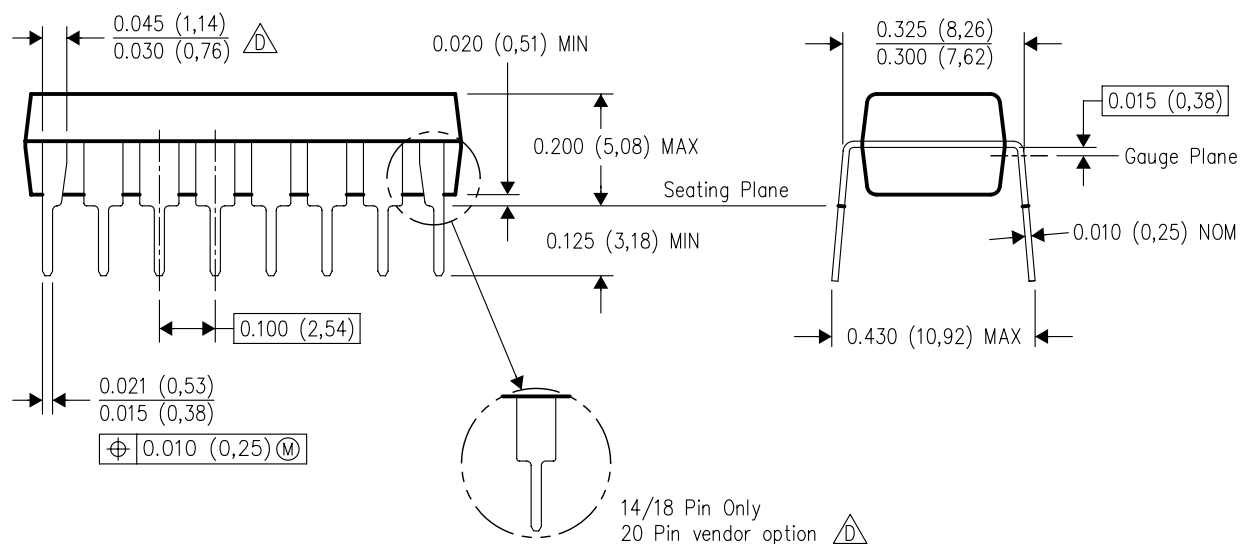
## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



| PINS **             | 14               | 16               | 18               | 20               |
|---------------------|------------------|------------------|------------------|------------------|
| DIM                 |                  |                  |                  |                  |
| A MAX               | 0.775<br>(19,69) | 0.775<br>(19,69) | 0.920<br>(23,37) | 1.060<br>(26,92) |
| A MIN               | 0.745<br>(18,92) | 0.745<br>(18,92) | 0.850<br>(21,59) | 0.940<br>(23,88) |
| MS-001<br>VARIATION | AA               | BB               | AC               | AD               |

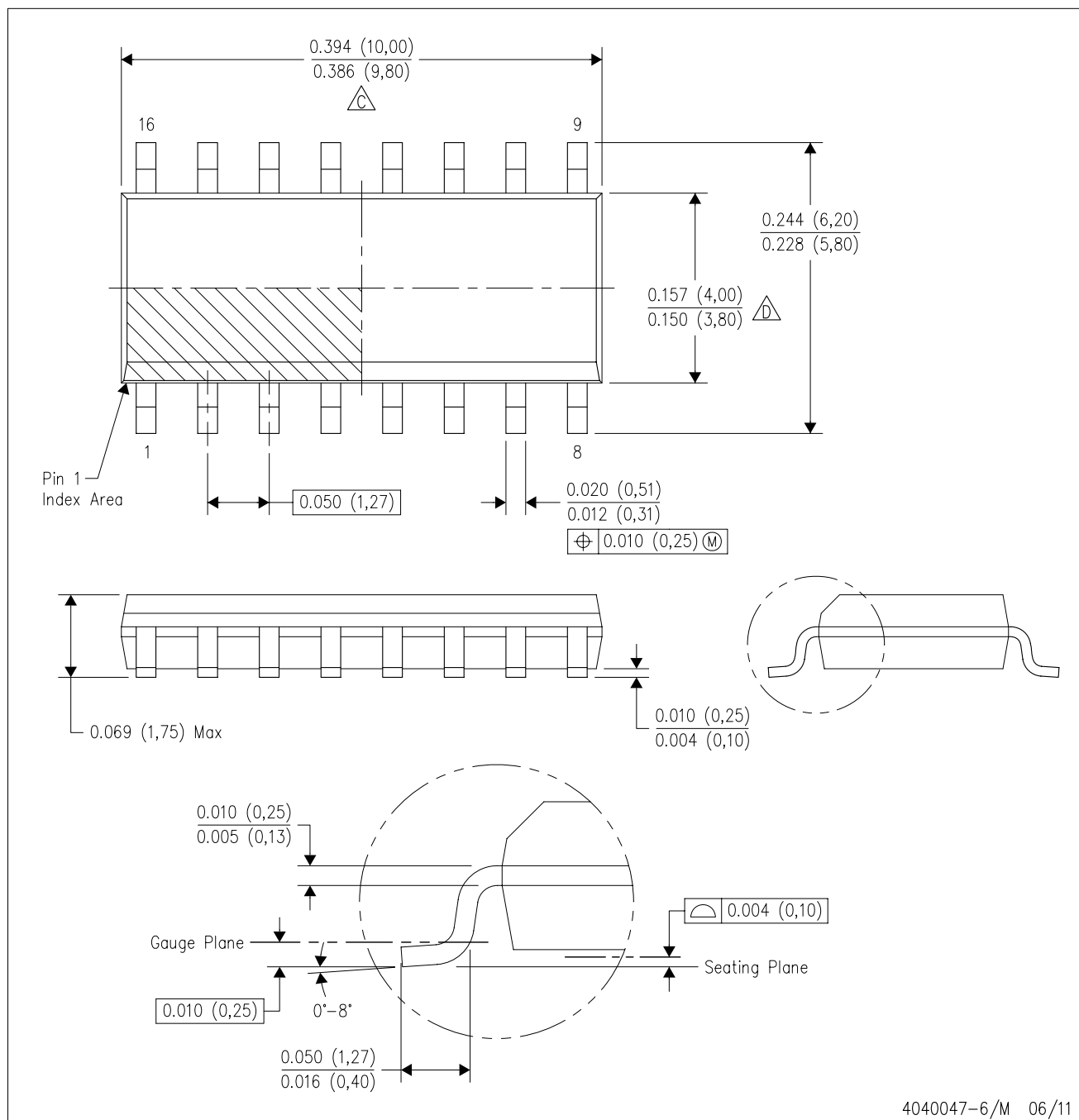


4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G16)

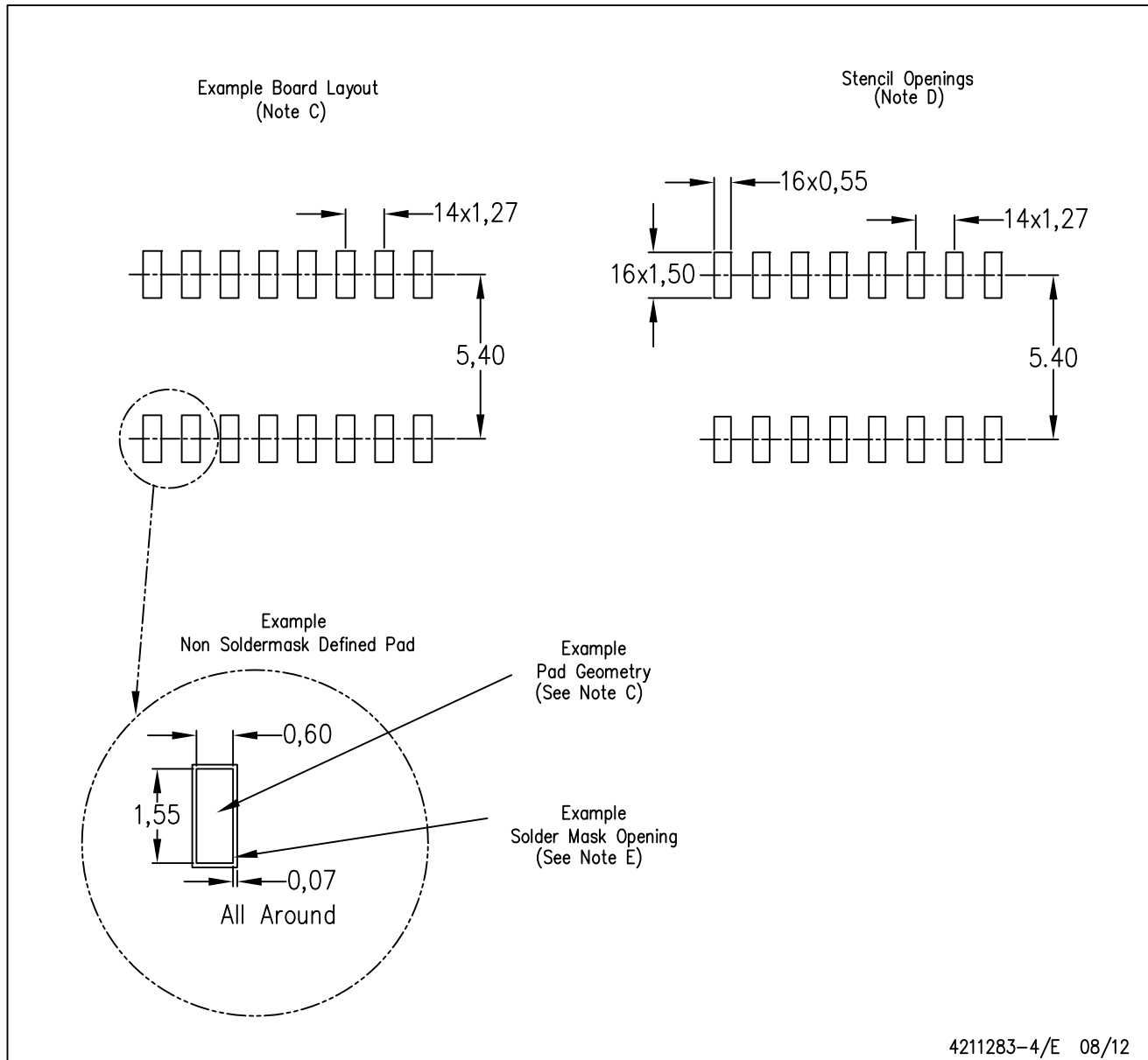
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - $\triangle D$  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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