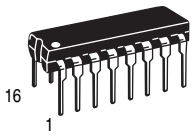
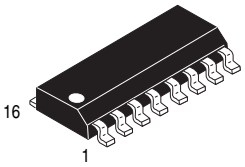
**Freescale Semiconductor**
Technical Data

MC145026/D
Rev. 4, 1/2005

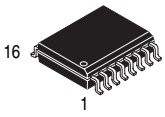
# MC145026, MC145027 MC145028




P Suffix
Plastic DIP
Case 648




D Suffix
SOG Package
Case751B




DW Suffix
SOG Package
Case 751G

# MC145026, MC145027, MC145028

## Encoder and Decoder Pairs CMOS

## 1 Introduction

These devices are designed to be used as encoder/decoder pairs in remote control applications.

The MC145026 encodes nine lines of information and serially sends this information upon receipt of a transmit enable ($\overline{TE}$) signal. The nine lines may be encoded with trinary data (low, high, or open) or binary data (low or high). The words are transmitted twice per encoding sequence to increase security.

The MC145027 decoder receives the serial stream and interprets five of the trinary digits as an address code. Thus, 243 addresses are possible. If binary data is used at the encoder, 32 addresses are possible. The remaining serial information is interpreted as four bits of binary data. The valid transmission (VT) output goes high on the MC145027 when two conditions are met. First, two addresses must be consecutively received (in one encoding sequence) which both match the local address. Second, the 4 bits of data must match the last valid data received. The active VT indicates that the information at the Data output pins has been updated.

**Ordering Information**

| Device | Package |
|---|---|
| MC145026P | Plastic DIP |
| MC145026D | SOG Package |
| MC145027P | Plastic DIP |
| MC145027DW | SOG Package |
| MC145028P | Plastic DIP |
| MC145028DW | SOG Package |

### Contents





freescale™ semiconductor

The MC145028 decoder treats all nine trinary digits as an address which allows 19,683 codes. If binary data is encoded, 512 codes are possible. The VT output goes high on the MC145028 when two addresses are consecutively received (in one encoding sequence) which both match the local address.

- Operating Temperature Range: - 40 to + 85°C
- Very-Low Standby Current for the Encoder: 300 nA Maximum @ 25°C
- Interfaces with RF, Ultrasonic, or Infrared Modulators and Demodulators
- RC Oscillator, No Crystal Required
- High External Component Tolerance; Can Use ± 5% Components
- Internal Power-On Reset Forces All Decoder Outputs Low
- Operating Voltage Range:

  MC145026 = 2.5 to 18 V

  MC145027, MC145028 = 4.5 to 18 V

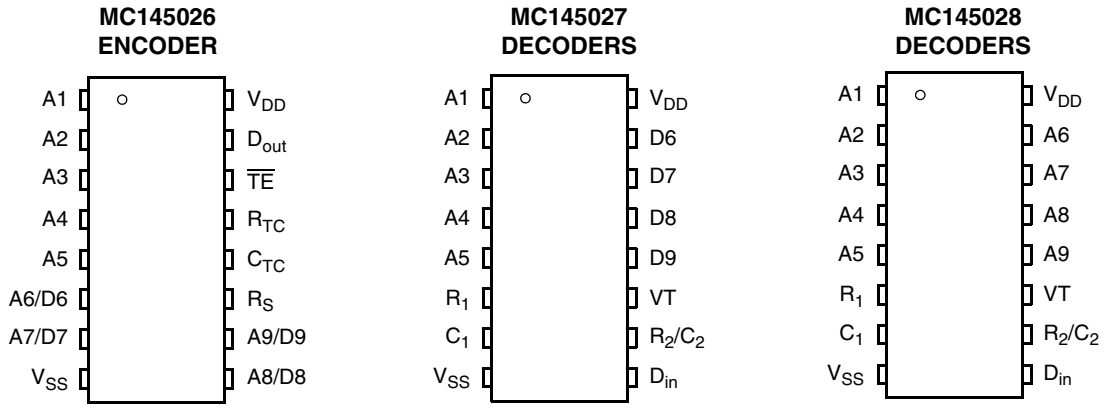



**Figure 1. Pin Assignments**

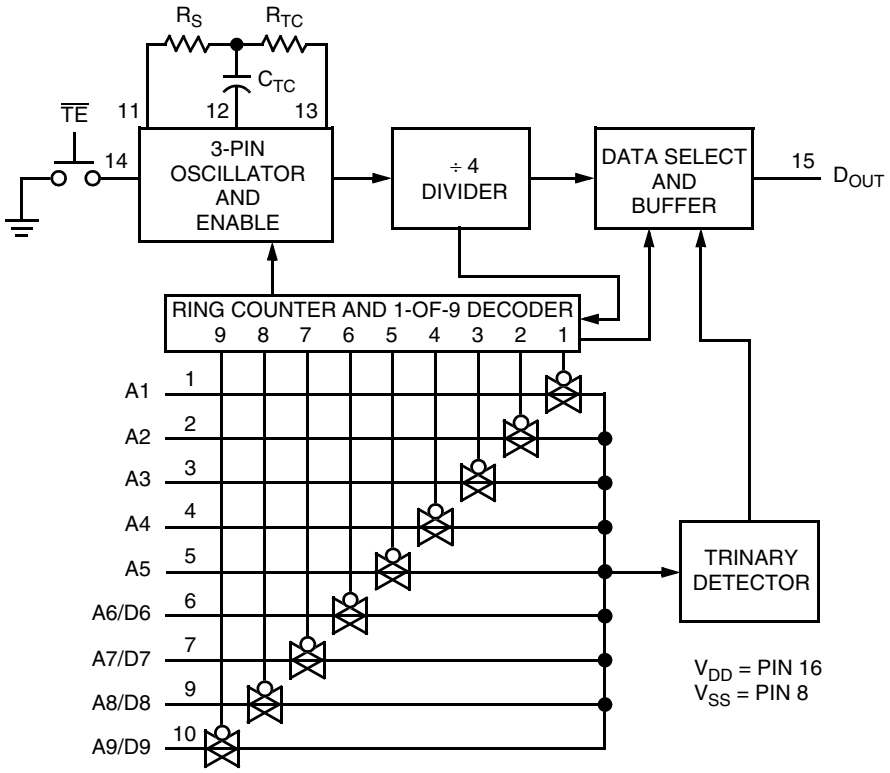



**Figure 2. MC145026 Encoder Block Diagram**

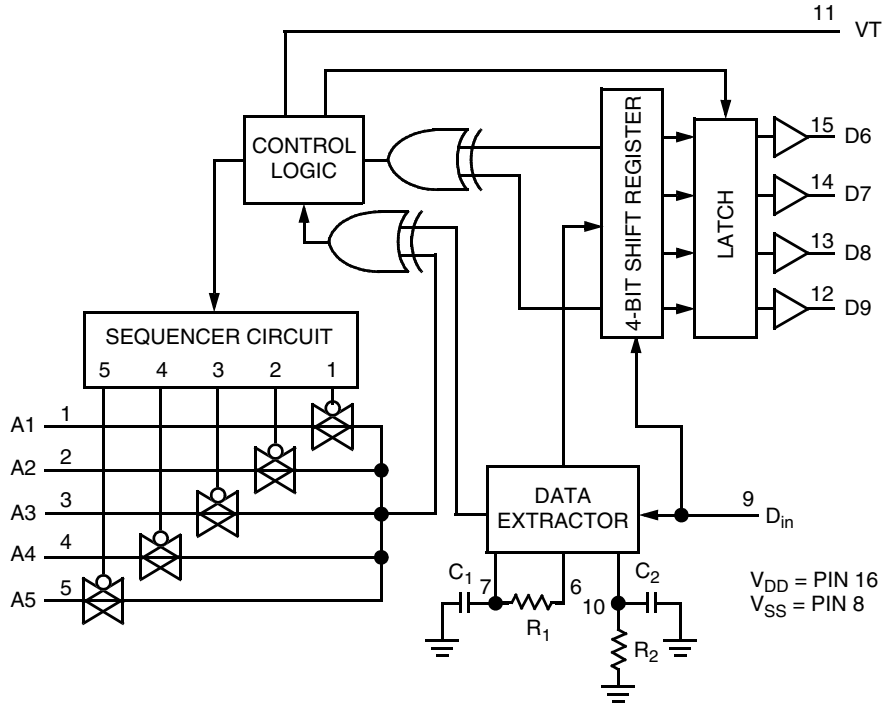



**Figure 3. MC145027 Decoder Block Diagram**

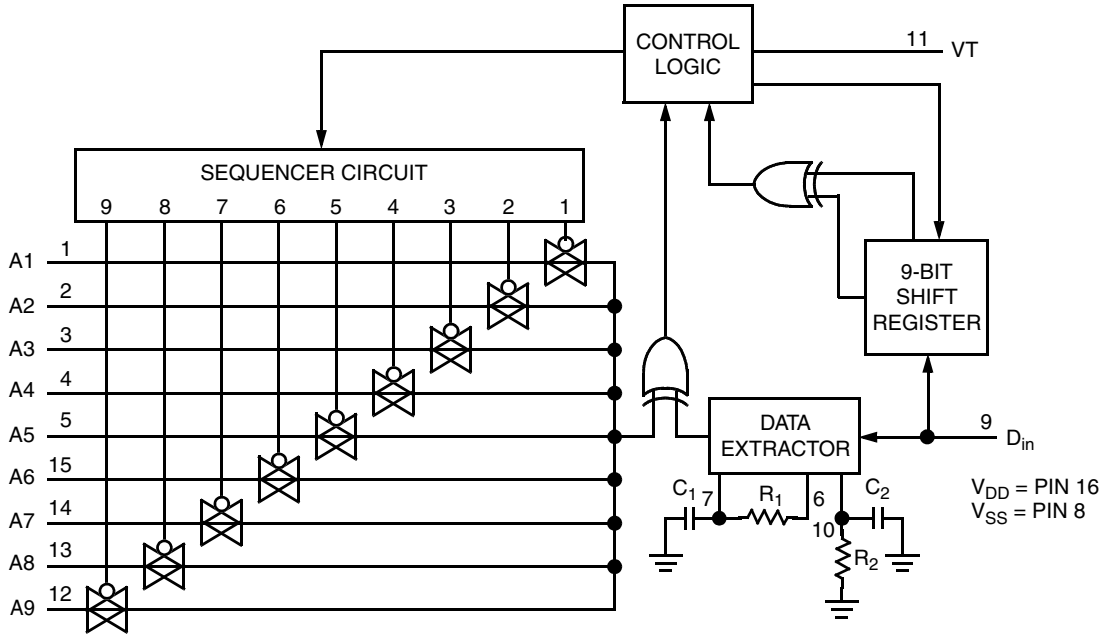



**Figure 4. MC145028 Decoder Block Diagram**

# 2 Electrical Specifications

**Table 1. Maximum Ratings*** (Voltages Referenced to $V_{SS}$)

| Ratings | Symbol | Value | Unit |
|---|---|---|---|
| DC Supply Voltage | $V_{DD}$ | - 0.5 to + 18 | V |
| DC Input Voltage | $V_{in}$ | - 0.5 to $V_{DD}$ + 0.5 | V |
| DC Output Voltage | $V_{out}$ | - 0.5 to $V_{DD}$ + 0.5 | V |
| DC Input Current, per Pin | $I_{in}$ | ± 10 | mA |
| DC Output Current, per Pin | $I_{out}$ | ± 10 | mA |
| Power Dissipation, per Package | $P_D$ | 500 | mW |
| Storage Temperature | $T_{stg}$ | - 65 to + 150 | °C |
| Lead Temperature, 1 mm from Case for 10 Seconds | $T_L$ | 260 | °C |

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, $V_{in}$ and $V_{out}$ should be constrained to the range VSS ≤ ($V_{in}$ or $V_{out}$) ≤ VDD.

**Table 2. Electrical Characteristics - MC145026[1], MC145027, and MC145028**
(Voltage Referenced to $V_{SS}$)

| Symbol | Characteristic | $V_{DD}$ V | Guaranteed Limit | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | - 40°C | | 25°C | | 85°C | | |
| | | | Min | Max | Min | Max | Min | Max | |
| $V_{OL}$ | Low-Level Output Voltage ($V_{in}$ = $V_{DD}$ or 0) | 5.0 | - | 0.05 | - | 0.05 | - | 0.05 | V |
| | | 10 | - | 0.05 | - | 0.05 | - | 0.05 | |
| | | 15 | - | 0.05 | - | 0.05 | - | 0.05 | |
| $V_{OH}$ | High-Level Output Voltage ($V_{in}$ = 0 or $V_{DD}$) | 5.0 | 4.95 | - | 4.95 | - | 4.95 | - | V |
| | | 10 | 9.95 | - | 9.95 | - | 9.95 | - | |
| | | 15 | 14.95 | - | 14.95 | - | 14.95 | - | |
| $V_{IL}$ | Low-Level Input Voltage | | | | | | | | V |
| | ($V_{out}$ = 4.5 or 0.5 V) | 5.0 | - | 1.5 | - | 1.5 | - | 1.5 | |
| | ($V_{out}$ = 9.0 or 1.0 V) | 10 | - | 3.0 | - | 3.0 | - | 3.0 | |
| | ($V_{out}$ = 13.5 or 1.5 V) | 15 | - | 4.0 | - | 4.0 | - | 4.0 | |
| $V_{IH}$ | High-Level Input Voltage | | | | | | | | V |
| | ($V_{out}$ = 0.5 or 4.5 V) | 5.0 | 3.5 | - | 3.5 | - | 3.5 | - | |
| | ($V_{out}$ = 1.0 or 9.0 V) | 10 | 7.0 | - | 7.0 | - | 7.0 | - | |
| | ($V_{out}$ = 1.5 or 13.5 V) | 15 | 11 | - | 11 | - | 11 | - | |
| $I_{OH}$ | High-Level Output Current | | | | | | | | mA |
| | ($V_{out}$ = 2.5 V) | 5.0 | - 2.5 | - | - 2.1 | - | - 1.7 | - | |
| | ($V_{out}$ = 4.6 V) | 5.0 | - 0.52 | - | - 0.44 | - | - 0.36 | - | |
| | ($V_{out}$ = 9.5 V) | 10 | - 1.3 | - | - 1.1 | - | - 0.9 | - | |
| | ($V_{out}$ = 13.5 V) | 15 | - 3.6 | - | - 3.0 | - | - 2.4 | - | |
| $I_{OL}$ | Low-Level Output Current | | | | | | | | mA |
| | ($V_{out}$ = 0.4 V) | 5.0 | 0.52 | - | 0.44 | - | 0.36 | - | |
| | ($V_{out}$ = 0.5 V) | 10 | 1.3 | - | 1.1 | - | 0.9 | - | |
| | ($V_{out}$ = 1.5 V) | 15 | 3.6 | - | 3.0 | - | 2.4 | - | |
| $I_{in}$ | Input Current - $\overline{TE}$ | 5.0 | - | - | 3.0 | 11 | - | - | μA |
| | (MC145026, Pull-Up Device) | 10 | - | - | 16 | 60 | - | - | |
| | | 15 | - | - | 35 | 120 | - | - | |
| $I_{in}$ | Input Current | 15 | - | ± 0.3 | - | ± 0.3 | - | ± 1.0 | μA |
| | $R_S$ (MC145026), $D_{in}$ (MC145027, MC145028) | | | | | | | | |
| $I_{in}$ | Input Current | | | | | | | | μA |
| | A1 - A5, A6/D6 - A9/D9 (MC145026), | 5.0 | - | - | - | ± 110 | - | - | |
| | A1 - A5 (MC145027), | 10 | - | - | - | ± 500 | - | - | |
| | A1 - A9 (MC145028) | 15 | - | - | - | ± 1000 | - | - | |
| $C_{in}$ | Input Capacitance ($V_{in}$ = 0) | - | - | - | - | 7.5 | - | - | pF |
| $I_{DD}$ | Quiescent Current - MC145026 | 5.0 | - | - | - | 0.1 | - | - | μA |
| | | 10 | - | - | - | 0.2 | - | - | |
| | | 15 | - | - | - | 0.3 | - | - | |
| $I_{DD}$ | Quiescent Current - MC145027, MC145028 | 5.0 | - | - | - | 50 | - | - | μA |
| | | 10 | - | - | - | 100 | - | - | |
| | | 15 | - | - | - | 150 | - | - | |

[1] Also see next Electrical Characteristics table for 2.5 V specifications.

**Table 2. Electrical Characteristics - MC145026[1], MC145027, and MC145028 (continued)**
(Voltage Referenced to $V_{SS}$)

| Symbol | Characteristic | $V_{DD}$ V | Guaranteed Limit | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | - 40°C | | 25°C | | 85°C | | |
| | | | Min | Max | Min | Max | Min | Max | |
| $I_{dd}$ | Dynamic Supply Current - MC145026 ($f_c$ = 20 kHz) | 5.0<br>10<br>15 | -<br>-<br>- | -<br>-<br>- | -<br>-<br>- | 200<br>400<br>600 | -<br>-<br>- | -<br>-<br>- | μA |
| $I_{dd}$ | Dynamic Supply Current - MC145027, MC145028 ($f_c$ = 20 kHz) | 5.0<br>10<br>15 | -<br>-<br>- | -<br>-<br>- | -<br>-<br>- | 400<br>800<br>1200 | -<br>-<br>- | -<br>-<br>- | μA |

[1] Also see next Electrical Characteristics table for 2.5 V specifications.

**Table 3. Electrical Characteristics - MC145026** (Voltage Referenced to $V_{SS}$)

| Symbol | Characteristic | $V_{DD}$ V | Guaranteed Limit | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | - 40°C | | 25°C | | 85°C | | |
| | | | Min | Max | Min | Max | Min | Max | |
| $V_{OL}$ | Low-Level Output Voltage ($V_{in}$ = 0 V or $V_{DD}$) | 2.5 | - | 0.05 | - | 0.05 | - | 0.05 | V |
| $V_{OH}$ | High-Level Output Voltage ($V_{in}$ = 0 V or $V_{DD}$) | 2.5 | 2.45 | - | 2.45 | - | 2.45 | - | V |
| $V_{IL}$ | Low-Level Input Voltage ($V_{out}$ = 0.5 V or 2.0 V) | 2.5 | - | 0.3 | - | 0.3 | - | 0.3 | V |
| $V_{IH}$ | High-Level Input Voltage ($V_{out}$ = 0.5 V or 2.0 V) | 2.5 | 2.2 | - | 2.2 | - | 2.2 | - | V |
| $I_{OH}$ | High-Level Output Current ($V_{out}$ = 1.25 V) | 2.5 | 0.28 | - | 0.25 | - | 0.2 | - | mA |
| $I_{OL}$ | Low-Level Output Current ($V_{out}$ = 0.4 V) | 2.5 | 0.22 | - | 0.2 | - | 0.16 | - | mA |
| $I_{in}$ | Input Current ($\overline{TE}$ - Pull-Up Device) | 2.5 | - | - | 0.09 | 1.8 | - | - | μA |
| $I_{in}$ | Input Current (A1-A5, A6/D6-A9/D9) | 2.5 | - | - | - | ± 25 | - | - | μA |
| $I_{DD}$ | Quiescent Current | 2.5 | - | - | - | 0.05 | - | - | μA |
| $I_{dd}$ | Dynamic Supply Current ($f_c$ = 20 kHz) | 2.5 | - | - | - | 40 | - | - | μA |

**Table 4. Switching Characteristics - MC145026[1], MC145027, and MC145028** ($C_L$ = 50 pF, $T_A$ = 25°C)

| Symbol | Characteristic | Figure No. | $V_{DD}$ | Guaranteed Limit | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| $t_{TLH}$, $t_{THL}$ | Output Transition Time | 5, 9 | 5.0<br>10<br>15 | -<br>-<br>- | 200<br>100<br>80 | ns |
| $t_r$ | $D_{in}$ Rise Time - Decoders | 6 | 5.0<br>10<br>15 | -<br>-<br>- | 15<br>15<br>15 | µs |
| $t_f$ | $D_{in}$ Fall Time - Decoders | 6 | 5.0<br>10<br>15 | -<br>-<br>- | 15<br>5.0<br>4.0 | µs |
| $f_{osc}$ | Encoder Clock Frequency | 7 | 5.0<br>10<br>15 | 0.001<br>0.001<br>0.001 | 2.0<br>5.0<br>10 | MHz |
| f | Decoder Frequency - Referenced to Encoder Clock | 13 | 5.0<br>10<br>15 | 1.0<br>1.0<br>1.0 | 240<br>410<br>450 | kHz |
| $t_w$ | $\overline{TE}$ Pulse Width - Encoders | 8 | 5.0<br>10<br>15 | 65<br>30<br>20 | -<br>-<br>- | ns |

[1] Also see next Electrical Characteristics table for 2.5 V specifications.

**Table 5. Switching Characteristics - MC145026** ($C_L$ = 50 pF, $T_A$ = 25°C)

| Symbol | Characteristic | Figure No. | $V_{DD}$ | Guaranteed Limit | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| $t_{TLH}$, $t_{THL}$ | Output Transition Time | 5, 9 | 2.5 | - | 450 | ns |
| $f_{osc}$ | Encoder Clock Frequency | 7 | 2.5 | 1.0 | 250 | kHz |
| $t_w$ | $\overline{TE}$ Pulse Width | 8 | 2.5 | 1.5 | - | µs |

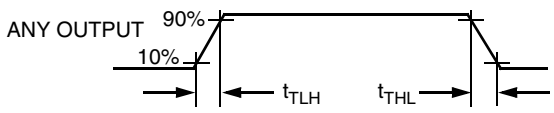



**Figure 5. Output Transition Time**

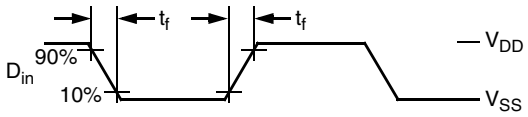



**Figure 6. $D_{in}$ Rise and Fall Time**

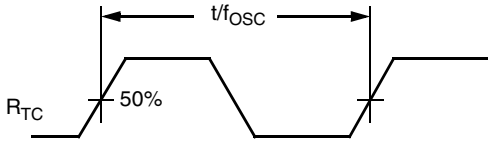



**Figure 7. Encoder Clock Frequency**

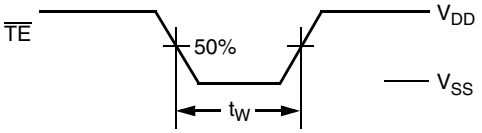
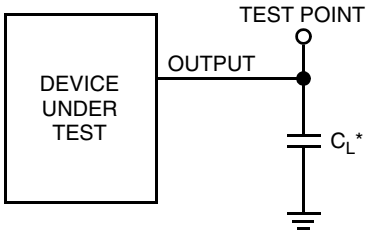



**Figure 8. $\overline{TE}$ Pulse Width**




* Includes all probe and fixture capacitance.

**Figure 9. Test Circuit**

# 3 Operating Characteristics

## 3.1 MC145026

The encoder serially transmits trinary data as defined by the state of the A1 - A5 and A6/D6 - A9/D9 input pins. These pins may be in either of three states (low, high, or open) allowing 19,683 possible codes. The transmit sequence is initiated by a low level on the $\overline{TE}$ input pin. Upon power-up, the MC145026 can continuously transmit as long as $\overline{TE}$ remains low (also, the device can transmit two-word sequences by pulsing $\overline{TE}$ low). However, no MC145026 application should be designed to rely upon the first data word transmitted immediately after power-up because this word may be invalid. Between the two data words, no signal is sent for three data periods (see Figure 11).

Each transmitted trinary digit is encoded into pulses (see Figure 12). A logic 0 (low) is encoded as two consecutive short pulses, a logic 1 (high) as two consecutive long pulses, and an open (high impedance) as a long pulse followed by a short pulse. The input state is determined by using a weak “output” device to try to force each input high then low. If only a high state results from the two tests, the input is assumed to be hardwired to $V_{DD}$. If only a low state is obtained, the input is assumed to be hardwired to $V_{SS}$. If both a high and a low can be forced at an input, an open is assumed and is encoded as such. The “high” and

"low" levels are 70% and 30% of the supply voltage as shown in the Electrical Characteristics table. The weak "output" device sinks/sources up to 110 μA at a 5 V supply level, 500 μA at 10 V, and 1 mA at 15 V.

The $\overline{TE}$ input has an internal pull-up device so that a simple switch may be used to force the input low. While $\overline{TE}$ is high, the encoder is completely disabled, the oscillator is inhibited, and the current drain is reduced to quiescent current. When $\overline{TE}$ is brought low, the oscillator is started and the transmit sequence begins. The inputs are then sequentially selected, and determinations are made as to the input logic states. This information is serially transmitted via the $D_{out}$ pin.

## 3.2 MC145027

This decoder receives the serial data from the encoder and outputs the data, if it is valid. The transmitted data, consisting of two identical words, is examined bit by bit during reception. The first five trinary digits are assumed to be the address. If the received address matches the local address, the next four (data) bits are internally stored, but are not transferred to the output data latch. As the second encoded word is received, the address must again match. If a match occurs, the new data bits are checked against the previously stored data bits. If the two nibbles of data (four bits each) match, the data is transferred to the output data latch by VT and remains until new data replaces it. At the same time, the VT output pin is brought high and remains high until an error is received or until no input signal is received for four data periods (see Figure 11).

Although the address information may be encoded in trinary, the data information must be either a 1 or 0. A trinary (open) data line is decoded as a logic 1.

## 3.3 MC145028

This decoder operates in the same manner as the MC145027 except that nine address lines are used and no data output is available. The VT output is used to indicate that a valid address has been received. For transmission security, two identical transmitted words must be consecutively received before a VT output signal is issued.

The MC145028 allows 19,683 addresses when trinary levels are used. 512 addresses are possible when binary levels are used.

# 4 Pin Descriptions

## 4.1 MC145026 Encoder

### A1 - A5, A6/D6 - A9/D9 Address, Address/Data Inputs (Pins 1 - 7, 9, and 10)

These address/data inputs are encoded and the data is sent serially from the encoder via the $D_{out}$ pin.

### $R_S$, $C_{TC}$, $R_{TC}$ (Pins 11, 12, and 13)

These pins are part of the oscillator section of the encoder (see Figure 10).

If an external signal source is used instead of the internal oscillator, it should be connected to the $R_S$ input and the $R_{TC}$ and $C_{TC}$ pins should be left open.

### $\overline{TE}$
### Transmit Enable (Pin 14)

This active-low transmit enable input initiates transmission when forced low. An internal pull-up device keeps this input normally high. The pull-up current is specified in the Electrical Characteristics table.

### $D_{out}$
### Data Out (Pin 15)

This is the output of the encoder that serially presents the encoded data word.

### $V_{SS}$
### Negative Power Supply (Pin 8)

The most-negative supply potential. This pin is usually ground.

### $V_{DD}$
### Positive Power Supply (Pin 16)

The most-positive power supply pin.

## 4.2 MC145027 and MC145028 Decoders

### A1 - A5, A1 - A9
### Address Inputs (Pins 1 - 5)-MC145027,
### Address Inputs (Pins 1 - 5, 15, 14, 13, 12)-MC145028

These are the local address inputs. The states of these pins must match the appropriate encoder inputs for the VT pin to go high. The local address may be encoded with trinary or binary data.

### D6 - D9
### Data Outputs (Pins 15, 14, 13, 12)-MC145027 Only

These outputs present the binary information that is on encoder inputs A6/D6 through A9/D9. Only binary data is acknowledged; a trinary open at the MC145026 encoder is decoded as a high level (logic 1).

### $D_{in}$
### Data In (Pin 9)

This pin is the serial data input to the decoder. The input voltage must be at CMOS logic levels. The signal source driving this pin must be dc coupled.

### $R_1$, $C_1$
### Resistor 1, Capacitor 1 (Pins 6, 7)

As shown in Figure 3 and Figure 4, these pins accept a resistor and capacitor that are used to determine whether a narrow pulse or wide pulse has been received. The time constant $R_1 \times C_1$ should be set to 1.72 encoder clock periods:

$$R_1 C_1 = 3.95 R_{TC} C_{TC}$$

### $R_2/C_2$
### Resistor 2/Capacitor 2 (Pin 10)

As shown in Figure 3 and Figure 4, this pin accepts a resistor and capacitor that are used to detect both the end of a received word and the end of a transmission. The time constant $R_2$ x $C_2$ should be 33.5 encoder clock periods (four data periods per Figure 12): $R_2 C_2 = 77 R_{TC} C_{TC}$. This time constant is used to determine whether the $D_{in}$ pin has remained low for four data periods (end of transmission). A separate on-chip comparator looks at the voltage-equivalent two data periods ($0.4 R_2 C_2$) to detect the dead time between received words within a transmission.

### VT
### Valid Transmission Output (Pin 11)

This valid transmission output goes high after the second word of an encoding sequence when the following conditions are satisfied:

1. the received addresses of both words match the local decoder address, and
2. the received data bits of both words match.

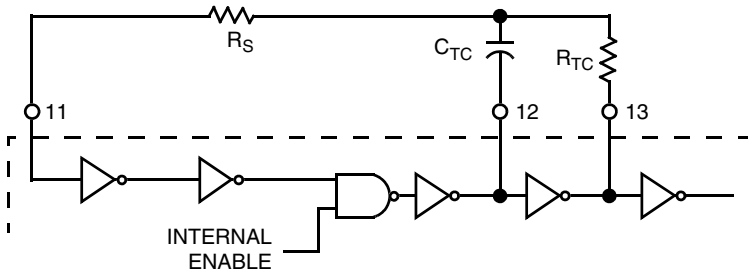
VT remains high until either a mismatch is received or no input signal is received for four data periods.

### $V_{SS}$
### Negative Power Supply (Pin 8)

The most-negative supply potential. This pin is usually ground.

### $V_{DD}$
### Positive Power Supply (Pin 16)

The most-positive power supply pin.




This oscillator operates at a frequency determined by the external RC network; i.e.,

$$f \approx \frac{1}{2.3\ R_{TC}\ C_{TC}'} \quad \text{(Hz)}$$

for 1 kHz ≤ f ≤ 400 kHz

where: $C_{TC}' = C_{TC} + C_{layout} + 12$ pF

$R_S \approx 2\ R_{TC}$

$R_S \geq 20$ k

$R_{TC} \geq 10$ k

400 pF < $C_{TC}$ < 15 μF

The value for $R_S$ should be chosen to be ≥ 2 times $R_{TC}$. This range ensures that current through $R_S$ is insignificant compared to current through $R_{TC}$. The upper limit for $R_S$ must ensure that $R_S$ x 5 pF (input capacitance) is small compared to $R_{TC}$ x $C_{TC}$.

For frequencies outside the indicated range, the formula is less accurate. The minimum recommended oscillation frequency of this circuit is 1 kHz. Susceptibility to externally induced noise signals may occur for frequencies below 1 kHz and/or when resistors utilized are greater than 1 MΩ.

**Figure 10. Encoder Oscillator Information**

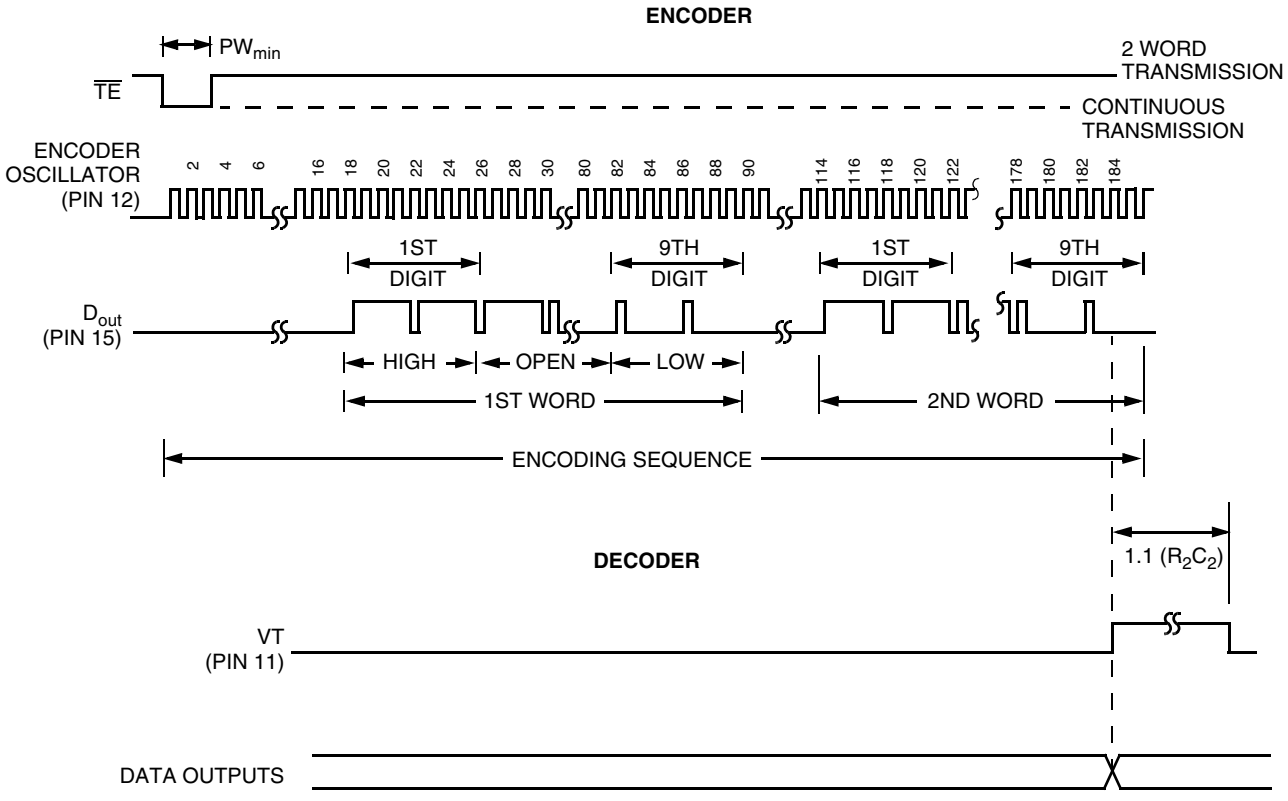



**Figure 11. Timing Diagram**

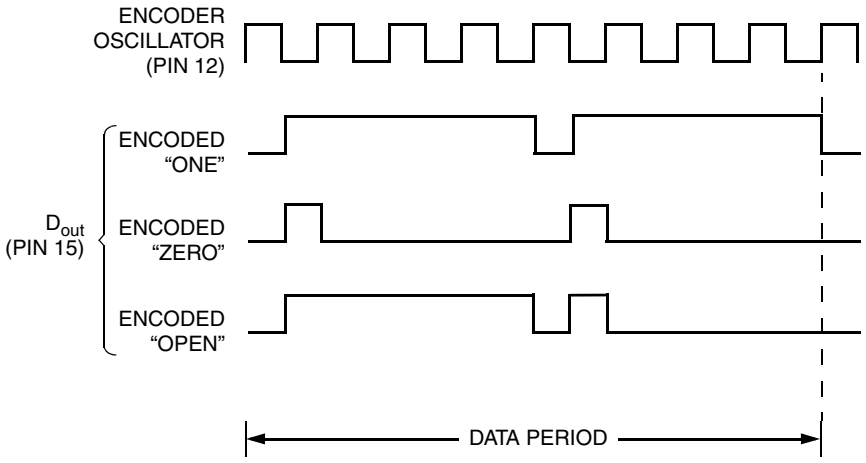



**Figure 12. Encoder Data Waveforms**

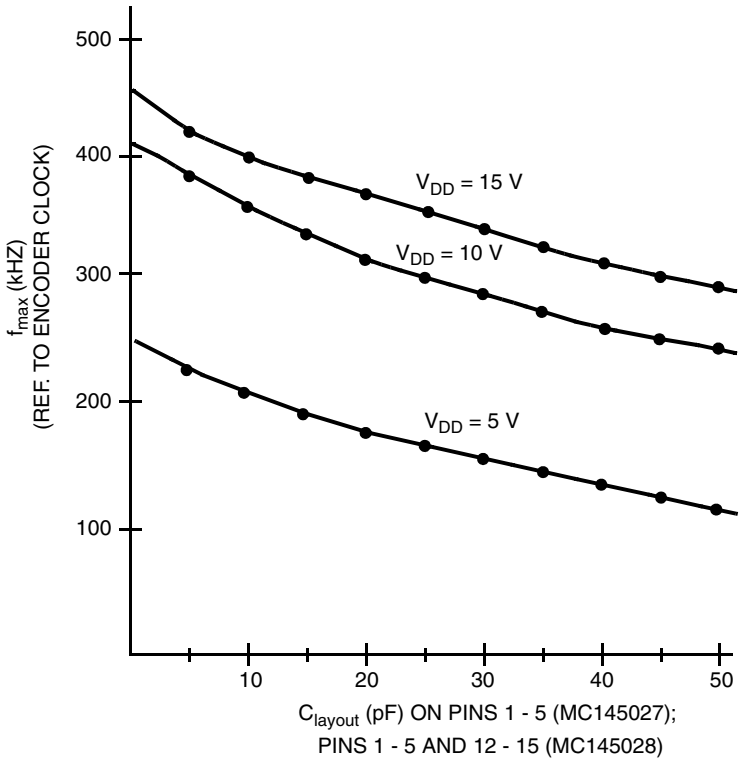



**Figure 13. $f_{max}$ vs $C_{layout}$ - Decoders Only**

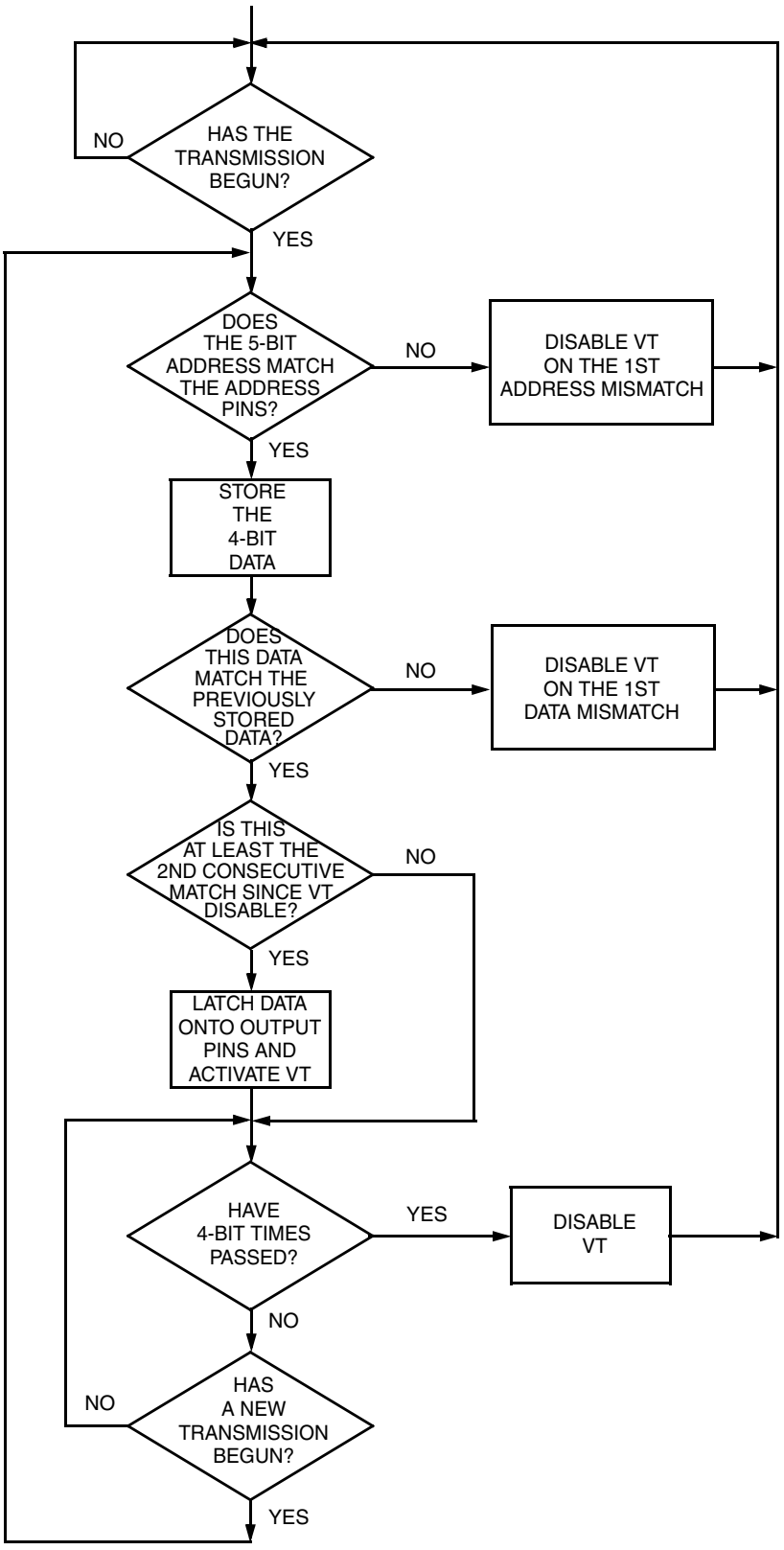



**Figure 14. MC145027 Flowchart**

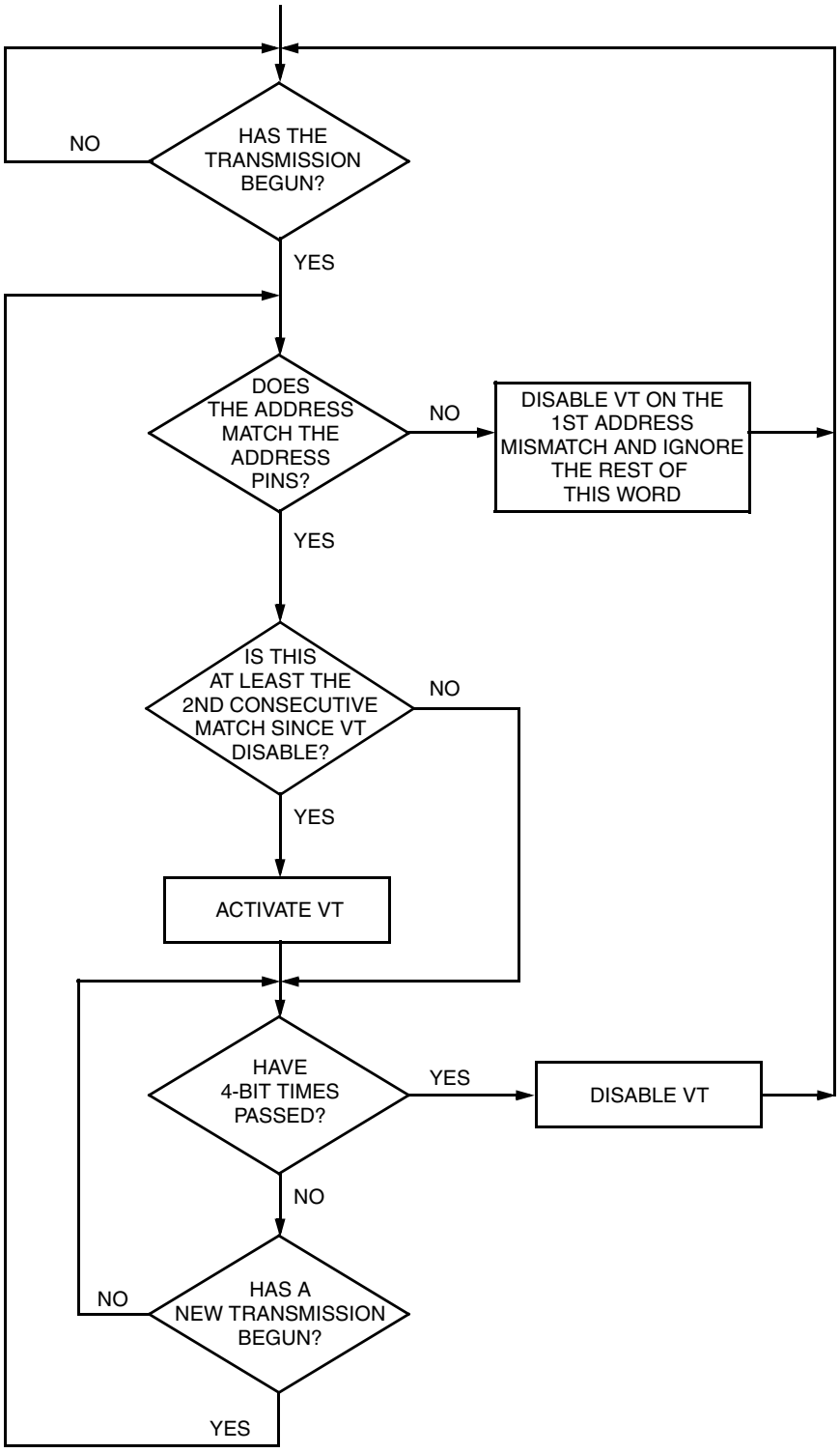



**Figure 15. MC145028 Flowchart**

# 5 MC145027 and MC145028 Timing

To verify the MC145027 or MC145028 timing, check the waveforms on C1 (Pin 7) and R2/C2 (Pin 10) as compared to the incoming data waveform on $D_{in}$ (Pin 9).

The R-C decay seen on C1 discharges down to 1/3 $V_{DD}$ before being reset to $V_{DD}$. This point of reset (labelled “DOS” in Figure 16) is the point in time where the decision is made whether the data seen on $D_{in}$ is a 1 or 0. DOS should not be too close to the $D_{in}$ data edges or intermittent operation may occur.

The other timing to be checked on the MC145027 and MC145028 is on R2/C2 (see Figure 17). The R-C decay is continually reset to $V_{DD}$ as data is being transmitted. Only between words and after the end-of-transmission (EOT) does R2/C2 decay significantly from $V_{DD}$. R2/C2 can be used to identify the internal end-of-word (EOW) timing edge which is generated when R2/C2 decays to 2/3 $V_{DD}$. The internal EOT timing edge occurs when R2/C2 decays to 1/3 $V_{DD}$. When the waveform is being observed, the R-C decay should go down between the 2/3 and 1/3 $V_{DD}$ levels, but not too close to either level before data transmission on $D_{in}$ resumes.

Verification of the timing described above should ensure a good match between the MC145026 transmitter and the MC145027 and MC145028 receivers.

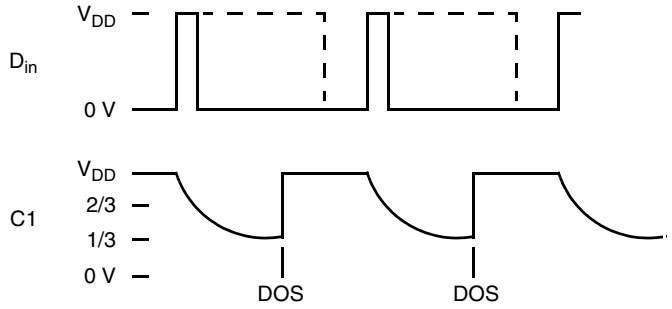



**Figure 16. R-C Decay on Pin 7 (C1)**

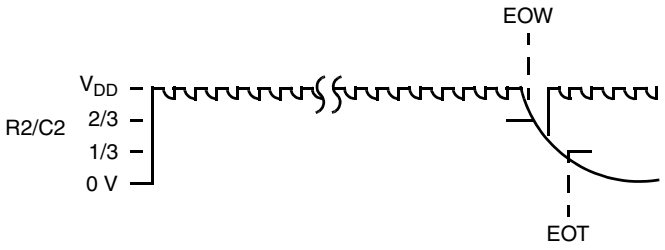
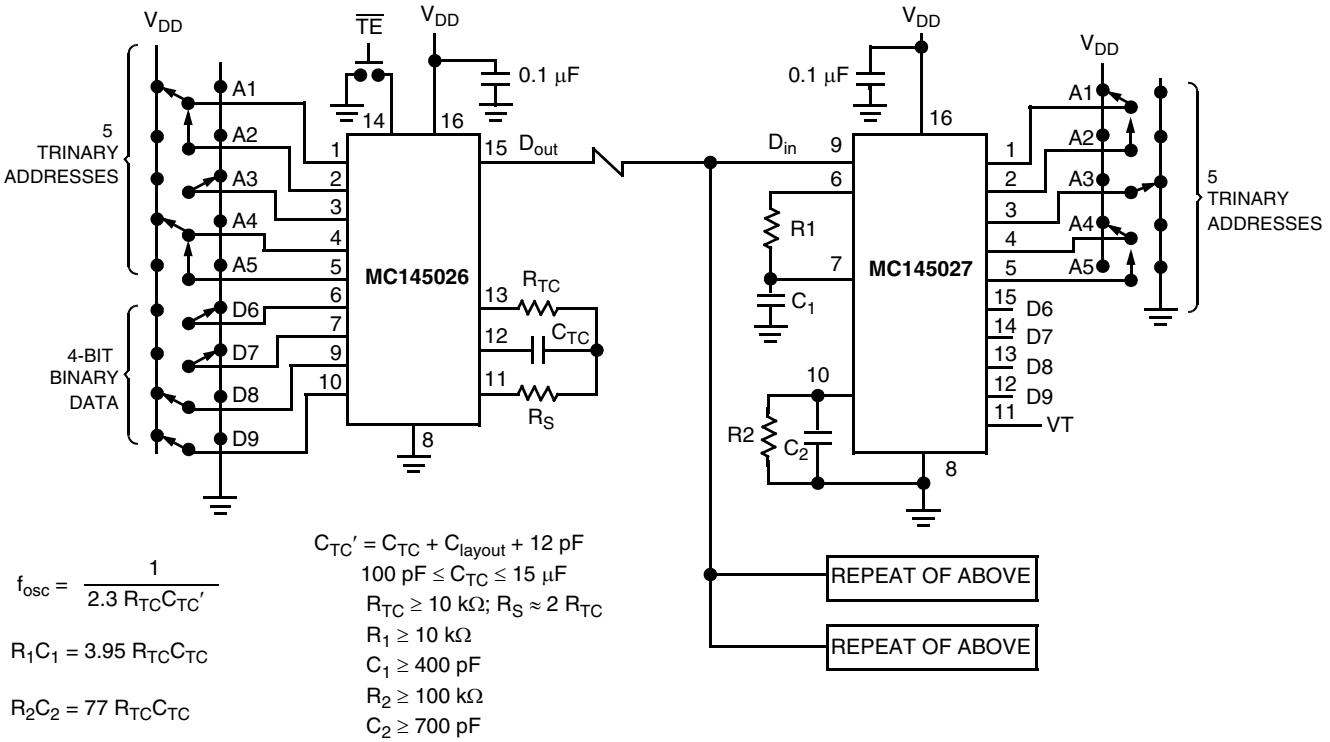



**Figure 17. R-C Decay on Pin 10 (R2/C2)**




$$f_{osc} = \frac{1}{2.3\ R_{TC}C_{TC'}}$$

$R_1C_1 = 3.95\ R_{TC}C_{TC}$

$R_2C_2 = 77\ R_{TC}C_{TC}$

$C_{TC'} = C_{TC} + C_{layout} + 12\ pF$

$100\ pF \le C_{TC} \le 15\ \mu F$

$R_{TC} \ge 10\ k\Omega$; $R_S \approx 2\ R_{TC}$

$R_1 \ge 10\ k\Omega$

$C_1 \ge 400\ pF$

$R_2 \ge 100\ k\Omega$

$C_2 \ge 700\ pF$

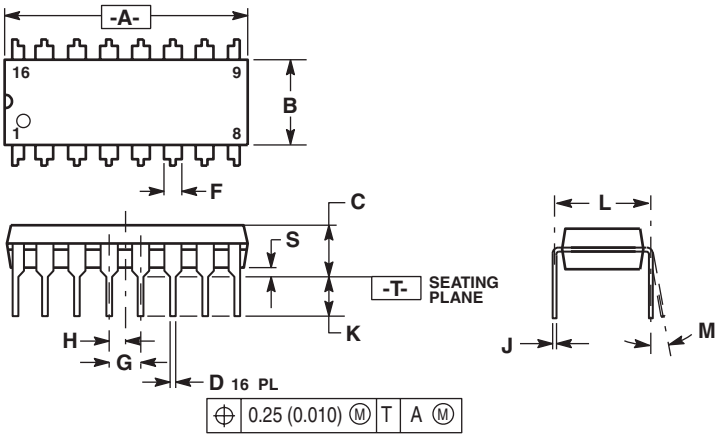
**Example R/C Values (All Resistors and Capacitors are ± 5%)**

($C_{TC'} = C_{TC} + 20\ pF$)

| $f_{osc}$ (kHz) | $R_{TC}$ | $C_{TC'}$ | $R_S$ | $R_1$ | $C_1$ | $R_2$ | $C_2$ |
|---|---|---|---|---|---|---|---|
| 362 | 10 k | 120 pF | 20 k | 10 k | 470 pF | 100 k | 910 pF |
| 181 | 10 k | 240 pF | 20 k | 10 k | 910 pF | 100 k | 1800 pF |
| 88.7 | 10 k | 490 pF | 20 k | 10 k | 2000 pF | 100 k | 3900 pF |
| 42.6 | 10 k | 1020 pF | 20 k | 10 k | 3900 pF | 100 k | 7500 pF |
| 21.5 | 10 k | 2020 pF | 20 k | 10 k | 8200 pF | 100 k | 0.015 μF |
| 8.53 | 10 k | 5100 pF | 20 k | 10 k | 0.02 μF | 200 k | 0.02 μF |
| 1.71 | 50 k | 5100 pF | 100 k | 50 k | 0.02 μF | 200 k | 0.1 μF |

**Figure 18. Typical Application**

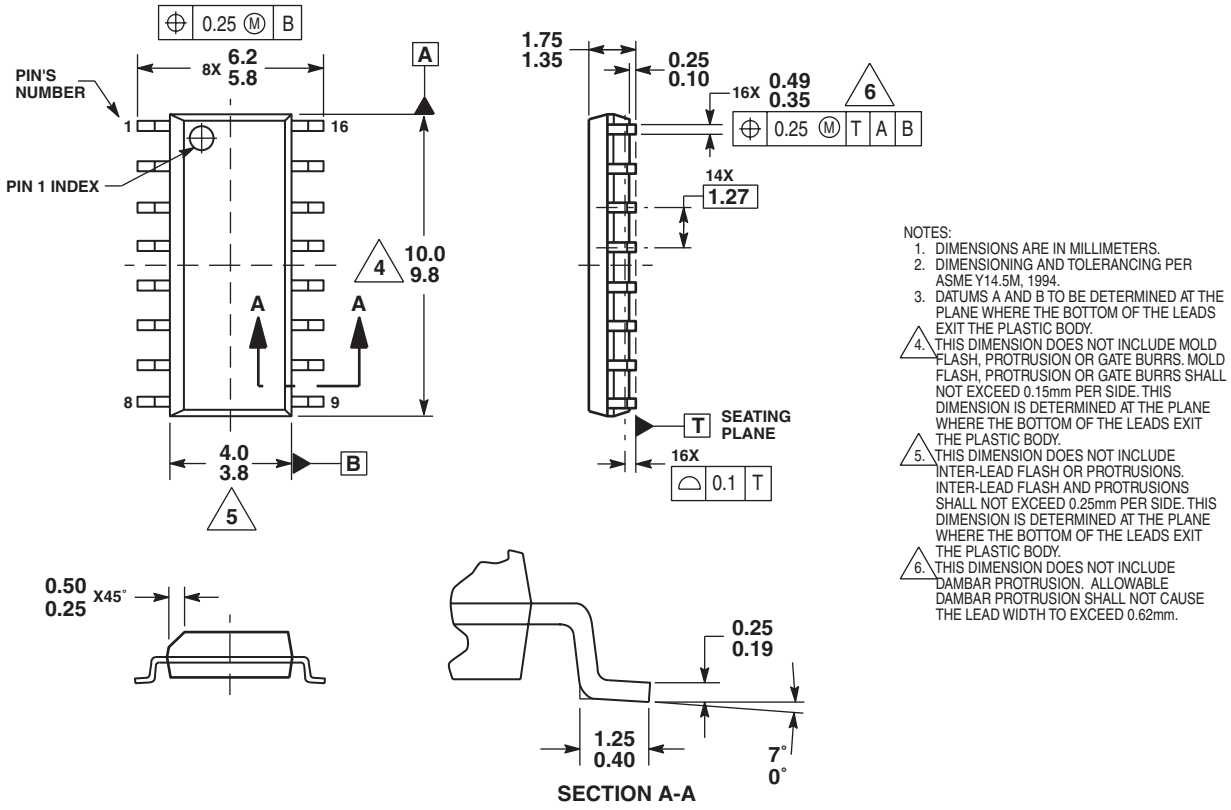
# 6 Package Dimensions




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.740 | 0.770 | 18.80 | 19.55 |
| B | 0.250 | 0.270 | 6.35 | 6.85 |
| C | 0.145 | 0.175 | 3.69 | 4.44 |
| D | 0.015 | 0.021 | 0.39 | 0.53 |
| F | 0.040 | 0.70 | 1.02 | 1.77 |
| G | 0.100 BSC | | 2.54 BSC | |
| H | 0.050 BSC | | 1.27 BSC | |
| J | 0.008 | 0.015 | 0.21 | 0.38 |
| K | 0.110 | 0.130 | 2.80 | 3.30 |
| L | 0.295 | 0.305 | 7.50 | 7.74 |
| M | 0° | 10° | 0° | 10° |
| S | 0.020 | 0.040 | 0.51 | 1.01 |

**Figure 19. Outline Dimensions for P SUFFIX PLASTIC DIP (DUAL IN-LINE PACKAGE) (Case Outline 648-08, Issue R)**




NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
3. DATUMS A AND B TO BE DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
4. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15mm PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
5. THIS DIMENSION DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25mm PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
6. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.62mm.

**Figure 20. Outline Dimensions for D SUFFIX SOG (SMALL OUTLINE GULL-WING) PACKAGE (Case Outline 751B-05, Issue K)**

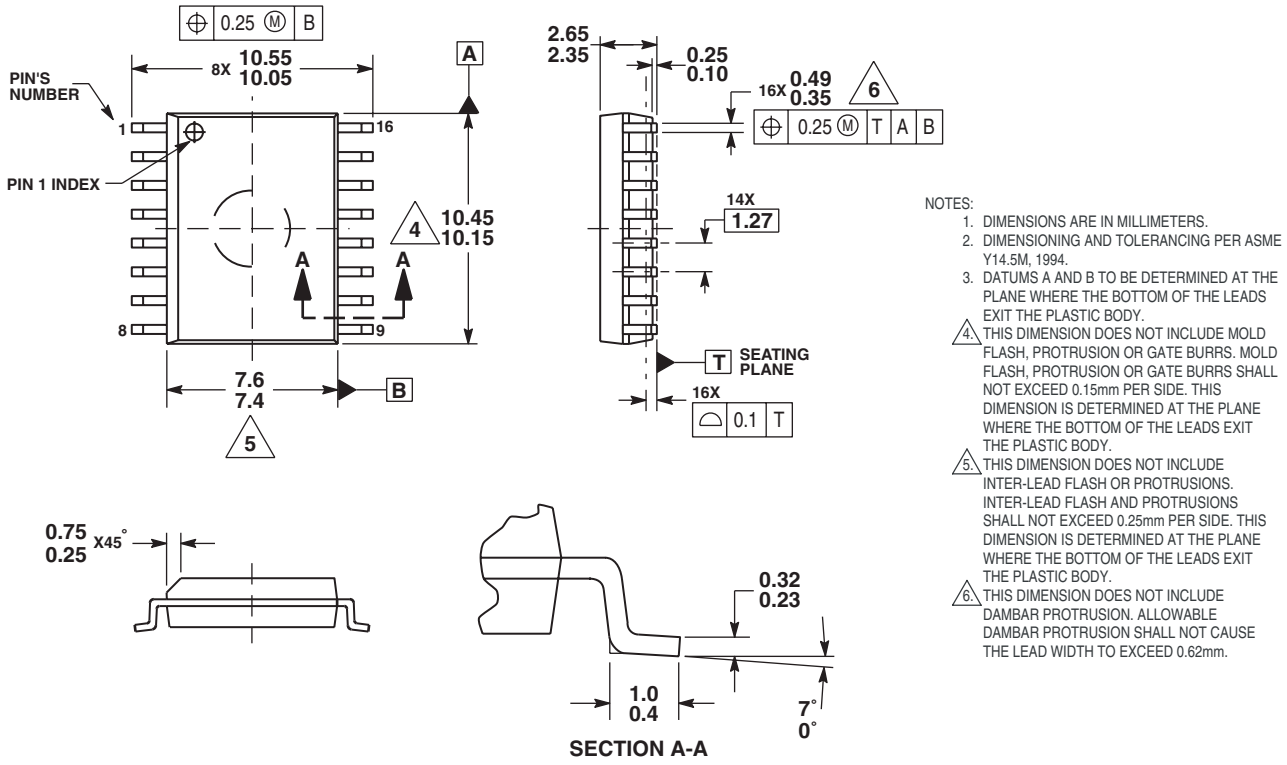



**Figure 21. Outline Dimensions for DW SUFFIX SOG (SMALL OUTLINE GULL-WING) PACKAGE (Case Outline 751G-04, Issue D)**

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