

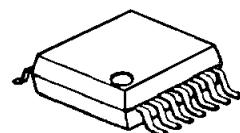
2V Operation Switching Driver for Class D Amplifier

■ GENERAL DESCRIPTION

The NJU8713 is a Switching Driver for a class D Amplifier including Separated Power Source terminals between Input and Output, BEEP and BPZ (Bipolar Zero) output circuits. It converts 1bit digital signal input, such as PWM or PDM signal, to an analog signal output through a simple external LC low-pass filter.

The NJU8713 realizes very high power-efficiency because of the class D operation. Therefore, it is suitable for portable audio set and others.

■ PACKAGE OUTLINE

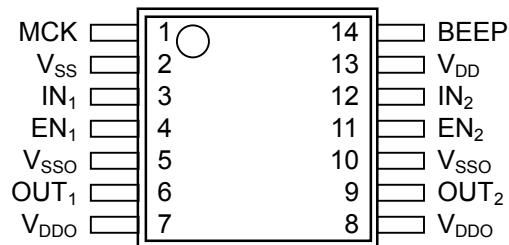


NJU8713V

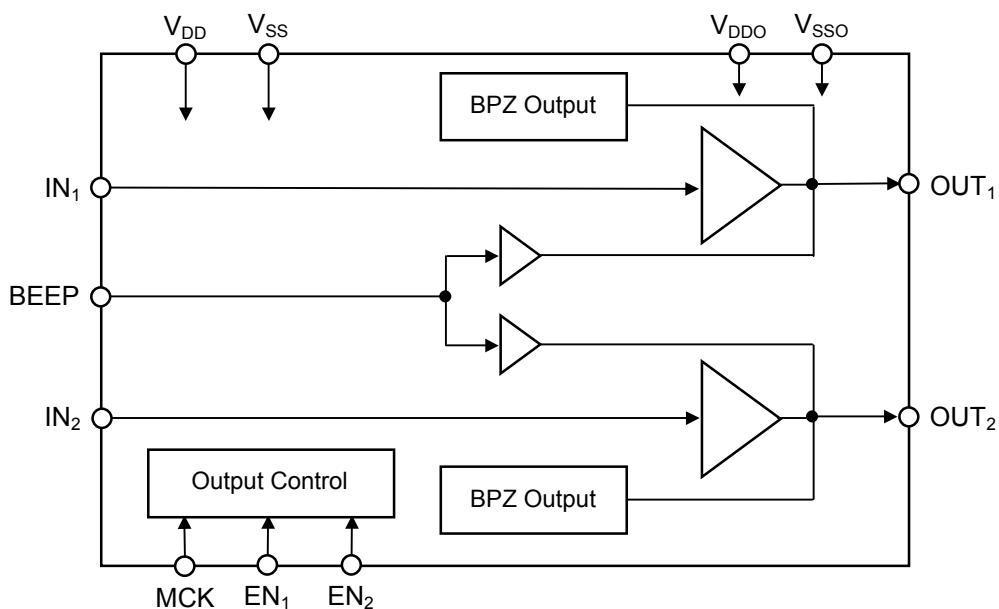
■ FEATURES

- 2-channel 1bit Audio Signal Input
- Standby(Hi-Z), BPZ Control
- Internal BPZ Charger
- Beep Function
- Operating Voltage : 1.7V to 2.7V
- Driving Voltage : 1.7V to V_{DD}
- CMOS Technology
- Package Outline : SSOP14

■ PIN CONFIGURATION



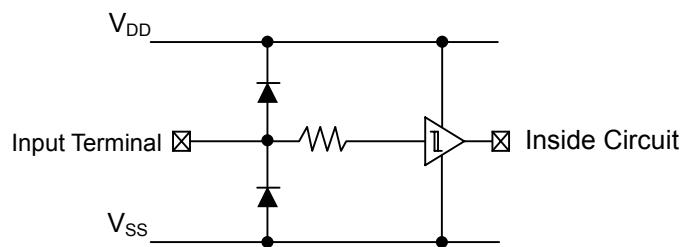
■ BLOCK DIAGRAM



■ TERMINAL DESCRIPTION

No.	SYMBOL	I/O	Function
13	V_{DD}	-	Operation Power Supply, $V_{DD}=2V$
2	V_{SS}	-	Operation Power GND, $V_{SS}=0V$
7 8	V_{DDO}	-	Driving Power Supply, $V_{DDO}=2V$ Terminal No.7 and No.8 should be connected to the same electric potential.
5 10	V_{SSO}	-	Driving Power GND, $V_{SSO}=0V$ Terminal No.5 and No.10 should be connected to the same electric potential.
1	MCK	I	Master Clock Input Terminal The condition of the data input terminal is fetched with the rising edge of this signal.
4 11	EN_1 EN_2	I	Output Control Terminal Output circuit is selected by the condition of this terminal.
3 12	IN_1 IN_2	I	Audio Signal Input Terminal 1-bit Audio Signal inputs into this terminal.
14	BEEP	I	Beep Signal Input Terminal Beep signal inputs into this terminal.
6 9	OUT_1 OUT_2	O	Output Terminal <ul style="list-style-type: none"> When Output Terminal selects Audio Signal, IN_1 terminal input data outputs from OUT_1 terminal and IN_2 terminal input data outputs from OUT_2 terminal. When Output Terminal selects Beep Signal, BEEP terminal input data outputs from OUT_1 and OUT_2 terminals.

■ INPUT TERMINAL STRUCTURE



■ FUNCTIONAL DESCRIPTION

(1) Signal Output

PWM signals of L channel and R output from OUT₁ and OUT₂ terminals respectively. These signals are converted to analog signal by external 2nd-order or over LC filter. The output driver power supplied from V_{DDO} and V_{SSO} are required high response power supply against voltage fluctuation like as switching regulator because Output T.H.D is effected by power supply stability.

(2) Master Clock

Master clock (MCK) synchronizes the Audio signal inputs (IN₁ and IN₂). The setup time and the hold time should be kept in the AC characteristics because IN₁ and IN₂ are fetched with the rising edge of MCK. MCK requires jitter-free or jitter as small as possible because the jitter downs S/N ratio.

OUT₁ and OUT₂ occur the pop noise when MCK is stopped in operation without standby mode. Therefore, the standby mode should be set before MCK stop.

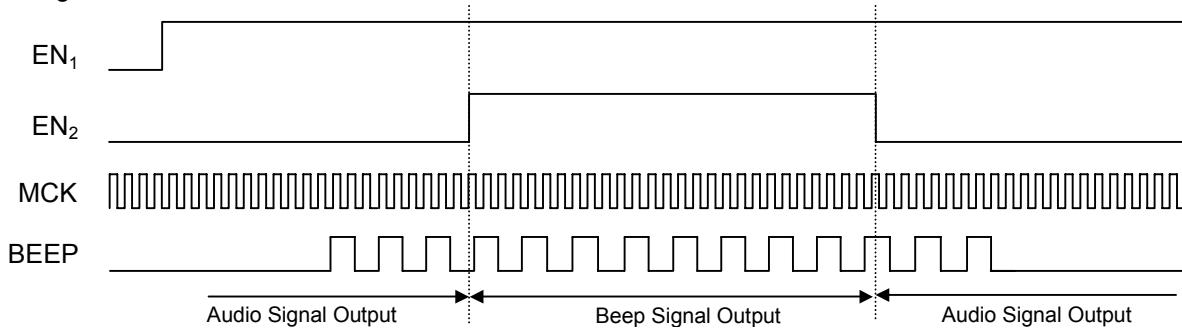
(3) Output Control

Output circuit is selected by the conditions of EN₁ and EN₂ terminals.

EN ₂	EN ₁	Output State of OUT ₁ & OUT ₂
0	0	Standby(High impedance)
0	1	Audio Signal Output
1	0	BPZ Output
1	1	Beep Signal Output

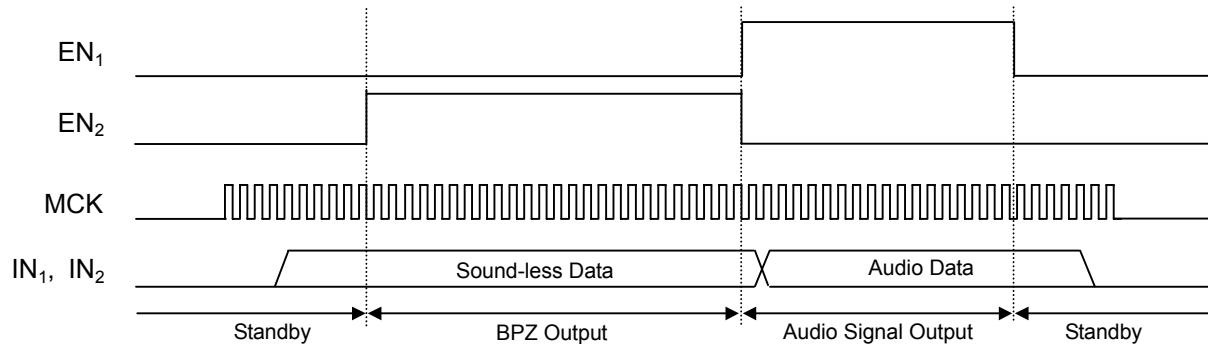
(4) Beep Function

The beep signal must be input before the rising edge of EN₂ signal and must be stopped after the falling edge of EN₂ signal.



(5) BPZ Function

BPZ Function operates to charge the external AC coupling capacitor for the BPZ level which is a point of the analog signal common. Be sure to input sound-less data to IN₁ and IN₂ in busy of the BPZ function. At this time, the sound-less signal must be input before the rising edge of EN₂ signal and must be continue after the falling edge of EN₂ signal. The charging time is in proportion to the capacity value of the external AC coupling capacitor.



■ ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)			
PARAMETER	SYMBOL	RATING	UNIT
Operation Supply Voltage	V _{DD}	-0.3 to +4.0	V
Driving Supply Voltage	V _{DDO}	-0.3 to +2.7	V
Input Voltage	V _{in}	-0.3 to V _{DD} +0.3	V
Operating Temperature	T _a	-40 to +85	°C
Storage Temperature	T _{stg}	-40 to +125	°C
Power Dissipation	SSOP14	P _D	300 mW
Power Supply Voltage Condition	-	V _{DD} ≥ V _{DDO}	V

Note 1) All voltage values are specified as V_{SS}=V_{SSO}=0V.

Note 2) If the LSI is used on condition beyond the absolute maximum rating, the LSI may be destroyed. Using LSI within electrical characteristics is strongly recommended for normal operation. Use beyond the electrical characteristics conditions will cause malfunction and poor reliability.

Note 3) Decoupling capacitors should be connected between V_{DD}-V_{SS} and V_{DDO}-V_{SSO} due to the stabilized operation.

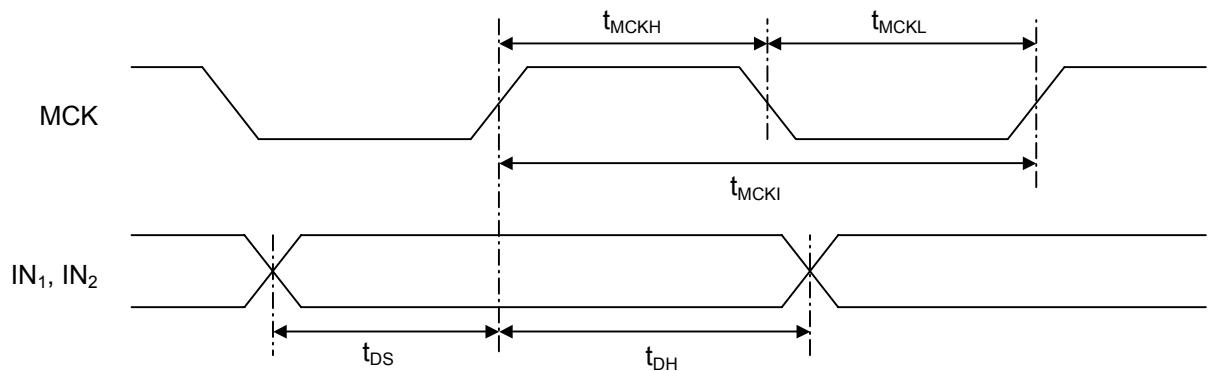
■ ELECTRICAL CHARACTERISTICS

(Ta=25°C, V_{DD}=V_{DDO}=2.0V, V_{SS}=V_{SSO}=0.0V, Load Impedance=32Ω, f_S=44.1kHz, unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V _{DD} Supply Voltage	V _{DD}		1.7	2.0	2.7	V
V _{DDO} Supply Voltage	V _{DDO}		1.7	2.0	V _{DD}	V
BPZ Driving Voltage	V _{BPZ}	load operating MCK=256f _S IN ₁ , IN ₂ =32f _S Duty50%	V _{DDO} /2-0.2	V _{DDO} /2	V _{DDO} /2+0.2	V
Output Driver High side Resistance	R _H	V _{OUT} =V _{DDO} -0.1V	-	1.5	2	Ω
Output Driver Low side Resistance	R _L	V _{OUT} =0.1V	-	1.5	2	Ω
Beep High side Current	I _{BH}	V _{OUT} =V _{DDO} -1V	20	50	150	uA
Beep Low side Current	I _{BL}	V _{OUT} =1V	20	50	150	uA
Operating Current At Standby	I _{ST}	Stopping MCK, IN ₁ , IN ₂ , BEEP	-	-	1	uA
Operating Current At no input signal	I _{DD}	No-load operating IN ₁ , IN ₂ =32f _S MCK=256f _S	-	0.05	0.1	mA
	I _{DDO}		-	0.6	1.2	
Input Voltage	V _{IH}		0.7V _{DD}	-	V _{DD}	V
	V _{IL}		0	-	0.3V _{DD}	V
Input Leakage Current	I _{LK}		-	-	±1	uA

■ TIMING CHARACTERISTICS

- Audio Signal Input

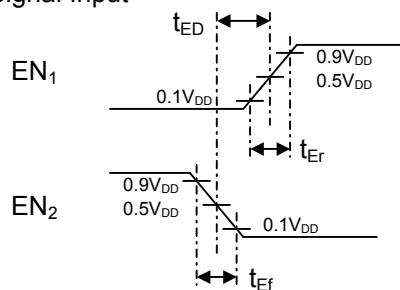


(Ta=25°C, V_{DD}=V_{DDO}=2.0V, V_{SS}=V_{SSO}=0.0V, unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
MCK Frequency	f _{MCKI}		8	-	25	MHz
MCK Pulse Width (H)	t _{MCKH}		12	-	-	ns
MCK Pulse Width (L)	t _{MCKL}		12	-	-	ns
IN ₁ ,IN ₂ Setup Time	t _{DS}		20	-	-	ns
IN ₁ ,IN ₂ Hold Time	t _{DH}		20	-	-	ns
BEEP Frequency	f _{BEEP}		0.1	-	20	kHz

Note 4) t_{MCKI} shows the cycle of the MCK signal.

- Output Control Signal Input



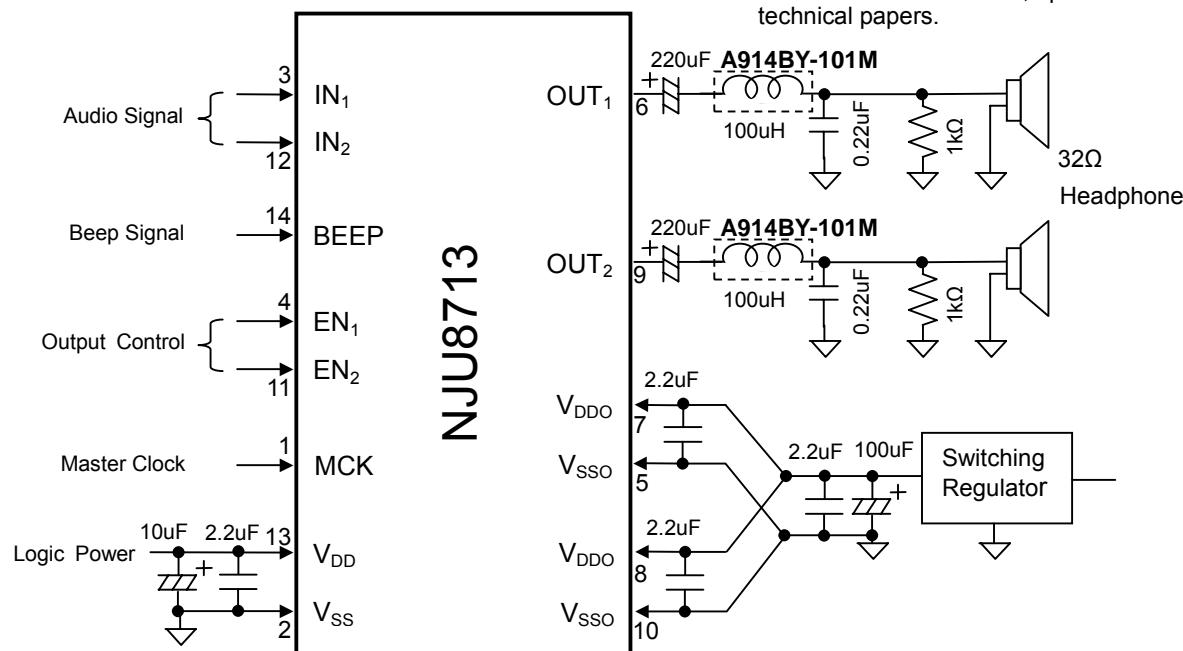
(Ta=25°C, V_{DD}=V_{DDO}=2.0V, V_{SS}=V_{SSO}=0.0V, unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Rise Time	t _{ER}		-	-	50	ns
Fall Time	t _{EF}		-	-	50	ns
Switching Time	t _{ED}				100	ns

Note 5) All timings are based on 30% and 70% voltage level of V_{DD}.

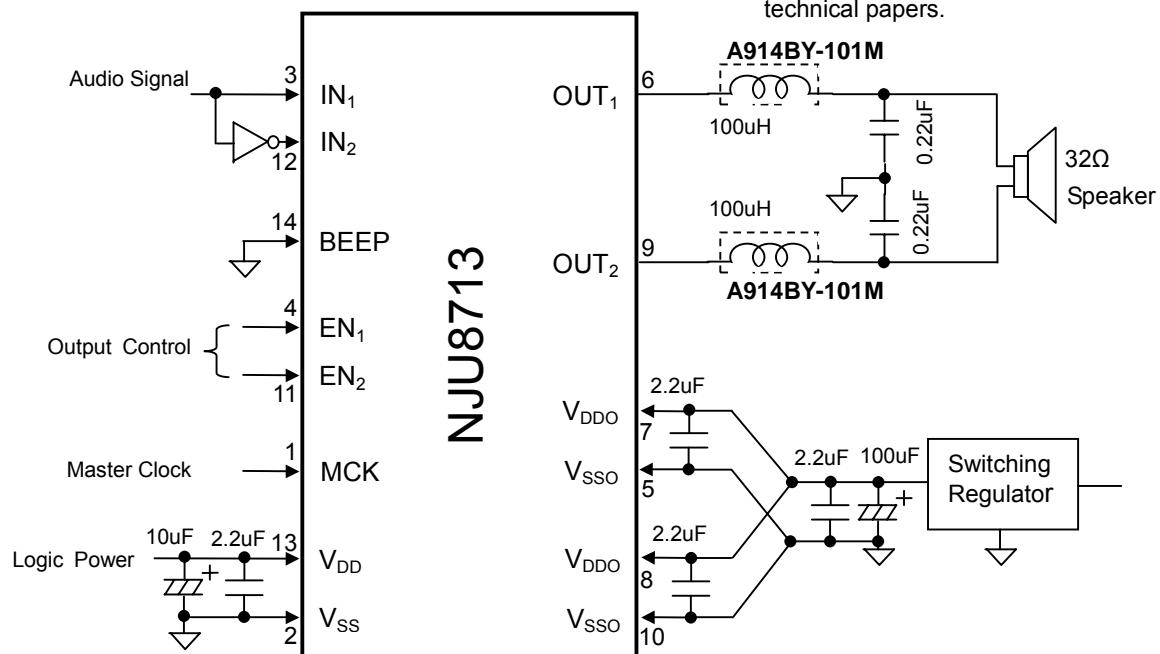
■ APPLICATION CIRCUIT

- Stereo OTL application example



• A914BY-101M is manufactured by TOKO, INC.
For further information, please refer to its technical papers.

- 1 channel BTL application example



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Note 6) De-coupling capacitors must be connected between each power supply pin and GND pin.

Note 7) The power supply for V_{DDO} requires fast driving response performance such as a switching regulator for T.H.D.

Note 8) The bigger capacitor value of external AC-coupling capacitors realize better low frequency response characteristics. In addition, ESR(Equivalent Series Resistance) should be low.

Note 9) The above circuit shows only application example and does not guarantee the any electrical characteristics. Therefore, please consider and check the circuit carefully to fit your application.

[CAUTION]
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