CY7C441
CY7C443

Clocked 512 x 9, 2K x 9 FIFOs

Features

- **High-speed, low-power, first-in first-out (FIFO) memories**
- **512 x 9 (CY7C441)**
- **2,048 x 9 (CY7C443)**
- **0.65 micron CMOS for optimum speed/power**
- **High-speed 83-MHz operation (12 ns read/write cycle time)**
- **Low power — I_{CC}=70 mA**
- **Fully asynchronous and simultaneous read and write operation**
- **Empty, Almost Empty, and Almost Full status flags**
- **TTL compatible**
- **Parity generation/checking**
- **Independent read and write enable pins**
- **Supports free-running 50% duty cycle clock inputs**
- **Center power and ground pins for reduced noise**
- **Width Expansion Capability**
- **Available in PLCC packages**

Functional Description

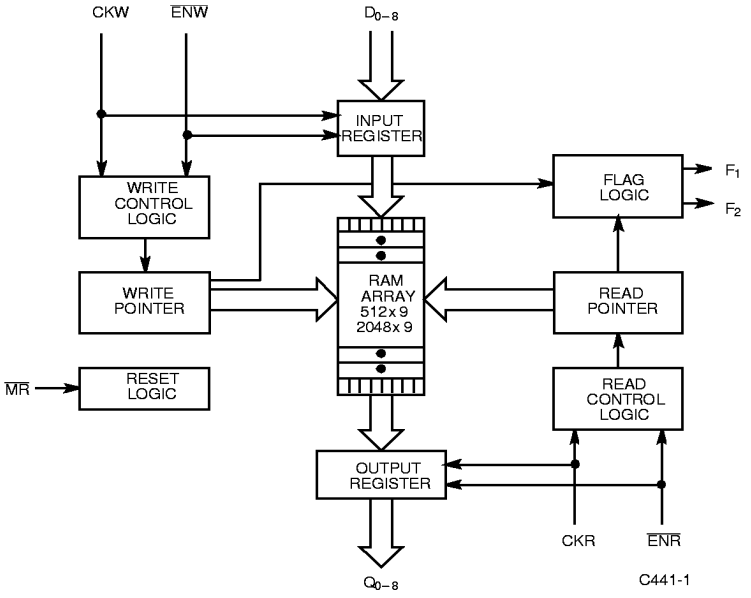
The CY7C441 and CY7C443 are high-speed, low-power, first-in first-out (FIFO) memories with clocked read and write interfaces. Both FIFOs are 9 bits wide. The CY7C441 has a 512 word by 9 bit memory array, while the CY7C443 has a 2048 word by 9 bit memory array. These devices provide solutions for a wide variety of data buffering needs, including high-speed data acquisition, multiprocessor interfaces, and communications buffering.

Both FIFOs have 9-bit input and output ports that are controlled by separate clock and enable signals. The input port is controlled by a free-running clock (CKW) and a write enable pin ($\overline{ENW}$). When $\overline{ENW}$ is asserted, data is written into the FIFO on the rising edge of the CKW signal. While $\overline{ENW}$ is held active, data is continually written into the FIFO on each CKW cycle. The output port is controlled in a similar manner by a free-running read clock (CKR) and a read enable pin ($\overline{ENR}$). The read (CKR) and write (CKW) clocks may be tied together for single-clock operation or the two clocks may be run independently for asynchronous read/write applications. Clock frequencies up to 83.3 MHz are acceptable.

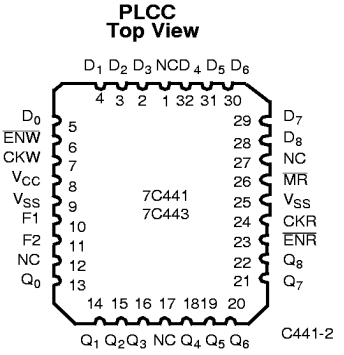
The CY7C441 and CY7C443 clocked FIFOs provide two status flag pins (F1 and F2). These flags are decoded to determine one of four states: Empty, Almost Empty, Intermediate, and Almost Full (*Table 1*). The flags are synchronous; i.e., change state relative to either the read clock (CKR) or the write clock (CKW). The Empty and Almost Empty states are updated exclusively by the CKR while Almost Full is updated exclusively by CKW. The synchronous flag architecture guarantees that the flags maintain their status for some minimum time.

The CY7C441 and the CY7C443 use center power and ground for reduced noise. Both configurations are fabricated using an advanced .65µm CMOS technology. Input ESD protection is greater than 2001V, and latch-up is prevented by reliable layout techniques and guard rings.

Logic Block Diagram



Pin Configuration



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Selection Guide

		7C441–12 7C443–12	7C441–14 7C443–14	7C441–20 7C443–20	7C441–30 7C443–30
Maximum Frequency (MHz)		83.3	71.4	50	33.3
Maximum Access Time (ns)		9	10	15	20
Minimum Cycle Time (ns)		12	14	20	30
Minimum Clock HIGH Time (ns)		5	6.5	9	12
Minimum Clock LOW Time (ns)		5	6.5	9	12
Minimum Data or Enable Set-Up (ns)		4	5	6	7
Minimum Data or Enable Hold (ns)		0	0	0	0
Maximum Flag Delay (ns)		9	10	15	20
Maximum Current (mA)	Commercial	140	140	120	100
	Military/Industrial	150	150	130	110

Selection Guide (continued)

	CY7C441	CY7C443
Density	512 x 9	2,048 x 9
Package	32-Pin PLCC	32-Pin PLCC

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–65°C to +150°C

Ambient Temperature with Power Applied.....–55°C to +125°C

Supply Voltage to Ground Potential.....–0.5V to +7.0V

DC Input Voltage.....–3.0V to +7.0V

Output Current into Outputs (LOW).....20 mA

Static Discharge Voltage ..... > 2001V (per MIL-STD-883, Method 3015)

Latch-Up Current..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	–40°C to +85°C	5V ± 10%

Pin Definitions

Signal Name	I/O	Description
D_{0-8}	I	Data Inputs: when the FIFO is not full and $\overline{ENW}$ is active, CKW (rising edge) writes data (D_0 – D_8) into the FIFO's memory
Q_{0-8}	O	Data Outputs: when the FIFO is not empty and $\overline{ENR}$ is active, CKR (rising edge) reads data (Q_0 – Q_8) out of the FIFO's memory
$\overline{ENW}$	I	Enable Write: enables the CKW input
$\overline{ENR}$	I	Enable Read: enables the CKR input
CKW	I	Write Clock: the rising edge clocks data into the FIFO when $\overline{ENW}$ is LOW and updates the Almost Full flag state
CKR	I	Read Clock: the rising edge clocks data out of the FIFO when $\overline{ENR}$ is LOW and updates the Almost Empty and Empty flag states
F1	O	Flag 1: is used in conjunction with Flag 2 to decode which state the FIFO is in (see *Table 1*)
F2	O	Flag 2: is used in conjunction with Flag 1 to decode which state the FIFO is in (see *Table 1*)
$\overline{MR}$	I	Master Reset: resets the device to an empty condition

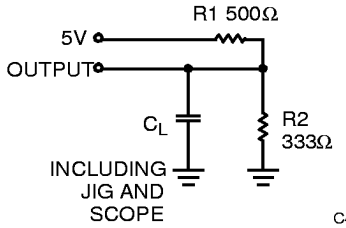
Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		7C441–12 7C443–12 Min.	7C441–12 7C443–12 Max.	7C441–14 7C443–14 Min.	7C441–14 7C443–14 Max.	7C441–20 7C443–20 Min.	7C441–20 7C443–20 Max.	7C441–30 7C443–30 Min.	7C441–30 7C443–30 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –2.0 mA		2.4		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage			–0.5	0.8	–0.5	0.8	–0.5	0.8	–0.5	0.8	V
I_{IX}	Input Leakage Current	V_{CC} = Max., GND ≤ V_I ≤ V_{CC}		–10	+10	–10	+10	–10	+10	–10	+10	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = GND		–90		–90		–90		–90		mA
I_{CC1}[2]	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		140		140		120		100	mA
			Mil/Ind		150		150		130		110	mA
I_{CC2}[3]	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		70		70		70		70	mA
			Mil/Ind		80		80		80		80	mA
I_{SB}[4]	Standby Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		30		30		30		30	mA
			Mil/Ind		30		30		30		30	mA

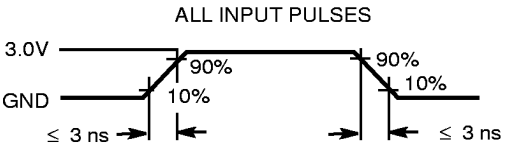
Capacitance[5]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF

AC Test Loads and Waveform[6,7]

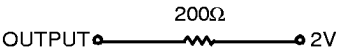


C441-4



C441-5

Equivalent to: THÉVENIN EQUIVALENT



Notes:

1. Test no more than one output at a time and do not test any output for more than one second.
2. Input signals switch from 0V to 3V with a rise/fall time of 3 ns or less, clocks and clock enables switch at maximum frequency (f_{MAX}), while data inputs switch at $f_{MAX}/2$. Outputs are unloaded.
3. Input signals switch from 0V to 3V with a rise/fall time less than 3 ns, clocks and clock enables switch at 20 MHz, while the data inputs switch at 10 MHz. Outputs are unloaded.
4. All inputs signals are connected to V_{CC}. All outputs are unloaded. Read and write clocks switch at maximum frequency (f_{MAX}).
5. Tested initially and after any design or process changes that may affect these parameters.
6. C_L = 30 pF for all AC parameters.
7. All AC measurements are referenced to 1.5V.

Switching Characteristics Over the Operating Range[8]

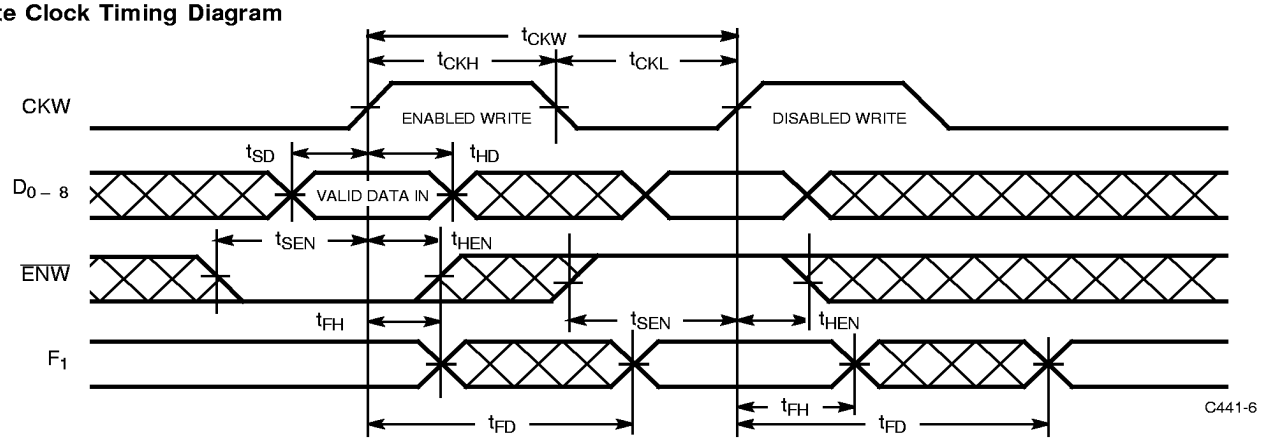
Parameter	Description	7C441–12 7C443–12		7C441–14 7C443–14		7C441–20 7C443–20		7C441–30 7C443–30		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{CKW}	Write Clock Cycle	12		14		20		30		ns
t_{CKR}	Read Clock Cycle	12		14		20		30		ns
t_{CKH}	Clock HIGH	5		6.5		9		12		ns
t_{CKL}	Clock LOW	5		6.5		9		12		ns
t_A[9]	Data Access Time		9		10		15		20	ns
t_{OH}	Previous Output Data Hold After Read HIGH	0		0		0		0		ns
t_{FH}	Previous Flag Hold After Read/Write HIGH	0		0		0		0		ns
t_{SD}	Data Set-Up	4		5		6		7		ns
t_{HD}	Data Hold	0		0		0		0		ns
t_{SEN}	Enable Set-Up	4		5		6		7		ns
t_{HEN}	Enable Hold	0		0		0		0		ns
t_{FD}	Flag Delay		9		10		15		20	ns
t_{SKEW1}[10]	Opposite Clock After Clock	0		0		0		0		ns
t_{SKEW2}[11]	Opposite Clock Before Clock	12		14		20		30		ns
t_{PMR}	Master Reset Pulse Width ($\overline{MR}$ LOW)	12		14		20		30		ns
t_{SCMR}	Last Valid Clock LOW Set-Up to $\overline{MR}$ LOW	0		0		0		0		ns
t_{OHMR}	Data Hold From $\overline{MR}$ LOW	0		0		0		0		ns
t_{MRR}	Master Reset Recovery ($\overline{MR}$ HIGH Set-Up to First Enabled Write/Read)	12		14		20		30		ns
t_{MRF}	$\overline{MR}$ HIGH to Flags Valid		12		14		20		30	ns
t_{AMR}	$\overline{MR}$ HIGH to Data Outputs LOW		12		14		20		30	ns

Notes:

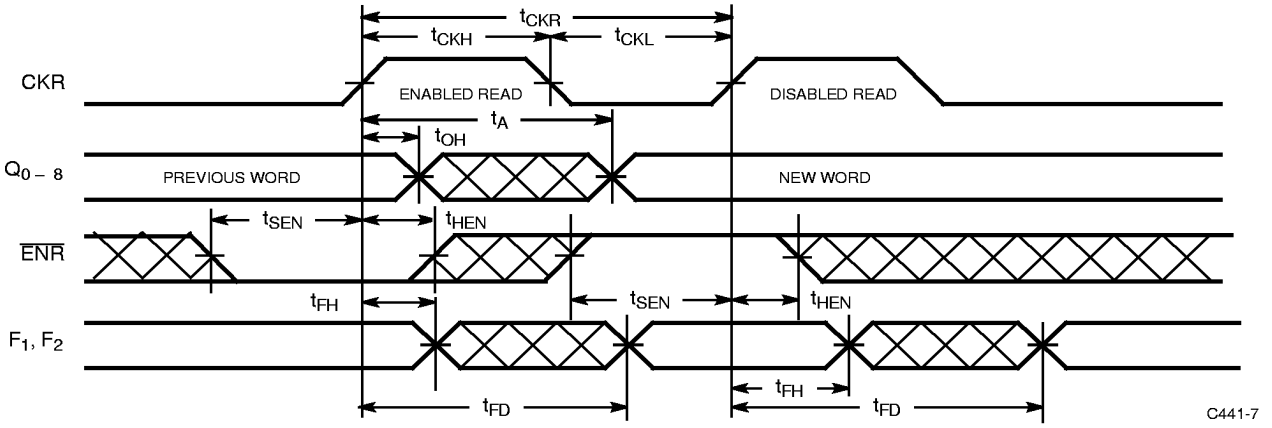
8. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, and output loading as shown in the AC Test Loads and Waveforms and capacitance as in Note 6, unless otherwise specified.
9. Access time includes all data outputs switching simultaneously.
10. t_{SKEW1} is the minimum time an opposite clock can occur after a clock and still be guaranteed not to be included in the current clock cycle (for purposes of flag update). If the opposite clock occurs less than t_{SKEW1} after the clock, the decision of whether or not to include the opposite clock in the current clock cycle is arbitrary. *Note*: The opposite clock is the signal to which a flag is not synchronized; i.e., CKW is the opposite clock for Empty and Almost Empty flags, CKR is the opposite clock for the Almost Full flag. The clock is the signal to which a flag is synchronized; i.e., CKW is the clock for the Almost Full flag, CKR is the clock for Empty and Almost Empty flags.
11. t_{SKEW2} is the minimum time an opposite clock can occur before a clock and still be guaranteed to be included in the current clock cycle (for purposes of flag update). If the opposite clock occurs less than t_{SKEW2} before the clock, the decision of whether or not to include the opposite clock in the current clock cycle is arbitrary. See Note 10 for definition of clock and opposite clock.

Switching Waveforms

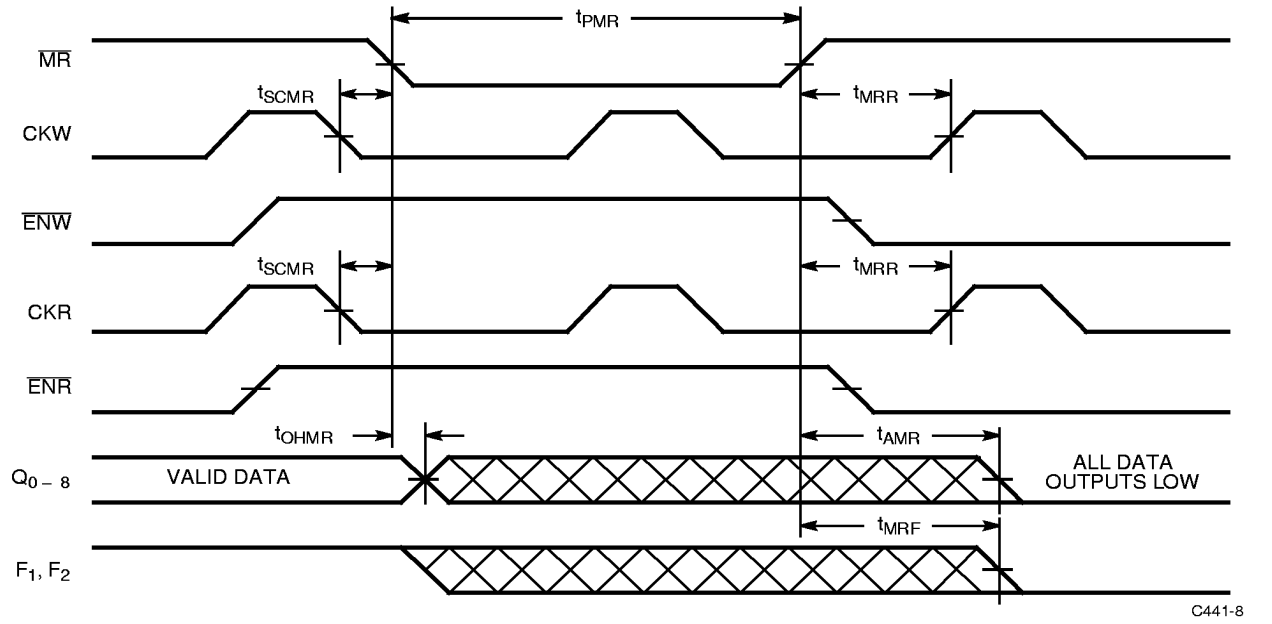
Write Clock Timing Diagram



Read Clock Timing Diagram

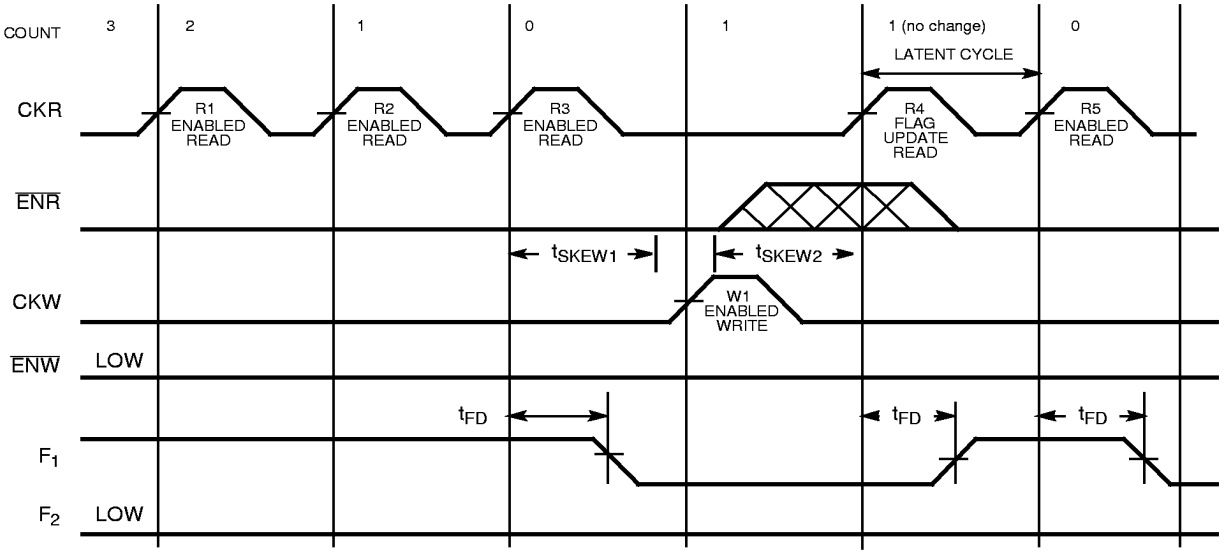


Master Reset Timing Diagram[12, 13, 14, 15]



Switching Waveforms (continued)

Read to Empty Timing Diagram[16, 17, 18]



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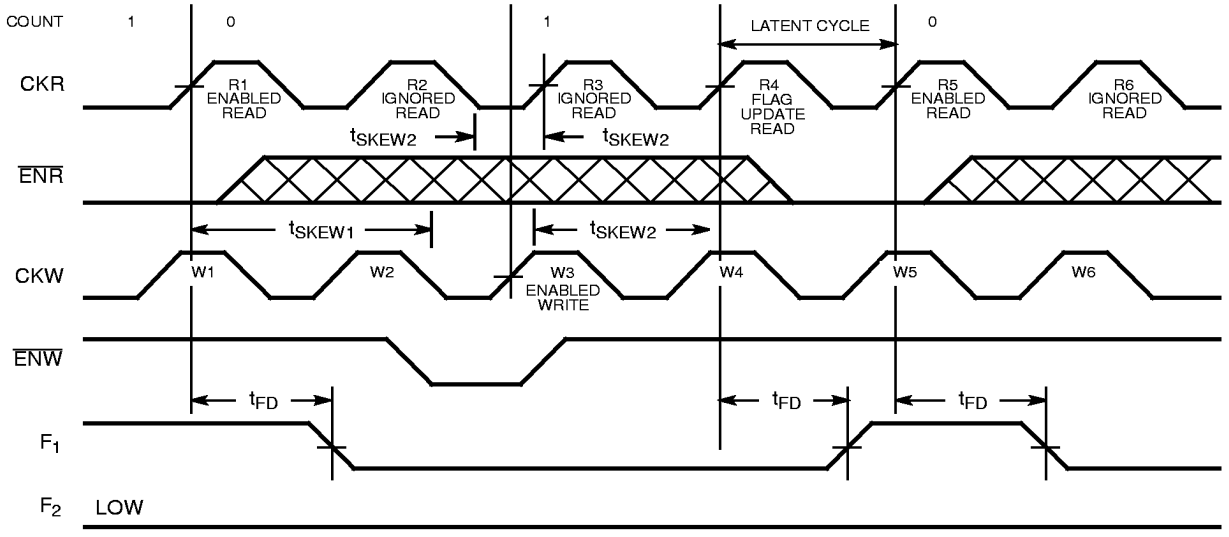
Read to Empty Timing Diagram with Free-Running Clocks[16, 17, 19]



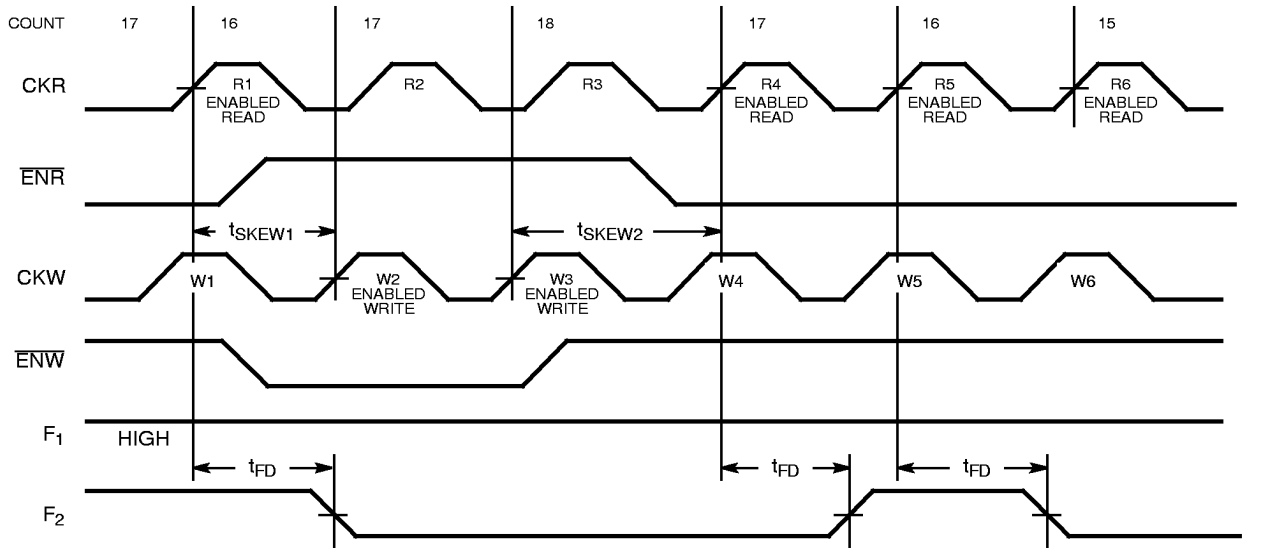
C441-9

Notes:

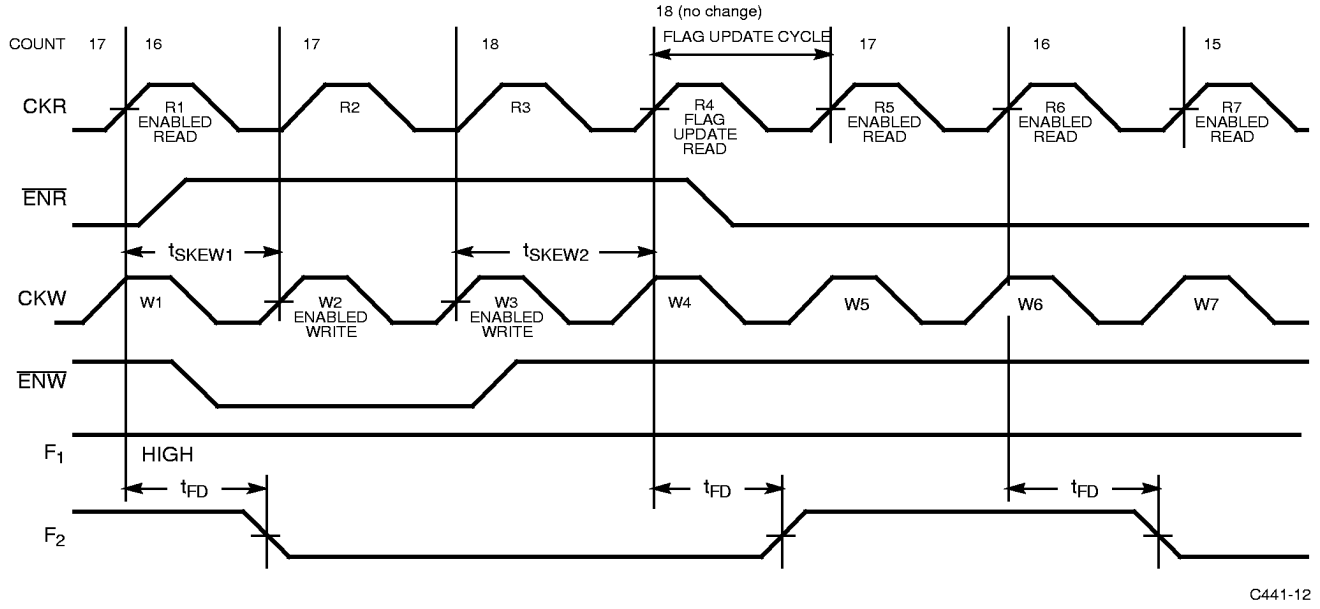
12. $\overline{ENW}$ or CKW must be inactive while $\overline{MR}$ is LOW.
13. $\overline{ENR}$ or CKR must be inactive while $\overline{MR}$ is LOW.
14. All data outputs (Q_{0-8}) go LOW as a result of the rising edge of $\overline{MR}$.
15. In this example, Q_{0-8} will remain valid until t_{OHMR} if the first read shown did not occur or if the read occurred soon enough such that the valid data was caused by it.
16. "Count" is the number of words in the FIFO.
17. CKR is clock and CKW is opposite clock.
18. R3 updates the flags to the Empty state by bringing F1 LOW. Because W1 occurs greater than t_{SKEW1} after R3, R3 does not recognize W1 when updating flag status. But because W1 occurs greater than t_{SKEW2} before R4, R4 includes W1 in the flag update and therefore updates the FIFO to the Almost Empty state. It is important to note that R4 is a latent cycle; i.e., it only updates the flag status, regardless of the state of $\overline{ENR}$. It does not change the count or the FIFO's data outputs.
19. R2 is ignored because the FIFO is empty (count = 0). It is important to note that R3 is also ignored because W3, the first enabled write after empty, occurs less than t_{SKEW2} before R3. Therefore, the FIFO still appears empty when R3 occurs. Because W3 occurs greater than t_{SKEW2} before R4, R4 includes W3 in the flag update.

Switching Waveforms (continued)

Read to Almost Empty Timing Diagram with Free-Running Clocks[16, 17]



Read to Almost Empty Timing Diagram with Read Flag Update Cycle and Free-Running Clocks[16, 17, 20, 21]

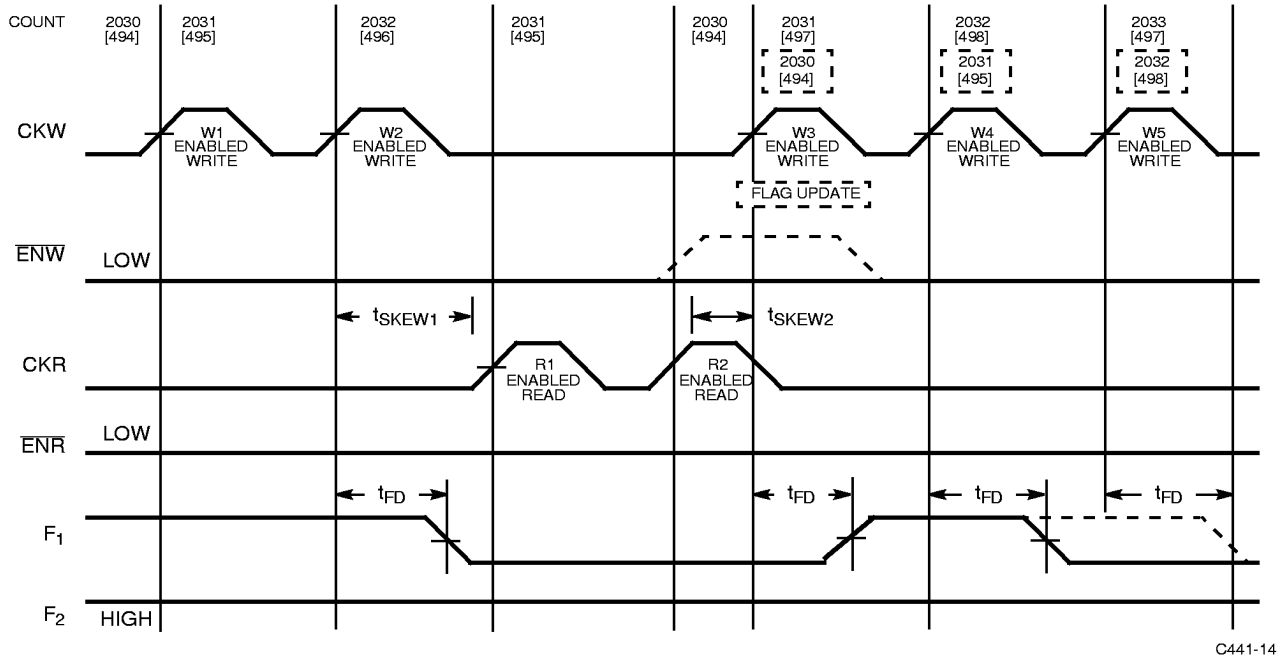


Notes:

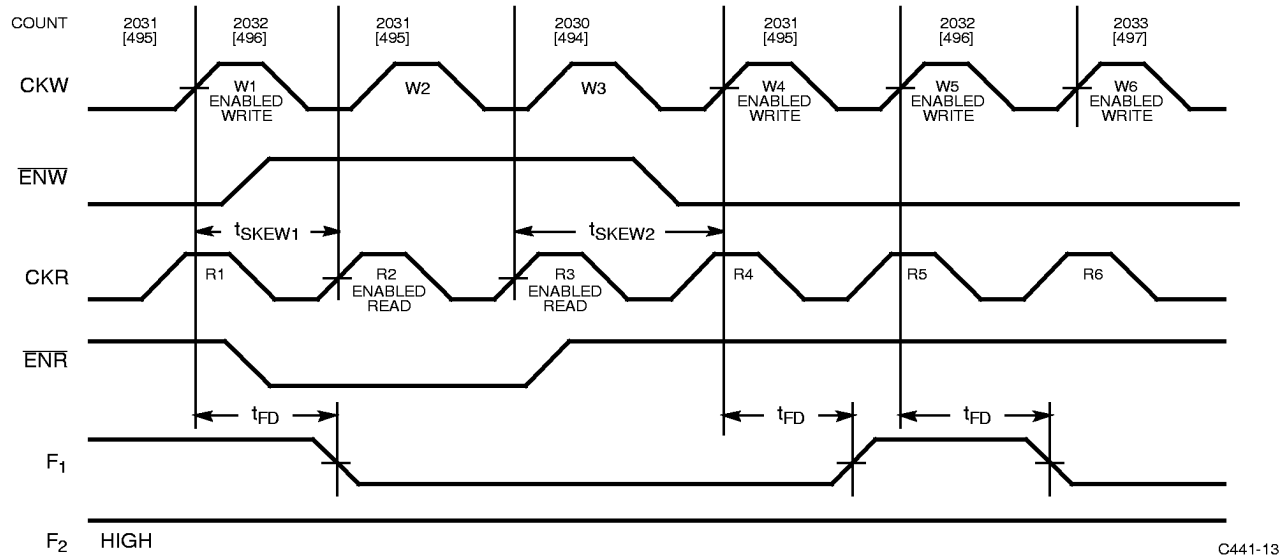
20. R4 only updates the flag status. It does not affect the count because $\overline{ENR}$ is HIGH.
21. When making the transition from Almost Empty to Intermediate, the count must increase by two (16 ➧18; two enabled writes: W2, W3) before a read (R4) can update flags to the Intermediate state.

Switching Waveforms (continued)

Write to Almost Full Timing Diagram[16, 22, 23, 24, 25]



Write to Almost Full Timing Diagram with Free-Running Clocks[16, 22, 23]

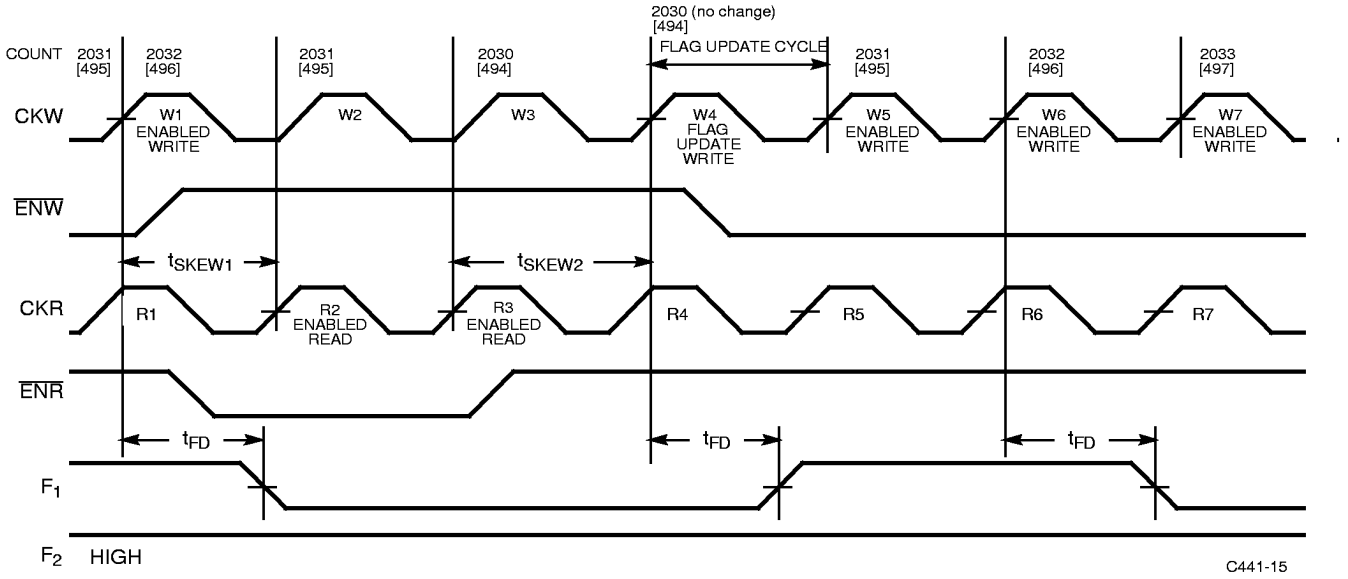


Notes:

22. CKW is clock and CKR is opposite clock.
23. Count = 2032 indicates Almost Full for CY7C443 and count = 496 indicates Almost Full for CY7C441. Values for the CY7C441 count are shown in brackets.
24. The dashed lines show W3 as flag update write rather than an enabled write because $\overline{ENW}$ is deasserted.
25. W2 updates the flags to the Almost Full state by bringing F1 LOW. Because R1 occurs greater than t_{SKEW1} after W2, W2 does not recognize R1 when updating the flag status. W3 includes R2 in the flag update because R2 occurs greater than t_{SKEW2} before W3. Note that W3 does not have to be enabled to update flags.
26. When making the transition from Almost Full to Intermediate, the count must decrease by two (2032 ➧ 2030; two enabled reads: R2, R3) before a write (W4) can update flags to Intermediate state.

Switching Waveforms (continued)

Write to Almost Full Timing Diagram with Write Flag Update Cycle and Free-Running Clocks[16, 22, 23, 26]



Architecture

The CY7C441/443 consist of an array of 512/2048 words of 9 bits each (implemented by an array of dual-port RAM cells), a read pointer, a write pointer, control signals (CKR, CKW, $\overline{ENR}$, $\overline{ENW}$, $\overline{MR}$), and flags (F1, F2).

Resetting the FIFO

Upon power-up, the FIFO must be reset with a Master Reset ($\overline{MR}$) cycle. This causes the FIFO to enter the Empty condition signified by both flags F1 and F2 being LOW. All data outputs (Q_{0-8}) go LOW at the rising edge of $\overline{MR}$. In order for the FIFO to reset to its default state, a falling edge must occur on $\overline{MR}$ and the user must not read or write while $\overline{MR}$ is LOW (unless $\overline{ENR}$ and $\overline{ENW}$ are HIGH). Upon completion of the Master Reset cycle, all data outputs will go LOW t_{AMR} after $\overline{MR}$ is deasserted. F1 and F2 are guaranteed to be valid t_{MRF} after $\overline{MR}$ is taken HIGH.

FIFO Operation

When the $\overline{ENW}$ signal is active (LOW), data on the D_{0-8} pins is written into the FIFO on each rising edge of the CKW signal. Similarly, when the $\overline{ENR}$ signal is active, data in the FIFO memory will be presented on the Q_{0-8} outputs. New data will be presented on each rising edge of CKR while $\overline{ENR}$ is active. $\overline{ENR}$ must set up t_{SEN} before CKR for it to be a valid read. $\overline{ENW}$ must occur t_{SEN} before CKW for it to be a valid write.

The FIFO contains overflow circuitry to disallow additional writes when the FIFO is full, and underflow circuitry to disallow additional reads when the FIFO is empty. An empty FIFO maintains the data of the last valid read on its Q_{0-8} outputs even after additional reads occur.

Flag Operation

The CY7C441/3 provide two flags, F1 and F2, which are used to decode four FIFO states (see *Table 1*). All flags are synchronous, meaning that the change of states is relative to one of the clocks (CKR or CKW, as appropriate; see *Figure 1*). The synchronous architecture guarantees some minimum valid time for the flags.

The Empty and Almost Empty flag states are exclusively updated by each rising edge of the read clock (CKR). For example, when the FIFO contains 1 word, the next read (rising edge of CKR while $\overline{ENR}$=LOW) causes the F1 and F2 pins to output a state signifying the Empty condition. The Almost Full flag is updated exclusively by the write clock (CKW). For example, if the CY7C443 FIFO contains 2031 words (2032 words or greater indicates Almost Full in the CY7C443), the next write (rising edge of CKW while $\overline{ENW}$=LOW) causes the F1 and F2 pins to output the Almost Full state.

Table 1. Flag Truth Table

F1	F2	State	CY7C441 Number of Words in FIFO	CY7C443 Number of Words in FIFO
0	0	Empty	0	0
1	0	Almost Empty	1 – 16	1 – 16
1	1	Intermediate Range	17 – 495	17 – 2031
0	1	Almost Full or Full	496 – 512	2032 – 2048

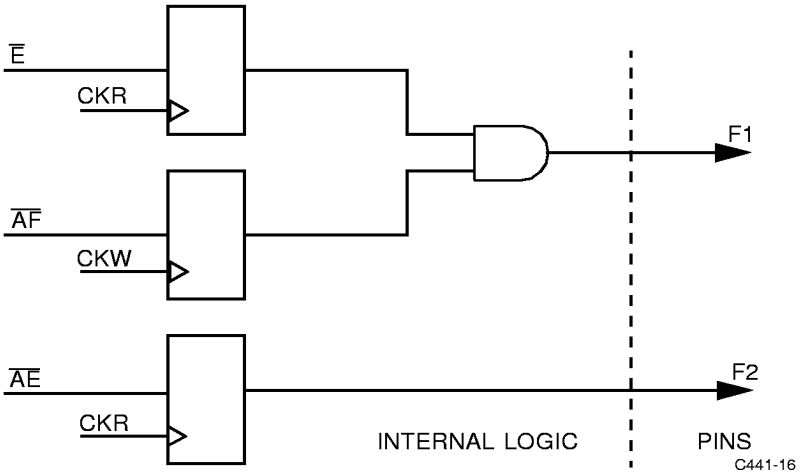


Figure 1. Flag Logic Diagram

Flag Operation (continued)

Since the flags denoting emptiness (Empty, Almost Empty) are only updated by CKR and the Almost Full flag is only updated by the CKW, careful attention must be given to the flag operation. The user must be aware that if a flag boundary (Empty, Almost Empty, and Almost Full) is crossed due to an operation from a clock that the flag is not synchronized to (i.e.,CKR does not effect Almost Full), a flag update is necessary to represent the FIFO's new state. This signal to which a flag is not synchronized will be referred to as the opposite clock (CKW is opposite clock for Empty and Almost Empty flags; CKR is the opposite clock for the Almost Full flag).

Until the flag update cycle is executed, the synchronous flags do not show the true state of the FIFO. For example, if 2,040 writes are performed to an empty CY7C443 without a single read, F1 and F2 will still exhibit an Empty flag. This is because F2 is exclusively updated by the CKR, therefore, a single read (flag update cycle) is necessary to update flags to Almost Full state. It should be noted that this flag update read does not require $\overline{ENR}$ = LOW, so a free-running read clock will initiate the flag update cycle.

When updating the flags, the CY7C441/443 decide whether or not the opposite clock was recognized when a clock updates the flag. For example, if a write occurs at least t_{SKEW1} after a read when updating the Empty flag, the write is guaranteed not to be included when CKR updates the flag. If a write occurs at least t_{SKEW2} before a read, the write is guaranteed to be included when CKR updates the flag. If a write occurs within t_{SKEW1}/t_{SKEW2} after or before CKR, then the decision of whether or not to include the write when the flag is updated by CKR is arbitrary.

The update cycle for non-boundary flags (Almost Empty, Almost Full) is different from that used to update the boundary flag (Empty). Both operations are described below.

Boundary Flag (Empty)

The Empty flag is synchronized to the CKR signal. The Empty flag can only be updated by a clock pulse on the CKR pin. An empty FIFO that is written to will be described with an Empty flag state until a clock pulse is presented on the CKR pin. When making the transition from Empty to Almost Empty (or Empty to Intermediate or Empty to Almost Full), a clock cycle on the CKR is necessary to update the flags to the current state. Such a state (flags displaying empty even though data has been written to the FIFO) would require two read cycles to read data out of FIFO. The first read serves only to update the flags to the Almost Empty, Intermediate, or Almost Full state, and the second read outputs the data. This first read cycle is known as the latent or flag update cycle because it does not affect the data in the FIFO or the count (number of words in FIFO). It simply deasserts the Empty flag. The flags are updated regardless of the $\overline{ENR}$ state. Therefore the update occurs even when $\overline{ENR}$ is deasserted (HIGH) so that a valid read is not necessary to update the flags to correctly describe the FIFO. With a free-running clock connected to CKR, the flag updates with each cycle. *Table 2* shows sample operations that update the Empty flag.

Although a Full flag is not supplied externally on the CY7C441/CY7C443, a Full flag exists internally. The operation of the FIFO at the Full boundary is analogous to its operation at the Empty boundary. See the text section "Boundary Flags (Full)" in the CY7C451/CY7C453 datasheet.

Non-Boundary Flags (Almost Empty, Almost Full)

The flag status pins, F1 and F2, exhibit the Almost Empty status when both the CY7C441 and the CY7C443 contain 16 words or less. The Almost Full Flag becomes active when the FIFO contains 16 or less empty locations. The CY7C441 becomes Almost Full when it contains 496 words. The CY7C443 becomes Almost Full when it contains 2032 words. The Almost Empty flag (like the Empty flag) is synchronous to the CKR signal, whereas the Almost Full flag is synchronous to the CKW signal. Non-boundary flags employ flag update cycles similar to the boundary flag latent cycles in order to update the FIFO state. For example, if the FIFO just reaches the Almost Empty state (16 words) and then two words are written, a read clock (CKR) will be required to update the flags to the Intermediate state. However, unlike the boundary (Empty) flag's update cycle, the state of the enable pin ($\overline{ENR}$ in this case) affects the operation. Therefore, ENR set-up (t_{SEN}) and hold (t_{HEN}) times must be met. If $\overline{ENR}$ is asserted ($\overline{ENR}$=LOW) during the latent cycle, the count and data update in addition to F1 and F2. If $\overline{ENR}$ is not active ($\overline{ENR}$=1) during the flag update cycle, only the flag is updated.

The same principles apply for updating the flags when a transition from the Almost Full to the Intermediate state occurs. If the CY7C443 just reaches the Almost Full state (2032 words) and then two words are read, a write clock (CKW) will be required to update the flag to the Intermediate state. If $\overline{ENW}$ is LOW during the flag update cycle, the count and data update in addition to the flags. If $\overline{ENW}$ is HIGH, only the flag is updated. Therefore, $\overline{ENW}$ set-up (t_{SEN}) and hold (t_{HEN}) times must be met. *Tables 3* and *4* show examples for a sequence of operations that affect the Almost Empty and Almost Full flags, respectively.

Width Expansion

The CY7C441/3 can be expanded in width to provide word width greater than 9 in increments of 9. During width expansion mode, all control inputs are common. When the FIFO is being read near the Empty boundary, it is important to note that both sets of flags should be checked to see if they have been updated to the Not Empty condition on all devices.

Checking all sets of flags is critical so that data is not read from the FIFOs "staggered" by one clock cycle. This situation could occur when the first write to an empty FIFO and a read are very close together. If the read occurs less than t_{SKEW2} after the first write to two width expanded devices (A and B), device A may go Almost Empty (read recognized as flag update) while device B stays Empty (read ignored).The first write occurs because a read within $t_{SKEW}2$ of the first write is only guaranteed to be either recognized or ignored, but which of the two is not guaranteed. The next read cycle outputs the first half of the first word on device A while device B updates its flags to Almost Empty. Subsequent reads will continue to output "staggered" data assuming more data has been written to the FIFOs.

In the width expansion configuration, any of the devices' flags may be monitored for the composite Almost Full status.

Table 2. Empty Flag Operation Example [27]

Status Before Operation						Status After Operation			
Current State of FIFO	F1	F2	Number of Words in FIFO	Operation	Next State of FIFO	F1	F2	Number of Words in FIFO	Comments
Empty	0	0	0	Write ($\overline{ENW}$ = LOW)	Empty	0	0	1	Write
Empty	0	0	1	Write ($\overline{ENW}$ = LOW)	Empty	0	0	2	Write
Empty	0	0	2	Read ($\overline{ENR}$ = HIGH)	AE	1	0	2	Flag Update
AE	1	0	2	Read ($\overline{ENR}$ = LOW)	AE	1	0	1	Read
AE	1	0	1	Read ($\overline{ENR}$ = LOW)	Empty	0	0	0	Read (Transition for Almost Empty to Empty)
Empty	0	0	0	Write ($\overline{ENW}$ = LOW)	Empty	0	0	1	Write
Empty	0	0	1	Read ($\overline{ENR}$ = X)	AE	1	0	1	Flag Update
AE	1	0	1	Read ($\overline{ENR}$ = LOW)	Empty	0	0	0	Read (Transition from Almost Empty to Empty)

Table 3. Almost Empty Flag Operation Example[27]

Status Before Operation						Status After Operation			
Current State of FIFO	F1	F2	Number of Words in FIFO	Operation	Next State of FIFO	F1	F2	Number of Words in FIFO	Comments
AE	1	0	16	Write ($\overline{ENW}$ = LOW)	AE	1	0	17	Write
AE	1	0	17	Write ($\overline{ENW}$ = LOW)	AE	1	0	18	Write
AE	1	0	18	Read ($\overline{ENR}$ = LOW)	Intermediate	1	1	17	Flag Update and Read
Intermediate	1	1	17	Read ($\overline{ENR}$ = LOW)	AE	1	0	16	Read (Transition from Intermediate to Almost Empty)
AE	1	0	16	Read ($\overline{ENR}$ = HIGH)	AE	1	0	16	Ignored Read

Note:
27. Applies to both the CY7C441 and CY7C443 operations.

Table 4. Almost Full Flag Operation Example[28,29]

Status Before Operation						Next State of FIFO	Status After Operation				
Current State of FIFO	F1	F2	Number of Words in FIFO CY7C441	Number of Words in FIFO CY7C443	Operation		F1	F2	Number of Words in FIFO CY7C441	Number of Words in FIFO CY7C443	Comments
AF	0	1	496	2032	Read ($\overline{ENR}$=LOW)	AF	0	1	495	2031	Read
AF	0	1	495	2031	Read ($\overline{ENR}$=LOW)	AF	0	1	494	2030	Read
AF	0	1	494	2030	Write ($\overline{ENW}$=HIGH)	Intermediate	1	1	494	2030	Flag Update
Intermediate	1	1	494	2030	Write ($\overline{ENW}$=LOW)	Intermediate	1	1	495	2031	Write
Intermediate	1	1	495	2031	Write ($\overline{ENW}$=LOW)	AF	0	1	496	2032	Write (Transition from Intermediate to Almost Full)

Note:
28. The CY7C441 Almost Full state is represented by 496 or more words.
29. The CY7C443 Almost Full state is represented by 2032 or more words.

Ordering Information

512x9 Clocked FIFO

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C441–12JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C441–12JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
14	CY7C441–14JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C441–14JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
20	CY7C441–20JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C441–20JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
30	CY7C441–30JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C441–30JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial

2Kx9 Clocked FIFO

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C443–12JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C443–12JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
14	CY7C443–14JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C443–14JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
20	CY7C443–20JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C443–20JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
30	CY7C443–30JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C443–30JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial

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Package Diagrams

32-Lead Plastic Leaded Chip Carrier J65