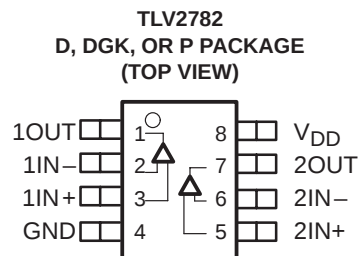


TLV2780, TLV2781, TLV2782, TLV2783, TLV2784, TLV2785, TLV278xA FAMILY OF 1.8 V HIGH-SPEED RAIL-TO-RAIL INPUT/OUTPUT OPERATIONAL AMPLIFIERS WITH SHUTDOWN

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- Supply Voltage Range . . . 1.8 V to 3.6 V
- Rail-to-Rail Input/Output
- High Bandwidth . . . 8 MHz
- High Slew Rate . . . 4.8 V/ μ s
- V_{ICR} Exceeds Rails . . . -0.2 V to $V_{DD} + 0.2$
- Supply Current . . . 650 μ A/Channel
- Input Noise Voltage . . . 9 nV/ $\sqrt{\text{Hz}}$ at 10 kHz
- Specified Temperature Range
 - 0°C to 70°C . . . Commercial Grade
 - -40°C to 125°C . . . Industrial Grade
- Ultra-Small Packaging
- Universal Op Amp EVM



description

The TLV278x single supply operational amplifiers provide rail-to-rail input and output capability. The TLV278x takes the minimum operating supply voltage down to 1.8 V over the extended industrial temperature range (-40°C to 125°C) while adding the rail-to-rail output swing feature. The TLV278x also provides 8 MHz bandwidth from only 650 μ A of supply current. The maximum recommended supply voltage is 3.6 V, which allows the devices to be operated from (± 1.8 V supplies down to ± 0.9 V) two rechargeable cells.

The combination of wide bandwidth, low noise, and low distortion makes it ideal for high speed and high resolution data converter applications. Its high output drive and bandwidth means that it is also suitable for video line driving applications.

All members are available in PDIP, SOIC, and the newer, smaller SOT-23 (singles), MSOP (duals), and TSSOP (quads).

FAMILY PACKAGE TABLE

DEVICE	NO. OF CHANNELS	PACKAGE TYPES					SHUTDOWN	UNIVERSAL EVM BOARD
		PDIP	SOIC	SOT-23	TSSOP	MSOP		
TLV2780 [†]	1	8	8	6	—	—	Yes	Refer to the EVM Selection Guide (Lit # SLOU060)
TLV2781 [†]	1	8	8	5	—	—	—	
TLV2782	2	8	8	—	—	8	—	
TLV2783	2	14	14	—	—	10	Yes	
TLV2784 [†]	4	14	14	—	14	—	—	
TLV2785 [†]	4	16	16	—	16	—	Yes	

[†] This device is in the Product Preview stage of development. Contact the local TI sales office for more information.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

This document contains information on products in more than one phase of development. The status of each device is indicated on the page(s) specifying its electrical characteristics.

**TEXAS
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TLV2780, TLV2781, TLV2782, TLV2783, TLV2784, TLV2785, TLV278xA

FAMILY OF 1.8 V HIGH-SPEED RAIL-TO-RAIL INPUT/OUTPUT

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TLV2780 and TLV2781 AVAILABLE OPTIONS

T _A	V _{IOmax} AT 25°C	PACKAGED DEVICES			
		SMALL OUTLINE (D) [†]	SOT-23		PLASTIC DIP (P)
			(DBV) [‡]	SYMBOL	
0°C to 70°C	3000 µV	TLV2780CD TLV2781CD	TLV2780CDBV TLV2781CDBV	VAOC VAPC	—
-40°C to 125°C		TLV2780ID TLV2781ID	TLV2780IDBV TLV2781IDBV	VAOI VAPI	TLV2780IP TLV2781IP

[†] This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., TLV2780CDR).

[‡] This package is only available taped and reeled. For standard quantities (3,000 pieces per reel), add a R suffix (i.e., TLV2780CDBVR). For smaller quantities (250 pieces per mini-reel), add a T suffix to the part number (e.g. TLV2780CDBVT).

TLV2782 and TLV2783 AVAILABLE OPTIONS

T _A	V _{IO} max AT 25°C	PACKAGED DEVICES						
		SMALL OUTLINE† (D)	MSOP				PLASTIC DIP (N)	PLASTIC DIP (P)
			(DGK)†	SYMBOL	(DGS)†	SYMBOL		
0°C to 70°C	3000 μV	TLV2782CD TLV2783CD	TLV2782CDGK —	xxTIAAI —	— TLV2783CDGS	— xxTIAAK	— —	— —
−40°C to 125°C	3000 μV	TLV2782ID TLV2783ID	TLV2782IDGK —	xxTIAAJ —	— TLV2783IDGS	— xxTIAAL	— TLV2783IN	TLV2782IP —
	2000 μV	TLV2782AID TLV2783AID	— —	— —	— —	— —	— —	— —

[†] This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., TLV2782CDR).

TLV2784 and TLV2785 AVAILABLE OPTIONS

T _A	V _{IOmax} AT 25°C	PACKAGED DEVICES		
		SMALL OUTLINE (D)	PLASTIC DIP (N)	TSSOP [†] (PW)
0°C to 70°C	3000 µV	TLV2784CD TLV2785CD	—	TLV2784CPW TLV2785CPW
-40°C to 125°C	3000 µV	TLV2784ID TLV2785ID	TLV2784IN TLV2785IN	TLV2784IPW TLV2785IPW
	2000 µV	TLV2784AID TLV2785AID	— —	TLV2784AIPW TLV2785AIPW

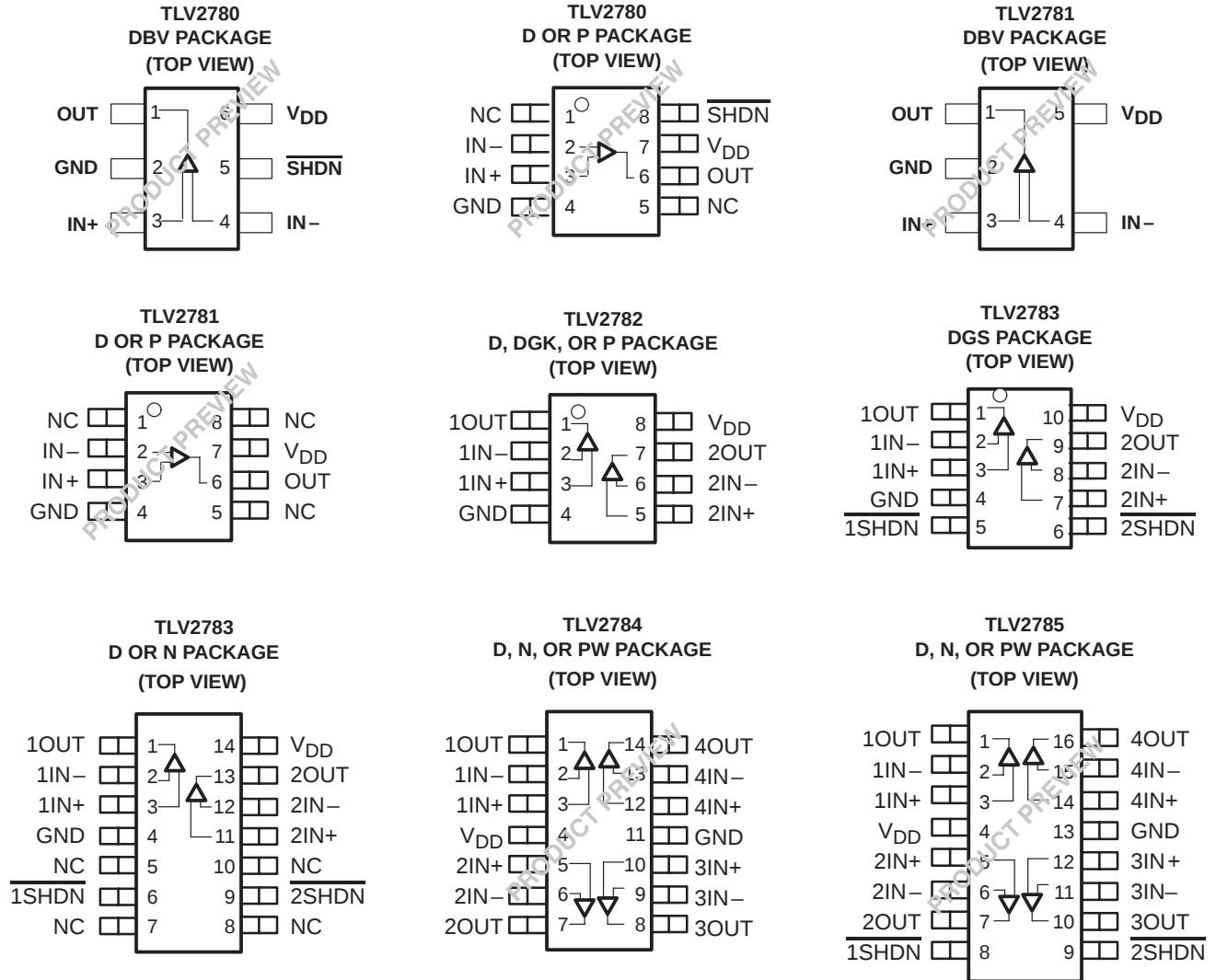
[†] This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., TLV2784CDR).



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TLV278x PACKAGE PINOUTS



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{DD} (see Note 1)	4 V
Differential input voltage, V_{ID}	$\pm V_{DD}$
Input current, I_I (any input)	± 10 mA
Output current, I_O	± 10 mA
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A : C suffix	0°C to 70°C
I suffix	–40°C to 125°C
Maximum junction temperature, T_J	150°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values, except differential voltages, are with respect to GND.

DISSIPATION RATING TABLE

PACKAGE	Θ_{JC} (°C/W)	Θ_{JA} (°C/W)	$T_A \leq 25^\circ\text{C}$ POWER RATING
D (8)	38.3	176	710 mW
D (14)	26.9	122.3	1022 mW
D (16)	25.7	114.7	1090 mW
DBV (5)	55	324.1	385 mW
DBV (6)	55	294.3	425 mW
DGK (8)	54.23	259.96	481 mW
DGS (10)	54.1	257.71	485 mW
N (14, 16)	32	78	1600 mW
P (8)	41	104	1200 mW
PW (14)	29.3	173.6	720 mW
PW (16)	28.7	161.4	774 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}	Single supply	1.8	3.6	V
	Split supply	± 0.9	± 1.8	
Common-mode input voltage range, V_{ICR}		–0.2	$V_{DD}+0.2$	V
Operating free-air temperature, T_A	C-suffix	0	70	°C
	I-suffix	–40	125	
Shutdown on/off voltage level [‡]	V_{IH}	$V_{DD} < 2.7$ V	$0.75V_{DD}$	V
		$V_{DD} = 2.7$ to 3.6 V	2	
	V_{IL}		0.6	

[‡] Relative to GND.



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electrical characteristics at specified free-air temperature, $V_{DD} = 1.8\text{ V}$, 2.7 V (unless otherwise noted)

dc performance

PARAMETER	TEST CONDITIONS		$T_A^\dagger$	MIN	TYP	MAX	UNIT
V_{IO} Input offset voltage	$V_{IC} = V_{DD}/2$, $V_O = V_{DD}/2$, $R_L = 2\text{ k}\Omega$, $R_S = 50\text{ }\Omega$	TLV278x	25°C		250	3000	μV
			Full range			4500	
		TLV278xA	25°C		250	2000	
			Full range			3000	
α_{VIO} Temperature coefficient of input offset voltage					8		$\mu\text{V}/^\circ\text{C}$
CMRR Common-mode rejection ratio	$V_{IC} = 0\text{ to }V_{DD}$, $R_S = 50\text{ }\Omega$	$V_{DD} = 1.8\text{ V}$	25°C	50	76		dB
			Full range	50			
		$V_{DD} = 2.7\text{ V}/3.6\text{ V}$	25°C	55	80		
			Full range	50			
	$V_{IC} = 1.2\text{ V to }V_{DD}$, $R_S = 50\text{ }\Omega$	$V_{DD} = 2.7\text{ V}/3.6\text{ V}$	25°C	70	100		
			Full range	70			
A_{VD} Large-signal differential voltage amplification	$R_L = 2\text{ k}\Omega$, $V_{O(PP)} = 1\text{ V}$	$V_{DD} = 1.8\text{ V}$	25°C	200	600		V/mV
			Full range	50			
		$V_{DD} = 2.7\text{ V}/3.6\text{ V}$	25°C	200	1000		
			Full range	70			

† Full range is 0°C to 70°C for the C suffix and –40°C to 125°C for the I suffix. If not specified, full range is –40°C to 125°C.

input characteristics

PARAMETER		TEST CONDITIONS		T _A [†]	MIN	TYP	MAX	UNIT
V _{ICR}	Common-mode input voltage range	Measured over CMRR range, R _S = 50 Ω	V _{DD} = 1.8 V	25°C or full range	−0.2 to 2			V
			V _{DD} = 2.7 V	25°C or-Full range	−0.2 to 2.9			
I _{IO}	Input offset current	V _{IC} = V _{DD} /2, V _O = V _{DD} /2, R _L = 2 kΩ, R _S = 50 Ω		25°C		2.5	15	pA
			TLV278xC	Full range			100	
			TLV278xI	Full range			300	
I _{IB}	Input bias current			25°C		2.5	15	pA
			TLV278xC	Full range			100	
			TLV278xI	Full range			300	
r _{i(d)}	Differential input resistance			25°C		1000		GΩ
C _{i(c)}	Common-mode input capacitance	f = 1 kHz		25°C		2.8		pF

† Full range is 0°C to 70°C for the C suffix and –40°C to 125°C for the I suffix. If not specified, full range is –40°C to 125°C.



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FAMILY OF 1.8 V HIGH-SPEED RAIL-TO-RAIL INPUT/OUTPUT
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electrical characteristics at specified free-air temperature, $V_{DD} = 1.8\text{ V}$, 2.7 V (unless otherwise noted) (continued)

output characteristics

PARAMETER	TEST CONDITIONS		$T_A^\dagger$	MIN	TYP	MAX	UNIT
V_{OH} High-level output voltage	$V_{IC} = V_{DD}/2$, $I_{OH} = -1\text{ mA}$	$V_{DD} = 1.8\text{ V}$	25°C	1.7	1.77		V
			Full range	1.63			
		$V_{DD} = 2.7\text{ V}$	25°C	2.6	2.68		
			Full range	2.6			
		$V_{DD} = 3.6\text{ V}$	25°C		3.58		
	$V_{IC} = V_{DD}/2$, $I_{OH} = -5\text{ mA}$	$V_{DD} = 1.8\text{ V}$	25°C	1.5	1.55		
			Full range	1.46			
		$V_{DD} = 2.7\text{ V}$	25°C	2.5	2.55		
			Full range	2.45			
		$V_{DD} = 3.6\text{ V}$	25°C		3.55		
V_{OL} Low-level output voltage	$V_{IC} = V_{DD}/2$, $I_{OL} = 1\text{ mA}$		25°C			70	mV
			Full range			80	
	$V_{IC} = V_{DD}/2$, $I_{OL} = 5\text{ mA}$	$V_{DD} = 1.8\text{ V}$	25°C		180	240	
			Full range			290	
		$V_{DD} = 2.7\text{ V}$	25°C		120	170	
			Full range			200	
I_O Output current	$V_{DD} = 1.8\text{ V}$, $V_O = 0.5\text{ V from}$	Positive rail	25°C		10		mA
		Negative rail			15		
	$V_{DD} = 2.7\text{ V}$, $V_O = 0.5\text{ V from}$	Positive rail			17		
		Negative rail			23		
I_{OS} Short-circuit output current	Sourcing	$V_{DD} = 1.8\text{ V}$	25°C		13		mA
		$V_{DD} = 2.7\text{ V}$			35		
	Sinking	$V_{DD} = 1.8\text{ V}$			21		
		$V_{DD} = 2.7\text{ V}$			45		

† Full range is 0°C to 70°C for the C suffix and –40°C to 125°C for the I suffix. If not specified, full range is –40°C to 125°C.

power supply

PARAMETER	TEST CONDITIONS		$T_A^\dagger$	MIN	TYP	MAX	UNIT
I_{DD} Supply current (per channel)	$V_O = V_{DD}/2$, $\overline{\text{SHDN}} = V_{DD}$		25°C		650	770	μA
			Full range			820	
k_{SVR} Supply voltage rejection ratio ($\Delta V_{DD} / \Delta V_{IO}$)	$V_{DD} = 1.8\text{ V to } 2.7\text{ V}$, $V_{IC} = V_{DD}/2$	No load,	25°C		60	75	dB
			Full range		58		
	$V_{DD} = 2.7\text{ V to } 3.6\text{ V}$, $V_{IC} = V_{DD}/2$	No load,	25°C		75	90	
			Full range		70		
	$V_{DD} = 1.8\text{ V to } 3.6\text{ V}$, $V_{IC} = V_{DD}/2$	No load,	25°C		65	80	
			Full range		60		

† Full range is 0°C to 70°C for the C suffix and –40°C to 125°C for the I suffix. If not specified, full range is –40°C to 125°C.

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electrical characteristics at specified free-air temperature, $V_{DD} = 1.8\text{ V}$, 2.7 V (unless otherwise noted) (continued)

dynamic performance

PARAMETER		TEST CONDITIONS		T _A [†]	MIN	TYP	MAX	UNIT
UGBW	Unity gain bandwidth	R _L = 2 kΩ, C _L = 25 pF		25°C	8			MHz
SR+	Positive slew rate at unity gain	V _{O(PP)} = 1 V, R _L = 2 kΩ, C _L = 50 pF	V _{DD} = 1.8 V	25°C	3.3	4.3	V/μs	
				Full range	3.1			
			V _{DD} = 2.7 V	25°C	3.8	4.8		
				Full range	3.5			
			V _{DD} = 3.6 V	25°C	4	5		
				Full range	3.6			
SR−	Negative slew rate at unity gain	V _{O(PP)} = 1 V, R _L = 2 kΩ, C _L = 50 pF	V _{DD} = 1.8 V	25°C	2.1	2.8		
				Full range	1.89			
			V _{DD} = 2.7 V	25°C	2.2	2.8		
				Full range	1.97			
			V _{DD} = 3.6 V	25°C	3.5	4.2		
				Full range	3.4			
φ _m	Phase margin	R _L = 2 kΩ, C _L = 25 pF		25°C	58°			dB
Gain margin					8			
t _s	Settling time	V _{DD} = 1.8 V, V _{(STEP)PP} = 1 V, A _V = −1, C _L = 10 pF, R _L = 2 kΩ	0.1%	25°C	1.7			μs
			0.01%		2.8			
		V _{DD} = 2.7 V, V _{(STEP)PP} = 1 V, A _V = −1, C _L = 10 pF, R _L = 2 kΩ	0.1%		1.7			
			0.01%		2.4			

† Full range is 0°C to 70°C for the C suffix and -40°C to 125°C for the I suffix. If not specified, full range is -40°C to 125°C .

noise/distortion performance

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
THD + N	Total harmonic distortion plus noise	$V_{O(PP)} = V_{DD}/2$, $R_L = 2\text{ k}\Omega$, $f = 10\text{ kHz}$	$A_V = 1$	25°C		0.055%		
			$A_V = 10$			0.08%		
			$A_V = 100$			0.45%		
V_n	Equivalent input noise voltage	$f = 1\text{ kHz}$				18		nV/ $\sqrt{\text{Hz}}$
		$f = 10\text{ kHz}$				9		
I_n	Equivalent input noise current	$f = 1\text{ kHz}$				0.9		fA/ $\sqrt{\text{Hz}}$

shutdown characteristics

PARAMETER		TEST CONDITIONS	$T_A^\dagger$	MIN	TYP	MAX	UNIT
$I_{DD}(\text{SHDN})$	Supply current, all channels in shutdown mode (TLV2780, TLV2783, TLV2785)	$\overline{\text{SHDN}} = 0\text{ V}$	25°C		900	1400	nA
			Full range			1700	
$t_{(on)}$	Amplifier turnon time ‡	$R_L = 2\text{ k}\Omega$	25°C		800		ns
$t_{(off)}$	Amplifier turnoff time ‡	$R_L = 2\text{ k}\Omega$			200		

† Full range is 0°C to 70°C for the C suffix and -40°C to 125°C for the I suffix. If not specified, full range is -40°C to 125°C .

‡ Disable time and enable time are defined as the interval between application of the logic signal to SHDN and the point at which the supply current has reached half its final value.



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TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	vs Common-mode input voltage	1, 2
CMRR	Common-mode rejection ratio	vs Frequency	3
V_{OH}	High-level output voltage	vs High-level output current	4, 6
V_{OL}	Low-level output voltage	vs Low-level output current	5, 7
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	8
Z_o	Output impedance	vs Frequency	9
I_{DD}	Supply current	vs Supply voltage	10
I_{DD}	Supply current	vs Free-air temperature	11
PSRR	Power supply rejection ratio	vs Frequency	12
A_{VD}	Differential voltage amplification & phase	vs Frequency	13
	Gain-bandwidth product	vs Free-air temperature	14
SR	Slew rate	vs Supply voltage	15
		vs Free-air temperature	16, 17
ϕ_m	Phase margin	vs Load capacitance	18
V_n	Equivalent input noise voltage	vs Frequency	19
	Voltage-follower large-signal pulse response	vs Time	20
	Voltage-follower small-signal pulse response	vs Time	21
	Inverting large-signal pulse response	vs Time	22
	Inverting small-signal pulse response	vs Time	23
	Crosstalk	vs Frequency	24
	Shutdown forward & reverse isolation	vs Frequency	25
$I_{DD(SHDN)}$	Shutdown supply current	vs Free-air temperature	26
$I_{DD(SHDN)}$	Shutdown supply current	vs Supply voltage	27
$I_{DD(SHDN)}$	Shutdown supply current/output voltage	vs Time	28



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TYPICAL CHARACTERISTICS

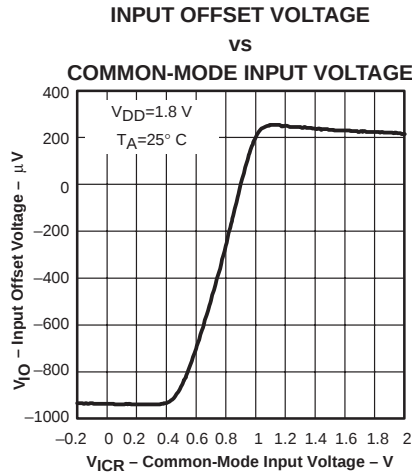


Figure 1

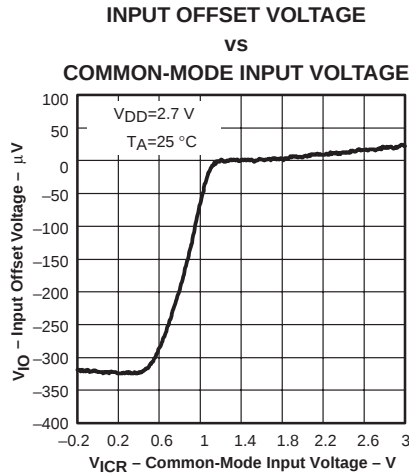


Figure 2

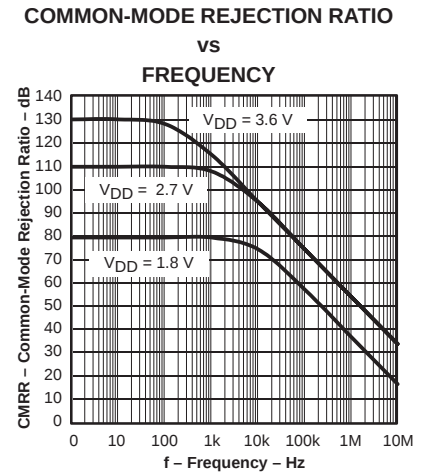


Figure 3

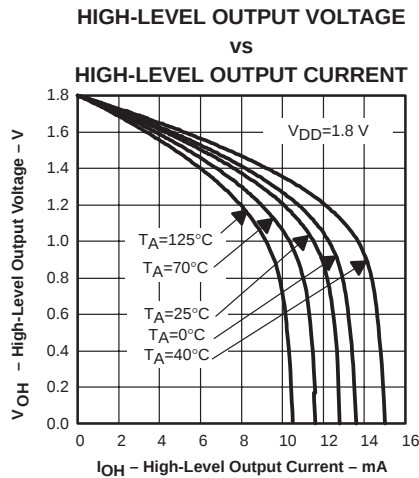


Figure 4

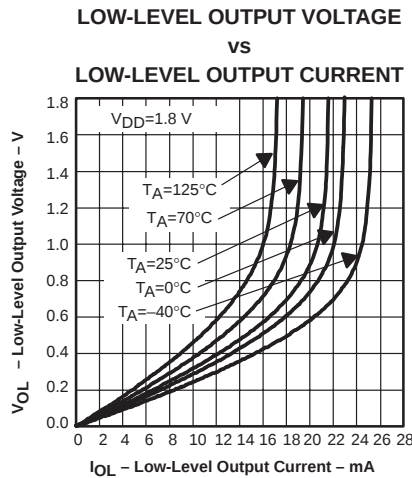


Figure 5

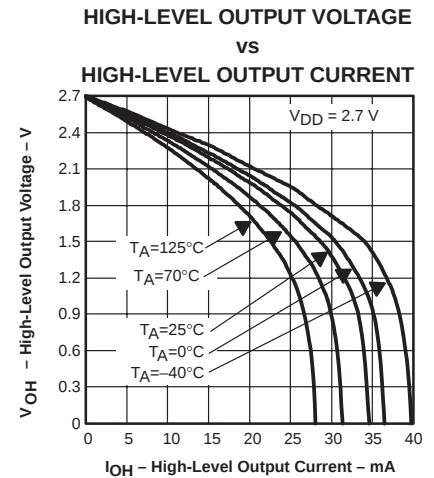


Figure 6

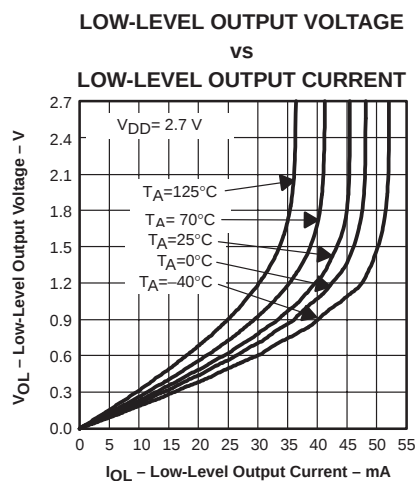


Figure 7

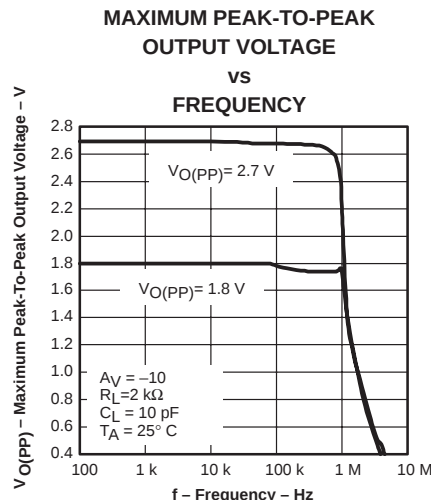


Figure 8

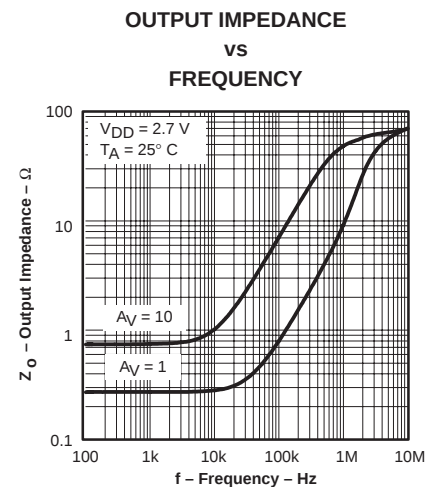


Figure 9



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TYPICAL CHARACTERISTICS

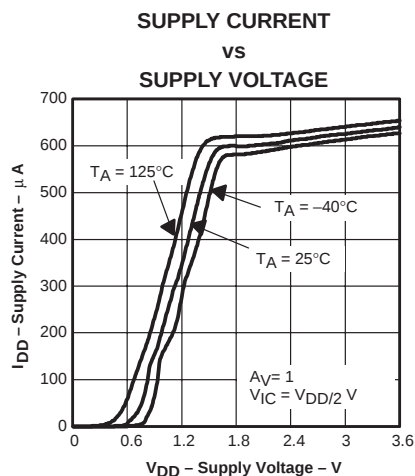


Figure 10

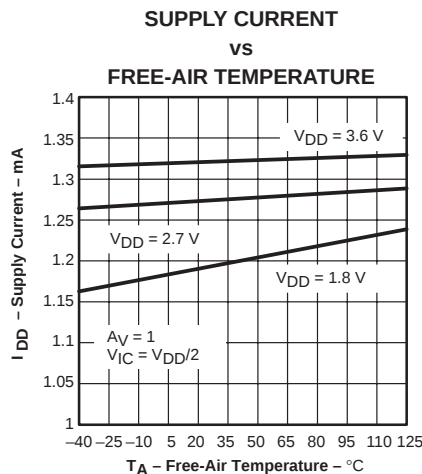


Figure 11

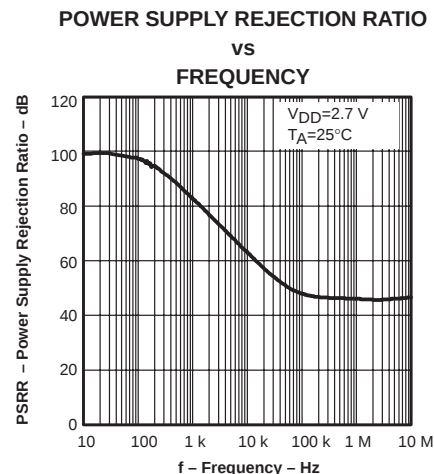


Figure 12

DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE

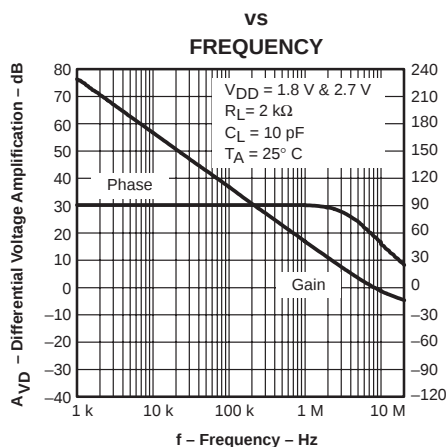


Figure 13

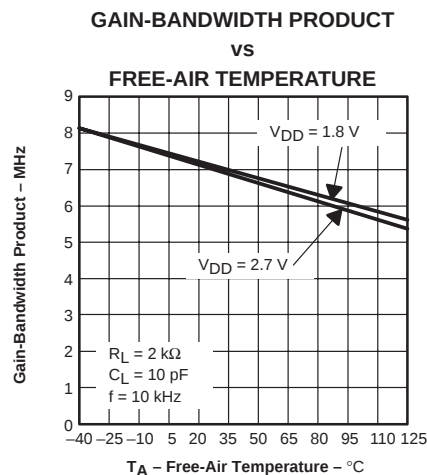


Figure 14

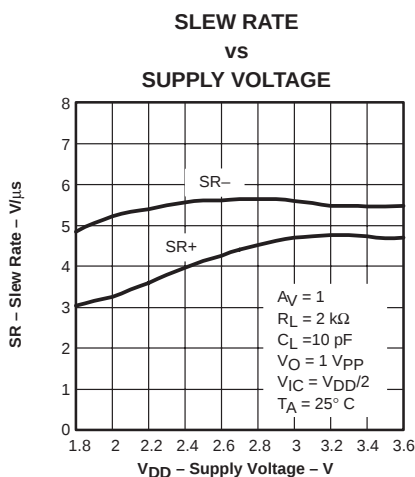


Figure 15

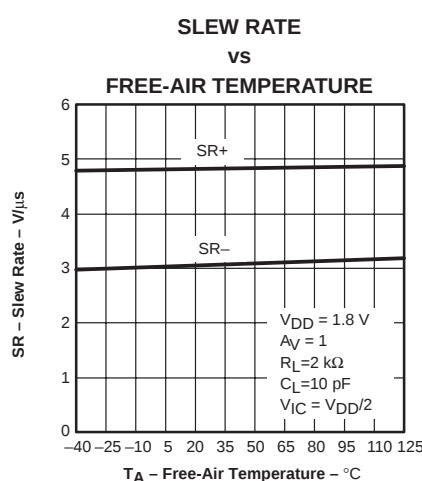


Figure 16

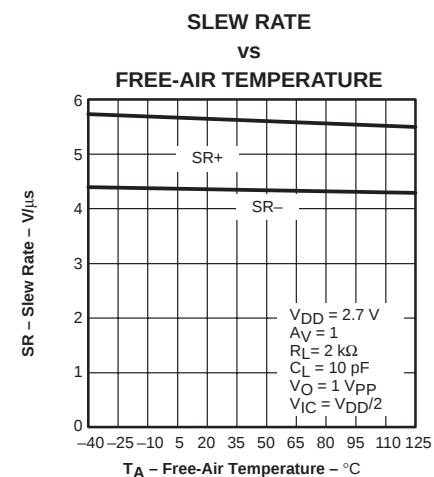


Figure 17

TLV2780, TLV2781, TLV2782, TLV2783, TLV2784, TLV2785, TLV278xA FAMILY OF 1.8 V HIGH-SPEED RAIL-TO-RAIL INPUT/OUTPUT OPERATIONAL AMPLIFIERS WITH SHUTDOWN

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TYPICAL CHARACTERISTICS

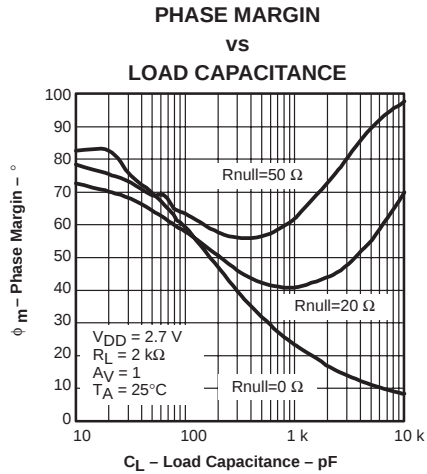


Figure 18

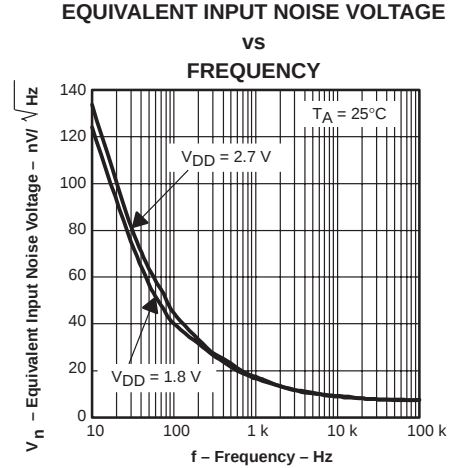


Figure 19

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

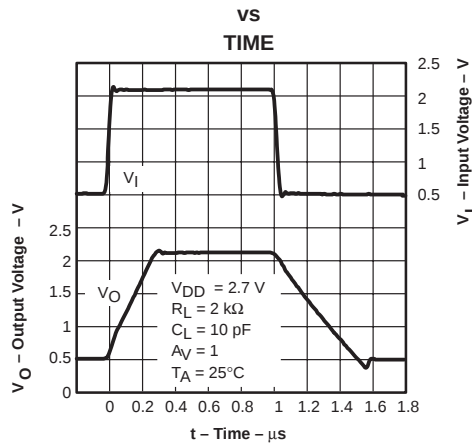


Figure 20

VOLTAGE-FOLLOWER SMALL-SIGNAL PULSE RESPONSE

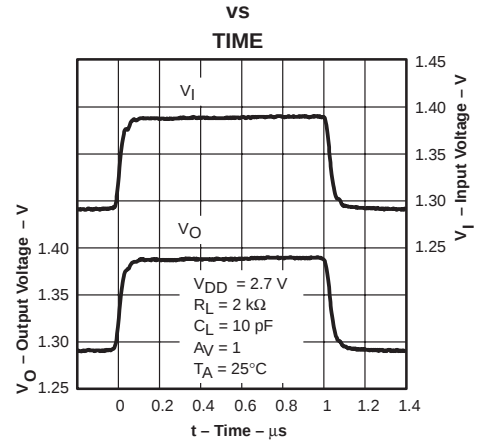


Figure 21

INVERTING LARGE-SIGNAL PULSE RESPONSE

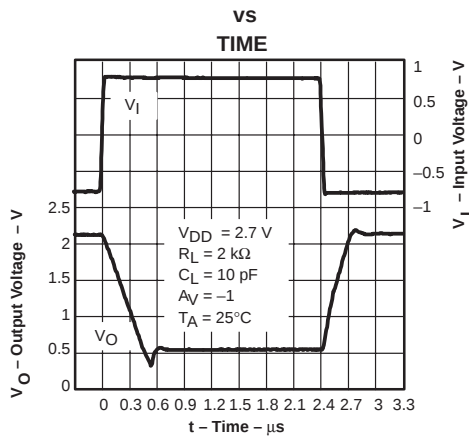


Figure 22

INVERTING SMALL-SIGNAL PULSE RESPONSE

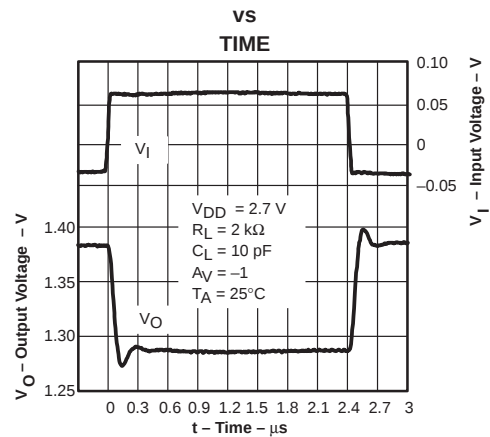
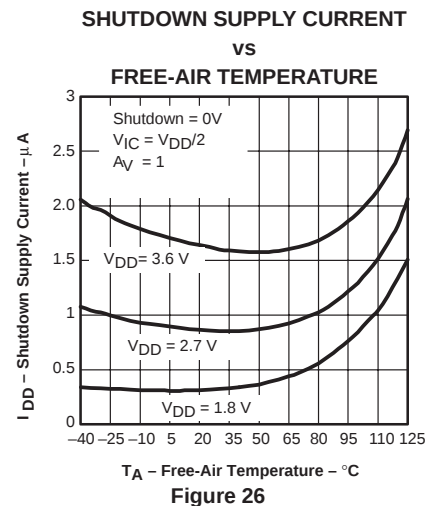
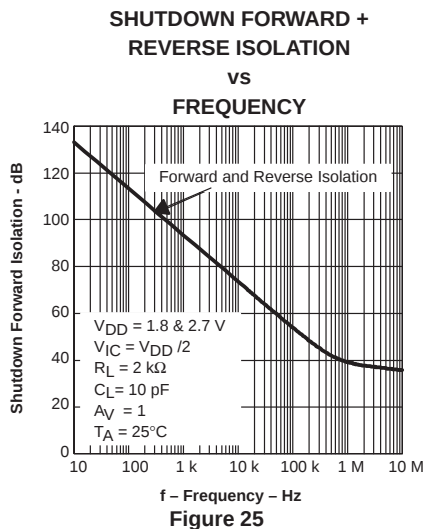
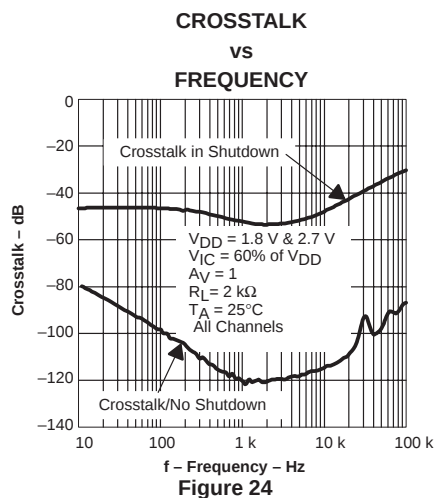


Figure 23

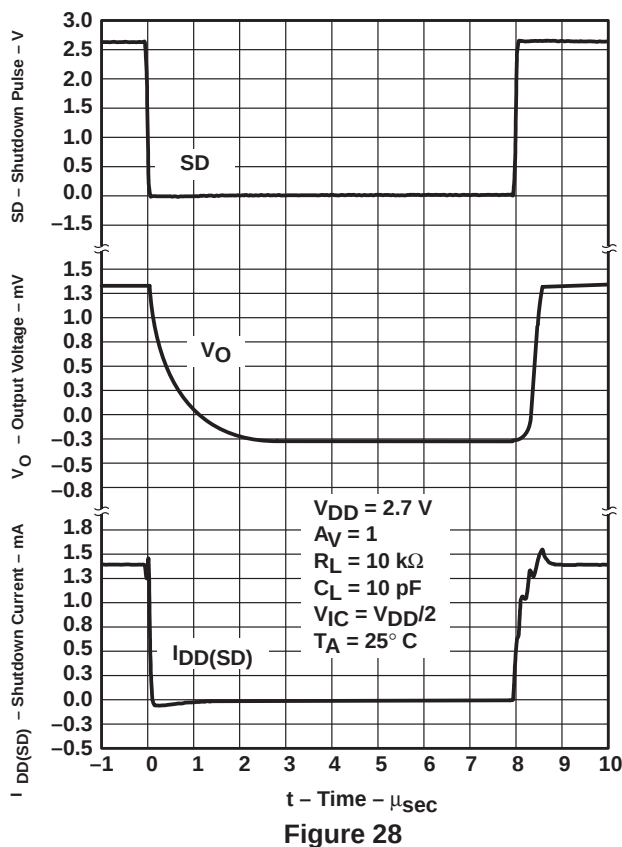
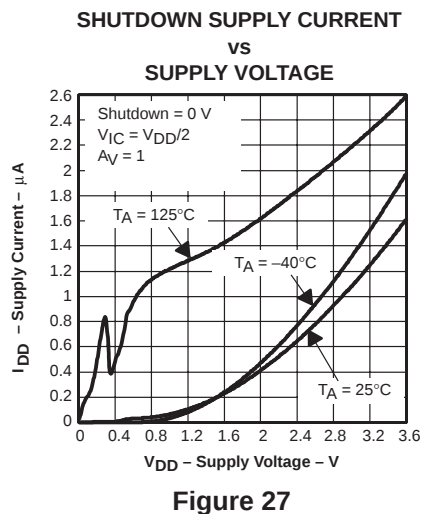
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TYPICAL CHARACTERISTICS



SHUTDOWN SUPPLY CURRENT / OUTPUT VOLTAGE VS TIME



PARAMETER MEASUREMENT INFORMATION

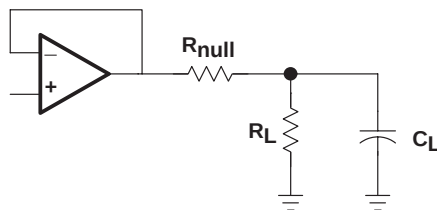


Figure 29

APPLICATION INFORMATION

driving a capacitive load

When the amplifier is configured in this manner, capacitive loading directly on the output will decrease the device's phase margin leading to high frequency ringing or oscillations. Therefore, for capacitive loads of greater than 10 pF, it is recommended that a resistor be placed in series (R_{NULL}) with the output of the amplifier, as shown in Figure 30.

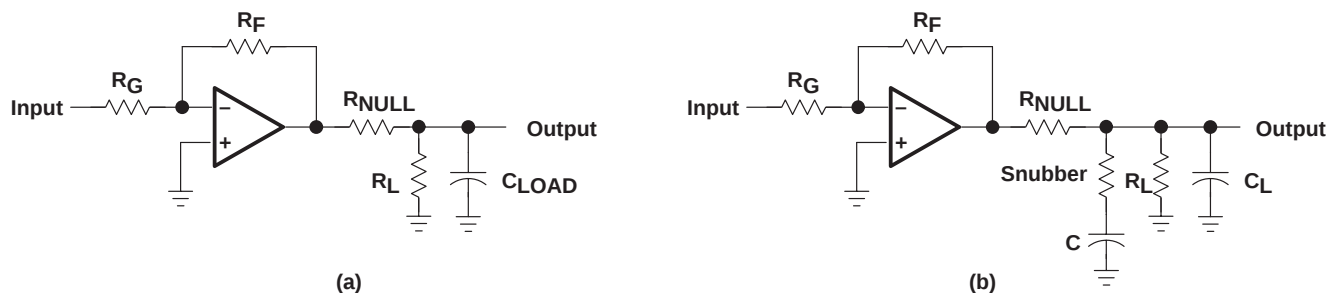


Figure 30. Driving a Capacitive Load

offset voltage

The output offset voltage, (V_{OO}) is the sum of the input offset voltage (V_{IO}) and both input bias currents (I_{IB}) times the corresponding gains. The following schematic and formula can be used to calculate the output offset voltage:

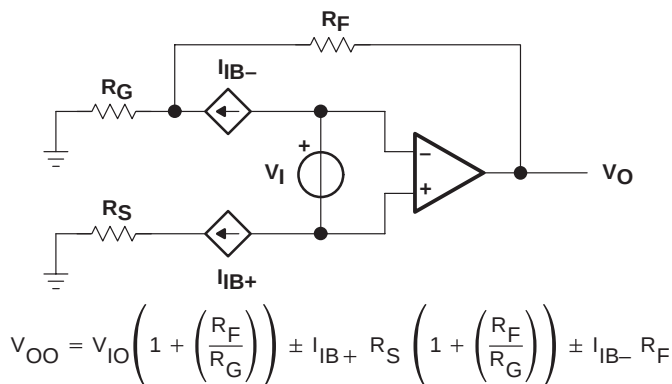


Figure 31. Output Offset Voltage Model

APPLICATION INFORMATION

general configurations

When receiving low-level signals, limiting the bandwidth of the incoming signals into the system is often required. The simplest way to accomplish this is to place an RC filter at the noninverting terminal of the amplifier (see Figure 32).

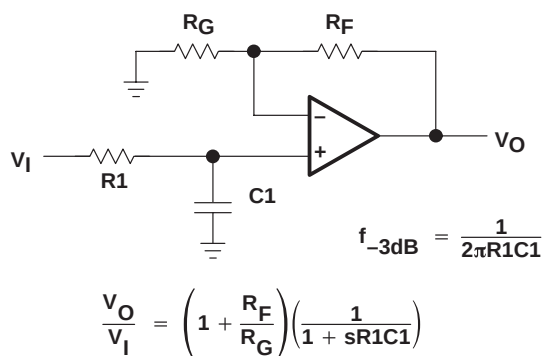


Figure 32. Single-Pole Low-Pass Filter

If even more attenuation is needed, a multiple pole filter is required. The Sallen-Key filter can be used for this task. For best results, the amplifier should have a bandwidth that is 8 to 10 times the filter frequency bandwidth. Failure to do this can result in phase shift of the amplifier.

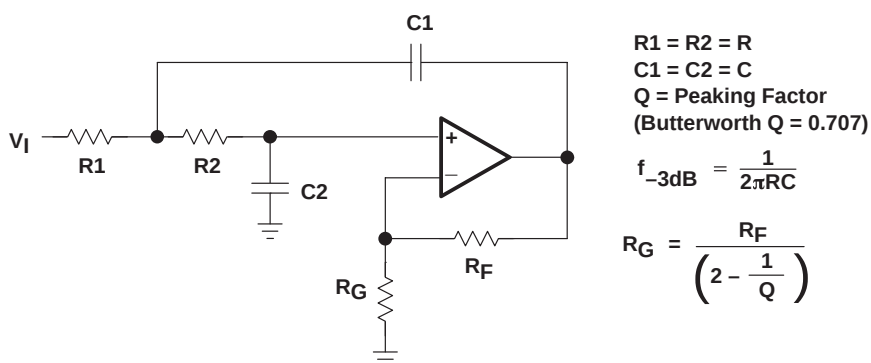


Figure 33. 2-Pole Low-Pass Sallen-Key Filter

APPLICATION INFORMATION

circuit layout considerations

To achieve the levels of high performance of the TLV278x, follow proper printed-circuit board design techniques. A general set of guidelines is given in the following.

- Ground planes – It is highly recommended that a ground plane be used on the board to provide all components with a low inductive ground connection. However, in the areas of the amplifier inputs and output, the ground plane can be removed to minimize the stray capacitance.
- Proper power supply decoupling – Use a 6.8- μ F tantalum capacitor in parallel with a 0.1- μ F ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1- μ F ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1- μ F capacitor should be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting trace makes the capacitor less effective. The designer should strive for distances of less than 0.1 inches between the device power terminals and the ceramic capacitors.
- Sockets – Sockets can be used but are not recommended. The additional lead inductance in the socket pins will often lead to stability problems. Surface-mount packages soldered directly to the printed-circuit board is the best implementation.
- Short trace runs/compact part placements – Optimum high performance is achieved when stray series inductance has been minimized. To realize this, the circuit layout should be made as compact as possible, thereby minimizing the length of all trace runs. Particular attention should be paid to the inverting input of the amplifier. Its length should be kept as short as possible. This will help to minimize stray capacitance at the input of the amplifier.
- Surface-mount passive components – Using surface-mount passive components is recommended for high performance amplifier circuits for several reasons. First, because of the extremely low lead inductance of surface-mount components, the problem with stray series inductance is greatly reduced. Second, the small size of surface-mount components naturally leads to a more compact layout thereby minimizing both stray inductance and capacitance. If leaded components are used, it is recommended that the lead lengths be kept as short as possible.

TLV2780, TLV2781, TLV2782, TLV2783, TLV2784, TLV2785, TLV278xA FAMILY OF 1.8 V HIGH-SPEED RAIL-TO-RAIL INPUT/OUTPUT OPERATIONAL AMPLIFIERS WITH SHUTDOWN

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APPLICATION INFORMATION

shutdown function

Three members of the TLV278x family (TLV2780/3/5) have a shutdown terminal for conserving battery life in portable applications. When the shutdown terminal is tied low, the supply current is reduced to 900 nA/channel, the amplifier is disabled, and the outputs are placed in a high impedance mode. To enable the amplifier, the shutdown terminal can either be left floating or pulled high. When the shutdown terminal is left floating, care should be taken to ensure that parasitic leakage current at the shutdown terminal does not inadvertently place the operational amplifier into shutdown.

general power dissipation considerations

For a given θ_{JA} , the maximum power dissipation is shown in Figure 34 and is calculated by the following formula:

$$P_D = \left(\frac{T_{MAX} - T_A}{\theta_{JA}} \right)$$

Where:

P_D = Maximum power dissipation of TLV278x IC (watts)

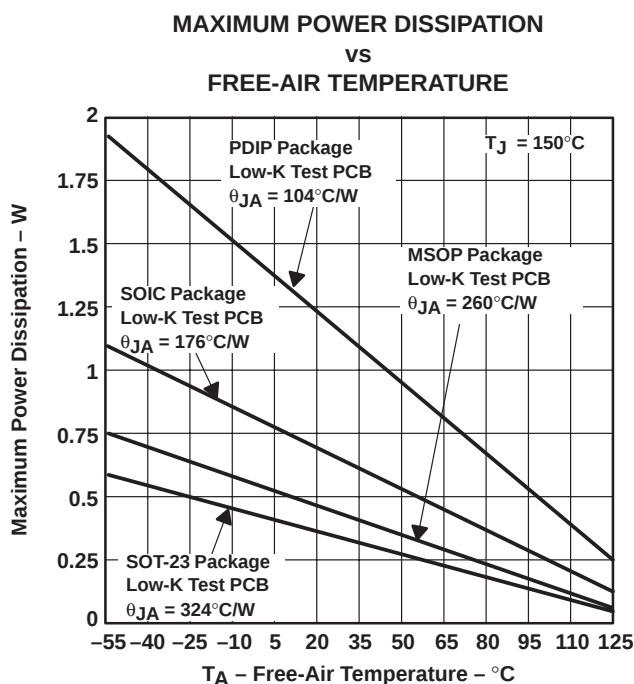
T_{MAX} = Absolute maximum junction temperature (150°C)

T_A = Free-ambient air temperature (°C)

$\theta_{JA} = \theta_{JC} + \theta_{CA}$

θ_{JC} = Thermal coefficient from junction to case

θ_{CA} = Thermal coefficient from case to ambient air (°C/W)



NOTE A: Results are with no air flow and using JEDEC Standard Low-K test PCB.

Figure 34. Maximum Power Dissipation vs Free-Air Temperature

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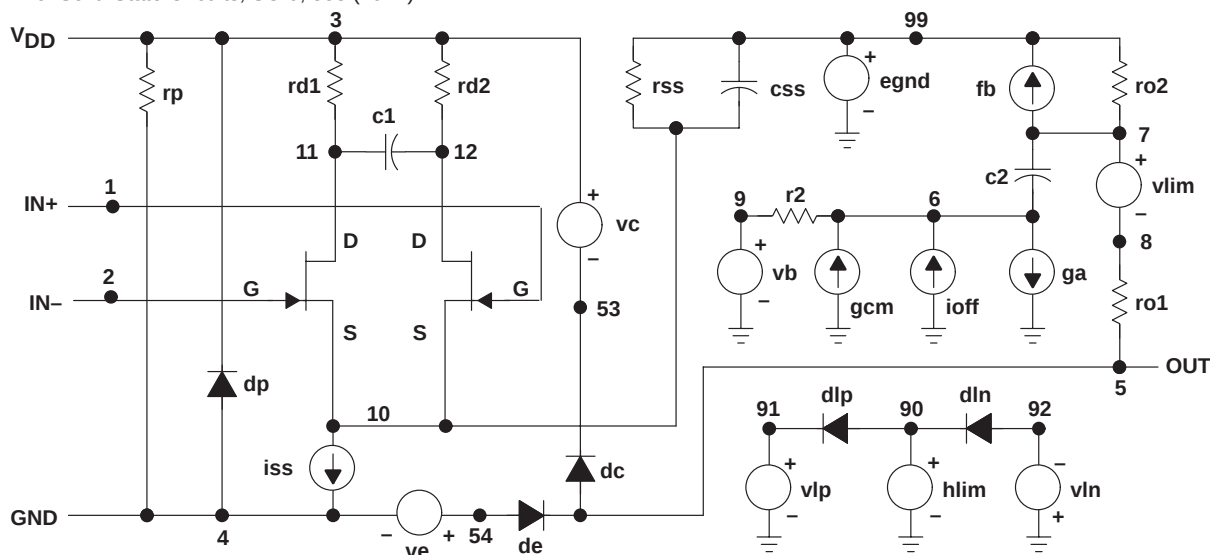
APPLICATION INFORMATION

macromodel information

Macromodel information provided was derived using Microsim *Parts*™ Release 9.1, the model generation software used with Microsim *PSpice*™. The Boyle macromodel (see Note 2) and subcircuit in Figure 35 are generated using TLV278x typical electrical and operating characteristics at $T_A = 25^\circ\text{C}$. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 2: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers," *IEEE Journal of Solid-State Circuits*, SC-9, 353 (1974).



* TLV2782_HVDD operational amplifier "macromodel" subcircuit
* created using Model Editor release 9.1 on 03/3/00 at 9:47
* Model Editor is an OrCAD product.

* connections: non-inverting input
* | inverting input
* | positive power supply
* | negative power supply
* | output
* |
*.subckt TLV2782_HVDD 1 2 3 4 5

```
c1      11      12      49.58E-15
c2      6       7       10.200E-12
css     10      99      1.0000E-30
dc      5       53      dy
de      54      5       dy
dlp     90      91      dx
dln     92      90      dx
dp      4       3       dx
egnd    99      0       poly(2) (3,0) (4,0) 0 .5 .5
fb      7       99      poly(5) vb vc ve vlp vln 0
                        41.096E6 -1E3 1E3 41E6
                        -41E6
```

```
ga      6       0       11 12 544.75E-6
gcm     0       6       10 99 1.1538E-9
iss     10      4       dc 56.957E-6
hlim    90      0       vlim 1K
j1      11      2       10 jx1
j2      12      1       10 jx2
r2      6       9       100.00E3
rd1     3       11      1.8357E3
rd2     3       12      1.8357E3
ro1     8       5       10
ro2     7       99      10
rp      3       4       2.1845E3
rss     10      99      3.5114E6
vb      9       0       dc 0
vc      3       53      dc .81911
ve      54      4       dc .81911
vlim    7       8       dc 0
vlp     91      0       dc 45.400
vln     0       92      dc 45.400
.model  dx      D(Is=800.00E-18)
.model  dy      D(Is=800.00E-18 Rs=1m Cjo=10p)
.model  jx1     NJF(Is=500.00E-15 Beta=5.2102E-3 Vto=-1)
.model  jx2     NJF(Is=500.00E-15 Beta=5.2102E-3 Vto=-1)
.ends
```

Figure 35. Boyle Macromodel and Subcircuit

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TLV2780, TLV2781, TLV2782, TLV2783, TLV2784, TLV2785, TLV278xA
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OPERATIONAL AMPLIFIERS WITH SHUTDOWN

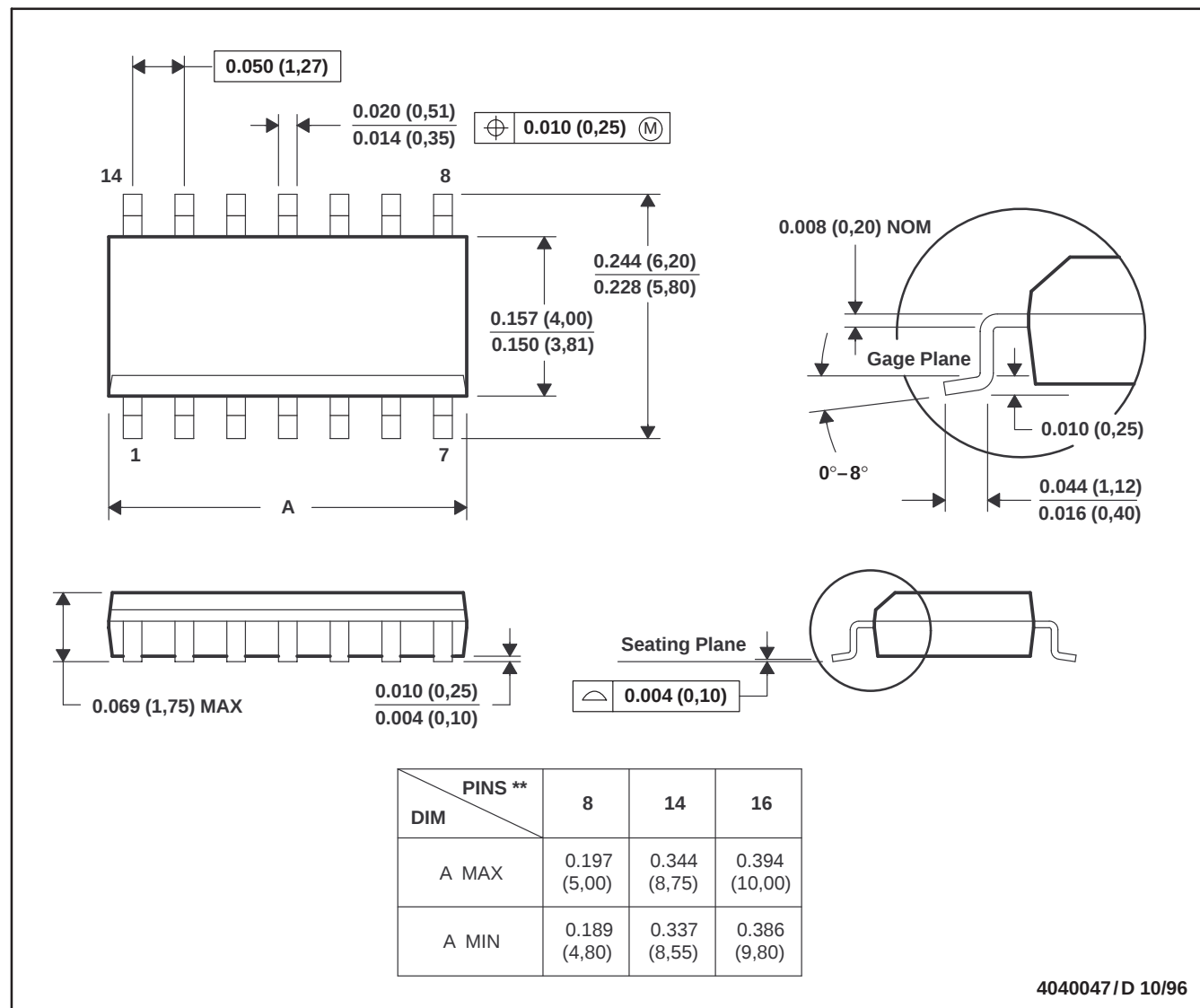
SLOS245 – MARCH 2000

MECHANICAL DATA

D (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

14 PIN SHOWN



- NOTES: B. All linear dimensions are in inches (millimeters).
 C. This drawing is subject to change without notice.
 D. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
 E. Falls within JEDEC MS-012

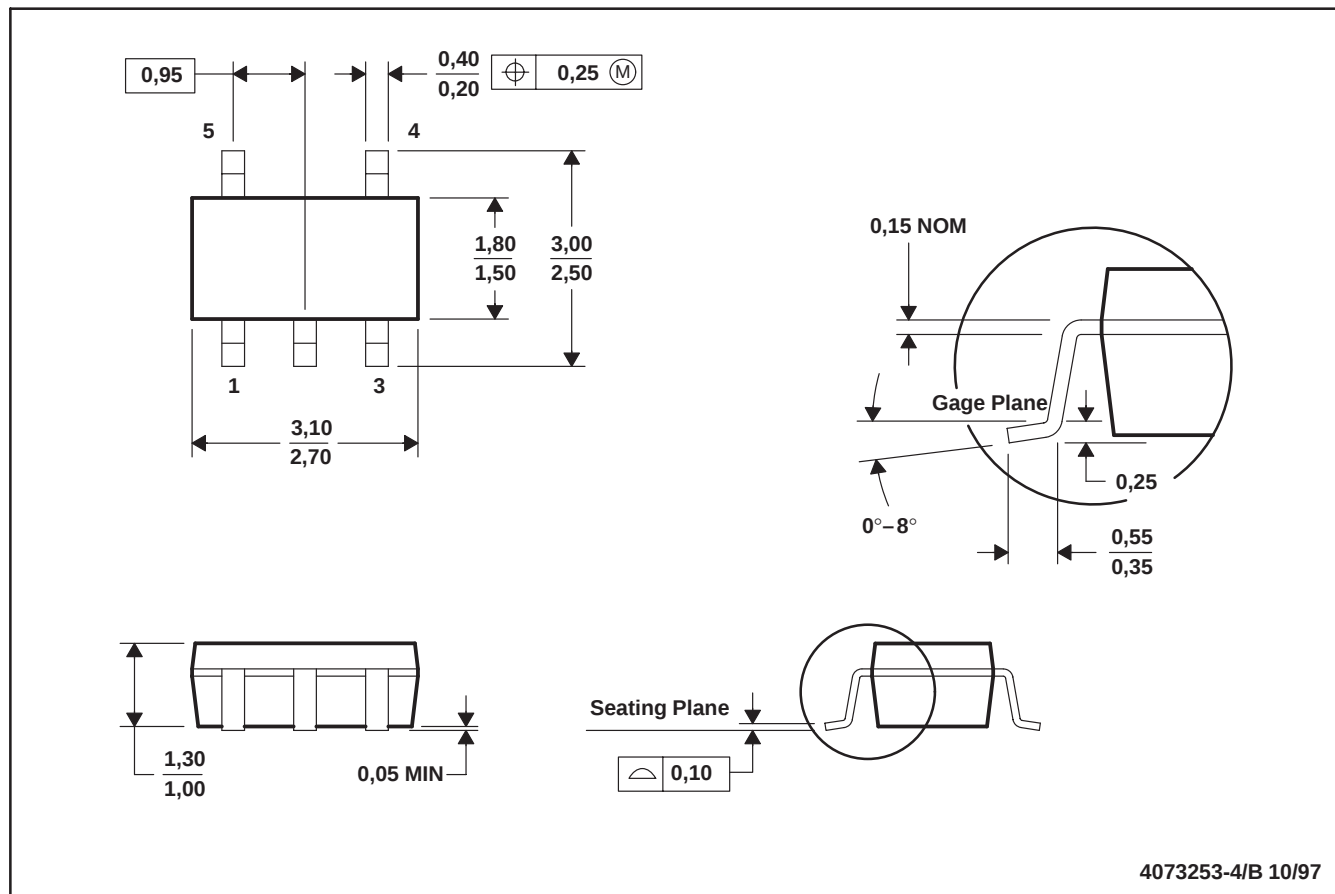
TLV2780, TLV2781, TLV2782, TLV2783, TLV2784, TLV2785, TLV278xA
FAMILY OF 1.8 V HIGH-SPEED RAIL-TO-RAIL INPUT/OUTPUT
OPERATIONAL AMPLIFIERS WITH SHUTDOWN

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MECHANICAL DATA

DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions include mold flash or protrusion.

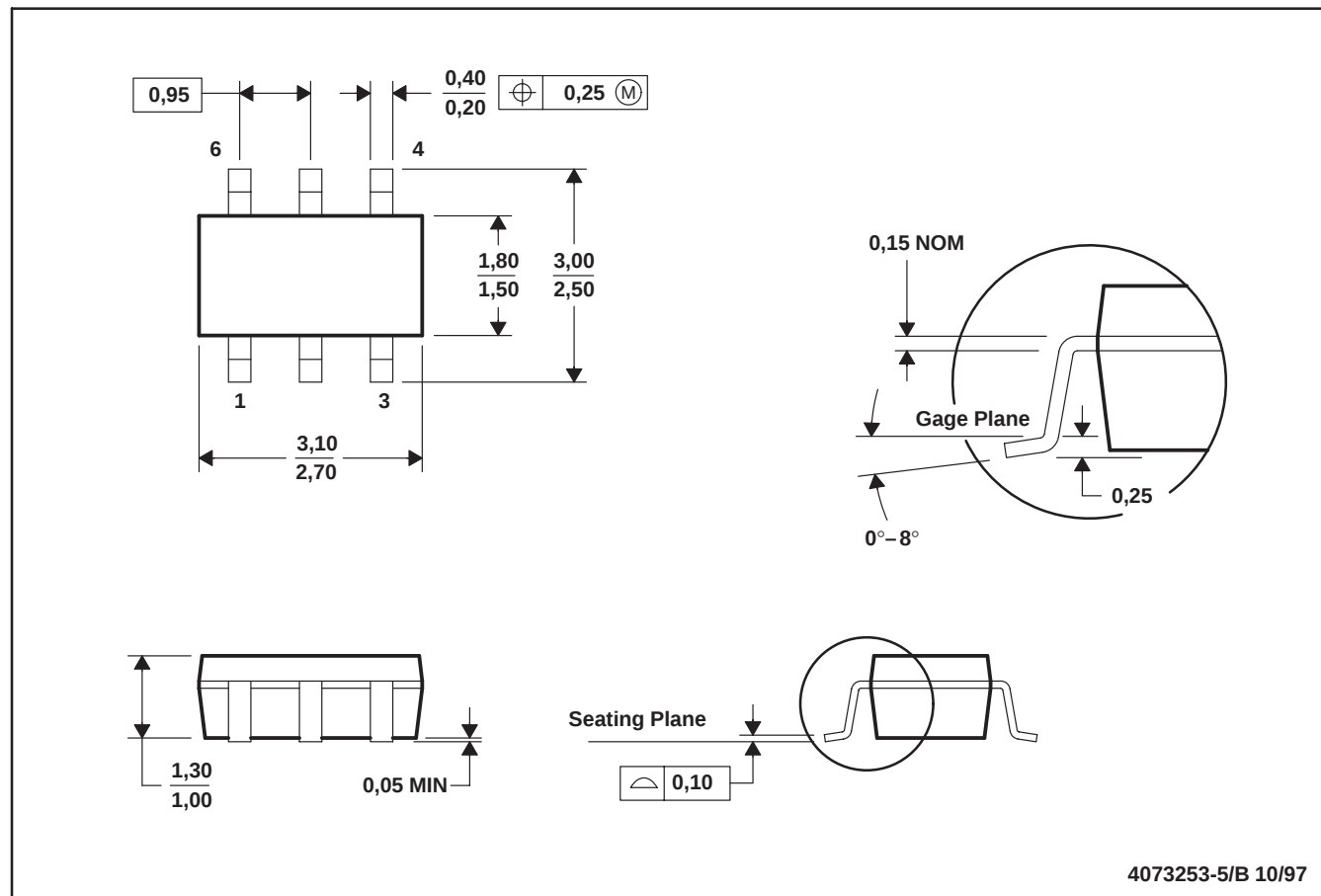
TLV2780, TLV2781, TLV2782, TLV2783, TLV2784, TLV2785, TLV278xA
FAMILY OF 1.8 V HIGH-SPEED RAIL-TO-RAIL INPUT/OUTPUT
OPERATIONAL AMPLIFIERS WITH SHUTDOWN

SLOS245 – MARCH 2000

MECHANICAL DATA

DBV (R-PDSO-G6)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions include mold flash or protrusion.

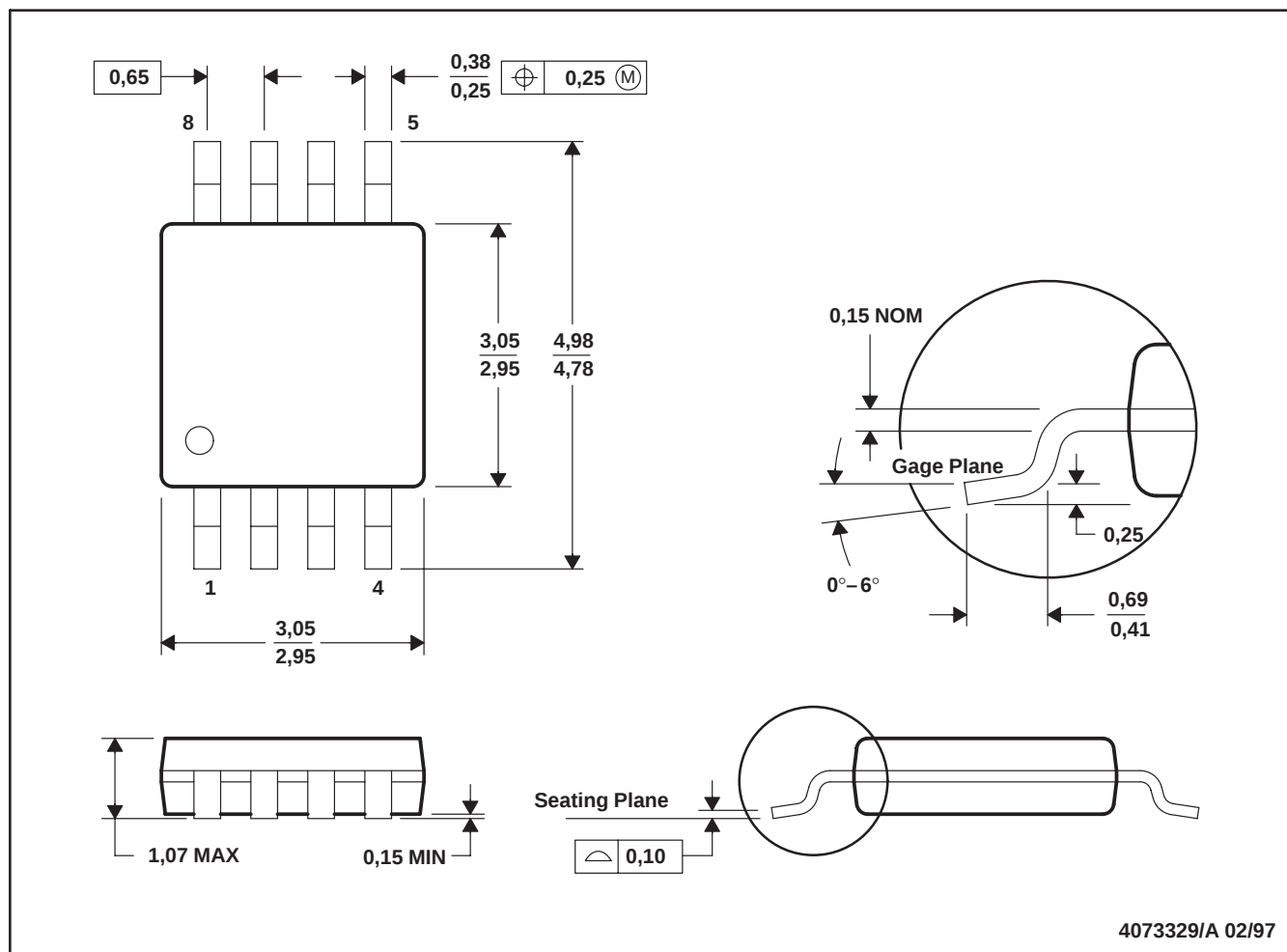
TLV2780, TLV2781, TLV2782, TLV2783, TLV2784, TLV2785, TLV278xA
FAMILY OF 1.8 V HIGH-SPEED RAIL-TO-RAIL INPUT/OUTPUT
OPERATIONAL AMPLIFIERS WITH SHUTDOWN

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MECHANICAL DATA

DGK (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO-187

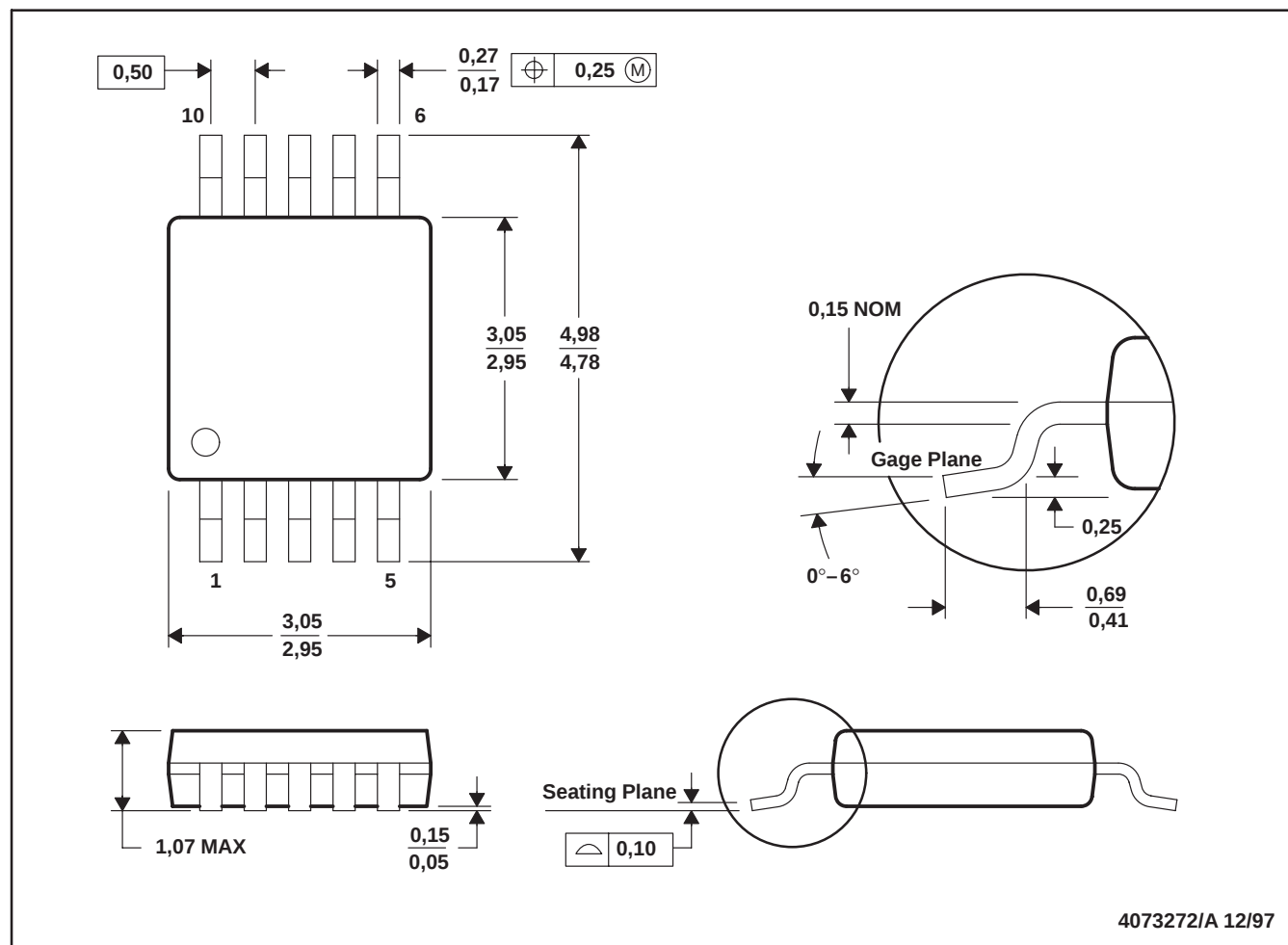
TLV2780, TLV2781, TLV2782, TLV2783, TLV2784, TLV2785, TLV278xA
FAMILY OF 1.8 V HIGH-SPEED RAIL-TO-RAIL INPUT/OUTPUT
OPERATIONAL AMPLIFIERS WITH SHUTDOWN

SLOS245 – MARCH 2000

MECHANICAL DATA

DGS (S-PDSO-G10)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion.

TLV2780, TLV2781, TLV2782, TLV2783, TLV2784, TLV2785, TLV278xA
FAMILY OF 1.8 V HIGH-SPEED RAIL-TO-RAIL INPUT/OUTPUT
OPERATIONAL AMPLIFIERS WITH SHUTDOWN

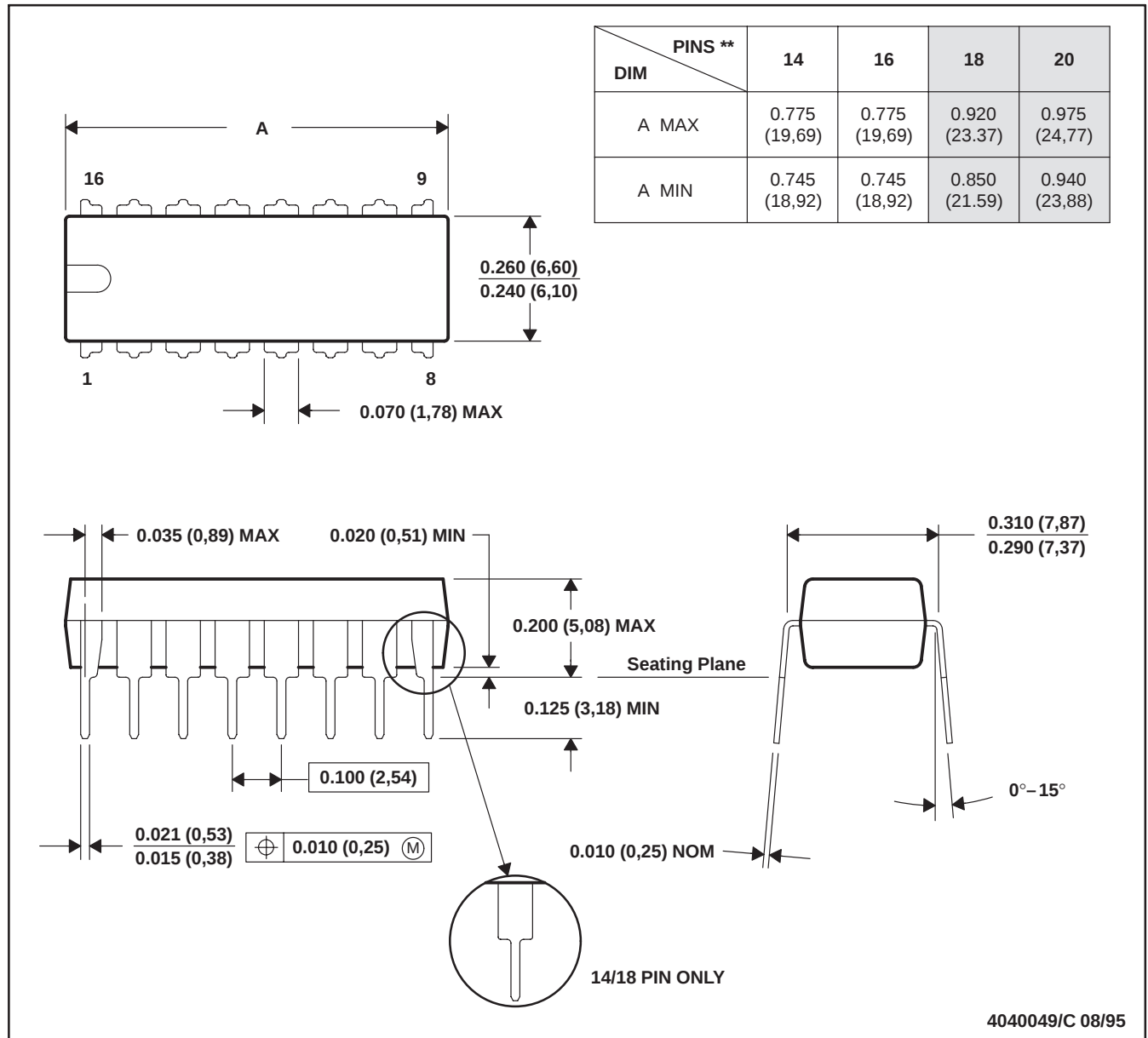
SLOS245 – MARCH 2000

MECHANICAL DATA

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PIN SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-001 (20 pin package is shorter than MS-001.)

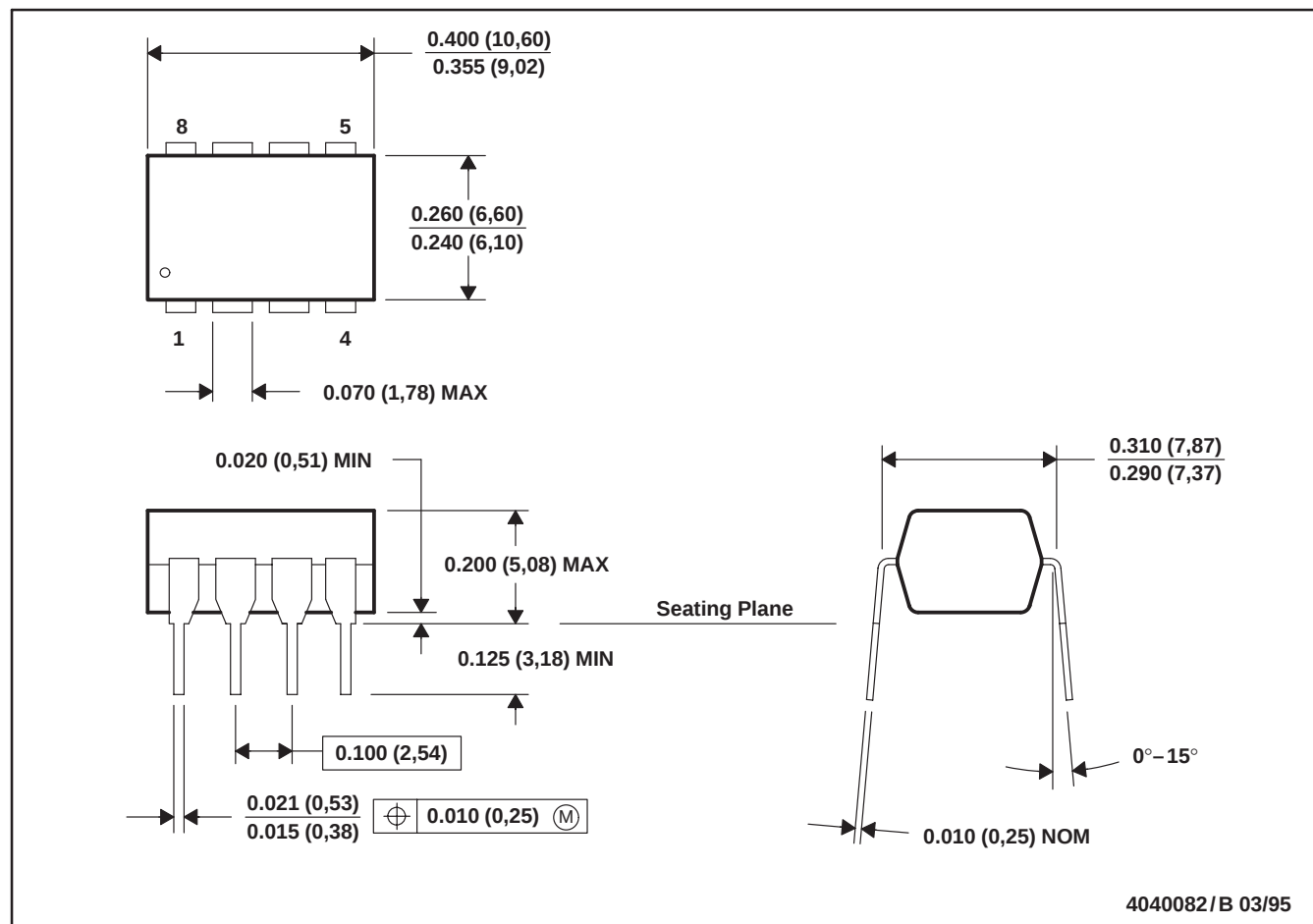
TLV2780, TLV2781, TLV2782, TLV2783, TLV2784, TLV2785, TLV278xA
FAMILY OF 1.8 V HIGH-SPEED RAIL-TO-RAIL INPUT/OUTPUT
OPERATIONAL AMPLIFIERS WITH SHUTDOWN

SLOS245 – MARCH 2000

MECHANICAL DATA

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-001

TLV2780, TLV2781, TLV2782, TLV2783, TLV2784, TLV2785, TLV278xA
FAMILY OF 1.8 V HIGH-SPEED RAIL-TO-RAIL INPUT/OUTPUT
OPERATIONAL AMPLIFIERS WITH SHUTDOWN

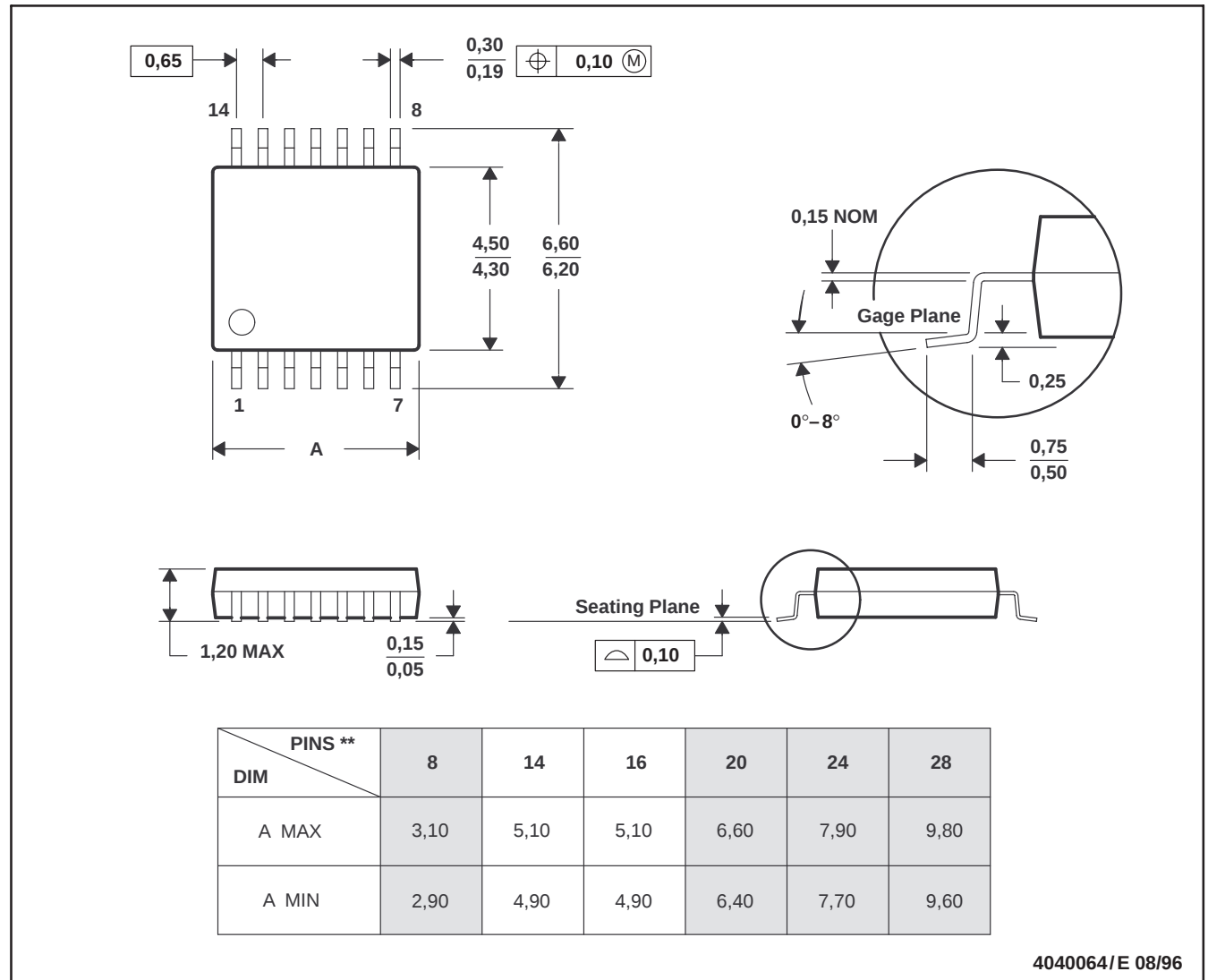
SLOS245 – MARCH 2000

MECHANICAL DATA

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PIN SHOWN



- NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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