Voltage Regulator - Low Power Low, Dropout

100 mA

LP2950, LP2951, NCV2951

The LP2950 and LP2951 are micropower voltage regulators that are specifically designed to maintain proper regulation with an extremely low input−to−output voltage differential. These devices feature a very low quiescent bias current of 75 μA and are capable of supplying output currents in excess of 100 mA. Internal current and thermal limiting protection is provided.

The LP2951 has three additional features. The first is the $\overline{\text{Error}}$ Output that can be used to signal external circuitry of an out of regulation condition, or as a microprocessor power−on reset. The second feature allows the output voltage to be preset to 5.0 V, 3.3 V or 3.0 V output (depending on the version) or programmed from 1.25 V to 29 V. It consists of a pinned out resistor divider along with direct access to the Error Amplifier feedback input. The third feature is a Shutdown input that allows a logic level signal to turn−off or turn−on the regulator output.

Due to the low input−to−output voltage differential and bias current specifications, these devices are ideally suited for battery powered computer, consumer, and industrial equipment where an extension of useful battery life is desirable. The LP2950 is available in the three pin case 29 and DPAK packages, and the LP2951 is available in the eight pin dual−in−line, SOIC−8 and Micro8 surface mount packages. The 'A' suffix devices feature an initial output voltage tolerance ±0.5%.

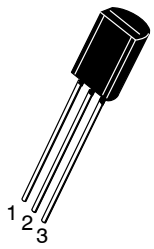
Features

- Low Quiescent Bias Current of 75 μA
- Low Input−to−Output Voltage Differential of 50 mV at 100 μA and 380 mV at 100 mA
- 5.0 V, 3.3 V or 3.0 V ±0.5% Allows Use as a Regulator or Reference
- Extremely Tight Line and Load Regulation
- Requires Only a 1.0 μF Output Capacitor for Stability
- Internal Current and Thermal Limiting
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free and RoHS Compliant

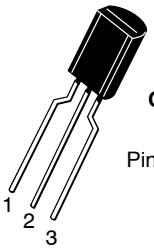
LP2951 Additional Features

- $\overline{\text{Error}}$ Output Signals an Out of Regulation Condition
- Output Programmable from 1.25 V to 29 V
- Logic Level Shutdown Input

(See Following Page for Device Information.)



STRAIGHT LEAD

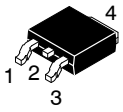


BENT LEAD

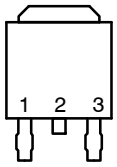
TO−92
CASE 29−10

Pin: 1. Output
2. Ground
3. Input

PIN CONNECTIONS



DPAK
CASE 369C



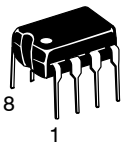
(Top View)

Pin: 1. Input
2. Ground
3. Output

Heatsink surface (shown as terminal 4 in case outline drawing) is connected to Pin 2.

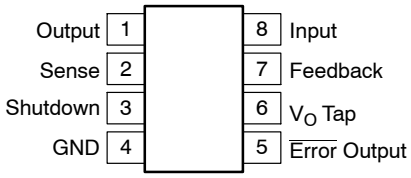
SOIC−8
CASE 751

PDIP−8
CASE 626



Micro8
CASE 846A

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on pages 14 and 15 of this data sheet.

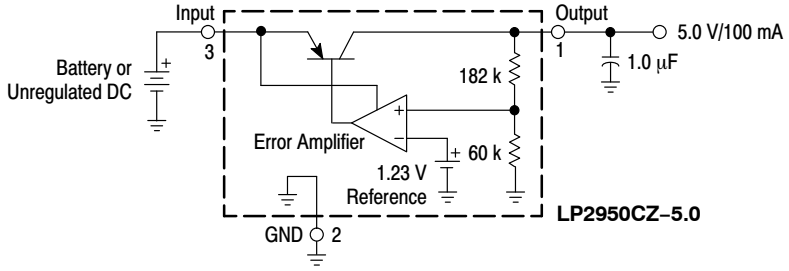
DEVICE MARKING INFORMATION

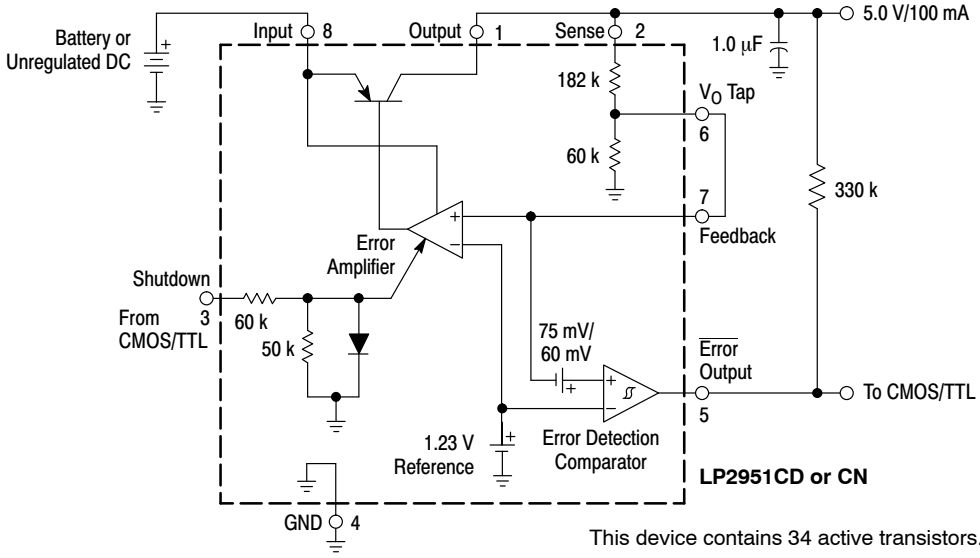
See general marking information in the device marking section on page 16 of this data sheet.

DEVICE INFORMATION

Package	Output Voltage				Operating Ambient Temperature Range
	3.0 V	3.3 V	5.0 V	Adjustable	
TO−92 Suffix Z	LP2950ACZ−3.0G	LP2950ACZ−3.3G	LP2950ACZ−5.0G	Not Available	T_A = −40° to +125°C
	LP2950ACZ−3.0RAG	LP2950ACZ−3.3RAG	LP2950ACZ−5.0RAG		
	LP2950CZ−3.0G	LP2950CZ−3.3G	LP2950CZ−5.0G		
	LP2950CZ−3.0RAG	LP2950CZ−3.3RAG	LP2950CZ−5.0RAG		
			LP2950CZ−5.0RPG		
DPAK Suffix DT	LP2950CDT−3.0RKG	LP2950ACDT−3.3RG	LP2950ACDT−5.0G	Not Available	T_A = −40° to +125°C
		LP2950CDT−3.3G	LP2950ACDT−5RKG		
		LP2950CDT−3.3RKG	LP2950CDT−5.0G		
			LP2950CDT−5.0RKG		
SOIC−8 Suffix D	LP2951ACD−3.0R2G	LP2951ACD−3.3R2G	LP2951ACDR2G	LP2951ACDR2G	T_A = −40° to +125°C
	LP2951CD−3.0R2G	LP2951CD−3.3R2G	LP2951CDR2G	LP2951CDR2G	
		NCV2951ACD−3.3R2G*	NCV2951ACDR2G*	NCV2951ACDR2G*	
			NCV2951CDR2G*	NCV2951CDR2G*	
Micro8 Suffix DM	LP2951ACDM−3.0RG	LP2951ACDM−3.3RG	LP2951ACDMR2G	LP2951ACDMR2G	T_A = −40° to +125°C
			LP2951CDMR2G	LP2951CDMR2G	
			NCV2951ACDMR2G*	NCV2951ACDMR2G*	

*NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.
LP2950Cx−xx / LP2951Cxx−xx / NCV2951Cx−xx 1% Output Voltage Precision at T_A = 25°C
LP2950ACx−xx / LP2951ACxx−xx / NCV2951Ax−xx 0.5% Output Voltage Precision at T_A = 25°C





This device contains 34 active transistors.

Figure 1. Representative Block Diagrams

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage	V_{CC}	30	Vdc
Peak Transient Input Voltage (t < 300 ms)	V_{CC}	32	Vdc
Power Dissipation and Thermal Characteristics			
Maximum Power Dissipation	P_D	Internally Limited	W
Case 751(SOIC−8) D Suffix			
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	180	°C/W
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	45	°C/W
Case 369A (DPAK) DT Suffix (Note 1)			
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	92	°C/W
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	6.0	°C/W
Case 29 (TO−226AA/TO−92) Z Suffix			
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	160	°C/W
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	83	°C/W
Case 626 N Suffix			
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	105	°C/W
Case 846A (Micro8) DM Suffix			
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	240	°C/W
Feedback Input Voltage	V_{fb}	−1.5 to +30	Vdc
Shutdown Input Voltage	V_{sd}	−0.3 to +30	Vdc
Error Comparator Output Voltage	V_{err}	−0.3 to +30	Vdc
Operating Ambient Temperature Range	T_A	−40 to +125	°C
Maximum Die Junction Temperature Range	T_J	+150	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

ELECTRICAL CHARACTERISTICS

(V_{in} = V_O + 1.0 V, I_O = 100 μA, C_O = 1.0 μF, T_A = 25°C [Note 3], unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage, 5.0 V Versions	V_O				V
V_{in} = 6.0 V, I_O = 100 μA, T_A = 25°C					
LP2950C−5.0/LP2951C/NCV2951C*		4.950	5.000	5.050	
LP2950AC−5.0/LP2951AC/NCV2951AC*		4.975	5.000	5.025	
T_A = −40 to +125°C					
LP2950C−5.0/LP2951C/NCV2951C*		4.900	–	5.100	
LP2950AC−5.0/LP2951AC/NCV2951AC*		4.940	–	5.060	
V_{in} = 6.0 to 30 V, I_O = 100 μA to 100 mA, T_A = −40 to +125°C					
LP2950C−5.0/LP2951C/NCV2951C*		4.880	–	5.120	
LP2950AC−5.0/LP2951AC/NCV2951AC*		4.925	–	5.075	
Output Voltage, 3.3 V Versions	V_O				V
V_{in} = 4.3 V, I_O = 100 μA, T_A = 25°C					
LP2950C−3.3/LP2951C−3.3		3.267	3.300	3.333	
LP2950AC−3.3/LP2951AC−3.3/NCV2951AC−3.3*		3.284	3.300	3.317	
T_A = −40 to +125°C					
LP2950C−3.3/LP2951C−3.3		3.234	–	3.366	
LP2950AC−3.3/LP2951AC−3.3/NCV2951AC−3.3*		3.260	–	3.340	
V_{in} = 4.3 to 30 V, I_O = 100 μA to 100 mA, T_A = −40 to +125°C					
LP2950C−3.3/LP2951C−3.3		3.221	–	3.379	
LP2950AC−3.3/LP2951AC−3.3/NCV2951AC−3.3*		3.254	–	3.346	
Output Voltage, 3.0 V Versions	V_O				V
V_{in} = 4.0 V, I_O = 100 μA, T_A = 25°C					
LP2950C−3.0/LP2951C−3.0		2.970	3.000	3.030	
LP2950AC−3.0/LP2951AC−3.0		2.985	3.000	3.015	
T_A = −40 to +125°C					
LP2950C−3.0/LP2951C−3.0		2.940	–	3.060	
LP2950AC−3.0/LP2951AC−3.0		2.964	–	3.036	
V_{in} = 4.0 to 30 V, I_O = 100 μA to 100 mA, T_A = −40 to +125°C					
LP2950C−3.0/LP2951C−3.0		2.928	–	3.072	
LP2950AC−3.0/LP2951AC−3.0		2.958	–	3.042	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. The Junction−to−Ambient Thermal Resistance is determined by PCB copper area per Figure 29.
2. This device series contains ESD protection and exceeds the following tests:
   Human Body Model (HBM), 2000 V, Class 2, JESD22 A114−C
   Machine Model (MM), 200 V, Class B, JESD22 A115−A
   Charged Device Model (CDM), 2000 V, Class IV, JESD22 C101−C
3. Low duty pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
4. $V_{O(nom)}$ is the part number voltage option.
5. Noise tests on the LP2951 are made with a 0.01 μF capacitor connected across Pins 7 and 1.
6. Latch−up Current Maximum Rating tested per JEDEC standard: JESD78
   − Inputs Low: passing positive current 100 mA and negative current −100 mA
   − Inputs High: passing positive current 100 mA and negative current −10 mA.

*NCV prefix is for automotive and other applications requiring site and change control.

ELECTRICAL CHARACTERISTICS (continued)
(V_{in} = V_O + 1.0 V, I_O = 100 μA, C_O = 1.0 μF, T_A = 25°C [Note 9], unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Line Regulation (V_{in} = $V_{O(nom)}$ +1.0 V to 30 V) (Note 10)	Reg_{line}				%
LP2950C−XX/LP2951C/LP2951C−XX/NCV2951C*		–	0.08	0.20	
LP2950AC−XX/LP2951AC/LP2951AC−XX/NCV2951AC*		–	0.04	0.10	
Load Regulation (I_O = 100 μA to 100 mA)	Reg_{load}				%
LP2950C−XX/LP2951C/LP2951C−XX/NCV2951C*		–	0.13	0.20	
LP2950AC−XX/LP2951AC/LP2951AC−XX/NCV2951AC*		–	0.05	0.10	
Dropout Voltage	$V_I - V_O$				mV
I_O = 100 μA		–	30	80	
I_O = 100 mA		–	350	450	
Supply Bias Current	I_{CC}				
I_O = 100 μA		–	93	120	μA
I_O = 100 mA		–	4.0	12	mA
Dropout Supply Bias Current (V_{in} = $V_{O(nom)}$ − 0.5 V, I_O = 100 μA) (Note 10)	$I_{CCdropout}$	–	110	170	μA
Current Limit (V_O Shorted to Ground)	I_{Limit}	–	220	300	mA
Thermal Regulation	$Reg_{thermal}$	–	0.05	0.20	%/W
Output Noise Voltage (10 Hz to 100 kHz) (Note 11)	V_n				μVrms
C_L = 1.0 μF		–	126	–	
C_L = 100 μF		–	56	–	
LP2951A/LP2951AC Only					
Reference Voltage (T_A = 25°C)	V_{ref}				V
LP2951C/LP2951C−XX/NCV2951C*		1.210	1.235	1.260	
LP2951AC/LP2951AC−XX/NCV2951AC*		1.220	1.235	1.250	
Reference Voltage (T_A = −40 to +125°C)	V_{ref}				V
LP2951C/LP2951C−XX/NCV2951C*		1.200	–	1.270	
LP2951AC/LP2951AC−XX/NCV2951AC*		1.200	–	1.260	
Reference Voltage (T_A = −40 to +125°C)	V_{ref}				V
I_O = 100 μA to 100 mA, V_{in} = 23 to 30 V					
LP2951C/LP2951C−XX/NCV2951C*		1.185	–	1.285	
LP2951AC/LP2951AC−XX/NCV2951AC*		1.190	–	1.270	
Feedback Pin Bias Current	I_{FB}	–	15	40	nA
Error Comparator					
Output Leakage Current (V_{OH} = 30 V)	I_{lkg}	–	0.01	1.0	μA
Output Low Voltage (V_{in} = 4.5 V, I_{OL} = 400 μA)	V_{OL}	–	150	250	mV
Upper Threshold Voltage (V_{in} = 6.0 V)	V_{thu}	40	45	–	mV
Lower Threshold Voltage (V_{in} = 6.0 V)	V_{thl}	–	60	95	mV
Hysteresis (V_{in} = 6.0 V)	V_{hy}	–	15	–	mV
Shutdown Input					
Input Logic Voltage	V_{shtdn}				V
Logic “0” (Regulator “On”)		0	–	0.7	
Logic “1” (Regulator “Off”)		2.0	–	30	
Shutdown Pin Input Current	I_{shtdn}				μA
V_{shtdn} = 2.4 V		–	35	50	
V_{shtdn} = 30 V		–	450	600	
Regulator Output Current in Shutdown Mode (V_{in} = 30 V, V_{shtdn} = 2.0 V, V_O = 0, Pin 6 Connected to Pin 7)	I_{off}	–	3.0	10	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7. The Junction−to−Ambient Thermal Resistance is determined by PCB copper area per Figure 29.
8. ESD data available upon request.
9. Low duty pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
10. $V_{O(nom)}$ is the part number voltage option.
11. Noise tests on the LP2951 are made with a 0.01 μF capacitor connected across Pins 7 and 1.

*NCV prefix is for automotive and other applications requiring site and change control.

DEFINITIONS

Dropout Voltage – The input/output voltage differential at which the regulator output no longer maintains regulation against further reductions in input voltage. Measured when the output drops 100 mV below its nominal value (which is measured at 1.0 V differential), dropout voltage is affected by junction temperature, load current and minimum input supply requirements.

Line Regulation – The change in output voltage for a change in input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that average chip temperature is not significantly affected.

Load Regulation – The change in output voltage for a change in load current at constant chip temperature.

Maximum Power Dissipation – The maximum total device dissipation for which the regulator will operate within specifications.

Bias Current – Current which is used to operate the regulator chip and is not delivered to the load.

Output Noise Voltage – The RMS ac voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

Leakage Current – Current drawn through a bipolar transistor collector−base junction, under a specified collector voltage, when the transistor is “off”.

Upper Threshold Voltage – Voltage applied to the comparator input terminal, below the reference voltage which is applied to the other comparator input terminal, which causes the comparator output to change state from a logic “0” to “1”.

Lower Threshold Voltage – Voltage applied to the comparator input terminal, below the reference voltage which is applied to the other comparator input terminal, which causes the comparator output to change state from a logic “1” to “0”.

Hysteresis – The difference between Lower Threshold voltage and Upper Threshold voltage.

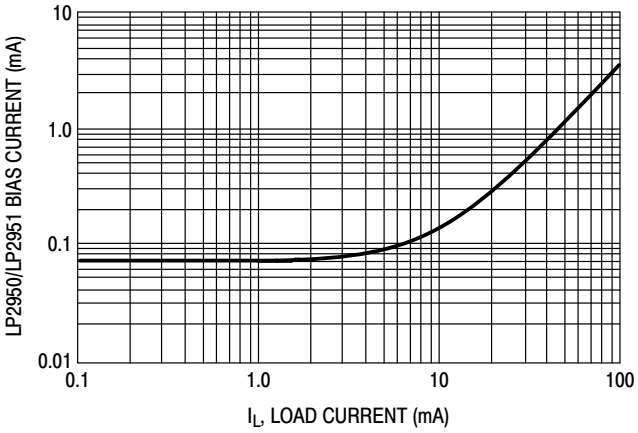


Figure 2. Quiescent Current

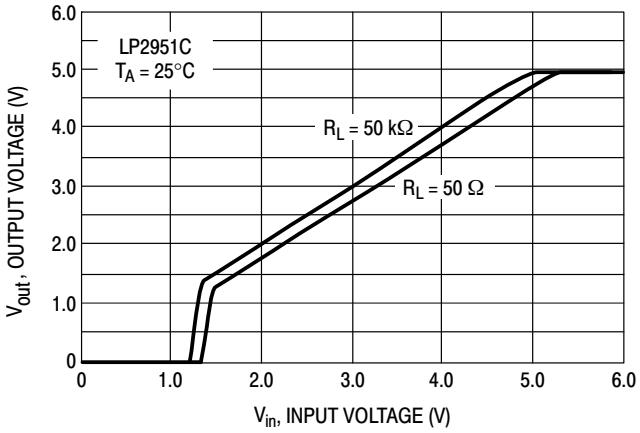


Figure 3. 5.0 V Dropout Characteristics over Load

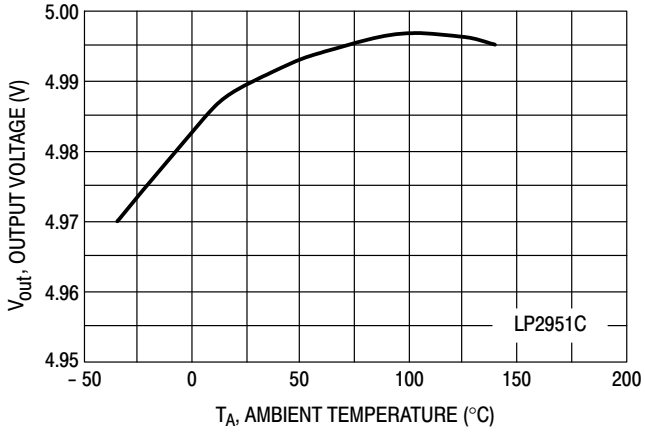


Figure 4. Output Voltage versus Temperature

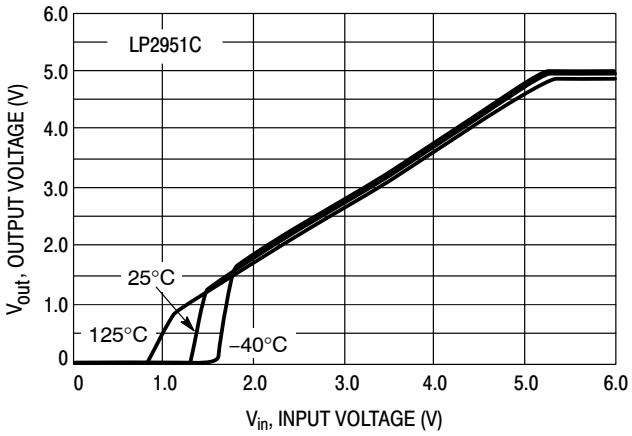


Figure 5. 5.0 V Dropout Characteristics with R_L = 50 Ω

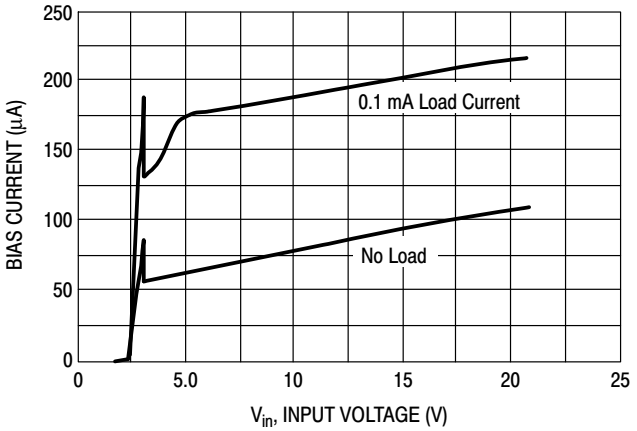


Figure 6. Input Current

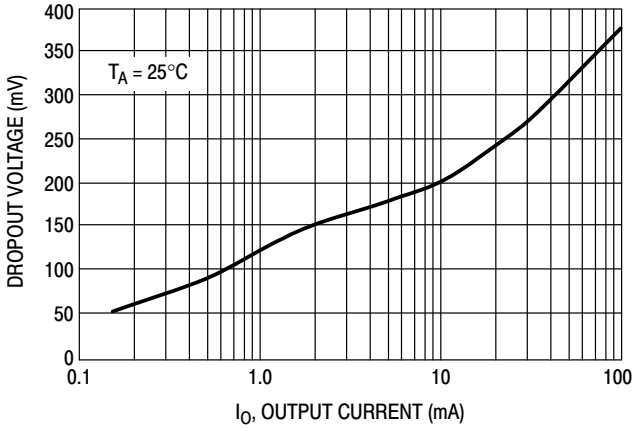


Figure 7. Dropout Voltage versus Output Current

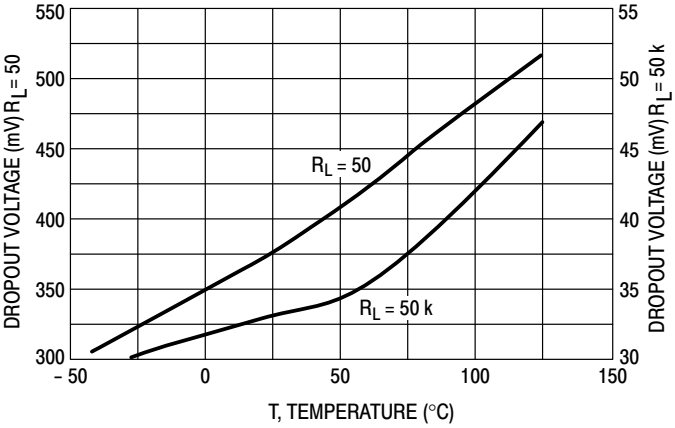


Figure 8. Dropout Voltage versus Temperature

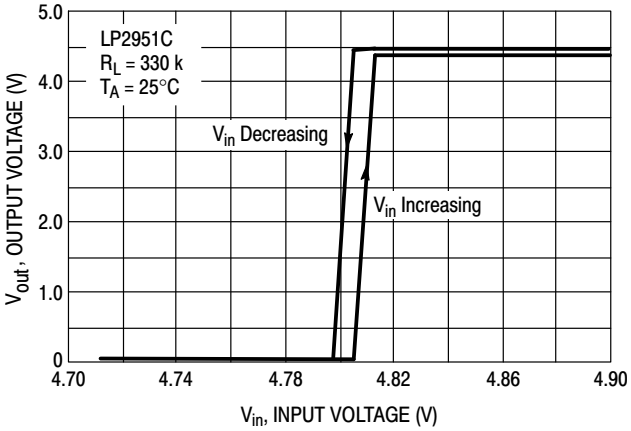


Figure 9. Error Comparator Output

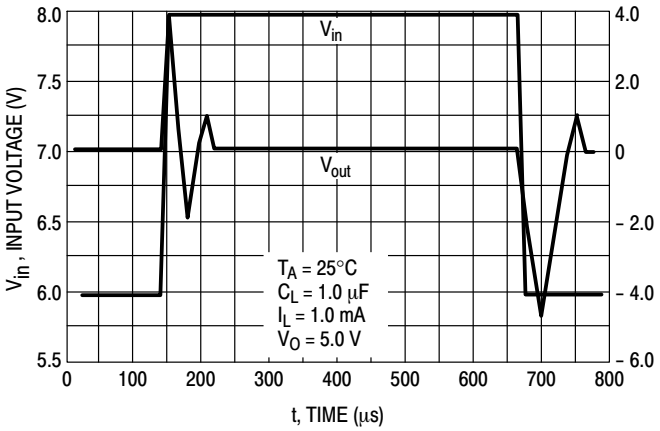


Figure 10. Line Transient Response

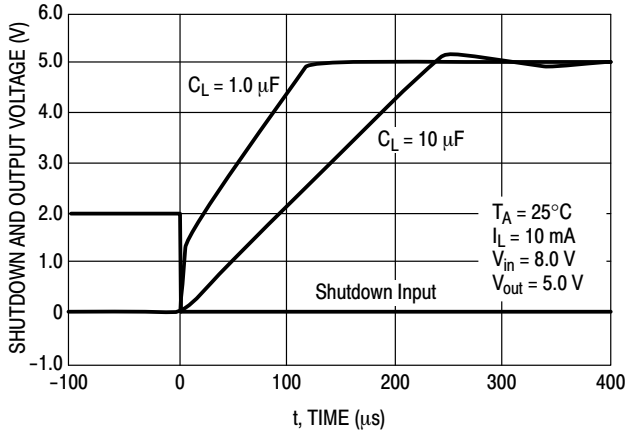


Figure 11. LP2951 Enable Transient

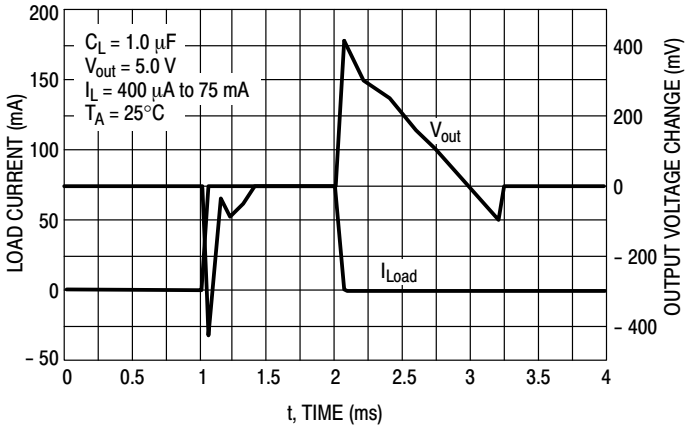


Figure 12. Load Transient Response

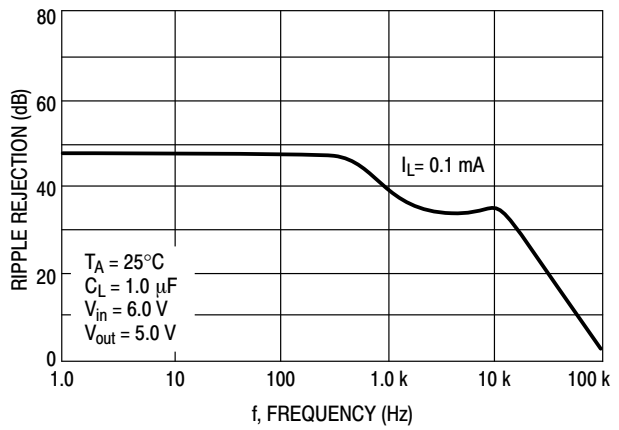


Figure 13. Ripple Rejection

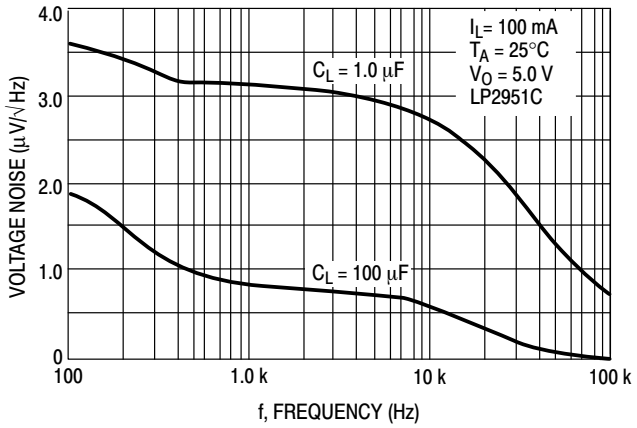


Figure 14. Output Noise

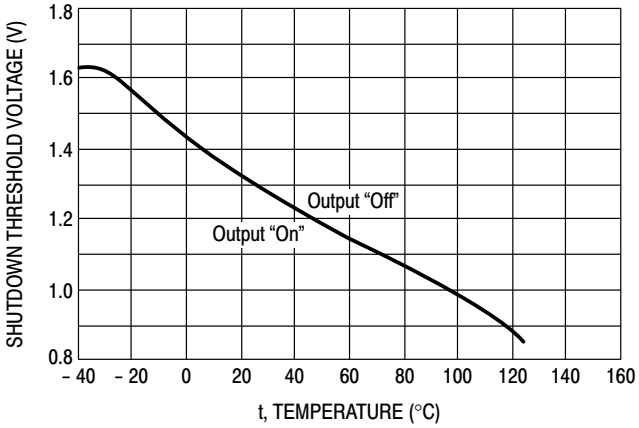


Figure 15. Shutdown Threshold Voltage versus Temperature

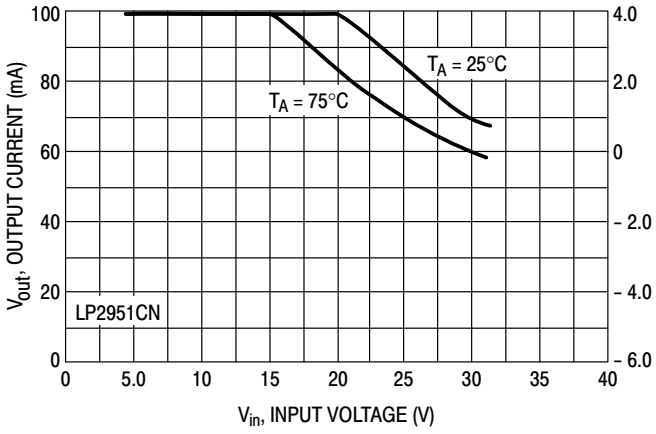


Figure 16. Maximum Rated Output Current

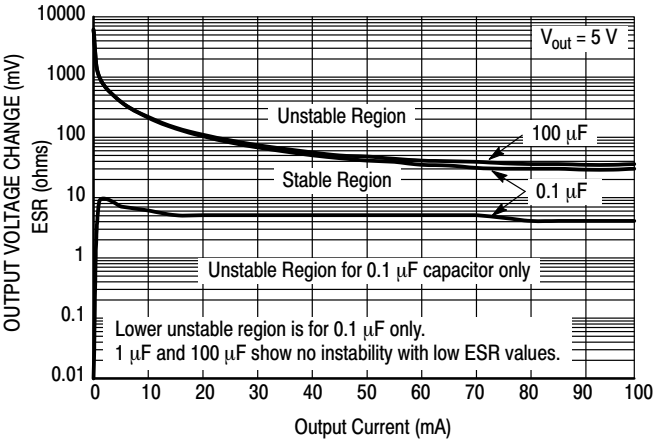


Figure 17. Output Stability versus Output Capacitor Change

APPLICATIONS INFORMATION

Introduction

The LP2950/LP2951 regulators are designed with internal current limiting and thermal shutdown making them user−friendly. Typical application circuits for the LP2950 and LP2951 are shown in Figures 20 through 28.

These regulators are not internally compensated and thus require a 1.0 μF (or greater) capacitance between the LP2950/LP2951 output terminal and ground for stability. Most types of aluminum, tantalum or multilayer ceramic will perform adequately. Solid tantalums or appropriate multilayer ceramic capacitors are recommended for operation below 25°C.

At lower values of output current, less output capacitance is required for output stability. The capacitor can be reduced to 0.33 μF for currents less than 10 mA, or 0.1 μF for currents below 1.0 mA. Using the 8 pin versions at voltages less than 5.0 V operates the error amplifier at lower values of gain, so that more output capacitance is needed for stability. For the worst case operating condition of a 100 mA load at 1.23 V output (output Pin 1 connected to the feedback Pin 7) a minimum capacitance of 3.3 μF is recommended.

The LP2950 will remain stable and in regulation when operated with no output load. When setting the output voltage of the LP2951 with external resistors, the resistance values should be chosen to draw a minimum of 1.0 μA.

A bypass capacitor is recommended across the LP2950/LP2951 input to ground if more than 4 inches of wire connects the input to either a battery or power supply filter capacitor.

Input capacitance at the LP2951 Feedback Pin 7 can create a pole, causing instability if high value external resistors are used to set the output voltage. Adding a 100 pF capacitor between the Output Pin 1 and the Feedback Pin 7 and increasing the output filter capacitor to at least 3.3 μF will stabilize the feedback loop.

Error Detection Comparator

The comparator switches to a positive logic low whenever the LP2951 output voltage falls more than approximately 5.0% out of regulation. This value is the comparator's designed−in offset voltage of 60 mV divided by the 1.235 V internal reference. As shown in the representative block diagram. This trip level remains 5.0% below normal regardless of the value of regulated output voltage. For example, the error flag trip level is 4.75 V for a normal 5.0 V regulated output, or 9.50 V for a 10 V output voltage.

Figure 2 is a timing diagram which shows the $\overline{\text{ERROR}}$ signal and the regulated output voltage as the input voltage to the LP2951 is ramped up and down. The $\overline{\text{ERROR}}$ signal becomes valid (low) at about 1.3 V input. It goes high when the input reaches about 5.0 V (V_{out} exceeds about 4.75 V). Since the LP2951's dropout voltage is dependent upon the load current (refer to the curve in the Typical Performance Characteristics), the input voltage trip point will vary with load current. The output voltage trip point does not vary with load.

The error comparator output is an open collector which requires an external pullup resistor. This resistor may be returned to the output or some other voltage within the system. The resistance value should be chosen to be consistent with the 400 μA sink capability of the error comparator. A value between 100 kΩ and 1.0 MΩ is suggested. No pullup resistance is required if this output is unused.

When operated in the power down mode (V_{in} = 0 V), the error comparator output will go high if it has been pulled up to an external supply (the output transistor is in high impedance state). To avoid this invalid response, the error comparator output should be pulled up to V_{out} (see Figure 18).

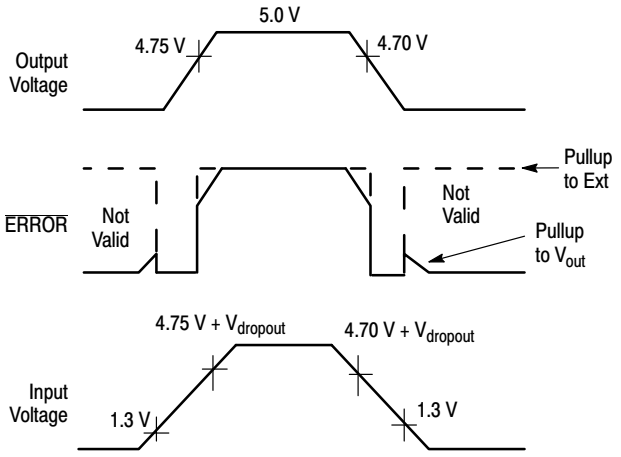


Figure 18. $\overline{\text{ERROR}}$ Output Timing

Programming the Output Voltage (LP2951)

The LP2951CX may be pin−strapped for the nominal fixed output voltage using its internal voltage divider by tying Pin 1 (output) to Pin 2 (sense) and Pin 7 (feedback) to Pin 6 (5.0 V tap). Alternatively, it may be programmed for any output voltage between its 1.235 reference voltage and its 30 V maximum rating. An external pair of resistors is required, as shown in Figure 19.

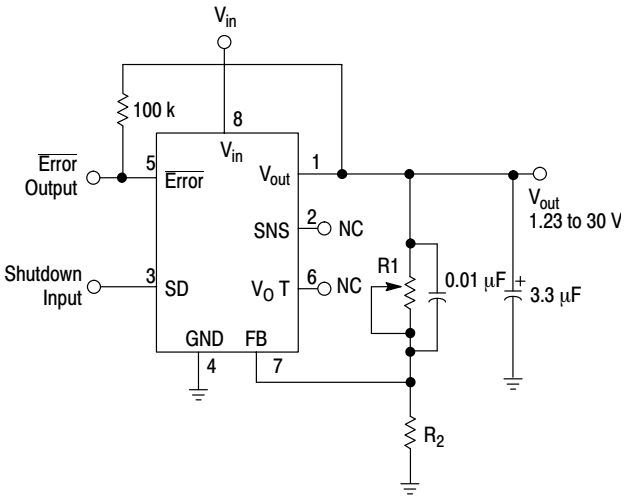


Figure 19. Adjustable Regulator

The complete equation for the output voltage is:

$$V_{out} = V_{ref}(1 + R1/R2) + I_{FB} R1$$

where V_{ref} is the nominal 1.235 V reference voltage and I_{FB} is the feedback pin bias current, nominally −20 nA. The minimum recommended load current of 1.0 μA forces an upper limit of 1.2 MΩ on the value of R2, if the regulator must work with no load. I_{FB} will produce a 2% typical error in V_{out} which may be eliminated at room temperature by adjusting R1. For better accuracy, choosing R2 = 100 k reduces this error to 0.17% while increasing the resistor program current to 12 μA. Since the LP2951 typically draws 75 μA at no load with Pin 2 open circuited, the extra 12 μA of current drawn is often a worthwhile tradeoff for eliminating the need to set output voltage in test.

Output Noise

In many applications it is desirable to reduce the noise present at the output. Reducing the regulator bandwidth by increasing the size of the output capacitor is the only method for reducing noise on the 3 lead LP2950. However, increasing the capacitor from 1.0 μF to 220 μF only decreases the noise from 430 μV to 160 μVrms for a 100 kHz bandwidth at the 5.0 V output.

Noise can be reduced fourfold by a bypass capacitor across R1, since it reduces the high frequency gain from 4 to unity. Pick

$$C_{Bypass} \approx \frac{1}{2\pi R1 \times 200\ Hz}$$

or about 0.01 μF. When doing this, the output capacitor must be increased to 3.3 μF to maintain stability. These changes reduce the output noise from 430 μV to 126 μVrms for a 100 kHz bandwidth at 5.0 V output. With bypass capacitor added, noise no longer scales with output voltage so that improvements are more dramatic at higher output voltages.

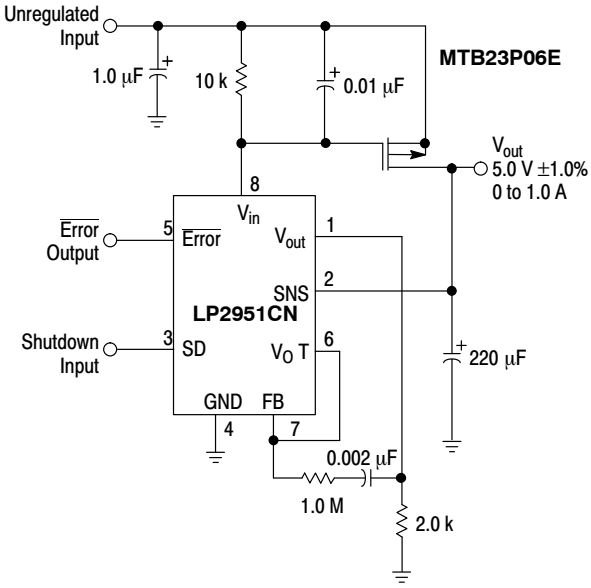


Figure 20. 1.0 A Regulator with 1.2 V Dropout

TYPICAL APPLICATIONS

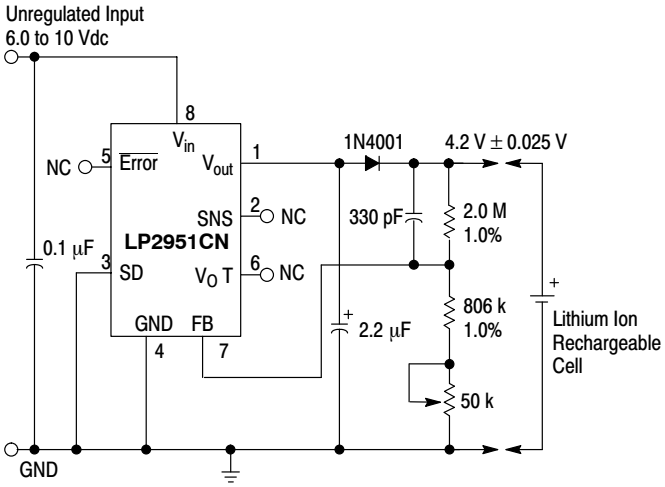


Figure 21. Lithium Ion Battery Cell Charger

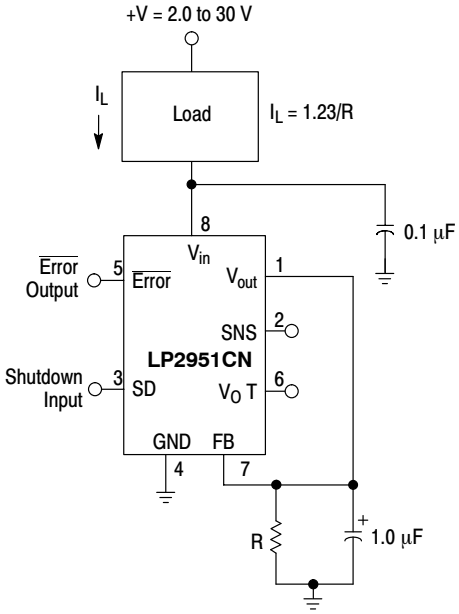
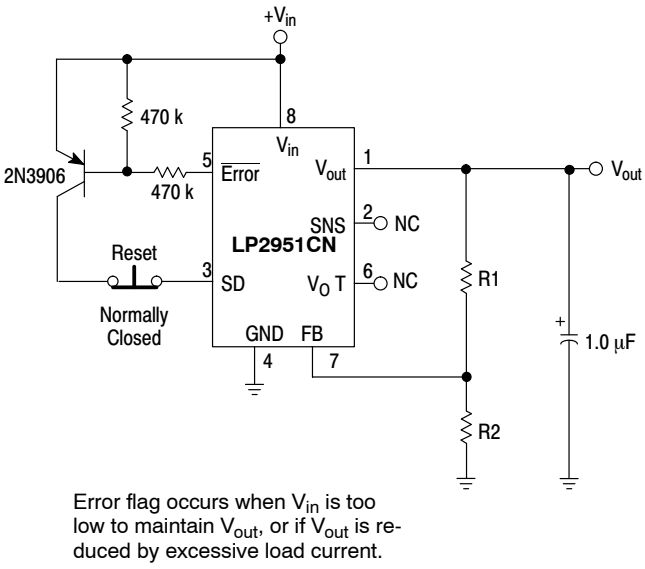


Figure 22. Low Drift Current Sink



Error flag occurs when V_{in} is too low to maintain V_{out}, or if V_{out} is reduced by excessive load current.

Figure 23. Latch Off When Error Flag Occurs

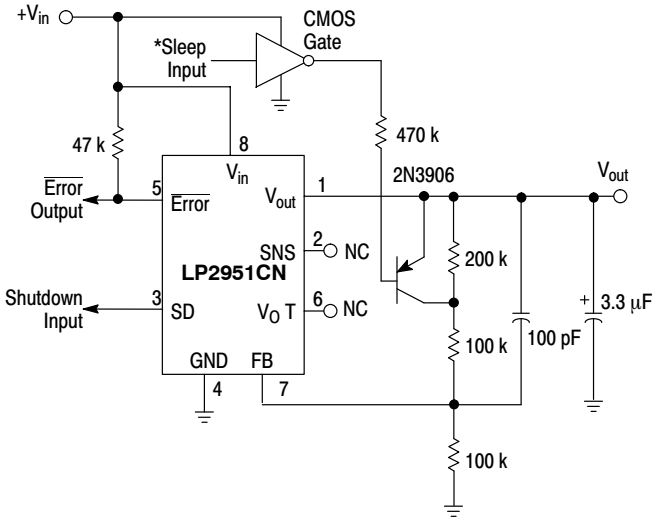
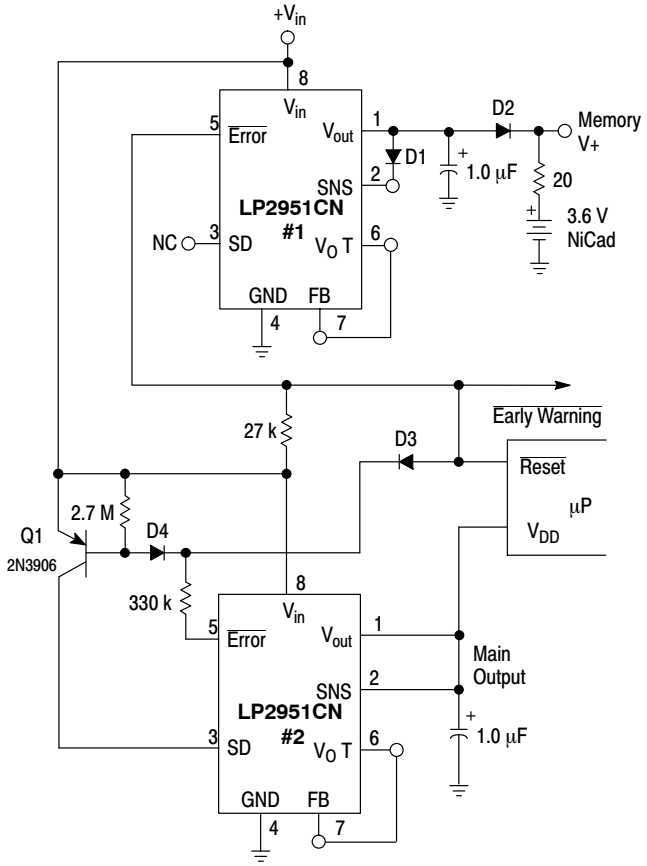


Figure 24. 5.0 V Regulator with 2.5 V Sleep Function



All diodes are 1N4148.

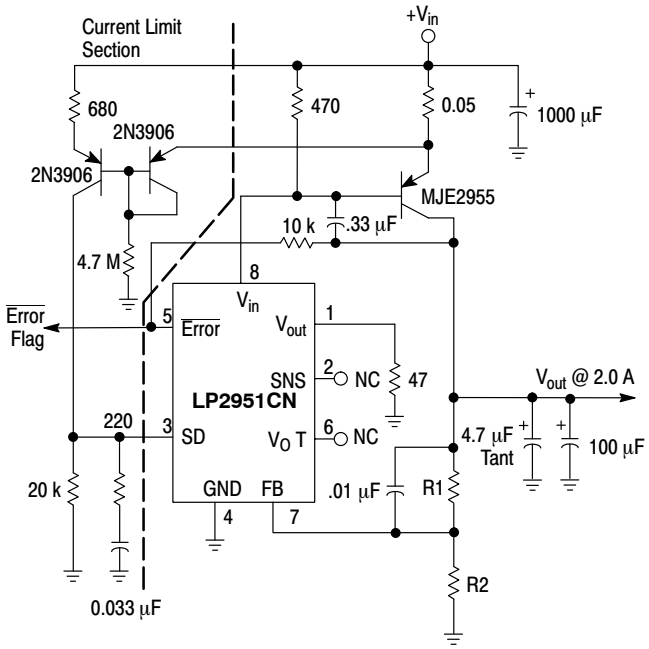
Early Warning flag on low input voltage.

Main output latches off at lower input voltages.

Battery backup on auxiliary output.

Operation: Regulator #1's V_{out} is programmed one diode drop above 5.0 V. Its error flag becomes active when $V_{in} \leq 5.7$ V. When V_{in} drops below 5.3 V, the error flag of regulator #2 becomes active and via Q1 latches the main output "off". When V_{in} again exceeds 5.7 V, regulator #1 is back in regulation and the early warning signal rises, unlatching regulator #2 via D3.

Figure 25. Regulator with Early Warning and Auxiliary Output



$V_{out} = 1.25V\ (1.0 + R1/R2)$

For 5.0 V output, use internal resistors. Wire Pin 6 to 7, and wire Pin 2 to $+V_{out}$ Bus.

Figure 26. 2.0 A Low Dropout Regulator

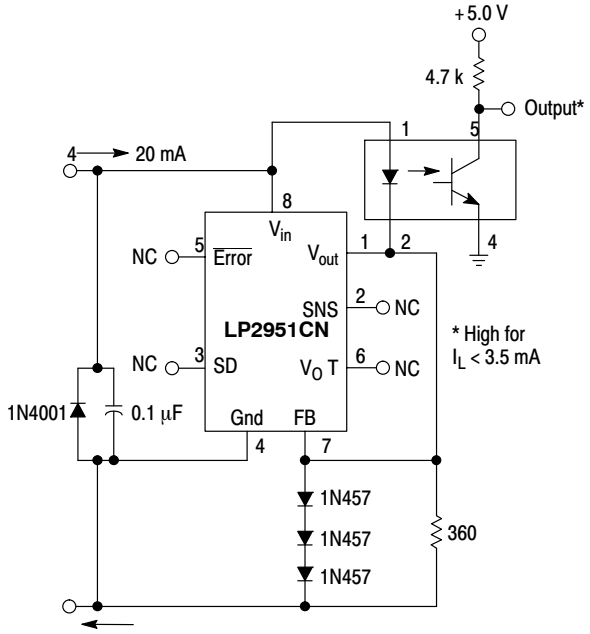


Figure 27. Open Circuit Detector for 4.0 to 20 mA Current Loop

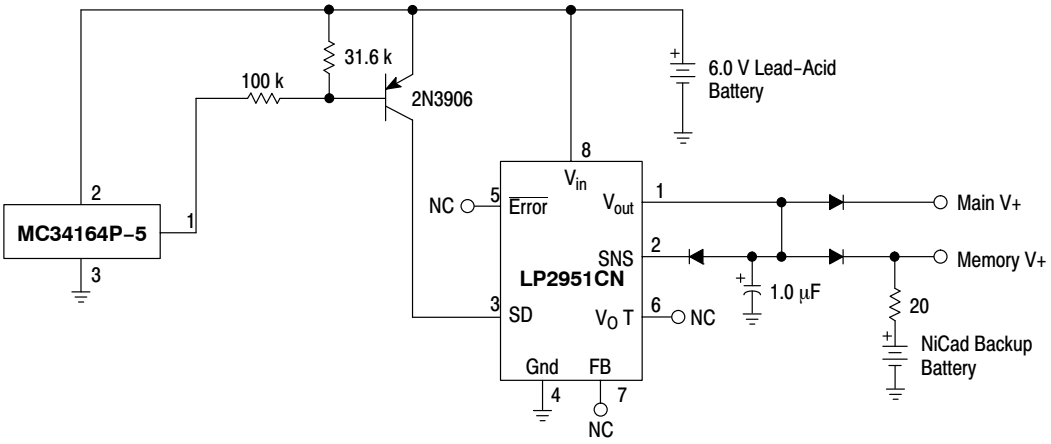


Figure 28. Low Battery Disconnect

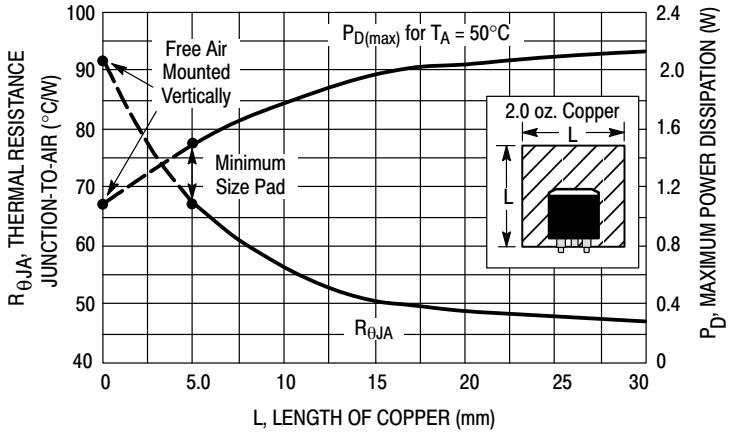


Figure 29. DPAK Thermal Resistance and Maximum Power Dissipation versus PCB Copper Length

ORDERING INFORMATION (LP2950)

Part Number	Output Voltage (Volts)	Tolerance (%)	Package	Shipping†
LP2950CZ−3.0G	3.0	1.0	TO−92 (Pb−Free)	2000 Units / Bag
LP2950CZ−3.0RAG	3.0	1.0	TO−92 (Pb−Free)	2000 Units / Tape & Reel
LP2950ACZ−3.0G	3.0	0.5	TO−92 (Pb−Free)	2000 Units / Bag
LP2950ACZ−3.0RAG	3.0	0.5	TO−92 (Pb−Free)	2000 Units / Tape & Reel
LP2950CZ−3.3G	3.3	1.0	TO−92 (Pb−Free)	2000 Units / Bag
LP2950CZ−3.3RAG	3.3	1.0	TO−92 (Pb−Free)	2000 Units / Tape & Reel
LP2950ACZ−3.3G	3.3	0.5	TO−92 (Pb−Free)	2000 Units / Bag
LP2950ACZ−3.3RAG	3.3	0.5	TO−92 (Pb−Free)	2000 Units / Tape & Reel
LP2950CZ−5.0G	5.0	1.0	TO−92 (Pb−Free)	2000 Units / Bag
LP2950CZ−5.0RAG	5.0	1.0	TO−92 (Pb−Free)	2000 Units / Tape & Reel
LP2950CZ−5.0RPG	5.0	1.0	TO−92 (Pb−Free)	2000 Units / Ammo Pack
LP2950ACZ−5.0G	5.0	0.5	TO−92 (Pb−Free)	2000 Units / Bag
LP2950ACZ−5.0RAG	5.0	0.5	TO−92 (Pb−Free)	2000 Units / Tape & Reel
LP2950CDT−3.0RKG	3.0	1.0	DPAK (Pb−Free)	2500 Units / Tape & Reel
LP2950CDT−3.3G	3.3	1.0	DPAK (Pb−Free)	75 Units / Rail
LP2950CDT−3.3RKG	3.3	1.0	DPAK (Pb−Free)	2500 Units / Tape & Reel
LP2950ACDT−3.3RG	3.3	0.5	DPAK (Pb−Free)	2500 Units / Tape & Reel
LP2950CDT−5.0G	5.0	1.0	DPAK (Pb−Free)	75 Units / Rail
LP2950CDT−5.0RKG	5.0	1.0	DPAK (Pb−Free)	2500 Units / Tape & Reel
LP2950ACDT−5.0G	5.0	0.5	DPAK (Pb−Free)	75 Units / Rail
LP2950ACDT−5RKG	5.0	0.5	DPAK (Pb−Free)	2500 Units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ORDERING INFORMATION (LP2951)

Part Number	Output Voltage (Volts)	Tolerance (%)	Package	Shipping†
LP2951CD−3.0R2G	3.0	1.0	SOIC−8 (Pb−Free)	2500 Units / Tape & Reel
LP2951ACD−3.0R2G	3.0	0.5	SOIC−8 (Pb−Free)	2500 Units / Tape & Reel
LP2951CD−3.3R2G	3.3	1.0	SOIC−8 (Pb−Free)	2500 Units / Tape & Reel
LP2951ACD−3.3G	3.3	0.5	SOIC−8 (Pb−Free)	98 Units / Rail
LP2951ACD−3.3R2G	3.3	0.5	SOIC−8 (Pb−Free)	2500 Units / Tape & Reel
LP2951CDG	5.0 or Adj.	1.0	SOIC−8 (Pb−Free)	98 Units / Rail
LP2951CDR2G	5.0 or Adj.	1.0	SOIC−8 (Pb−Free)	2500 Units / Tape & Reel
LP2951ACDG	5.0 or Adj.	0.5	SOIC−8 (Pb−Free)	98 Units / Rail
LP2951ACDR2G	5.0 or Adj.	0.5	SOIC−8 (Pb−Free)	2500 Units / Tape & Reel
LP2951ACDM−3.0RG	3.0	0.5	Micro8 (Pb−Free)	4000 Units / Tape & Reel
LP2951ACDM−3.3RG	3.3	0.5	Micro8 (Pb−Free)	4000 Units / Tape & Reel
LP2951CDMR2G	5.0 or Adj.	1.0	Micro8 (Pb−Free)	4000 Units / Tape & Reel
LP2951ACDMR2G	5.0 or Adj.	0.5	Micro8 (Pb−Free)	4000 Units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

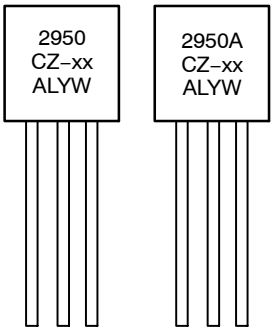
ORDERING INFORMATION (NCV2951)

Part Number	Output Voltage (Volts)	Tolerance (%)	Package	Shipping†
NCV2951ACD3.3R2G*	3.3	0.5	SOIC−8 (Pb−Free)	2500 Units / Tape & Reel
NCV2951ACDR2G*	5.0 or Adj.	0.5	SOIC−8 (Pb−Free)	2500 Units / Tape & Reel
NCV2951CDR2G*	5.0 or Adj.	1.0	SOIC−8 (Pb−Free)	2500 Units / Tape & Reel
NCV2951ACDMR2G*	5.0 or Adj.	0.5	Micro8 (Pb−Free)	4000 Units / Tape & Reel

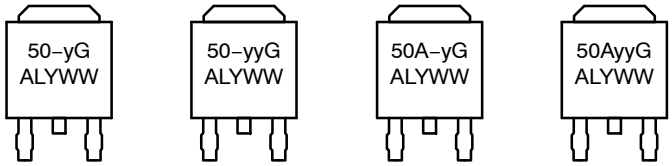
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

MARKING DIAGRAMS

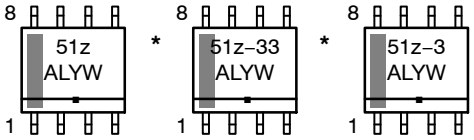
TO−92
CASE 029



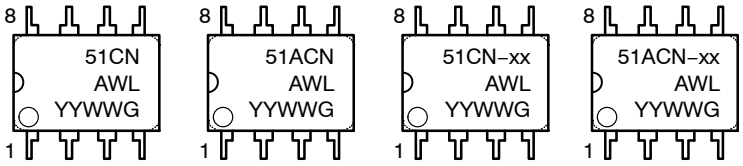
DPAK
CASE 369C



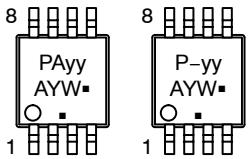
SOIC−8
CASE 751



PDIP−8
CASE 626



Micro8
CASE 846A



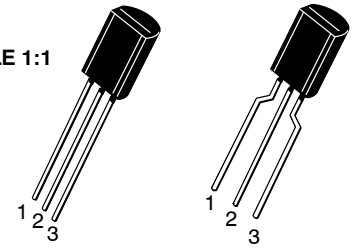
xx = 3.0, 3.3, or 5.0
y = 3 or 5
yy = 30, 33, or 50
z = A or C
A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G = Pb−Free Package
▪ = Pb−Free Package
(Note: Microdot may be in either location)

*This marking diagram also applies to NCV2951.

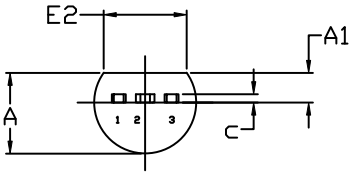
TO−92 (TO−226) 1 WATT
CASE 29−10
ISSUE D

DATE 05 MAR 2021

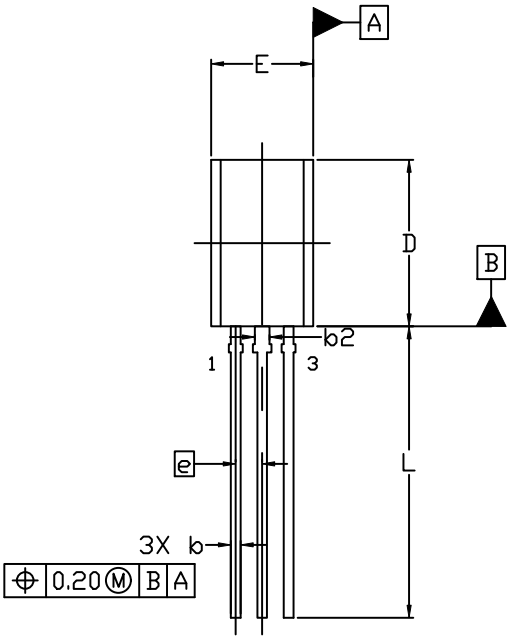
SCALE 1:1



STRAIGHT LEAD



END VIEW



TOP VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR GATE PROTRUSIONS.
4. DIMENSION b AND b2 DOES NOT INCLUDE DAMBAR PROTRUSION. LEAD WIDTH INCLUDING PROTRUSION SHALL NOT EXCEED 0.20. DIMENSION b2 LOCATED ABOVE THE DAMBAR PORTION OF MIDDLE LEAD.

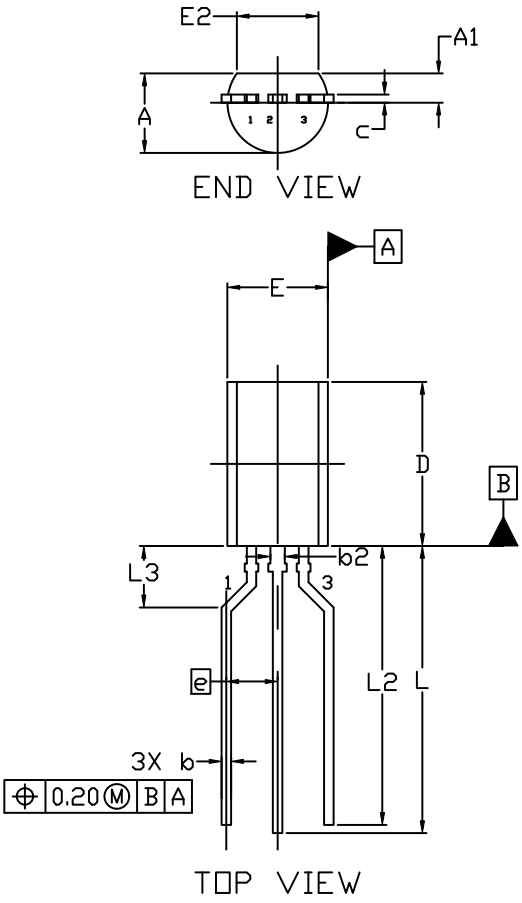
	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	3.75	3.90	4.05
A1	1.28	1.43	1.58
b	0.38	0.465	0.55
b2	0.62	0.70	0.78
c	0.35	0.40	0.45
D	7.85	8.00	8.15
E	4.75	4.90	5.05
E2	3.90	---	---
e	1.27 BSC		
L	13.80	14.00	14.20

STYLES AND MARKING ON PAGE 3

TO−92 (TO−226) 1 WATT
CASE 29−10
ISSUE D

DATE 05 MAR 2021

FORMED LEAD



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR GATE PROTRUSIONS.
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	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	3.75	3.90	4.05
A1	1.28	1.43	1.58
b	0.38	0.465	0.55
b2	0.62	0.70	0.78
c	0.35	0.40	0.45
D	7.85	8.00	8.15
E	4.75	4.90	5.05
E2	3.90	---	---
e	2.50 BSC		
L	13.80	14.00	14.20
L2	13.20	13.60	14.00
L3	3.00 REF		

STYLES AND MARKING ON PAGE 3

TO−92 (TO−226) 1 WATT
CASE 29−10
ISSUE D

DATE 05 MAR 2021

STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

STYLE 2:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 3:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 5:
PIN 1. DRAIN
2. SOURCE
3. GATE

STYLE 6:
PIN 1. GATE
2. SOURCE & SUBSTRATE
3. DRAIN

STYLE 7:
PIN 1. SOURCE
2. DRAIN
3. GATE

STYLE 8:
PIN 1. DRAIN
2. GATE
3. SOURCE & SUBSTRATE

STYLE 9:
PIN 1. BASE 1
2. EMITTER
3. BASE 2

STYLE 10:
PIN 1. CATHODE
2. GATE
3. ANODE

STYLE 11:
PIN 1. ANODE
2. CATHODE & ANODE
3. CATHODE

STYLE 12:
PIN 1. MAIN TERMINAL 1
2. GATE
3. MAIN TERMINAL 2

STYLE 13:
PIN 1. ANODE 1
2. GATE
3. CATHODE 2

STYLE 14:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

STYLE 15:
PIN 1. ANODE 1
2. CATHODE
3. ANODE 2

STYLE 16:
PIN 1. ANODE
2. GATE
3. CATHODE

STYLE 17:
PIN 1. COLLECTOR
2. BASE
3. EMITTER

STYLE 18:
PIN 1. ANODE
2. CATHODE
3. NOT CONNECTED

STYLE 19:
PIN 1. GATE
2. ANODE
3. CATHODE

STYLE 20:
PIN 1. NOT CONNECTED
2. CATHODE
3. ANODE

STYLE 21:
PIN 1. COLLECTOR
2. EMITTER
3. BASE

STYLE 22:
PIN 1. SOURCE
2. GATE
3. DRAIN

STYLE 23:
PIN 1. GATE
2. SOURCE
3. DRAIN

STYLE 24:
PIN 1. EMITTER
2. COLLECTOR/ANODE
3. CATHODE

STYLE 25:
PIN 1. MT 1
2. GATE
3. MT 2

STYLE 26:
PIN 1. V_{CC}
2. GROUND 2
3. OUTPUT

STYLE 27:
PIN 1. MT
2. SUBSTRATE
3. MT

STYLE 28:
PIN 1. CATHODE
2. ANODE
3. GATE

STYLE 29:
PIN 1. NOT CONNECTED
2. ANODE
3. CATHODE

STYLE 30:
PIN 1. DRAIN
2. GATE
3. SOURCE

STYLE 31:
PIN 1. GATE
2. DRAIN
3. SOURCE

STYLE 32:
PIN 1. BASE
2. COLLECTOR
3. EMITTER

STYLE 33:
PIN 1. RETURN
2. INPUT
3. OUTPUT

STYLE 34:
PIN 1. INPUT
2. GROUND
3. LOGIC

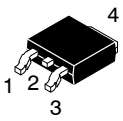
STYLE 35:
PIN 1. GATE
2. COLLECTOR
3. EMITTER

GENERIC MARKING DIAGRAM*

XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

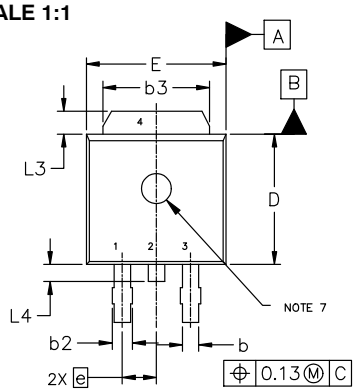
*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.



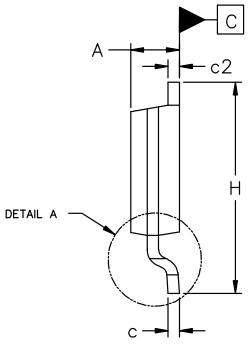
SCALE 1:1

DPAK3 6.10x6.54x2.28, 2.29P
CASE 369C
ISSUE J

DATE 12 AUG 2025

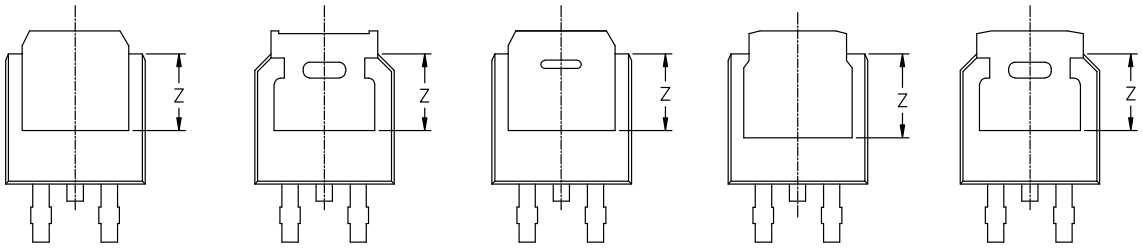


TOP VIEW



SIDE VIEW

MILLIMETERS			
DIM	MIN	NOM	MAX
A	2.18	2.28	2.38
A1	0.00	---	0.13
b	0.63	0.76	0.89
b2	0.72	0.93	1.14
b3	4.57	5.02	5.46
c	0.46	0.54	0.61
c2	0.46	0.54	0.61
D	5.97	6.10	6.22
E	6.35	6.54	6.73
e	2.29 BSC		
H	9.40	9.91	10.41
L	1.40	1.59	1.78
L1	2.90 REF		
L2	0.51 BSC		
L3	0.89	---	1.27
L4	---	---	1.01
Z	3.93	---	---

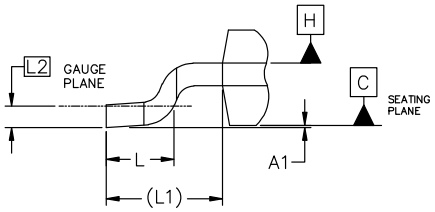


BOTTOM VIEW

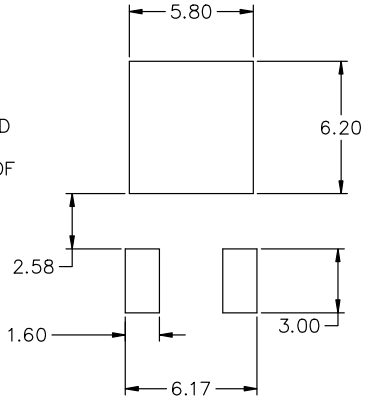
ALTERNATE CONSTRUCTIONS

NOTES:

1. DIMENSIONING AND TOLERANCING ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3, AND Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15mm PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.



DETAIL A
ROTATED 90° CW



RECOMMENDED MOUNTING FOOTPRINT*

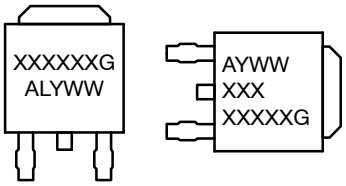
*FOR ADDITIONAL INFORMATION ON OUR PB–FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

DOCUMENT NUMBER:	**98AON10527D**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**DPAK3 6.10x6.54x2.28, 2.29P**	**PAGE 1 OF 2**

DPAK3 6.10x6.54x2.28, 2.29P
CASE 369C
ISSUE J

DATE 12 AUG 2025

GENERIC MARKING DIAGRAM*



IC **Discrete**

XXXXXX	= Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
WW	= Work Week
G	= Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 8:
PIN 1. N/C
2. CATHODE
3. ANODE
4. CATHODE

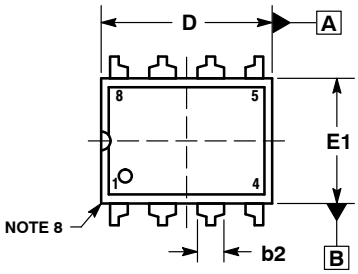
STYLE 9:
PIN 1. ANODE
2. CATHODE
3. RESISTOR ADJUST
4. CATHODE

STYLE 10:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

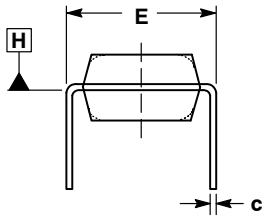
SCALE 1:1

PDIP–8
CASE 626–05
ISSUE P

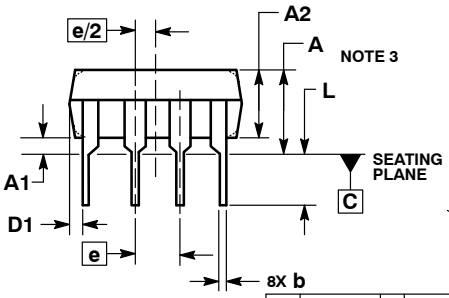
DATE 22 APR 2015



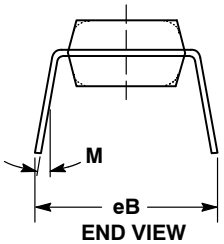
TOP VIEW



END VIEW
WITH LEADS CONSTRAINED
NOTE 5



SIDE VIEW



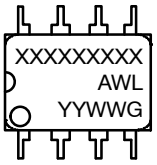
END VIEW
NOTE 6

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS–3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
6. DIMENSION eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	----	0.210	---	5.33
A1	0.015	----	0.38	---
A2	0.115	0.195	2.92	4.95
b	0.014	0.022	0.35	0.56
b2	0.060 TYP		1.52 TYP	
C	0.008	0.014	0.20	0.36
D	0.355	0.400	9.02	10.16
D1	0.005	----	0.13	---
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
eB	----	0.430	---	10.92
L	0.115	0.150	2.92	3.81
M	----	10°	---	10°

STYLE 1:
PIN 1. AC IN
2. DC + IN
3. DC – IN
4. AC IN
5. GROUND
6. OUTPUT
7. AUXILIARY
8. V_{CC}

GENERIC
MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb–Free Package

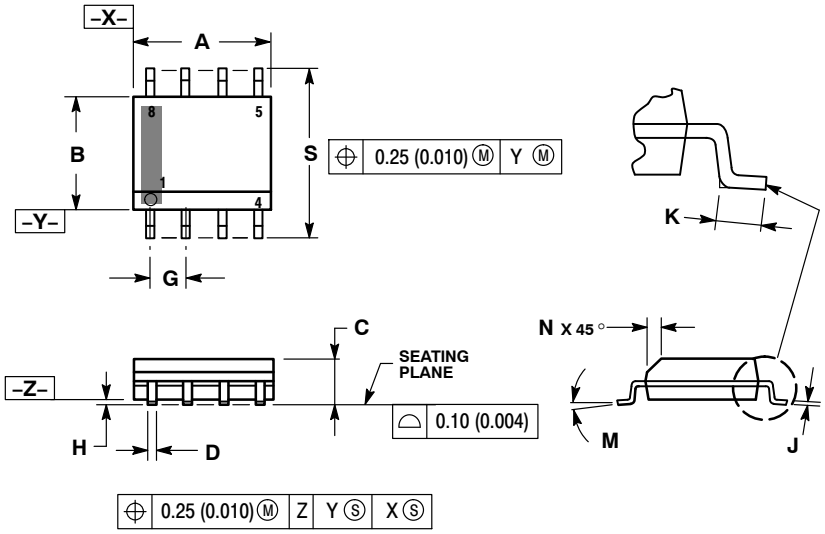
*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	**98ASB42420B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**PDIP–8**	**PAGE 1 OF 1**

SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

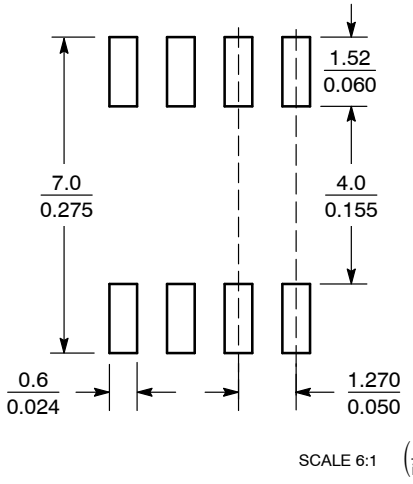
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

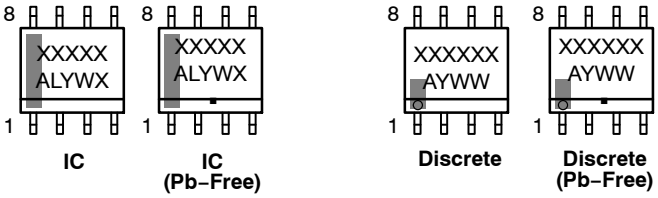
SOLDERING FOOTPRINT*



SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98ASB42564B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	**SOIC−8 NB**		**PAGE 1 OF 2**

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

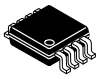
STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

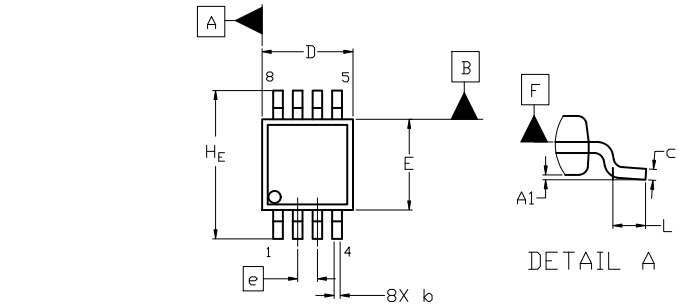
DOCUMENT NUMBER:	**98ASB42564B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	**SOIC−8 NB**		**PAGE 2 OF 2**

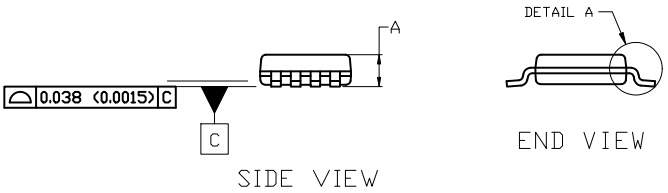


SCALE 2:1

Micro8
CASE 846A–02
ISSUE K

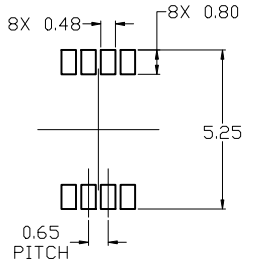
DATE 16 JUL 2020





NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.10 mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER SIDE. DIMENSION E DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm PER SIDE. DIMENSIONS D AND E ARE DETERMINED AT DATUM F.
5. DATUMS A AND B ARE TO BE DETERMINED AT DATUM F.
6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

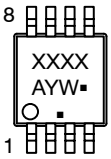


RECOMMENDED
MOUNTING FOOTPRINT

For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	---	---	1.10
A1	0.05	0.08	0.15
b	0.25	0.33	0.40
c	0.13	0.18	0.23
D	2.90	3.00	3.10
E	2.90	3.00	3.10
e	0.65 BSC		
H_E	4.75	4.90	5.05
L	0.40	0.55	0.70

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb–Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 2:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 3:
PIN 1. N-SOURCE
2. N-GATE
3. P-SOURCE
4. P-GATE
5. P-DRAIN
6. P-DRAIN
7. N-DRAIN
8. N-DRAIN

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DESCRIPTION:	**MICRO8**	**PAGE 1 OF 1**

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