

# SN65LBC173, SN75LBC173 Quadruple Low-Power Differential Line Receivers

## 1 Features

- Meets or exceeds the requirements of ANSI standards EIA/TIA-422-B, EIA/TIA-423-B, RS-485, and ITU recommendations V.10 and V.11.
- Designed to operate with pulse durations as short as 20 ns
- Designed for multipoint bus transmission on long bus lines in noisy environments
- Input Sensitivity:  $\pm 200$  mV
- Low-power consumption: 20 mA maximum
- Open-circuit fail-safe design
- Pin compatible with SN75173 and AM26LS32

## 2 Applications

- [Factory automation](#)
- ATM and cash counters
- [Smart grid](#)
- [AC and servo motor drives](#)

## 3 Description

The SN65LBC173 and SN75LBC173 are monolithic quadruple differential line receivers with 3-state outputs. Both are designed to meet the requirements of the ANSI standards EIA/TIA-422-B, EIA/TIA-423-B, RS-485, and ITU Recommendations V.10 and V.11. The devices are optimized for balanced multipoint bus transmission at data rates up to and exceeding 10 million bits per second. The four receivers share two

ORed enable inputs, one active when high, the other active when low.

Each receiver features high input impedance, input hysteresis for increased noise immunity, and input sensitivity of  $\pm 200$  mV over a common-mode input voltage range of 12 V to  $-7$  V. Fail-safe design ensures that if the inputs are open circuited, the output is always high. Both devices are designed using the Texas Instruments proprietary LinBiCMOS™ technology that provides low power consumption, high switching speeds, and robustness.

These devices offer optimum performance when used with the SN75LBC172 or SN75LBC174 quadruple line drivers. The SN65LBC173 and SN75LBC173 are available in the 16-pin DIP (N) and SOIC (D) packages.

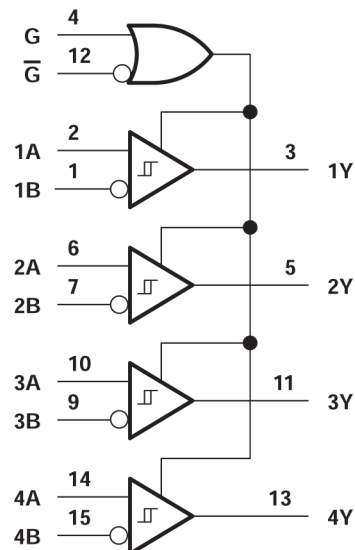
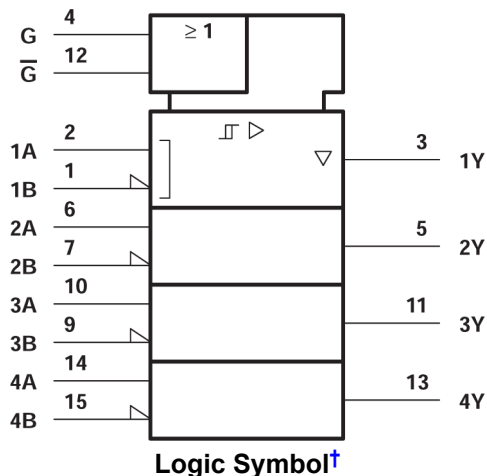
The SN65LBC173 is characterized over the industrial temperature range of  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ . The SN75LBC173 is characterized for operation over the commercial temperature range of  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

### Package Information

| PART NUMBER | PACKAGE <sup>(1)</sup> | PACKAGE SIZE <sup>(2)</sup> |
|-------------|------------------------|-----------------------------|
| SN65LBC173  | D (SOIC, 16)           | 9.9 mm × 6 mm               |
| SN75LBC173  | N (PDIP, 16)           | 19.3 mm × 9.4 mm            |

(1) For more information, see [Section 10](#).

(2) The package size (length × width) is a nominal value and includes pins, where applicable.



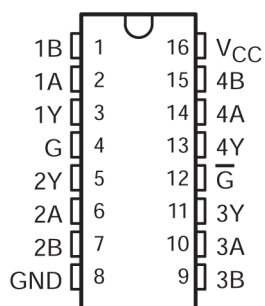
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



## Table of Contents

|                                                |          |                                                         |           |
|------------------------------------------------|----------|---------------------------------------------------------|-----------|
| <b>1 Features</b> .....                        | <b>1</b> | <b>6 Parameter Measurement Information</b> .....        | <b>8</b>  |
| <b>2 Applications</b> .....                    | <b>1</b> | <b>7 Detailed Description</b> .....                     | <b>10</b> |
| <b>3 Description</b> .....                     | <b>1</b> | 7.1 Device Functional Modes.....                        | 10        |
| <b>4 Pin Configuration and Functions</b> ..... | <b>3</b> | <b>8 Device and Documentation Support</b> .....         | <b>11</b> |
| <b>5 Specifications</b> .....                  | <b>4</b> | 8.1 Receiving Notification of Documentation Updates.... | 11        |
| 5.1 Absolute Maximum Ratings.....              | 4        | 8.2 Support Resources.....                              | 11        |
| 5.2 Dissipation Ratings.....                   | 4        | 8.3 Trademarks.....                                     | 11        |
| 5.3 Thermal Information.....                   | 4        | 8.4 Electrostatic Discharge Caution.....                | 11        |
| 5.4 Recommended Operating Conditions.....      | 5        | 8.5 Glossary.....                                       | 11        |
| 5.5 Electrical Characteristics.....            | 6        | <b>9 Revision History</b> .....                         | <b>11</b> |
| 5.6 Switching Characteristics.....             | 6        | <b>10 Mechanical, Packaging, and Orderable</b>          |           |
| 5.7 Typical Characteristics.....               | 7        | <b>Information</b> .....                                | <b>11</b> |

## 4 Pin Configuration and Functions



**Figure 4-1. D or N Package  
(Top View)**

**Table 4-1. Pin Functions**

| PIN             |     | TYPE <sup>(1)</sup> | DESCRIPTION                                |
|-----------------|-----|---------------------|--------------------------------------------|
| NAME            | NO. |                     |                                            |
| 1B              | 1   | I                   | Channel 1 Inverting Differential Input     |
| 1A              | 2   | I                   | Channel 1 Non-Inverting Differential Input |
| 1Y              | 3   | O                   | Channel 1 Output                           |
| G               | 4   | I                   | Active High Receiver Enable                |
| 2Y              | 5   | O                   | Channel 2 Output                           |
| 2A              | 6   | I                   | Channel 2 Non-Inverting Differential Input |
| 2B              | 7   | I                   | Channel 2 Inverting Differential Input     |
| GND             | 8   | GND                 | Device Ground                              |
| 3B              | 9   | I                   | Channel 3 Inverting Differential Input     |
| 3A              | 10  | I                   | Channel 3 Non-Inverting Differential Input |
| 3Y              | 11  | O                   | Channel 3 Output                           |
| $\overline{G}$  | 12  | I                   | Active Low Receiver Enable                 |
| 4Y              | 13  | O                   | Channel 4 Output                           |
| 4A              | 14  | I                   | Channel 4 Non-Inverting Differential Input |
| 4B              | 15  | I                   | Channel 4 Inverting Differential Input     |
| V <sub>CC</sub> | 16  | POW                 | Device Supply                              |

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                                |                                                              |            | MIN                          | MAX                   | UNIT |
|--------------------------------|--------------------------------------------------------------|------------|------------------------------|-----------------------|------|
| V <sub>CC</sub> <sup>(2)</sup> | Supply voltage range                                         |            | −0.3                         | 7                     | V    |
| V <sub>I</sub>                 | Input voltage (A or B inputs)                                |            |                              | ±25                   | V    |
| V <sub>ID</sub> <sup>(3)</sup> | Differential input voltage                                   |            |                              | ±25                   | V    |
|                                | Voltage range at Y, G, $\overline{G}$                        |            | −0.3                         | V <sub>CC</sub> + 0.5 | V    |
|                                | Continuous total dissipation                                 |            | See Dissipation Rating Table |                       |      |
| T <sub>A</sub>                 | Operating free-air temperature range:                        | SN65LBC173 | −40                          | 85                    | °C   |
|                                |                                                              | SN75LBC173 | 0                            | 70                    | °C   |
| T <sub>stg</sub>               | Storage temperature range                                    |            | −65                          | 150                   | °C   |
|                                | Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds |            |                              | 260                   | °C   |

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to GND.
- (3) Differential input voltage is measured at the noninverting input with respect to the corresponding inverting input.

### 5.2 Dissipation Ratings

| PACKAGE | $T_A \leq 25^\circ\text{C}$ POWER RATING | DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$ | $T_A = 70^\circ\text{C}$ POWER RATING | $T_A = 85^\circ\text{C}$ POWER RATING |
|---------|------------------------------------------|------------------------------------------------|---------------------------------------|---------------------------------------|
| D       | 1100 mW                                  | 8.7 mW/°C                                      | 708 mW                                | 578 mW                                |
| N       | 1150 mW                                  | 9.2 mW/°C                                      | 736 mW                                | 598 mW                                |

### 5.3 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |                                              | SOIC (D) | PDIP (N) | UNIT |
|-------------------------------|----------------------------------------------|----------|----------|------|
|                               |                                              | 16 Pins  | 16 Pins  |      |
| $R_{\theta JA}$               | Junction-to-ambient thermal resistance       | 84.6     | 60.6     | °C/W |
| $R_{\theta JC(top)}$          | Junction-to-case (top) thermal resistance    | 43.5     | 48.1     | °C/W |
| $R_{\theta JB}$               | Junction-to-board thermal resistance         | 43.1     | 40.6     | °C/W |
| $\Psi_{JT}$                   | Junction-to-top characterization parameter   | 10.4     | 27.5     | °C/W |
| $\Psi_{JB}$                   | Junction-to-board characterization parameter | 42.8     | 40.3     | °C/W |
| $R_{\theta JC(bot)}$          | Junction-to-case (bottom) thermal resistance | N/A      | N/A      | °C/W |

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.

## 5.4 Recommended Operating Conditions

|                                                |            | MIN  | NOM | MAX  | UNIT |
|------------------------------------------------|------------|------|-----|------|------|
| Supply voltage, V <sub>CC</sub>                |            | 4.75 | 5   | 5.25 | V    |
| Common-mode input voltage, V <sub>IC</sub>     |            | −7   |     | 12   | V    |
| Differential input voltage, V <sub>ID</sub>    |            |      |     | ±6   | V    |
| High-level input voltage, V <sub>IH</sub>      | G inputs   | 2    |     |      | V    |
| Low-level input voltage, V <sub>IL</sub>       |            |      |     | 0.8  | V    |
| High-level output current, I <sub>OH</sub>     |            |      |     | −8   | mA   |
| Low-level output current, I <sub>OL</sub>      |            |      |     | 8    | mA   |
| Operating free-air temperature, T <sub>A</sub> | SN65LBC173 | −40  |     | 85   | °C   |
|                                                | SN75LBC173 | 0    |     | 70   |      |

## 5.5 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER |                                            | TEST CONDITIONS                             | MIN                                                  | TYP <sup>(1)</sup> | MAX  | UNIT |
|-----------|--------------------------------------------|---------------------------------------------|------------------------------------------------------|--------------------|------|------|
| $V_{IT+}$ | Positive-going input threshold voltage     | $I_O = -8$ mA                               |                                                      |                    | 0.2  | V    |
| $V_{IT-}$ | Negative-going input threshold voltage     | $I_O = 8$ mA                                | -0.2                                                 |                    |      | V    |
| $V_{hys}$ | Hysteresis voltage ( $V_{IT+} - V_{IT-}$ ) |                                             |                                                      | 45                 |      | mV   |
| $V_{IK}$  | Enable input clamp voltage                 | $I_I = -18$ mA                              |                                                      | -0.9               | -1.5 | V    |
| $V_{OH}$  | High-level output voltage                  | $V_{ID} = 200$ mV, $I_{OH} = -8$ mA         | 3.5                                                  | 4.5                |      | V    |
| $V_{OL}$  | Low-level output voltage                   | $V_{ID} = -200$ mV, $I_{OL} = 8$ mA         | 0.3                                                  |                    | 0.5  | V    |
| $I_{OZ}$  | High-impedance-state output current        | $V_O = 0$ V to $V_{CC}$                     |                                                      |                    | ±20  | μA   |
| $I_I$     | Bus input current                          | A or B inputs                               | $V_{IH} = 12$ V, $V_{CC} = 5$ V, Other inputs at 0 V | 0.7                | 1    | mA   |
|           |                                            |                                             | $V_{IH} = 12$ V, $V_{CC} = 0$ V, Other inputs at 0 V | 0.8                | 1    |      |
|           |                                            |                                             | $V_{IH} = -7$ V, $V_{CC} = 5$ V, Other inputs at 0 V | -0.5               | -0.8 |      |
|           |                                            |                                             | $V_{IH} = -7$ V, $V_{CC} = 0$ V, Other inputs at 0 V | -0.4               | -0.8 |      |
| $I_{IH}$  | High-level input current                   | $V_{IH} = 5$ V                              |                                                      |                    | ±20  | μA   |
| $I_{IL}$  | Low-level input current                    | $V_{IL} = 0$ V                              |                                                      |                    | -20  | μA   |
| $I_{OS}$  | Short-circuit output current               | $V_O = 0$                                   |                                                      | -80                | -120 | mA   |
| $I_{CC}$  | Supply current                             | Outputs enabled, $I_O = 0$ , $V_{ID} = 5$ V |                                                      | 11                 | 20   | mA   |
|           |                                            | Outputs disabled                            |                                                      | 0.9                | 1.4  |      |

(1) All typical values are at  $V_{CC} = 5$  V and  $T_A = 25^\circ\text{C}$ .

## 5.6 Switching Characteristics

$V_{CC} = 5$  V,  $C_L = 15$  pF,  $T_A = 25^\circ\text{C}$

| PARAMETER          |                                                     | TEST CONDITIONS                                                   | MIN | TYP | MAX | UNIT |
|--------------------|-----------------------------------------------------|-------------------------------------------------------------------|-----|-----|-----|------|
| t <sub>PHL</sub>   | Propagation delay time, high- to low-level output   | V <sub>ID</sub> = −1.5 V to 1.5 V, See <a href="#">Figure 6-1</a> | 11  | 22  | 30  | ns   |
| t <sub>PLH</sub>   | Propagation delay time, low- to high-level output   |                                                                   | 11  | 22  | 30  | ns   |
| t <sub>PZH</sub>   | Output enable time to high level                    | See <a href="#">Figure 6-2</a>                                    |     | 17  | 30  | ns   |
| t <sub>PZL</sub>   | Output enable time to low level                     | See <a href="#">Figure 6-3</a>                                    |     | 18  | 30  | ns   |
| t <sub>PHZ</sub>   | Output disable time from high level                 | See <a href="#">Figure 6-2</a>                                    |     | 35  | 45  | ns   |
| t <sub>PLZ</sub>   | Output disable time from low level                  | See <a href="#">Figure 6-3</a>                                    |     | 25  | 40  | ns   |
| t <sub>sk(p)</sub> | Pulse skew ( t <sub>PHL</sub> − t <sub>PLH</sub>  ) | See <a href="#">Figure 6-2</a>                                    |     | 0.5 | 6   | ns   |
| t <sub>t</sub>     | Transition time                                     | See <a href="#">Figure 6-1</a>                                    |     | 5   | 10  | ns   |

## 5.7 Typical Characteristics

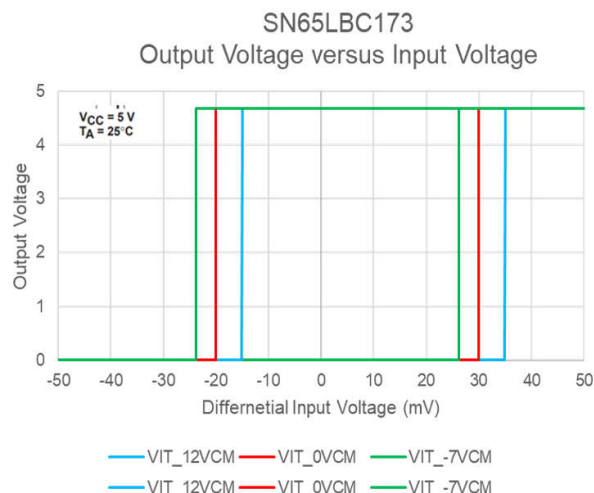


Figure 5-1. Output Voltage vs Differential Input Voltage

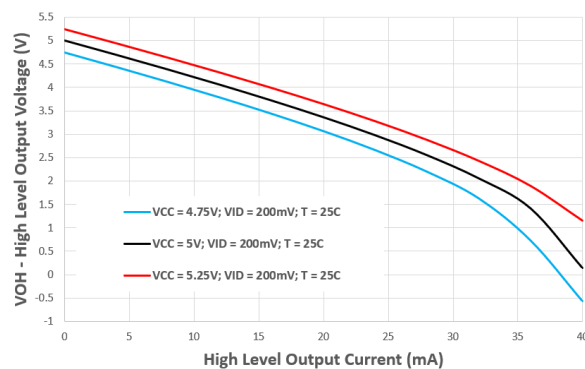


Figure 5-2. High-level Output Voltage vs High-level Output Current

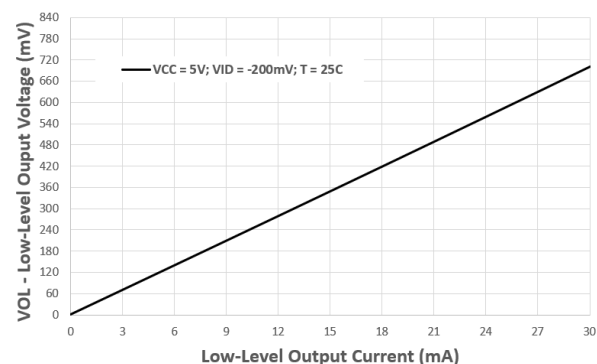


Figure 5-3. Low-level Output Voltage vs Low-level Output Current

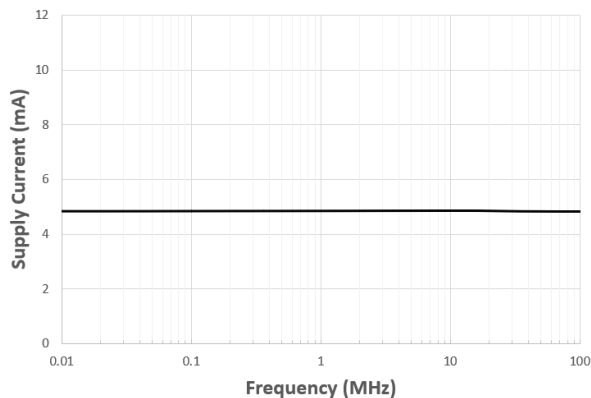


Figure 5-4. Average Supply Current vs Frequency

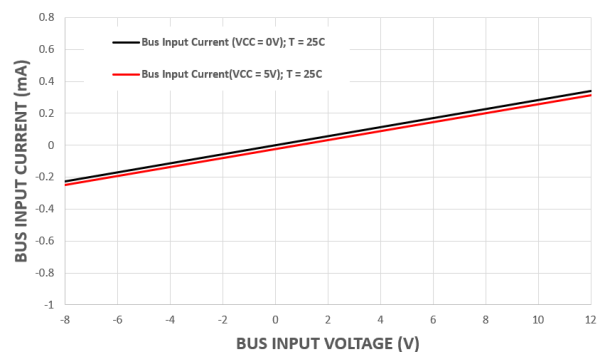


Figure 5-5. Bus Input Current vs Input Voltage (Complementary Input at 0 V)

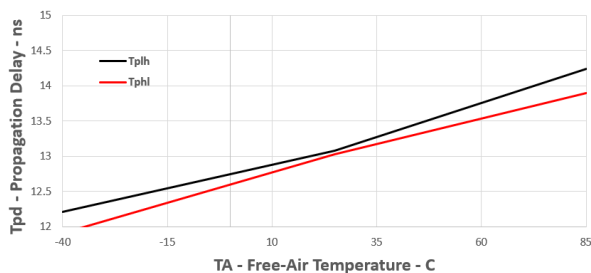


Figure 5-6. Propagation Delay Time vs Free-air Temperature

## 6 Parameter Measurement Information

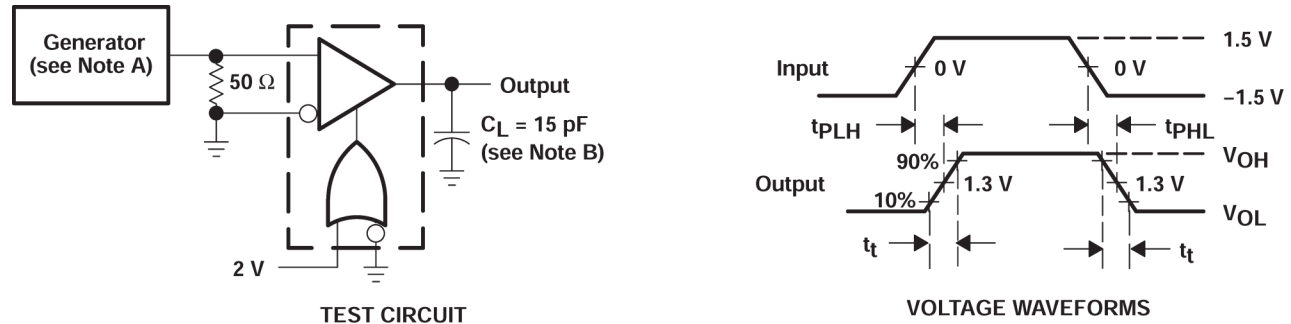
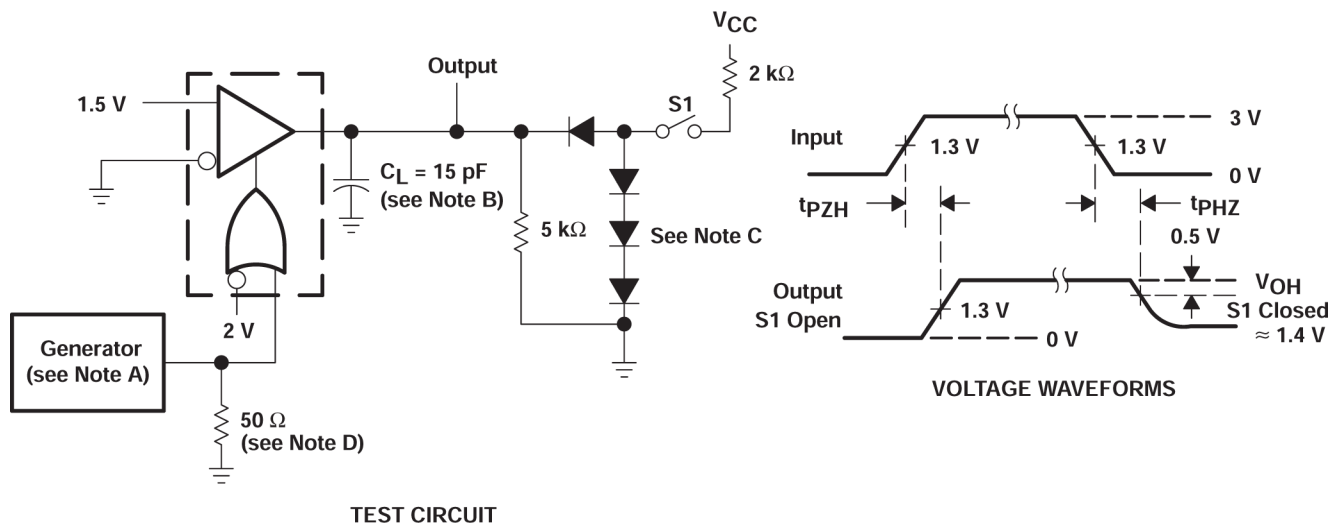


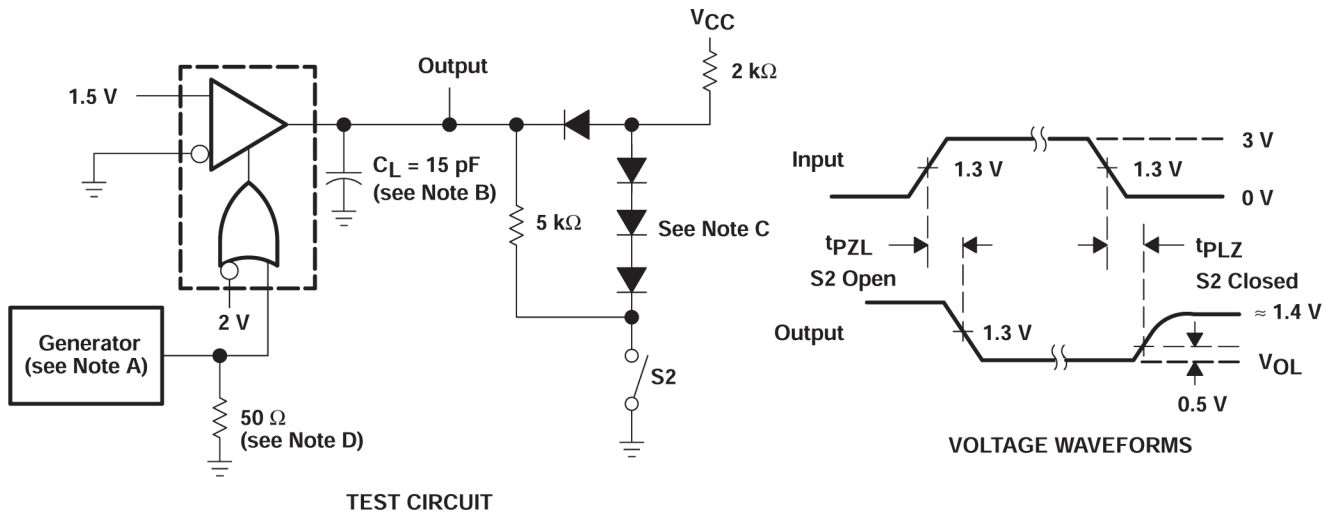
Figure 6-1.  $t_{pd}$  and  $t_t$  Test Circuit and Voltage Waveforms



- The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%,  $t_r \leq 6$  ns,  $t_f \leq 6$  ns,  $Z_O = 50 \Omega$ .
- $C_L$  includes probe and jig capacitance.
- All diodes are 1N916 or equivalent.
- To test the active-low enable  $\overline{G}$ , ground G and apply an inverted input waveform to  $\overline{G}$ .

Figure 6-2.  $t_{PHZ}$  and  $t_{PZH}$  Test Circuit and Voltage Waveforms





- A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%,  $t_r \leq 6$  ns,  $t_f \leq 6$  ns,  $Z_O = 50 \Omega$ .
- B.  $C_L$  includes probe and jig capacitance.
- C. All diodes are 1N916 or equivalent.
- D. To test the active-low enable  $\overline{G}$ , ground G and apply an inverted input waveform to  $\overline{G}$ .

**Figure 6-3.  $t_{PZL}$  and  $t_{PLZ}$  Test Circuit and Voltage Waveforms**

## 7 Detailed Description

### 7.1 Device Functional Modes

Table 7-1. Function Table (Each Receiver)

| DIFFERENTIAL INPUTS                     | ENABLES <sup>(1)</sup> |                | OUTPUT |
|-----------------------------------------|------------------------|----------------|--------|
| A-B                                     | G                      | $\overline{G}$ | Y      |
| $V_{ID} \geq 0.2\text{ V}$              | H                      | X              | H      |
|                                         | X                      | L              | H      |
| $-0.2\text{ V} < V_{ID} < 0.2\text{ V}$ | H                      | X              | ?      |
|                                         | X                      | L              | ?      |
| $V_{ID} \leq -0.2\text{ V}$             | H                      | X              | L      |
|                                         | X                      | L              | L      |
| X                                       | L                      | H              | Z      |
| Open Circuit                            | H                      | X              | H      |
|                                         | X                      | L              | H      |

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), ? = indeterminate

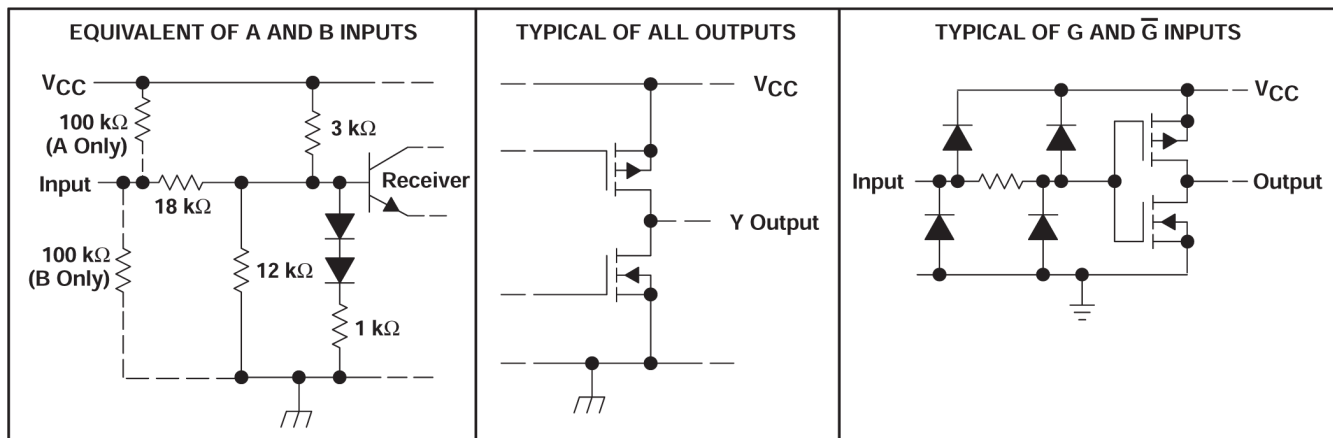


Figure 7-1. Schematics of Inputs and Outputs

## 8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 8.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 8.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.  
All trademarks are the property of their respective owners.

### 8.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 8.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| <b>Changes from Revision E (August 2000) to Revision F (August 2023)</b>                              | <b>Page</b> |
|-------------------------------------------------------------------------------------------------------|-------------|
| • Changed the numbering format for tables, figures, and cross-references throughout the document..... | <b>1</b>    |

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number        | Status<br>(1) | Material type<br>(2) | Package   Pins | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|------------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">SN65LBC173D</a>  | Obsolete      | Production           | SOIC (D)   16  | -                     | -           | Call TI                              | Call TI                           | -40 to 85    | 65LBC173            |
| <a href="#">SN65LBC173DR</a> | Active        | Production           | SOIC (D)   16  | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | 65LBC173            |
| SN65LBC173DR.A               | Active        | Production           | SOIC (D)   16  | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | 65LBC173            |
| SN65LBC173DRG4               | Active        | Production           | SOIC (D)   16  | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | 65LBC173            |
| SN65LBC173DRG4.A             | Active        | Production           | SOIC (D)   16  | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | 65LBC173            |
| <a href="#">SN65LBC173N</a>  | Active        | Production           | PDIP (N)   16  | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -40 to 85    | SN65LBC173N         |
| SN65LBC173N.A                | Active        | Production           | PDIP (N)   16  | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -40 to 85    | SN65LBC173N         |
| <a href="#">SN75LBC173D</a>  | Obsolete      | Production           | SOIC (D)   16  | -                     | -           | Call TI                              | Call TI                           | 0 to 70      | 75LBC173            |
| <a href="#">SN75LBC173N</a>  | Active        | Production           | PDIP (N)   16  | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | 0 to 70      | SN75LBC173N         |
| SN75LBC173N.A                | Active        | Production           | PDIP (N)   16  | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | 0 to 70      | SN75LBC173N         |
| SN75LBC173NE4                | Active        | Production           | PDIP (N)   16  | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | 0 to 70      | SN75LBC173N         |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

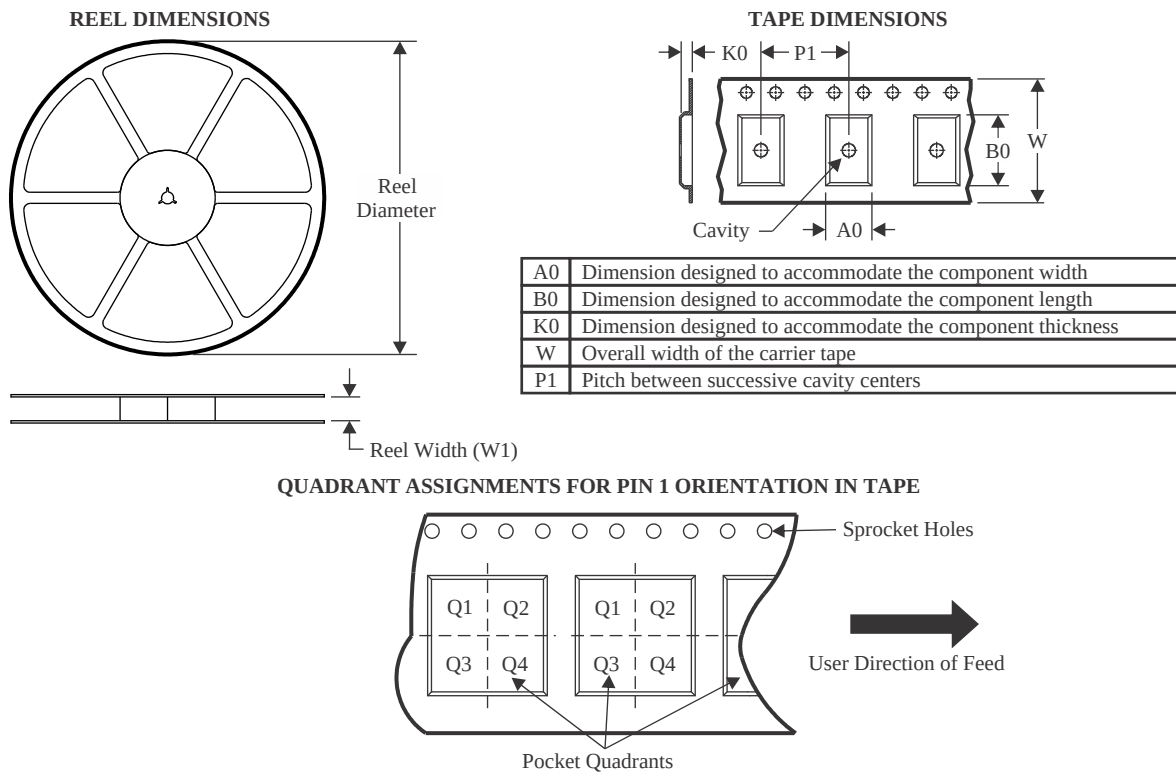
**OTHER QUALIFIED VERSIONS OF SN75LBC173 :**

- Military : [SN55LBC173](#)

NOTE: Qualified Version Definitions:

- Military - QML certified for Military and Defense Applications

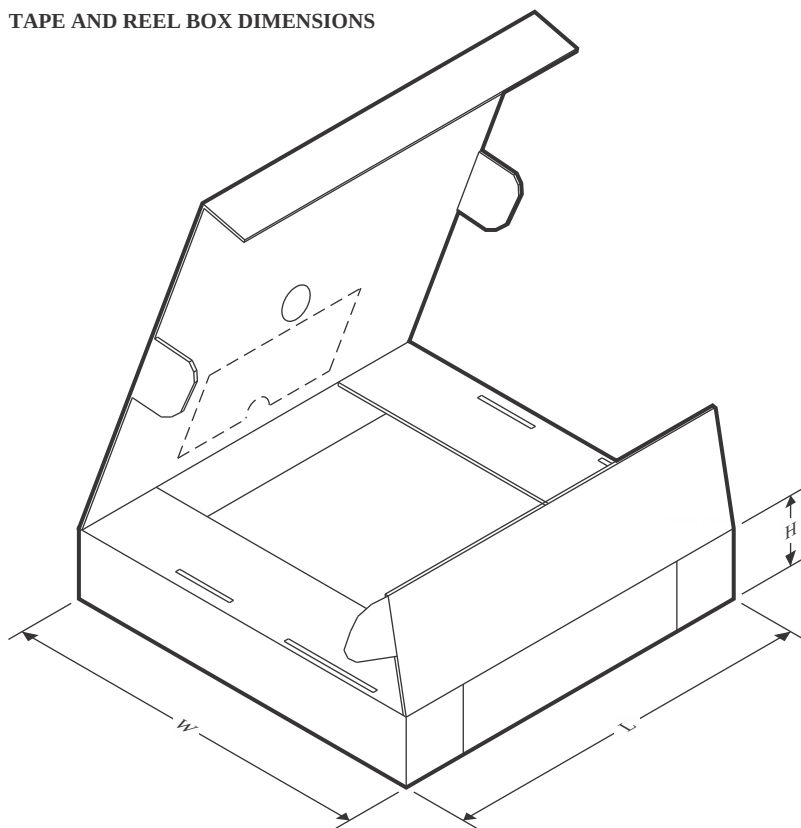
## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device         | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN65LBC173DR   | SOIC         | D               | 16   | 2500 | 330.0              | 16.4               | 6.5     | 10.3    | 2.1     | 8.0     | 16.0   | Q1            |
| SN65LBC173DRG4 | SOIC         | D               | 16   | 2500 | 330.0              | 16.4               | 6.5     | 10.3    | 2.1     | 8.0     | 16.0   | Q1            |

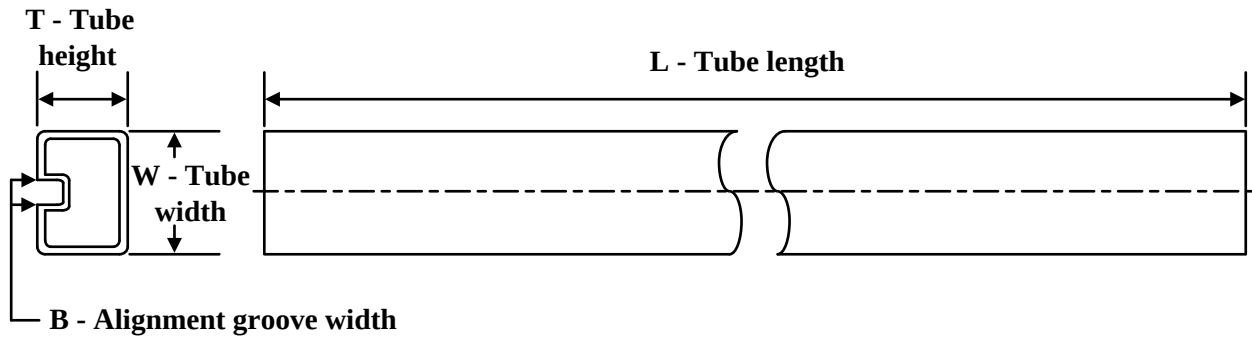
## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device         | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN65LBC173DR   | SOIC         | D               | 16   | 2500 | 340.5       | 336.1      | 32.0        |
| SN65LBC173DRG4 | SOIC         | D               | 16   | 2500 | 353.0       | 353.0      | 32.0        |

## TUBE



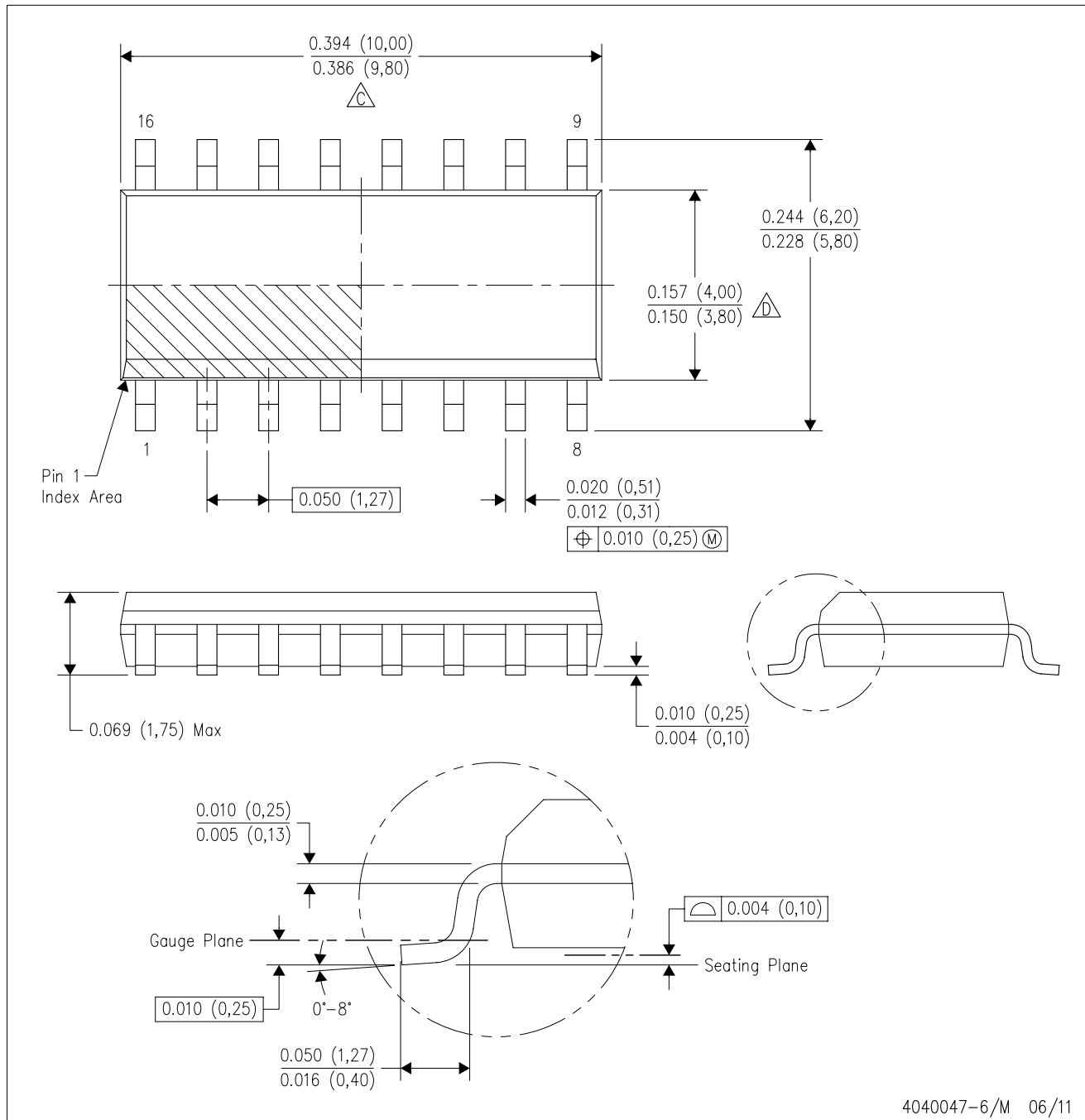
\*All dimensions are nominal

| Device        | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|---------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| SN65LBC173N   | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| SN65LBC173N.A | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| SN75LBC173N   | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| SN75LBC173N.A | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| SN75LBC173NE4 | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |



D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



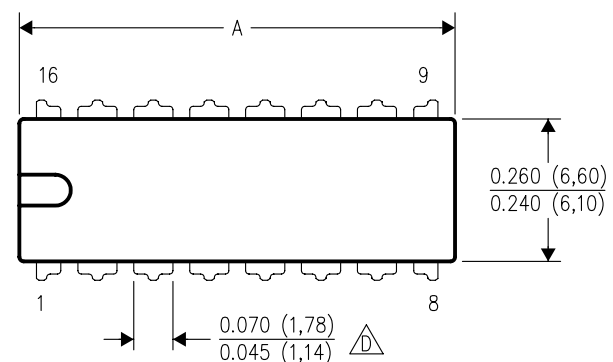
4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

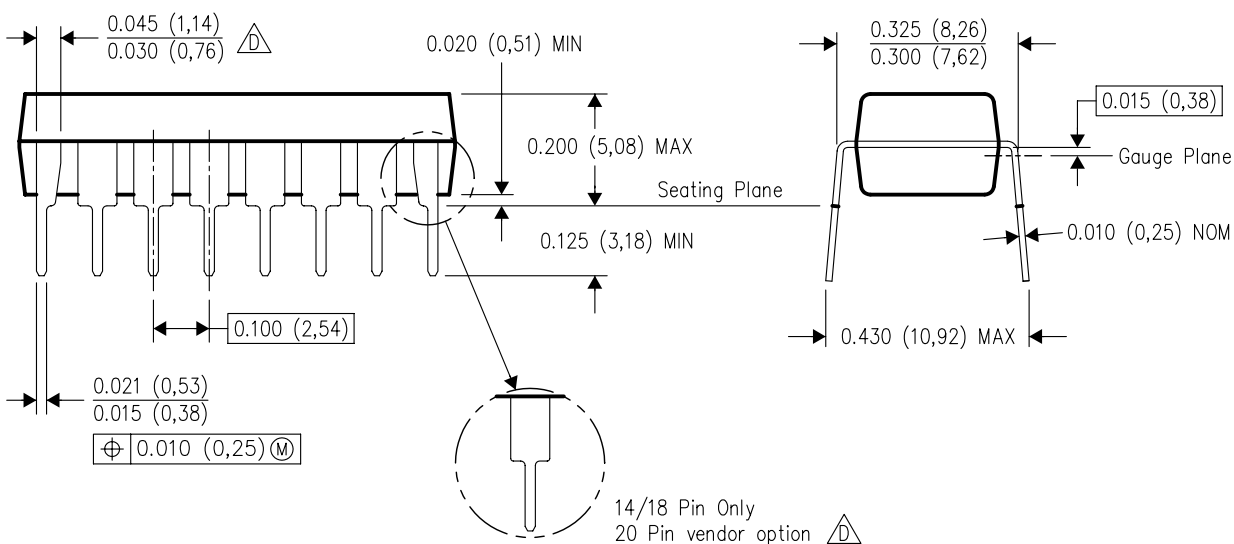
N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



| PINS **<br>DIM      | 14               | 16               | 18               | 20               |
|---------------------|------------------|------------------|------------------|------------------|
| A MAX               | 0.775<br>(19,69) | 0.775<br>(19,69) | 0.920<br>(23,37) | 1.060<br>(26,92) |
| A MIN               | 0.745<br>(18,92) | 0.745<br>(18,92) | 0.850<br>(21,59) | 0.940<br>(23,88) |
| MS-001<br>VARIATION | AA               | BB               | AC               | AD               |



4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).  
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2025, Texas Instruments Incorporated