

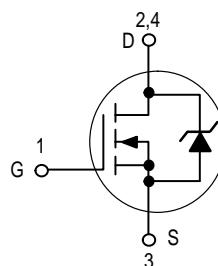
*Product Preview*

**TMOS E-FET™**  
**High Energy Power FET**

**N-Channel Enhancement-Mode Silicon Gate**

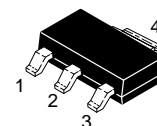
This advanced high voltage TMOS E-FET is designed to withstand high energy in the avalanche mode and switch efficiently. This new high energy device also offers a drain-to-source diode with fast recovery time. Designed for high voltage, high speed switching applications such as power supplies, PWM motor controls and other inductive loads, the avalanche energy capability is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Capability Specified at Elevated Temperature
- Internal Source-to-Drain Diode Designed to Replace External Zener Transient Suppressor – Absorbs High Energy in the Avalanche Mode
- Source-to-Drain Diode Recovery Time Comparable to Discrete Fast Recovery Diode



**MMFT2N25E**

**TMOS POWER FET**  
**2.0 AMPERES**  
**250 VOLTS**  
**R<sub>DS(on)</sub> = 3.5 Ω**



**CASE 318E-04, STYLE 3**  
**TO-261AA**

**MAXIMUM RATINGS** (T<sub>C</sub> = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V <sub>DSS</sub>	250	Vdc
Drain-to-Gate Voltage, R <sub>GS</sub> = 1.0 mΩ	V <sub>DGR</sub>	250	Vdc
Gate-to-Source Voltage — Continuous	V <sub>GS</sub>	±20	Vdc
Gate-to-Source Voltage — Single Pulse (tp ≤ 50 μs)	V <sub>GSM</sub>	±40	Vdc
Drain Current — Continuous @ T <sub>C</sub> = 25°C	I <sub>D</sub>	2.0	Adc
— Continuous @ T <sub>C</sub> = 100°C	I <sub>D</sub>	0.6	
— Single Pulse (tp ≤ 10 μs)	I <sub>DM</sub>	7.0	Apk
Total Power Dissipation @ T <sub>C</sub> = 25°C	P <sub>D</sub>	0.77	Watts
Derate above 25°C		6.2	mW/°C
Total P <sub>D</sub> @ T <sub>A</sub> = 25°C mounted on 1" Sq. Drain Pad on FR-4 Bd. Material		1.0	Watts
Total P <sub>D</sub> @ T <sub>A</sub> = 25°C mounted on 0.7" Sq. Drain Pad on FR-4 Bd. Material		1.2	
Total P <sub>D</sub> @ T <sub>A</sub> = 25°C mounted on min. Drain Pad on FR-4 Bd. Material		0.8	
Operating and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-55 to 150	°C

**UNCLAMPED DRAIN-TO-SOURCE AVALANCHE CHARACTERISTICS (T<sub>J</sub> < 150°C)**

Single Pulse Drain-to-Source Avalanche Energy — Starting T <sub>J</sub> = 25°C (V <sub>DD</sub> = 80 V, V <sub>GS</sub> = 10 V, Peak I <sub>L</sub> = 4.0 Apk, L = 3.0 mH, R <sub>G</sub> = 25 Ω)	E <sub>AS</sub>	26	mJ
------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------	-----------------	----	----

**THERMAL CHARACTERISTICS**

— Junction-to-Ambient on 1" Sq. Drain Pad on FR-4 Bd. Material	R <sub>θJA</sub>	90	°C/W
— Junction-to-Ambient on 0.7" Sq. Drain Pad on FR-4 Bd. Material		103	
— Junction-to-Ambient on min. Drain Pad on FR-4 Bd. Material		162	
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	T <sub>L</sub>	260	°C

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

TMOS is a registered trademark of Motorola, Inc.  
E-FET is a trademark of Motorola, Inc.

# MMFT2N25E

## ELECTRICAL CHARACTERISTICS (T<sub>C</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Drain-to-Source Breakdown Voltage (V <sub>GS</sub> = 0, I <sub>D</sub> = 0.25 mA) Temperature Coefficient (Positive)	BV <sub>DSS</sub>	250 —	— 324	— —	V <sub>dc</sub> V/°C
Zero Gate Voltage Drain Current (V <sub>DS</sub> = 250 V, V <sub>GS</sub> = 0) (V <sub>DS</sub> = 250 V, V <sub>GS</sub> = 0, T <sub>J</sub> = 125°C)	I <sub>DSS</sub>	— —	— —	10 100	μAdc
Gate-Body Leakage Current (V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0)	I <sub>GSS</sub>	—	—	100	nAdc

### ON CHARACTERISTICS (1)

Gate Threshold Voltage (V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 0.25 mA) Threshold Temperature Coefficient (Negative)	V <sub>GS(th)</sub>	2.0 —	2.8 5.7	4.0 —	V <sub>dc</sub> mV/°C
Static Drain-to-Source On-Resistance (V <sub>GS</sub> = 10 V, I <sub>D</sub> = 1.0 Adc)	R <sub>DSS(on)</sub>	—	2.1	3.5	Ohms
Drain-to-Source On-Voltage (V <sub>GS</sub> = 10 V, I <sub>D</sub> = 2.0 A) (V <sub>GS</sub> = 10 V, I <sub>D</sub> = 1.0 A, T <sub>J</sub> = 125°C)	V <sub>DS(on)</sub>	— —	— —	8.40 7.35	V <sub>dc</sub>
Forward Transconductance (V <sub>DS</sub> = 8.0 V, I <sub>D</sub> = 2.0 Adc)	g <sub>FS</sub>	0.44	1.2	—	mhos

### DYNAMIC CHARACTERISTICS

Input Capacitance	(V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0, f = 1.0 MHz)	C <sub>iss</sub>	—	137	190	pF
Output Capacitance		C <sub>oss</sub>	—	30	40	
Transfer Capacitance		C <sub>rss</sub>	—	7.0	10	

### SWITCHING CHARACTERISTICS (1)

Turn-On Delay Time	(V <sub>DS</sub> = 125 V, I <sub>D</sub> = 2.0 A, R <sub>G</sub> = 9.1 Ohms, V <sub>GS</sub> = 10 V)	t <sub>d(on)</sub>	—	9.2	20	ns
Rise Time		t <sub>r</sub>	—	6.6	10	
Turn-Off Delay Time		t <sub>d(off)</sub>	—	13	30	
Fall Time		t <sub>f</sub>	—	8.5	20	
Gate Charge	(V <sub>DS</sub> = 200 V, I <sub>D</sub> = 2.0 A, V <sub>GS</sub> = 10 V)	Q <sub>T</sub>	—	4.7	10	nC
		Q <sub>1</sub>	—	1.3	—	
		Q <sub>2</sub>	—	3.2	—	
		Q <sub>3</sub>	—	2.3	—	

### SOURCE-DRAIN DIODE CHARACTERISTICS

Forward On-Voltage	I <sub>S</sub> = 2.0 A, V <sub>GS</sub> = 0 V	V <sub>SD</sub>	—	0.94	2.0	V <sub>dc</sub>
	I <sub>S</sub> = 2.0 A, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125°C	V <sub>SD</sub>	—	0.83	—	
Reverse Recovery Time	(I <sub>S</sub> = 2.0 A, di <sub>S</sub> /dt = 100 A/μs)	t <sub>rr</sub>	—	104	—	nS
		t <sub>a</sub>	—	63	—	
		t <sub>b</sub>	—	41	—	
Reverse Recovery Stored Charge		q <sub>rr</sub>	—	0.365	—	

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

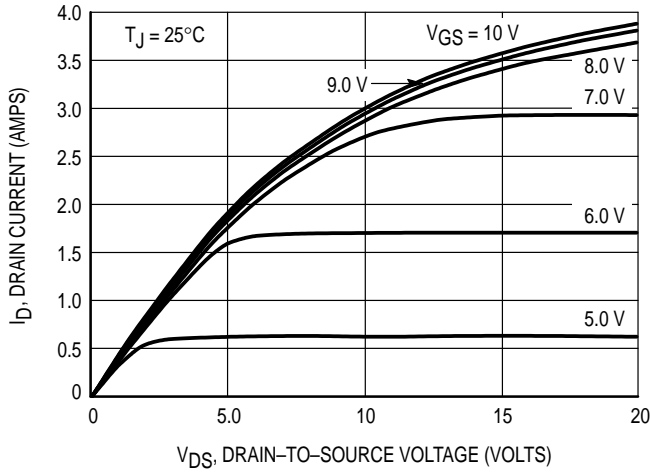


Figure 1. On-Region Characteristics

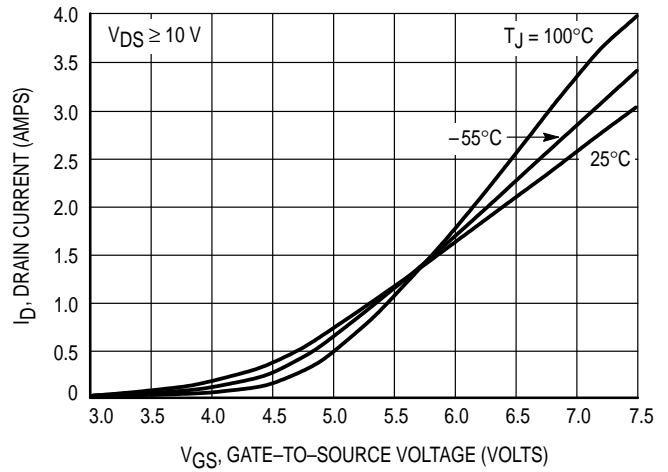


Figure 2. Transfer Characteristics

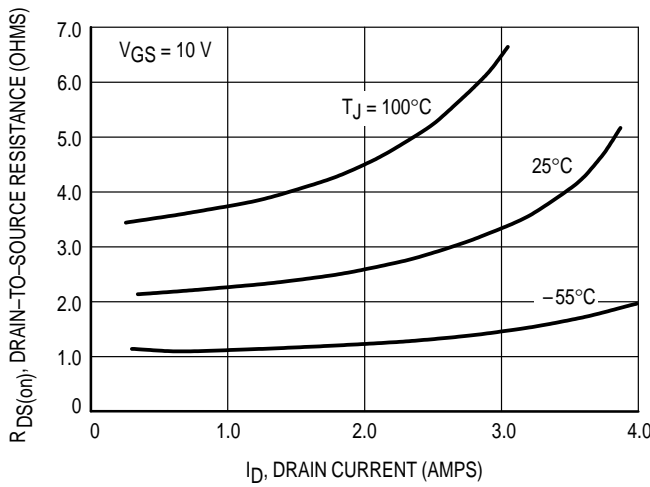


Figure 3. On-Resistance versus Drain Current and Temperature

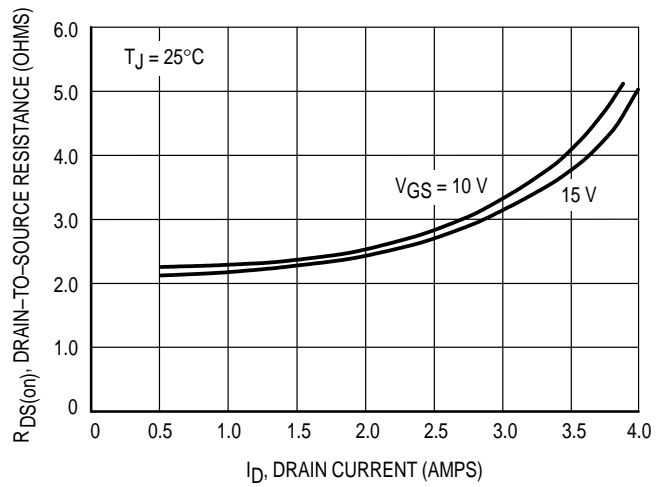


Figure 4. On-Resistance versus Drain Current and Gate Voltage

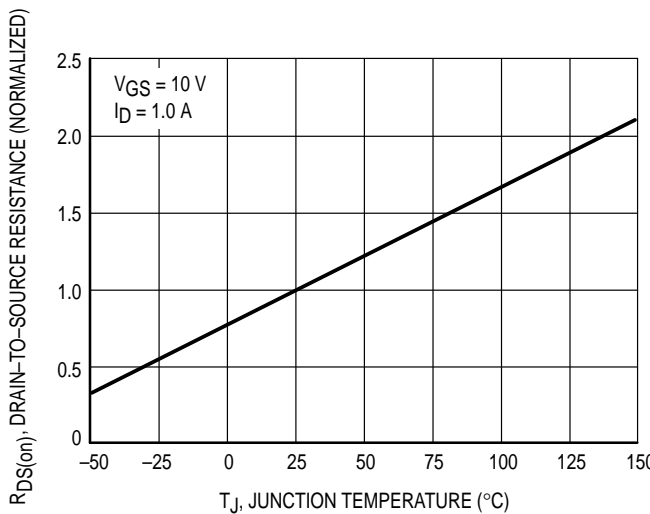


Figure 5. On-Resistance Variation versus Temperature

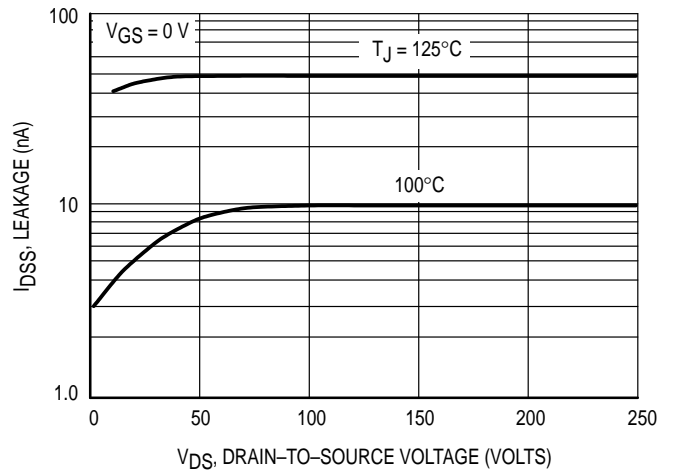
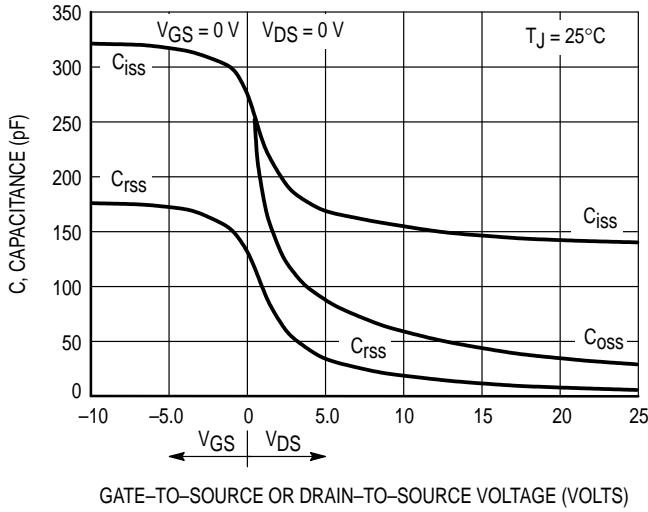
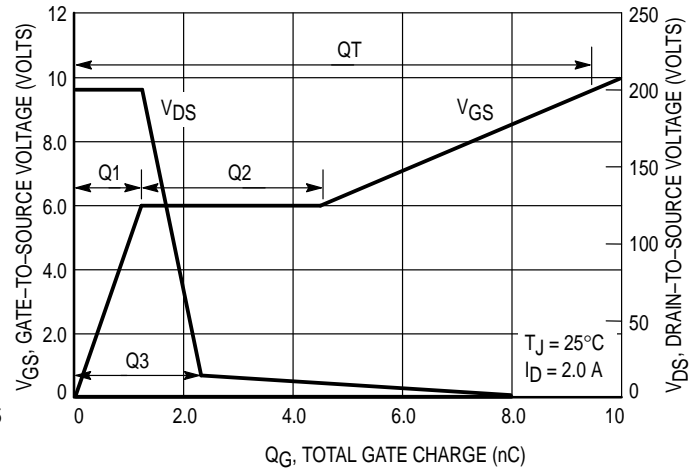


Figure 6. Drain-to-Source Leakage Current versus Voltage

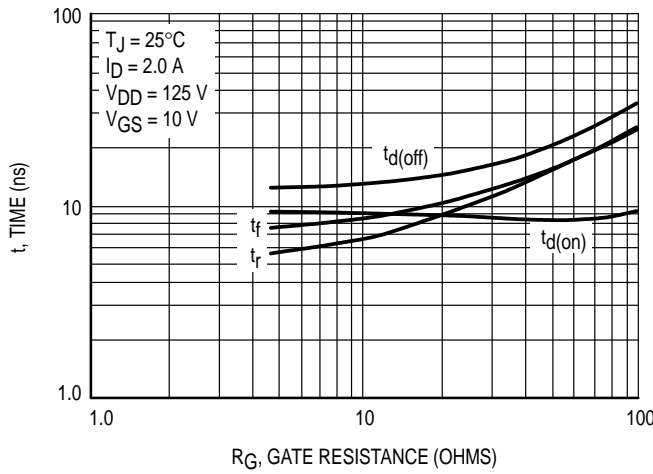
**MMFT2N25E**



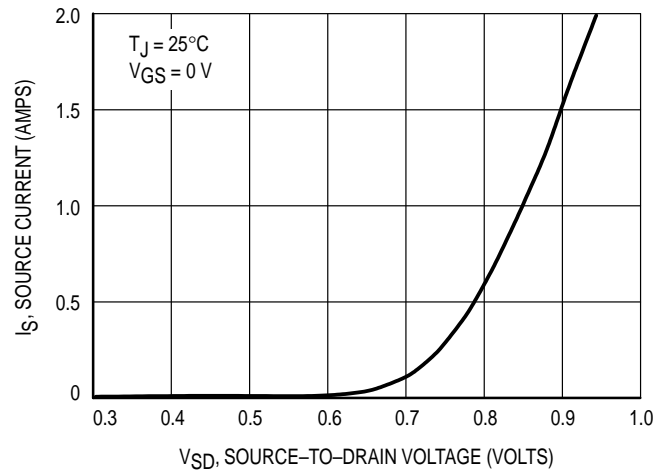
**Figure 7. Capacitance Variation**



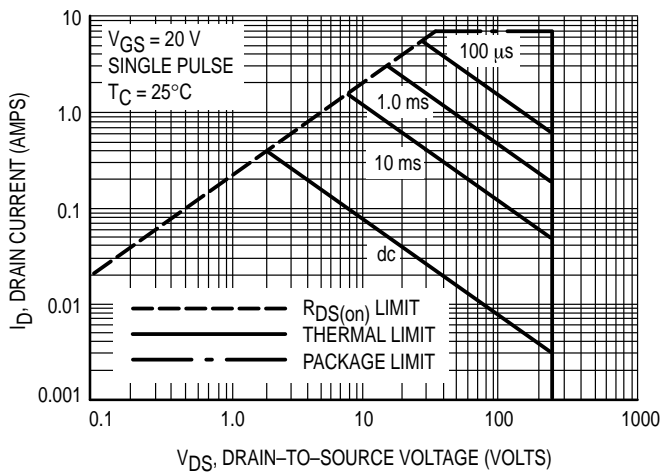
**Figure 8. Gate-to-Source and Drain-to-Source Voltage versus Total Charge**



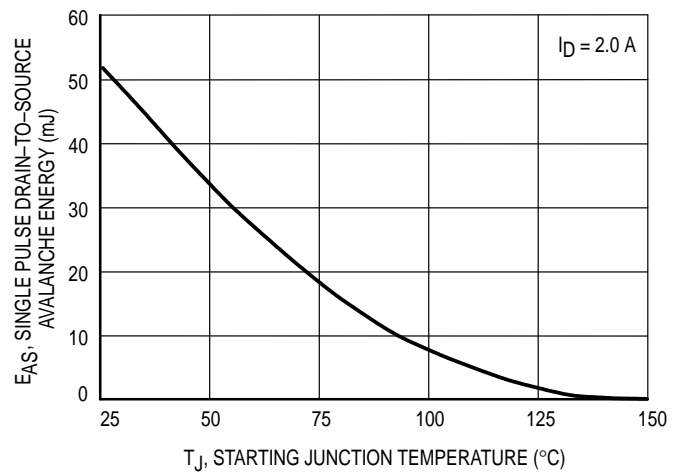
**Figure 9. Resistive Switching Time Variation versus Gate Resistance**



**Figure 10. Diode Forward Voltage versus Current**



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**



**Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature**

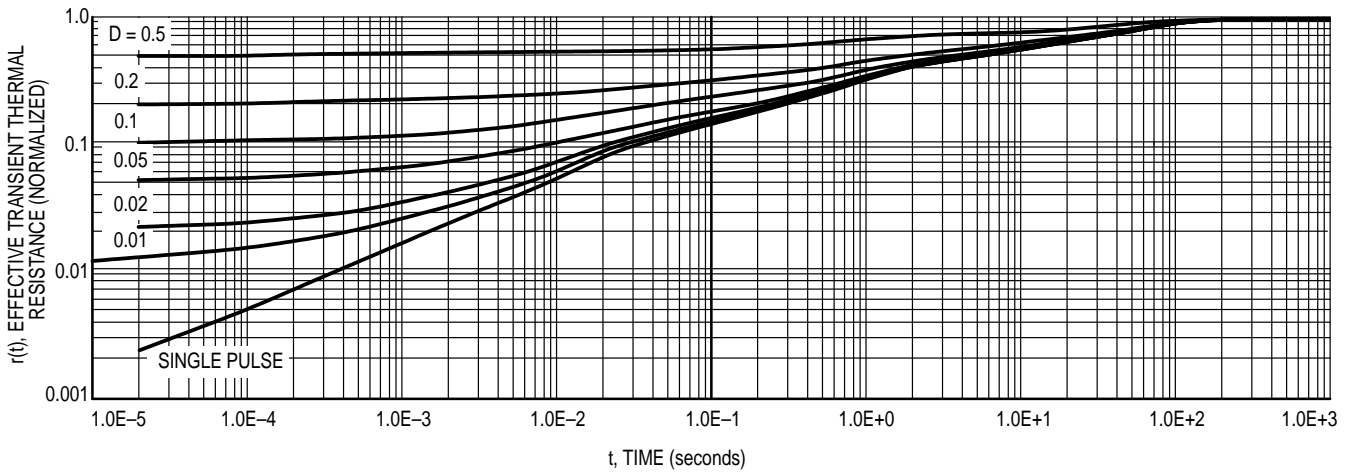
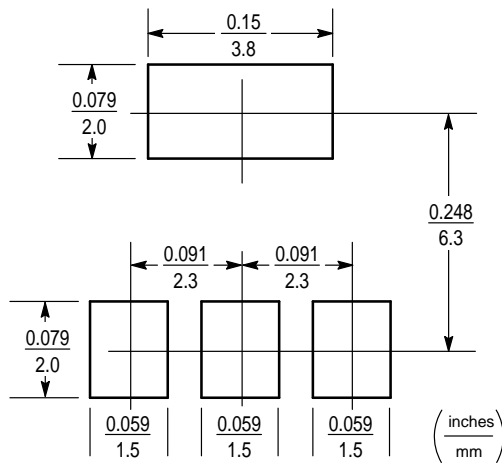


Figure 13. Thermal Response

**MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS**

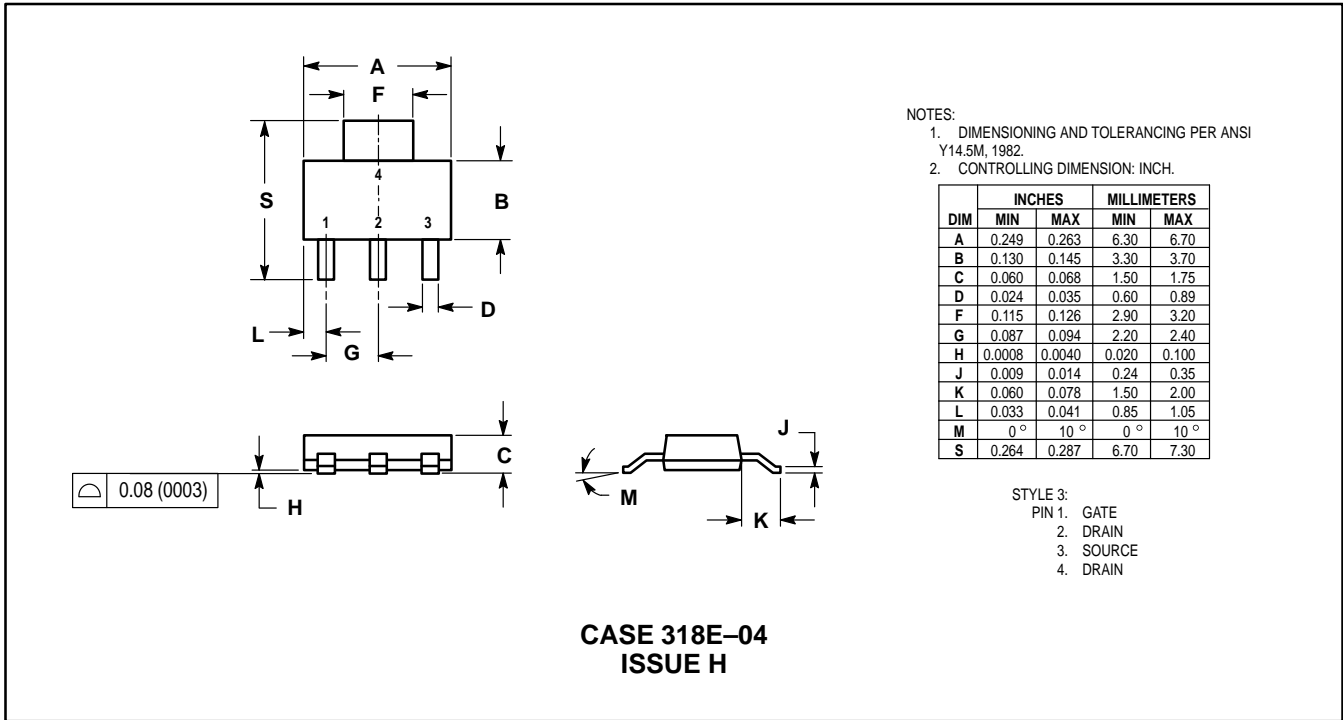
Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection interface

between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.



**SOT-223**

PACKAGE DIMENSIONS



Motorola reserves the right to make changes without further notice to any products herein. Motorola makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Motorola assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters which may be provided in Motorola data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. Motorola does not convey any license under its patent rights nor the rights of others. Motorola products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Motorola product could create a situation where personal injury or death may occur. Should Buyer purchase or use Motorola products for any such unintended or unauthorized application, Buyer shall indemnify and hold Motorola and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Motorola was negligent regarding the design or manufacture of the part. Motorola and are registered trademarks of Motorola, Inc. Motorola, Inc. is an Equal Opportunity/Affirmative Action Employer.

Mfax is a trademark of Motorola, Inc.

**How to reach us:**

**USA/EUROPE/Locations Not Listed:** Motorola Literature Distribution;  
 P.O. Box 5405, Denver, Colorado 80217. 1-303-675-2140 or 1-800-441-2447

**JAPAN:** Nippon Motorola Ltd.: SPD, Strategic Planning Office, 4-32-1,  
 Nishi-Gotanda, Shinagawa-ku, Tokyo 141, Japan. 81-3-5487-8488

**Customer Focus Center: 1-800-521-6274**

**Mfax™:** RMFAX0@email.sps.mot.com – TOUCHTONE 1-602-244-6609  
 Motorola Fax Back System – US & Canada ONLY 1-800-774-1848  
 – http://sps.motorola.com/mfax/

**ASIA/PACIFIC:** Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,  
 51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852-26629298

**HOME PAGE:** <http://motorola.com/sps/>

