

SN54LVT2952, SN74LVT2952 3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SCBS152E – MAY 1992 – REVISED JULY 1995

- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Support Live Insertion
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), and Ceramic (JT) DIPs

description

These octal bus transceivers and registers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The 'LVT2952 consist of two 8-bit back-to-back registers that store data flowing in both directions between two bidirectional buses. Data on the A or B bus is stored in the registers on the low-to-high transition of the clock (CLKAB or CLKBA) input provided that the clock-enable ($\overline{\text{CLKENAB}}$ or $\overline{\text{CLKENBA}}$) input is low. Taking the output-enable ($\overline{\text{OEAB}}$ or $\overline{\text{OEBA}}$) input low accesses the data on either port.

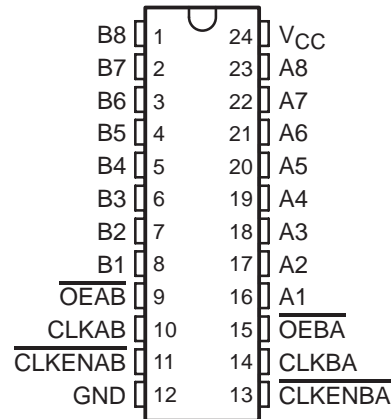
Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

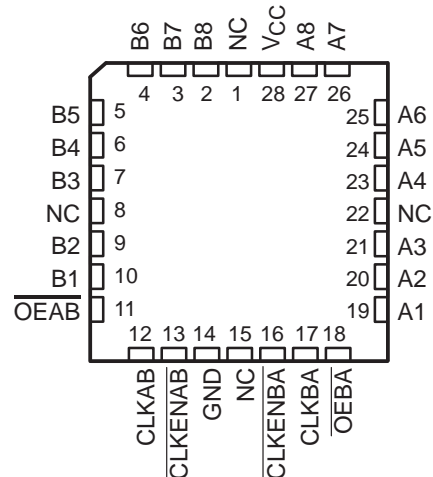
The SN74LVT2952 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54LVT2952 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVT2952 is characterized for operation from -40°C to 85°C .

SN54LVT2952 . . . JT PACKAGE
SN74LVT2952 . . . DB, DW, OR PW PACKAGE
(TOP VIEW)



SN54LVT2952 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection



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**TEXAS
INSTRUMENTS**

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SN54LVT2952, SN74LVT2952
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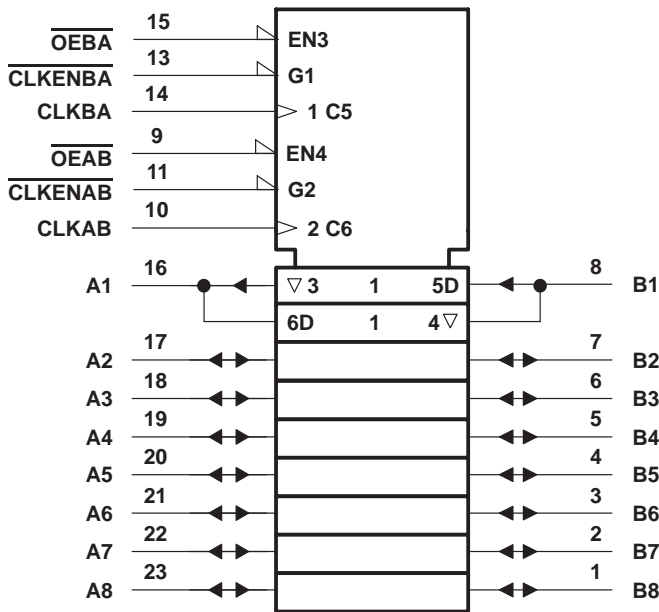
FUNCTION TABLE†

INPUTS				OUTPUT
CLKENAB	CLKAB	OEAB	A	B
H	X	L	X	B ₀ ‡
X	H or L	L	X	B ₀ ‡
L	↑	L	L	L
L	↑	L	H	H
X	X	H	X	Z

† A-to-B data flow is shown; B-to-A data flow is similar but uses CLKENBA, CLKBA, and OEBA.

‡ Level of B before the indicated steady-state input conditions were established

logic symbols§



§ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DB, DW, JT, and PW packages.

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The diagram illustrates a logic circuit for a 2-channel system. It features two main input sections, each with a clock signal (CLKENAB, CLKAB for channel A; CLKENBA, CLKBA for channel B) and an enable signal (OEAB, OEBA). These inputs are processed through a series of AND and OR gates to generate control signals. The core of the circuit consists of two D-type flip-flops, labeled C1 1D. The outputs of these flip-flops are fed back into the input section of the opposite channel, creating a cross-coupled configuration. Additionally, the outputs are connected to a common bus labeled 'To Seven Other Channels'. The final outputs are labeled A1 and B1.



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1)	–0.5 V to 7 V
Current into any output in the low state, I_O : SN54LVT2952	96 mA
SN74LVT2952	128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVT2952	48 mA
SN74LVT2952	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 3): DB package	0.65 W
DW package	1.7 W
PW package	0.7 W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions (see Note 4)

		SN54LVT2952		SN74LVT2952		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage		5.5		5.5	V
I_{OH}	High-level output current		–24		–32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10	10	ns/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54LVT2952		SN74LVT2952		UNIT	
			MIN	TYP†	MAX	MIN		TYP†
V _{IK}	V _{CC} = 2.7 V, I _I = −18 mA				−1.2	−1.2	V	
V _{OH}	V _{CC} = MIN to MAX‡, I _{OH} = −100 μA		V _{CC} − 0.2		V _{CC} − 0.2		V	
	V _{CC} = 2.7 V, I _{OH} = − 8 mA		2.4		2.4			
	V _{CC} = 3 V	I _{OH} = − 24 mA	2					
		I _{OH} = −32 mA			2			
V _{OL}	V _{CC} = 2.7 V	I _{OL} = 100 μA			0.2	0.2	V	
		I _{OL} = 24 mA			0.5	0.5		
	V _{CC} = 3 V	I _{OL} = 16 mA			0.4	0.4		
		I _{OL} = 32 mA			0.5	0.5		
		I _{OL} = 48 mA			0.55			
		I _{OL} = 64 mA				0.55		
		I _I	V _{CC} = 3.6 V, V _I = V _{CC} or GND	Control inputs				±1
V _{CC} = 0 or MAX‡, V _I = 5.5 V			10		10			
V _{CC} = 3.6 V	V _I = 5.5 V		A or B ports§			20	20	
	V _I = V _{CC}					5	5	
	V _I = 0					−10	−10	
I _{off}	V _{CC} = 0, V _I or V _O = 0 to 4.5 V				±100		μA	
I _I (hold)	V _{CC} = 3 V	V _I = 0.8 V	A or B ports	75	75	μA		
		V _I = 2 V		−75	−75	μA		
I _{OZH}	V _{CC} = 3.6 V, V _O = 3 V		1		1		μA	
I _{OZL}	V _{CC} = 3.6 V, V _O = 0.5 V		−1		−1		μA	
I _{CC}	V _{CC} = 3.6 V, V _I = V _{CC} or GND	I _O = 0,	Outputs high	0.13	0.19	0.13	0.19	mA
			Outputs low	8.8	12	8.8	12	
			Outputs disabled	0.13	0.19	0.13	0.19	
ΔI _{CC} ¶	V _{CC} = 3 V to 3.6 V, One input at V _{CC} − 0.6 V, Other inputs at V _{CC} or GND		0.2		0.2		mA	
C _i	V _I = 3 V or 0		4.5		4.5		pF	
C _{io}	V _O = 3 V or 0		11.5		11.5		pF	

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

§ Unused terminals at V_{CC} or GND

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

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timing requirement over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

			SN54LVT2952				SN74LVT2952				UNIT
			$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency						150		150		MHz
t_w	Pulse duration		CLK high				3.3		3.3		ns
			CLK low				3.3		3.3		
t_{su}	Setup time, A or B before CLK↑		Data high	2.6	2.9		2.5		2.8		ns
			Data low	2.6	3.1		2.5		3		
	Setup time, $\overline{\text{CE}}$ before CLK↑		Data high	0.9	0.8		0.9		0.8		
			Data low	2.5	2.7		2.4		2.7		
t_h	Hold time, A or B after CLK↑			1.5	0.7		1.5		0.7		ns
	Hold time, $\overline{\text{CE}}$ after CLK↑			2.6	2.6		2.5		2.6		

switching characteristics over recommended operating free-air temperature range, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT2952				SN74LVT2952				UNIT	
			V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V			V _{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN		MAX
f _{max}							150			150	MHz	
t _{PLH}	CLKBA or CLKAB	A or B	1.3	6.4	2.7	7.4	1.3	3.6	6.1	2.7	7.1	ns
t _{PHL}			1.8	6.1	2.7	7	1.8	3.7	6	2.7	6.9	
t _{PZH}	$\overline{\text{OEBA}}$ or $\overline{\text{OEAB}}$	A or B	1	6.3	2.6	7.3	1	3.2	5.6	2.6	6.7	ns
t _{PZL}			1.1	6.6	2.9	8.2	1.2	3.2	6.5	2.9	8	
t _{PHZ}	$\overline{\text{OEBA}}$ or $\overline{\text{OEAB}}$	A or B	1	7	2.7	7.6	1	4.1	6.3	2.7	6.9	ns
t _{PLZ}			1.6	5.8	1.7	6	1.6	3.3	5.1	1.8	5.3	

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

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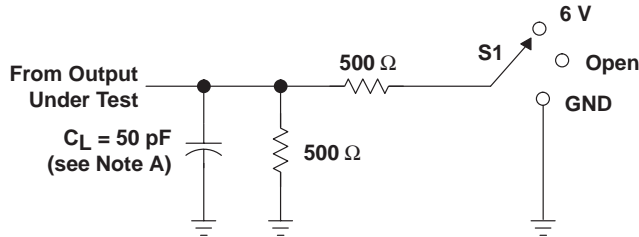


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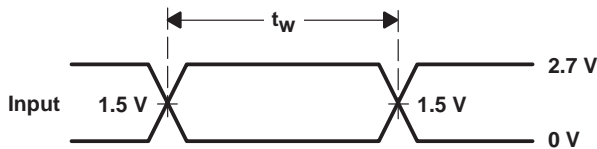
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PARAMETER MEASUREMENT INFORMATION

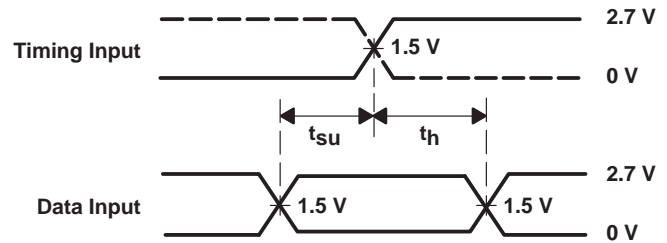


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

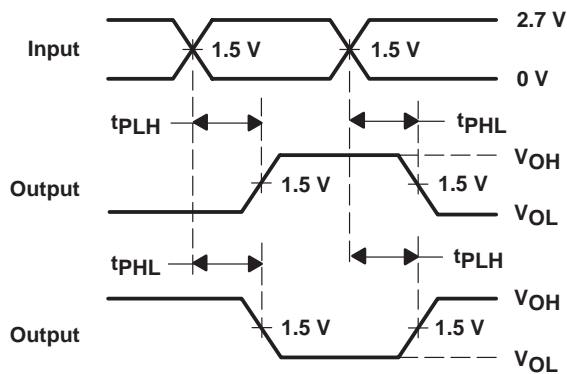
LOAD CIRCUIT FOR OUTPUTS



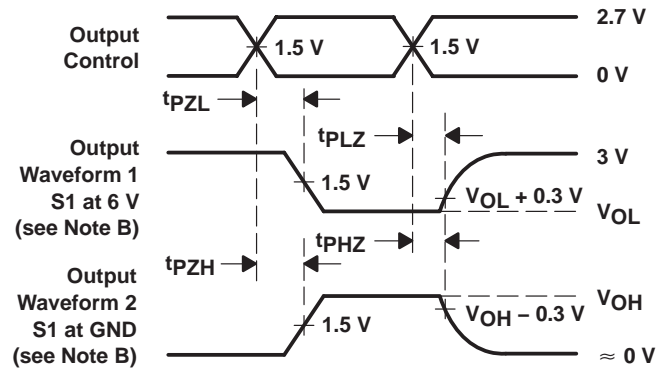
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

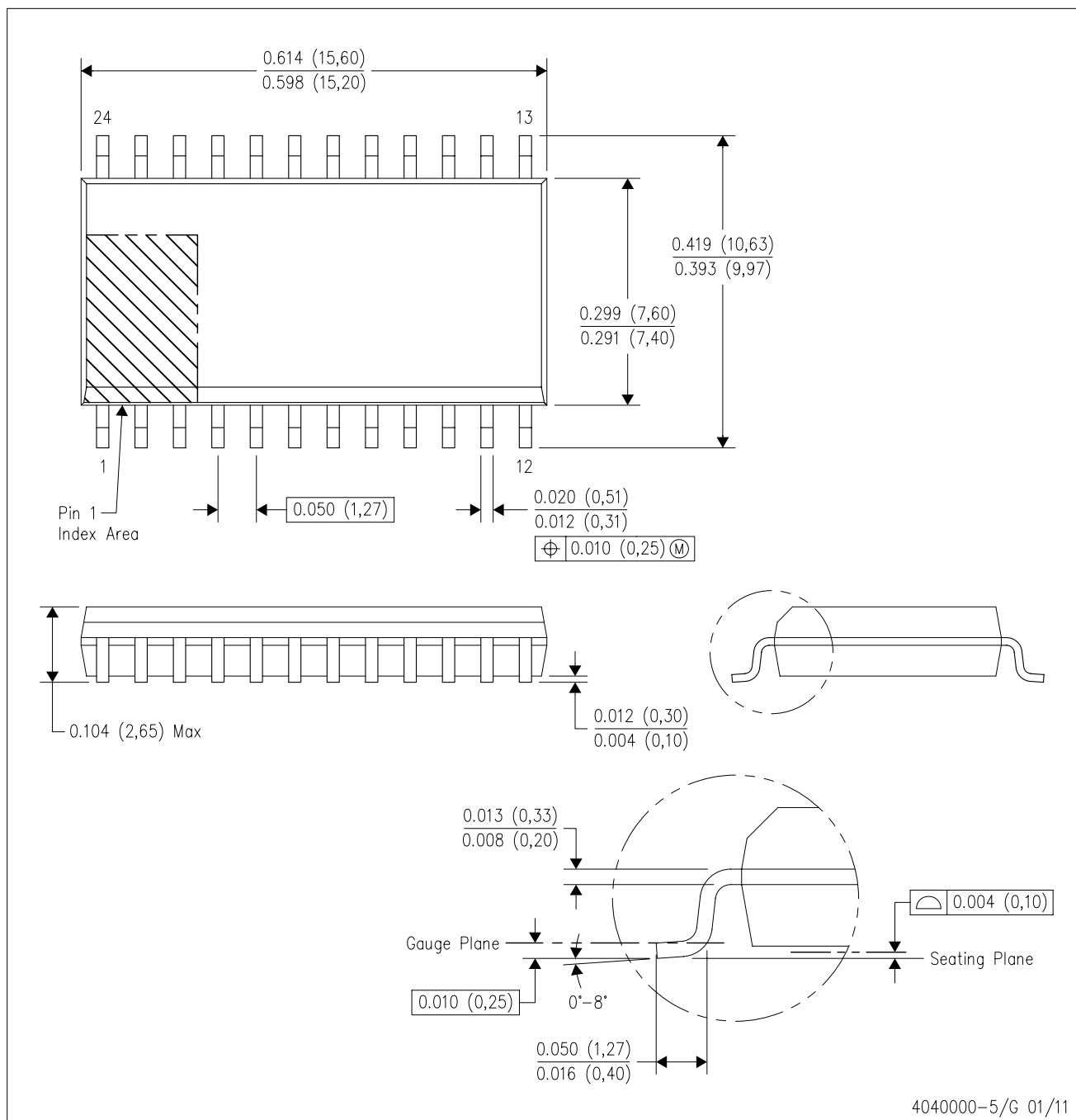
- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



DW (R-PDSO-G24)

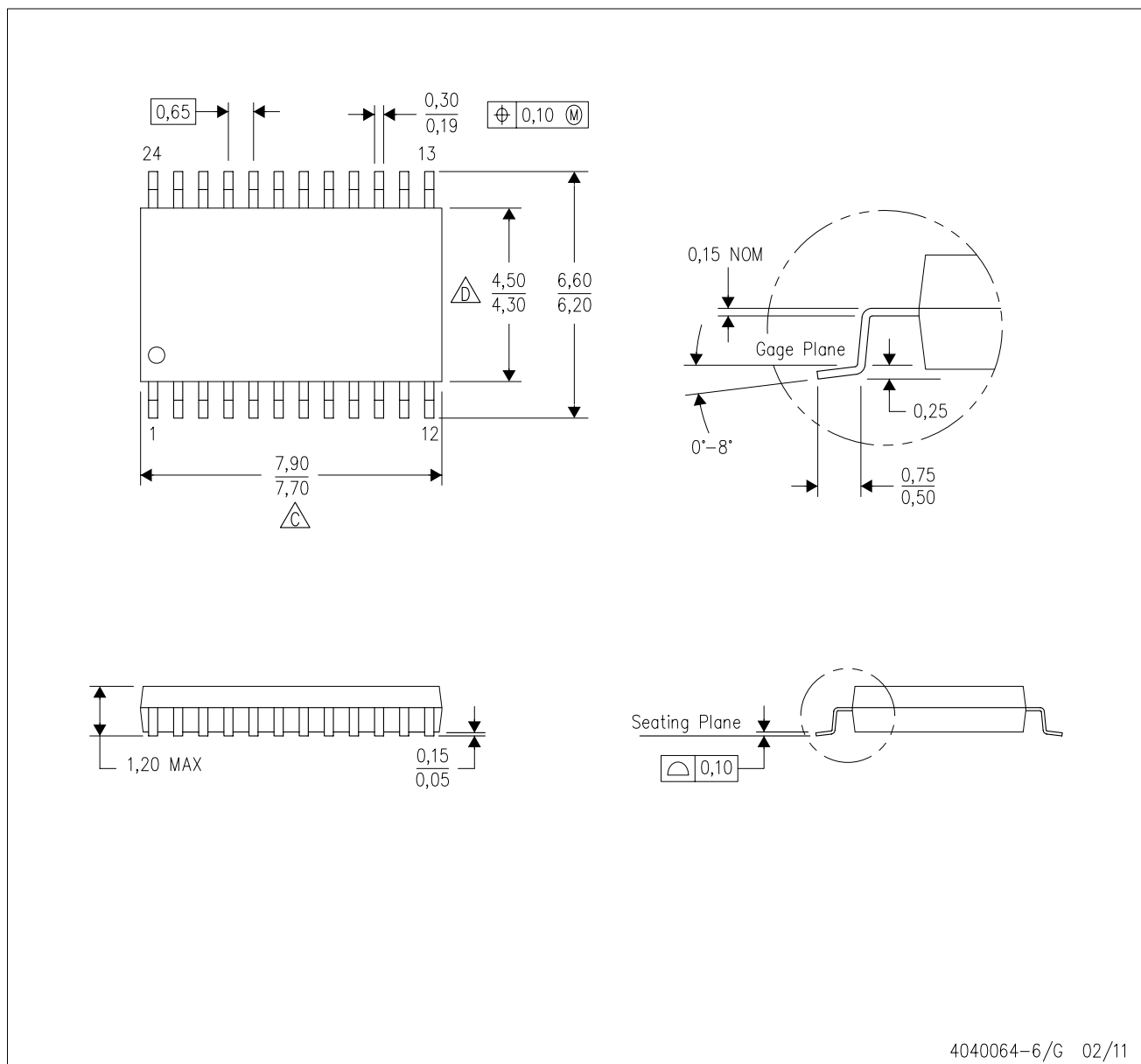
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AD.

PW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



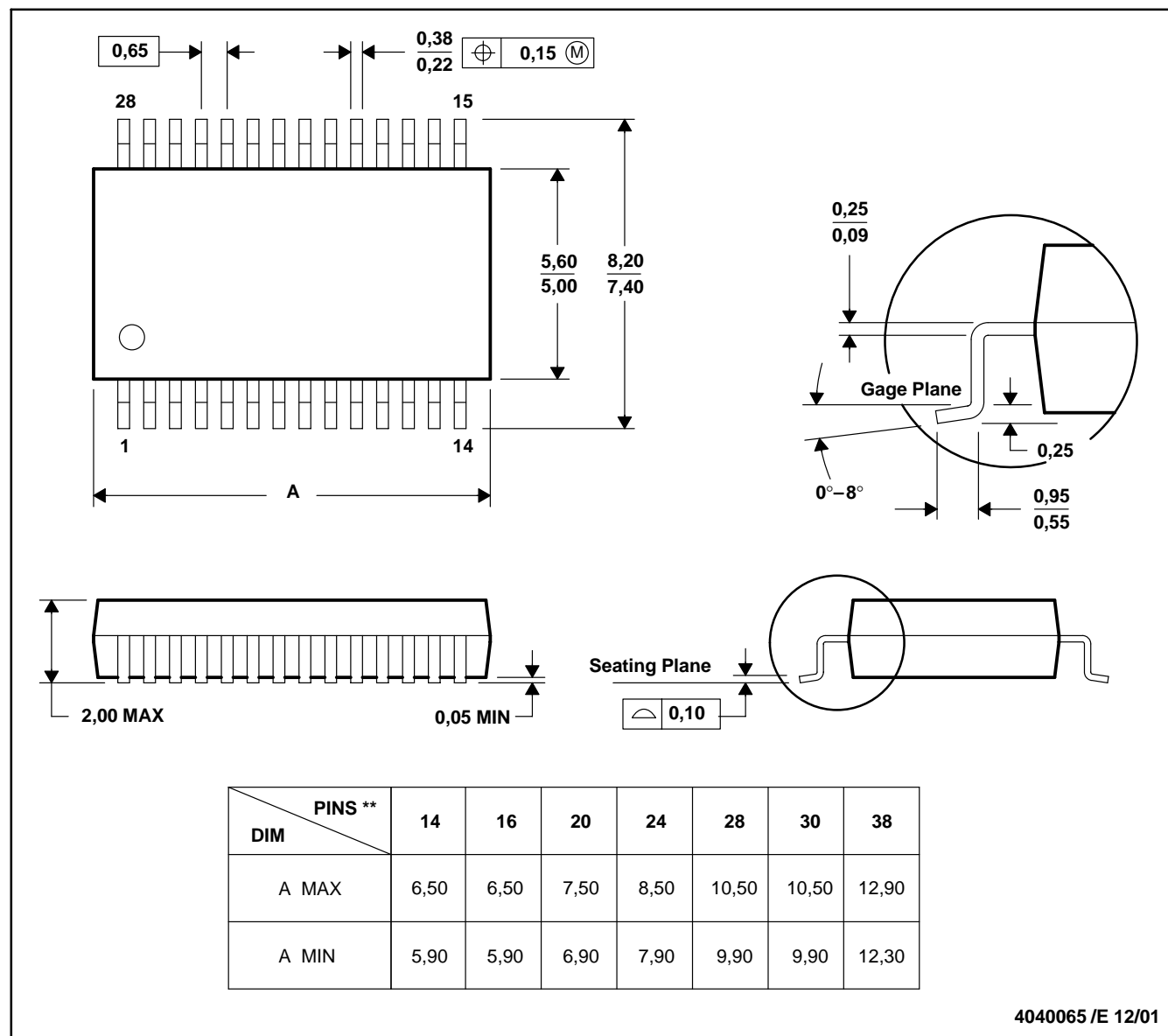
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- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

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