

N-channel 800 V, 0.95 Ω typ., 6 A MDmesh™ K5
Power MOSFETs in DPAK, TO-220 and IPAK packages

Datasheet - production data

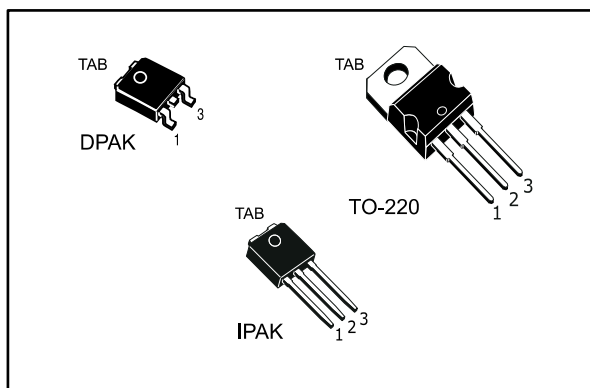
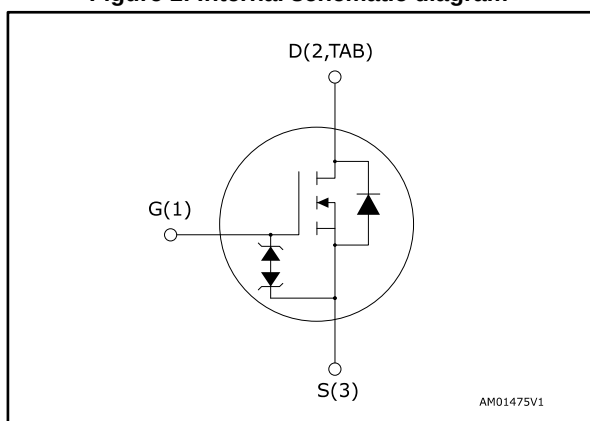


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max	I _D	P _{TOT}
STD7N80K5	800 V	1.2 Ω	6 A	110 W
STP7N80K5				
STU7N80K5				

- Industry's lowest R_{DS(on)} x area
- Industry's best FoM (figure of merit)
- Ultra-low gate charge
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

This very high voltage N-channel Power MOSFET is designed using MDmesh™ K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

Table 1: Device summary

Order code	Marking	Package	Packaging
STD7N80K5	7N80K5	DPAK	Tape and reel
STP7N80K5		TO-220	Tube
STU7N80K5		IPAK	

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V _{GS}	Gate- source voltage	± 30	V
I _D	Drain current (continuous) at T _C = 25 °C	6	A
I _D	Drain current (continuous) at T _C = 100 °C	3.8	A
I _{DM} ⁽¹⁾	Drain current (pulsed)	24	A
P _{TOT}	Total dissipation at T _C = 25 °C	110	W
I _{AR}	Max current during repetitive or single pulse avalanche (pulse width limited by T _{Jmax})	2	A
E _{AS}	Single pulse avalanche energy (starting T _J = 25 °C, I _D =I _{AS} , V _{DD} = 50 V)	88	mJ
dv/dt ⁽²⁾	Peak diode recovery voltage slope	4.5	V/ns
dv/dt ⁽³⁾	MOSFET dv/dt ruggedness	50	V/ns
T _j	Operating junction temperature range	-55 to 150	°C
T _{stg}	Storage temperature range		°C

Notes:⁽¹⁾Pulse width limited by safe operating area.⁽²⁾I_{SD} ≤ 6 A, di/dt ≤ 100 A/μs, V_{DS(peak)} ≤ V_{(BR)DSS}⁽³⁾V_{DS} ≤ 640 V

Table 3: Thermal data

Symbol	Parameter	Value			Unit
		DPAK	TO-220	IPAK	
R _{thj-case}	Thermal resistance junction-case	1.14			°C/W
R _{thj-amb}	Thermal resistance junction-amb		62.5	100	°C/W
R _{thj-pcb} ⁽¹⁾	Thermal resistance junction-pcb	50			°C/W

Notes:⁽¹⁾When mounted on 1 inch² FR-4, 2 Oz copper board.

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified).

Table 4: On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	V _{GS} = 0 V; I _D = 1 mA	800			V
I _{DSS}	Zero gate voltage drain current	V _{GS} = 0 V; V _{DS} = 800 V			1	μA
		V _{GS} = 0 V; V _{DS} = 800 V, T _C = 125 °C ⁽¹⁾			50	μA
I _{GSS}	Gate body leakage current	V _{DS} = 0 V; V _{GS} = ± 20 V			±10	μA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 100 μA	3	4	5	V
R _{DS(on)}	Static drain-source on-resistance	V _{GS} = 10 V, I _D = 3 A		0.95	1.2	Ω

Notes:

⁽¹⁾Defined by design, not subject to production test.

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C _{iss}	Input capacitance	V _{DS} = 100 V, f = 1 MHz, V _{GS} = 0 V	-	360	-	pF
C _{oss}	Output capacitance		-	30	-	pF
C _{rss}	Reverse transfer capacitance		-	1	-	pF
C _{o(tr)} ⁽¹⁾	Equivalent capacitance time related	V _{GS} = 0 V, V _{DS} = 0 to 640 V	-	47	-	pF
C _{o(er)} ⁽²⁾	Equivalent capacitance energy related		-	20	-	pF
R _G	Intrinsic gate resistance	f = 1 MHz, I _D = 0 A	-	6	-	Ω
Q _g	Total gate charge	V _{DD} = 640 V, I _D = 6 A	-	13.4	-	nC
Q _{gs}	Gate-source charge	V _{GS} = 0 to 10 V	-	3.7	-	nC
Q _{gd}	Gate-drain charge	(see Figure 18: "Test circuit for gate charge behavior")	-	7.5	-	nC

Notes:

⁽¹⁾Time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

⁽²⁾Energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 400\text{ V}$, $I_D = 3\text{ A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (see Figure 17: "Test circuit for resistive load switching times" and Figure 22: "Switching time waveform")	-	11.3	-	ns
t_r	Rise time		-	8.3	-	ns
$t_{d(off)}$	Turn-off delay time		-	23.7	-	ns
t_f	Fall time		-	20.2	-	ns

Table 7: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		6	A
I_{SDM}	Source-drain current (pulsed)		-		24	A
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD} = 6\text{ A}$, $V_{GS} = 0\text{ V}$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 6\text{ A}$, $V_{DD} = 60\text{ V}$ $di/dt = 100\text{ A}/\mu\text{s}$, (see Figure 19: "Test circuit for inductive load switching and diode recovery times")	-	315		ns
Q_{rr}	Reverse recovery charge		-	2.8		μC
I_{RRM}	Reverse recovery current		-	17.5		A
t_{rr}	Reverse recovery time	$I_{SD} = 6\text{ A}$, $V_{DD} = 60\text{ V}$ $di/dt = 100\text{ A}/\mu\text{s}$, $T_j = 150\text{ }^\circ\text{C}$ (see Figure 19: "Test circuit for inductive load switching and diode recovery times")	-	480		ns
Q_{rr}	Reverse recovery charge		-	3.8		μC
I_{RRM}	Reverse recovery current		-	16		A

Notes:

⁽¹⁾Pulsed: pulse duration = 300 μs , duty cycle 1.5%

Table 8: Gate-source Zener diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 1\text{ mA}$, $I_D = 0\text{ A}$	± 30	-	-	V

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area for DPAK and IPAK

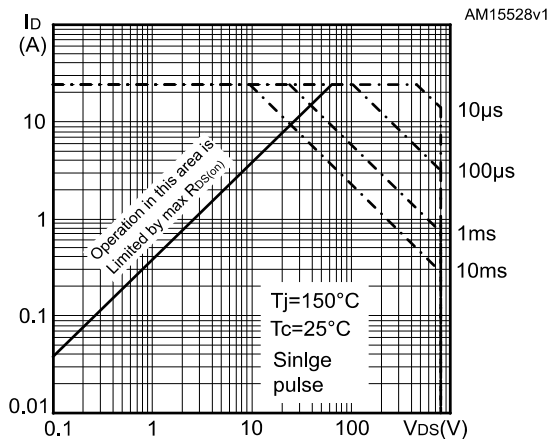


Figure 3: Thermal impedance for DPAK and IPAK

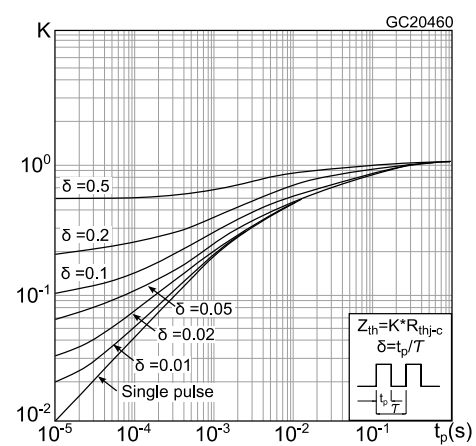


Figure 4: Safe operating area for TO-220

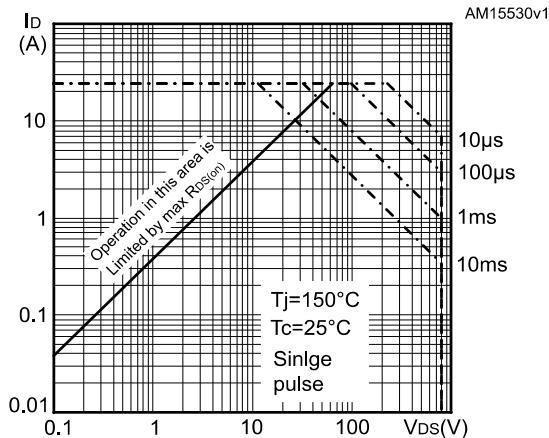


Figure 5: Thermal impedance for TO-220

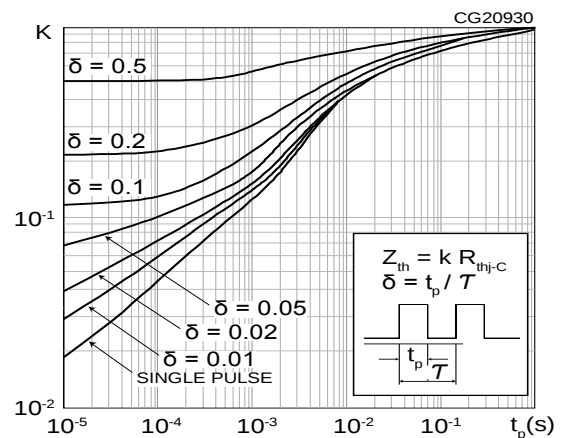


Figure 6: Output characteristics

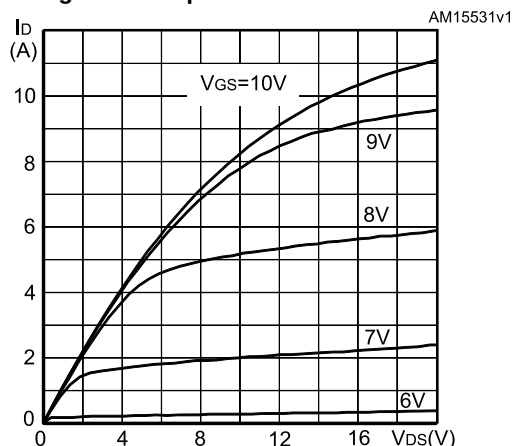


Figure 7: Transfer characteristics

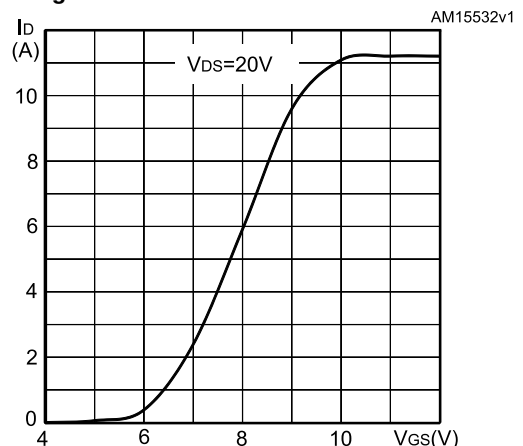


Figure 8: Gate charge vs gate-source voltage

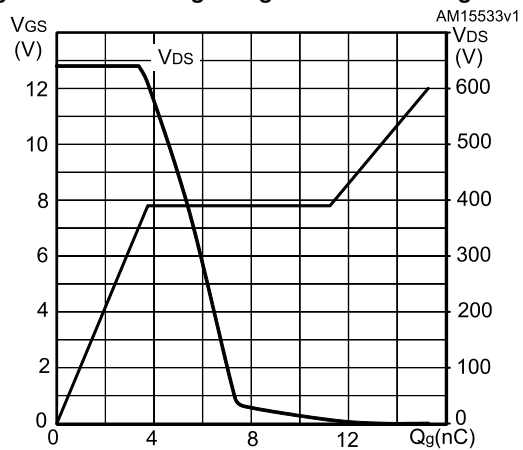


Figure 9: Static drain-source on-resistance

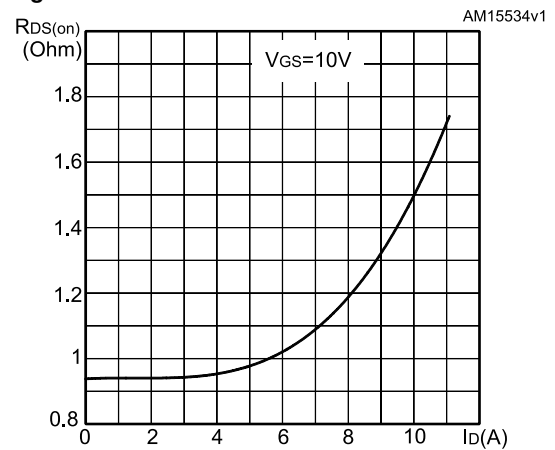


Figure 10: Capacitance variations

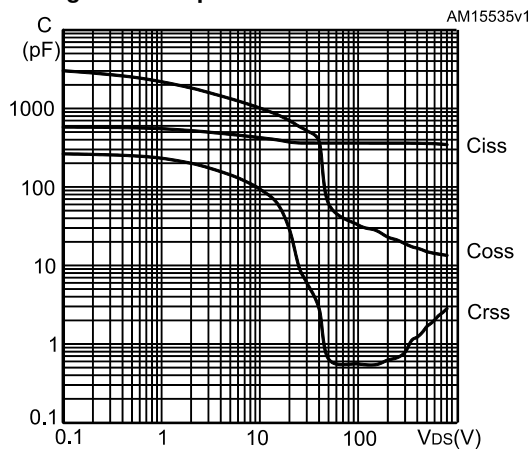


Figure 11: Output capacitance stored energy

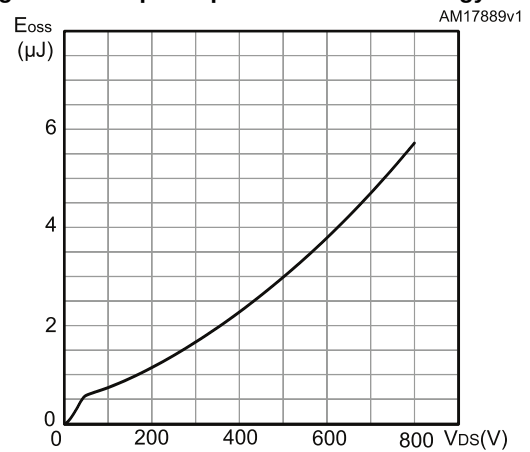


Figure 12: Normalized gate threshold voltage vs temperature

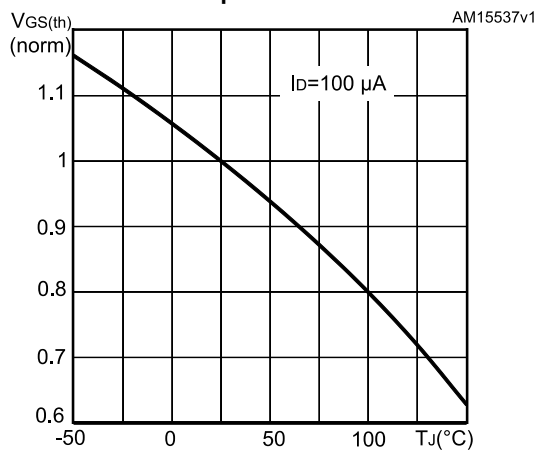


Figure 13: Normalized on-resistance vs temperature

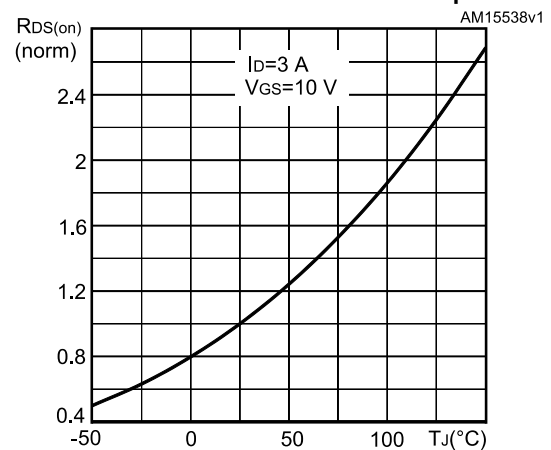


Figure 14: Maximum avalanche energy vs starting T_J

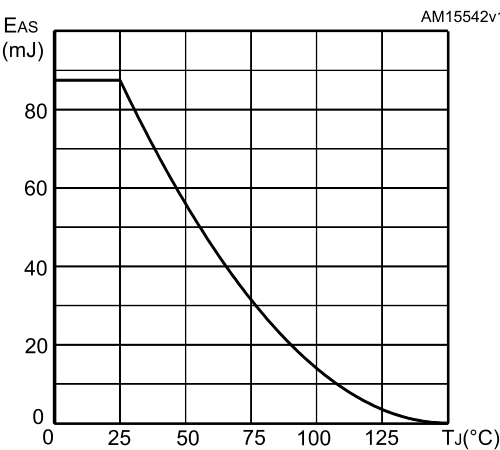


Figure 15: Normalized $V_{(BR)DSS}$ vs temperature

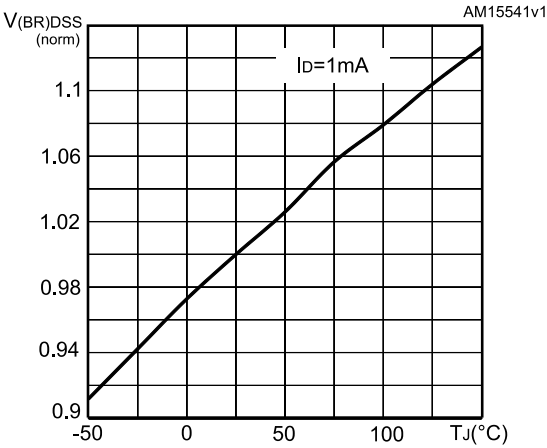
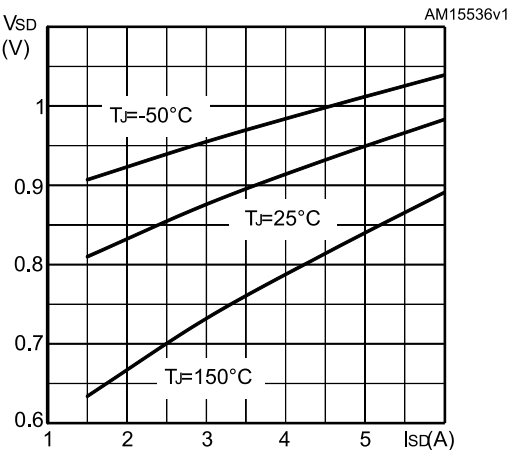


Figure 16: Source-drain diode forward characteristics



3 Test circuits

Figure 17: Test circuit for resistive load switching times



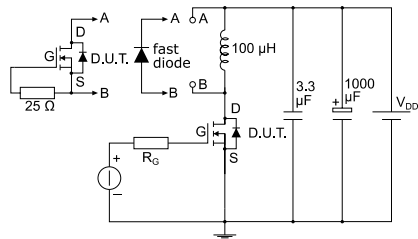
AM01468v1

Figure 18: Test circuit for gate charge behavior



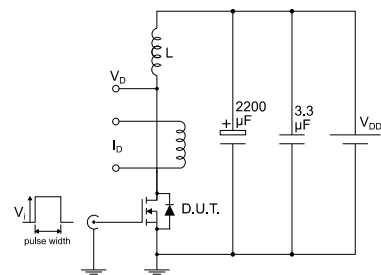
AM01469v1

Figure 19: Test circuit for inductive load switching and diode recovery times



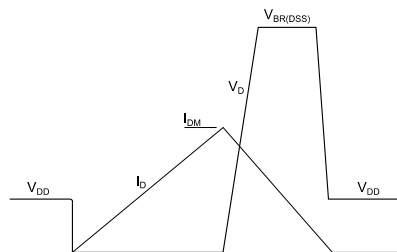
AM01470v1

Figure 20: Unclamped inductive load test circuit



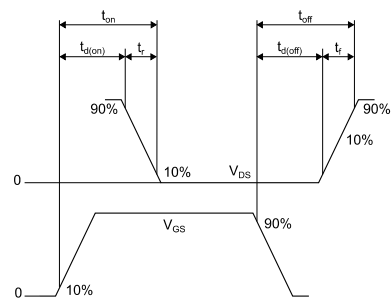
AM01471v1

Figure 21: Unclamped inductive waveform



AM01472v1

Figure 22: Switching time waveform



AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: **www.st.com**. ECOPACK® is an ST trademark.

4.1 DPAK type A2 package information

Figure 23: DPAK (TO-252) type A2 package outline

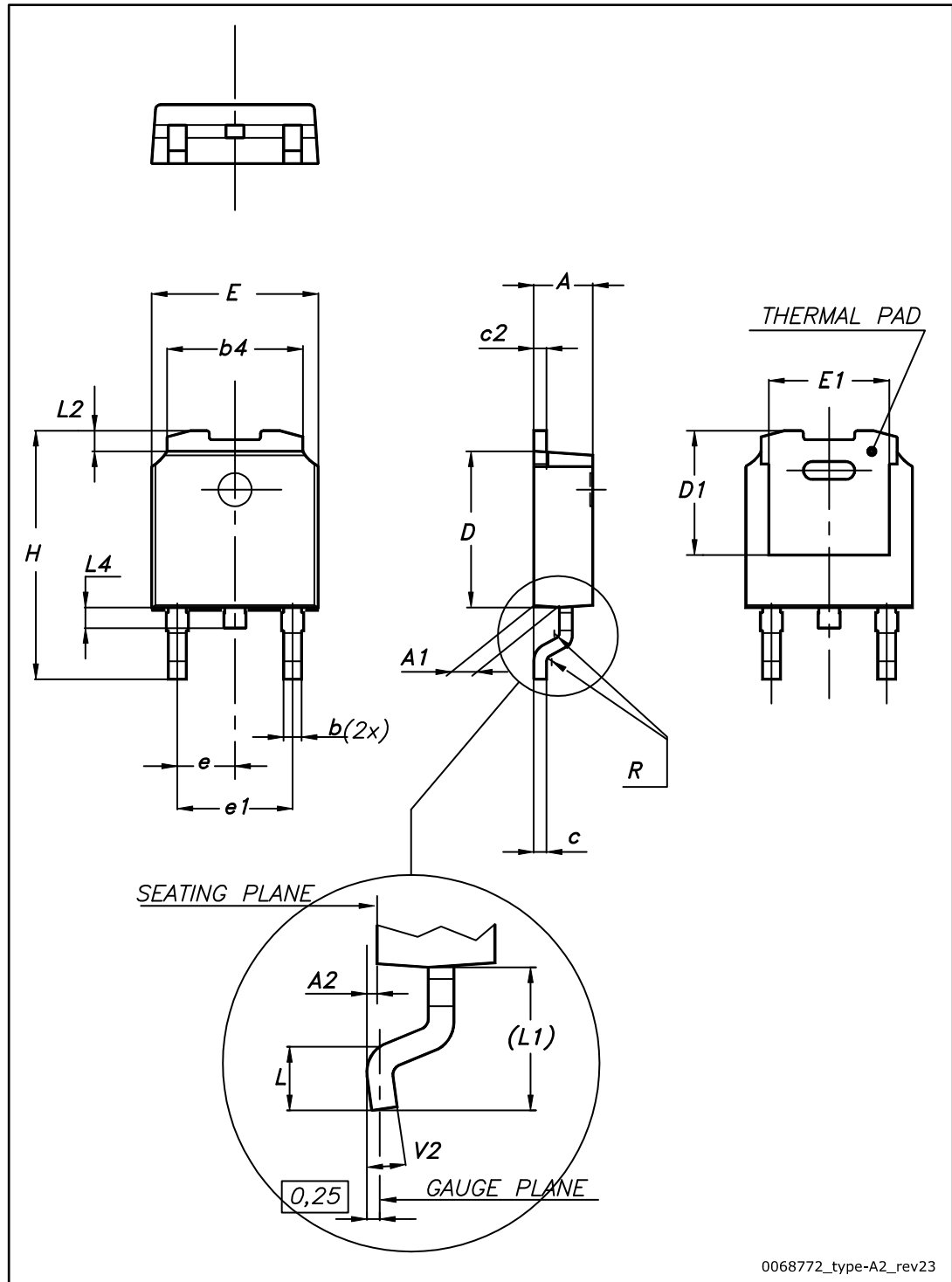
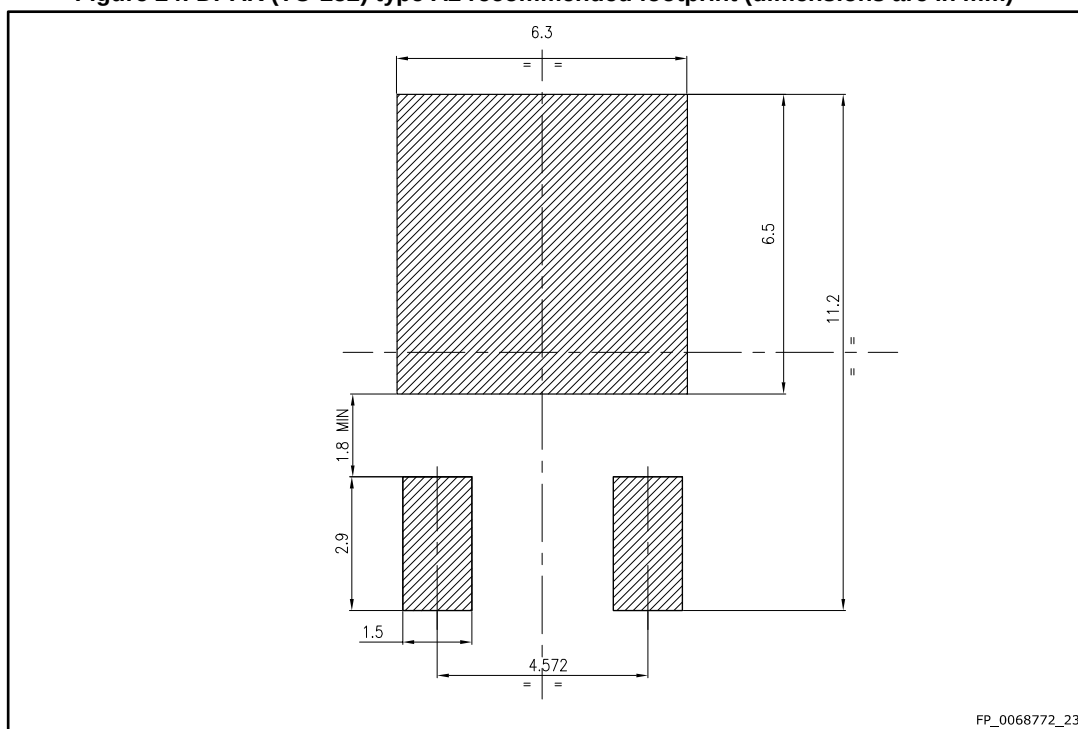


Table 9: DPAK (TO-252) type A2 mechanical data

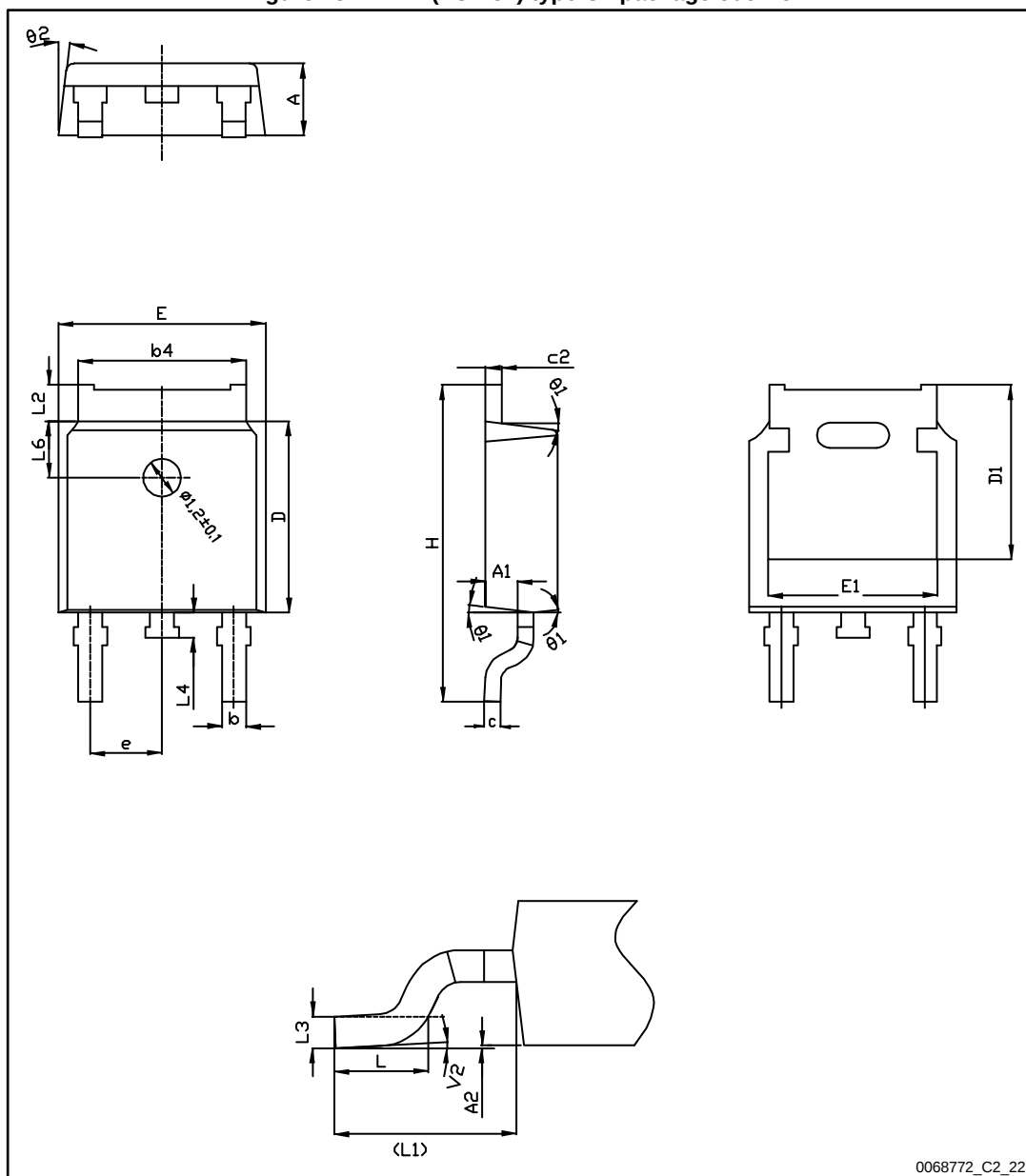
Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	5.10	5.20	5.30
e	2.16	2.28	2.40
e1	4.40		4.60
H	9.35		10.10
L	1.00		1.50
L1	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

Figure 24: DPAK (TO-252) type A2 recommended footprint (dimensions are in mm)



4.2 DPAK type C2 package information

Figure 25: DPAK (TO-252) type C2 package outline

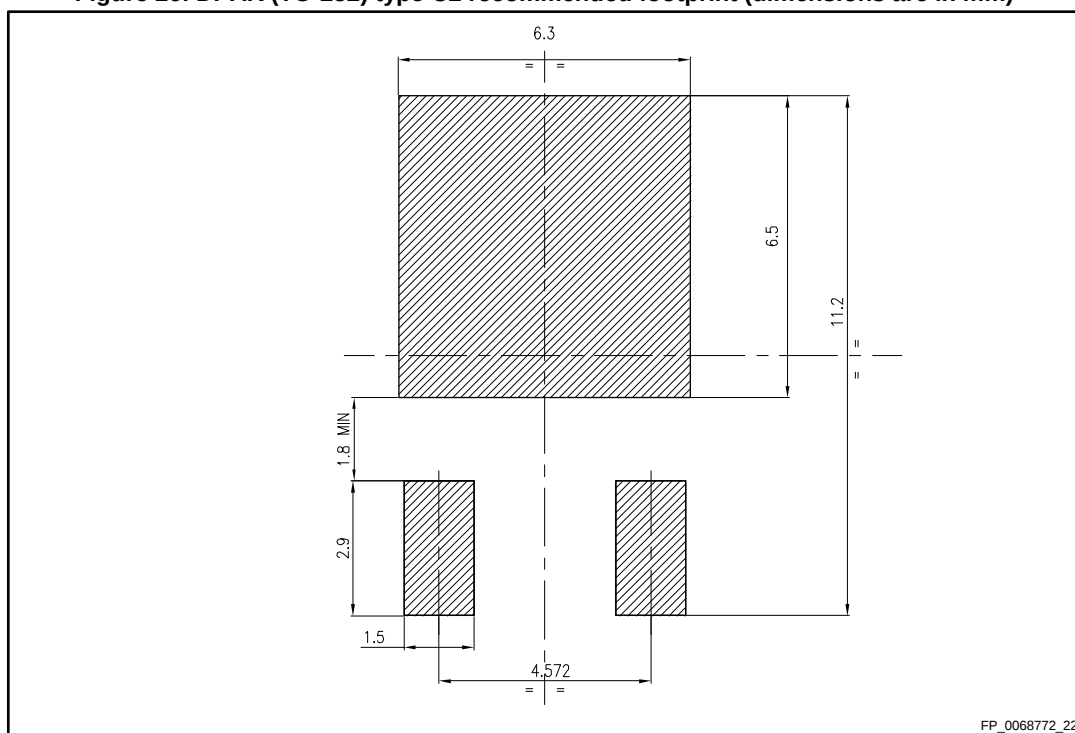


0068772_C2_22

Table 10: DPAK (TO-252) type C2 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20	2.30	2.38
A1	0.90	1.01	1.10
A2	0.00		0.10
b	0.72		0.85
b4	5.13	5.33	5.46
c	0.47		0.60
c2	0.47		0.60
D	6.00	6.10	6.20
D1	5.10		5.60
E	6.50	6.60	6.70
E1	5.20		5.50
e	2.186	2.286	2.386
H	9.80	10.10	10.40
L	1.40	1.50	1.70
L1	2.90 REF		
L2	0.90		1.25
L3	0.51 BSC		
L4	0.60	0.80	1.00
L6	1.80 BSC		
θ1	5°	7°	9°
θ2	5°	7°	9°
V2	0°		8°

Figure 26: DPAK (TO-252) type C2 recommended footprint (dimensions are in mm)



4.3 DPAK type E package information

Figure 27: DPAK (TO-252) type E package outline

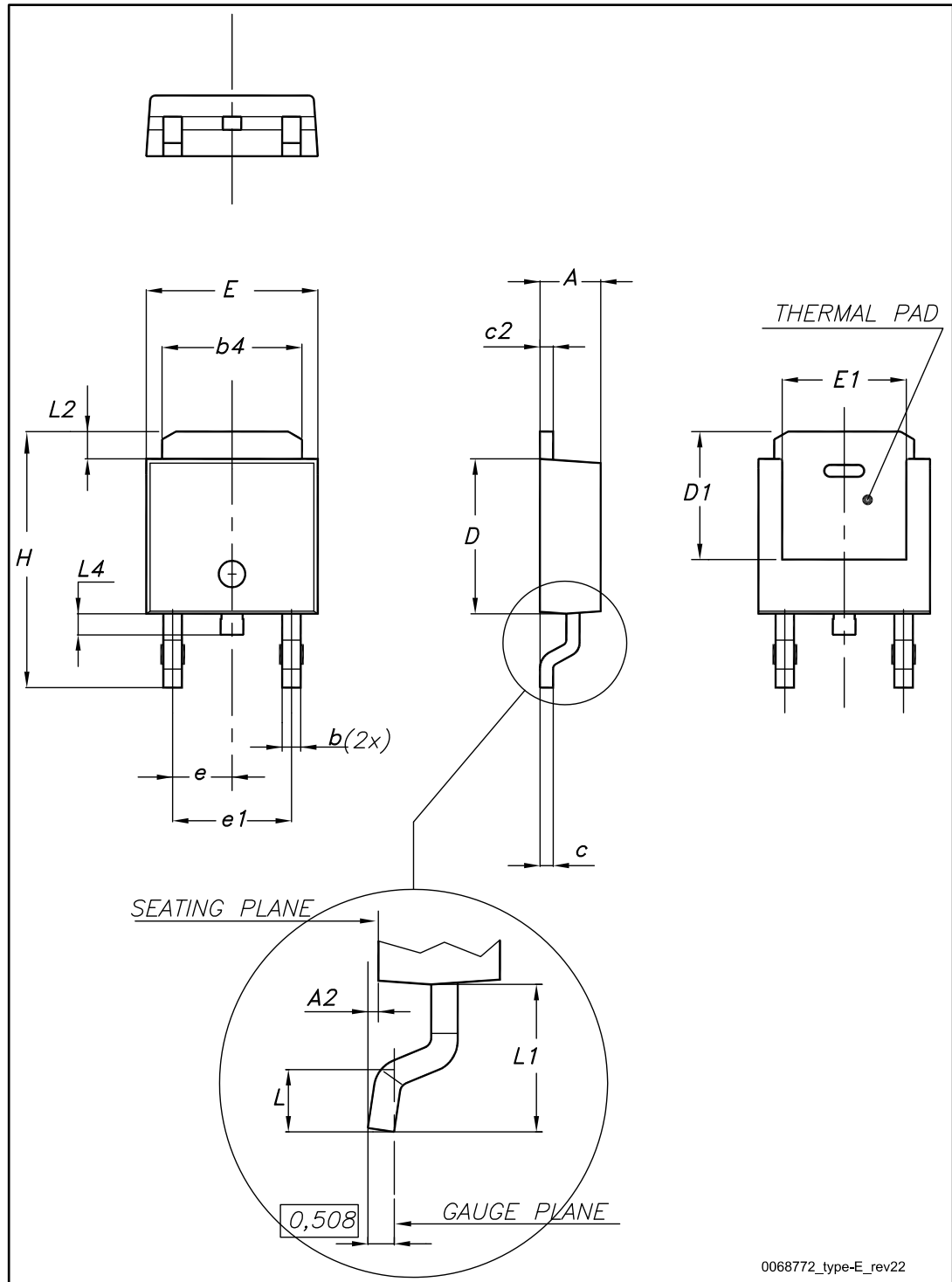
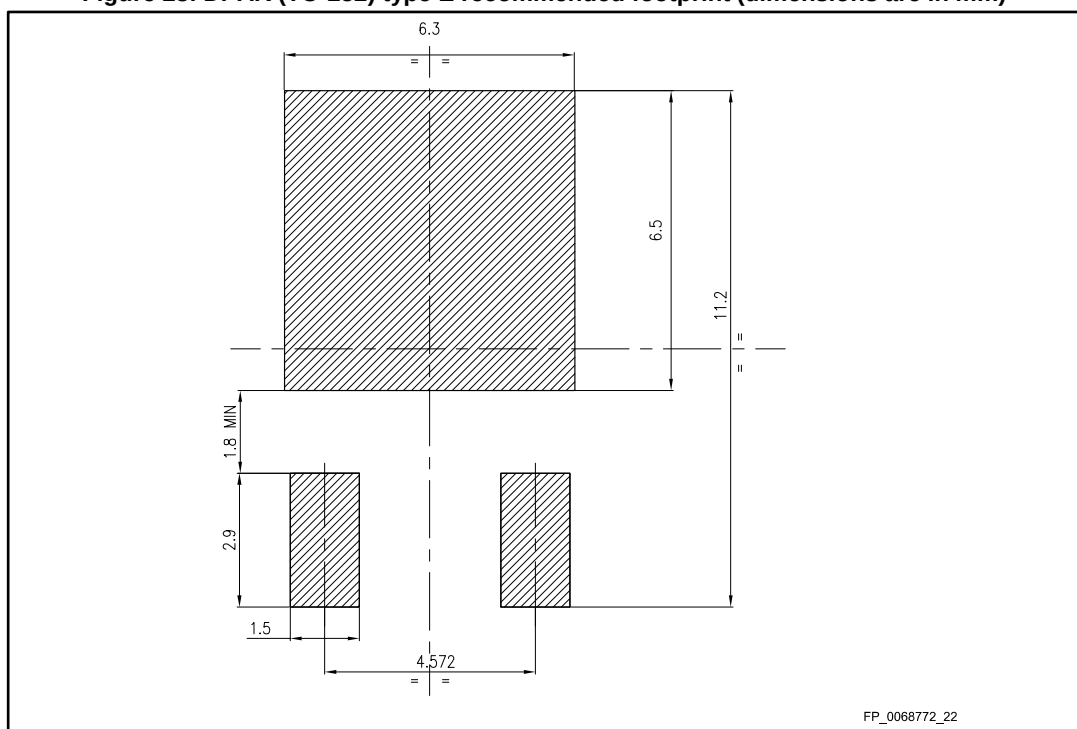


Table 11: DPAK (TO-252) type E mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.18		2.39
A2			0.13
b	0.65		0.884
b4	4.95		5.46
c	0.46		0.61
c2	0.46		0.60
D	5.97		6.22
D1	5.21		
E	6.35		6.73
E1	4.32		
e		2.286	
e1		4.572	
H	9.94		10.34
L	1.50		1.78
L1		2.74	
L2	0.89		1.27
L4			1.02

Figure 28: DPAK (TO-252) type E recommended footprint (dimensions are in mm)



4.4 TO-220 package information

Figure 29: TO-220 type A package outline

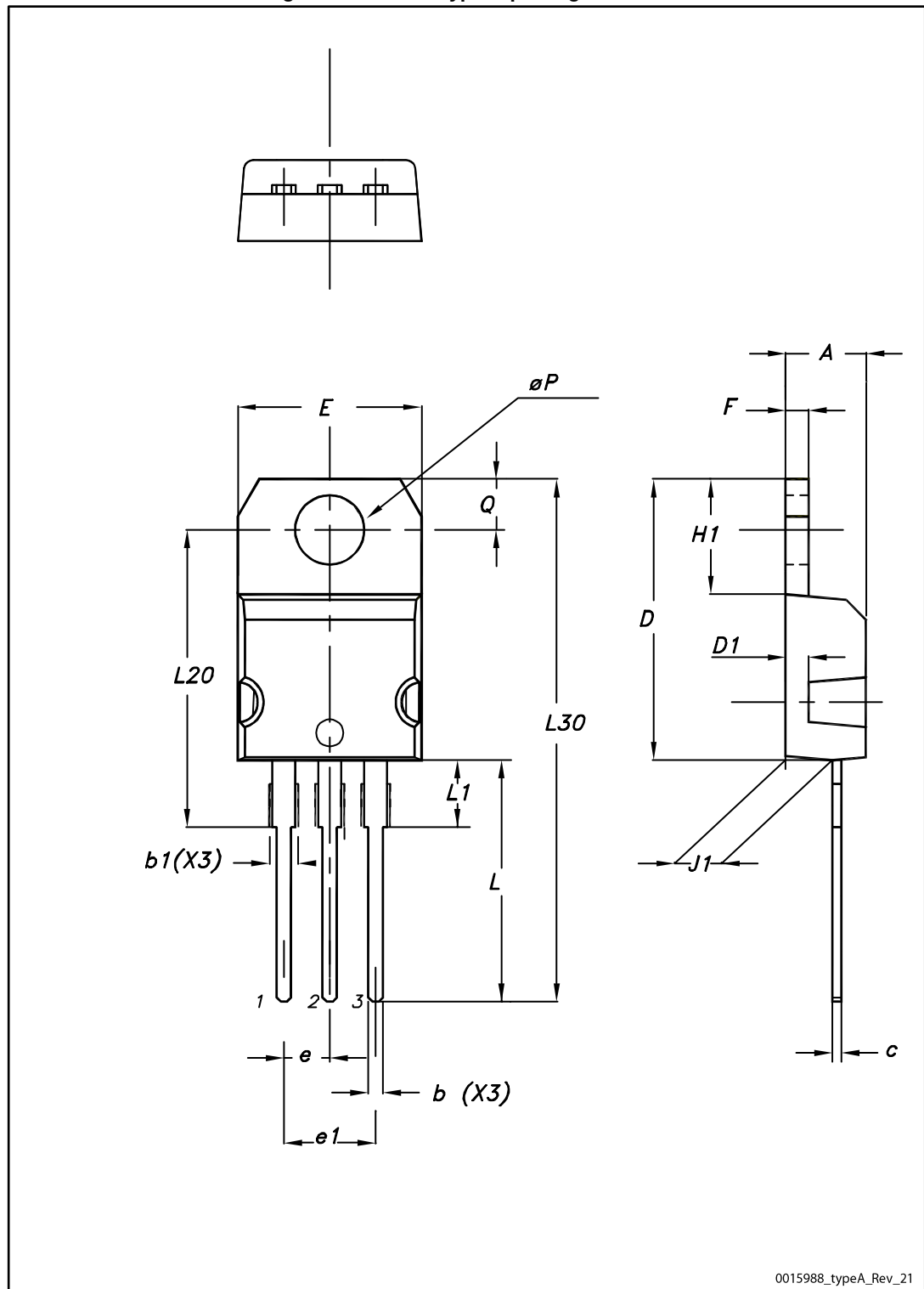


Table 12: TO-220 type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95

4.5 IPAK type A package information

Figure 30: IPAK (TO-251) type A package outline

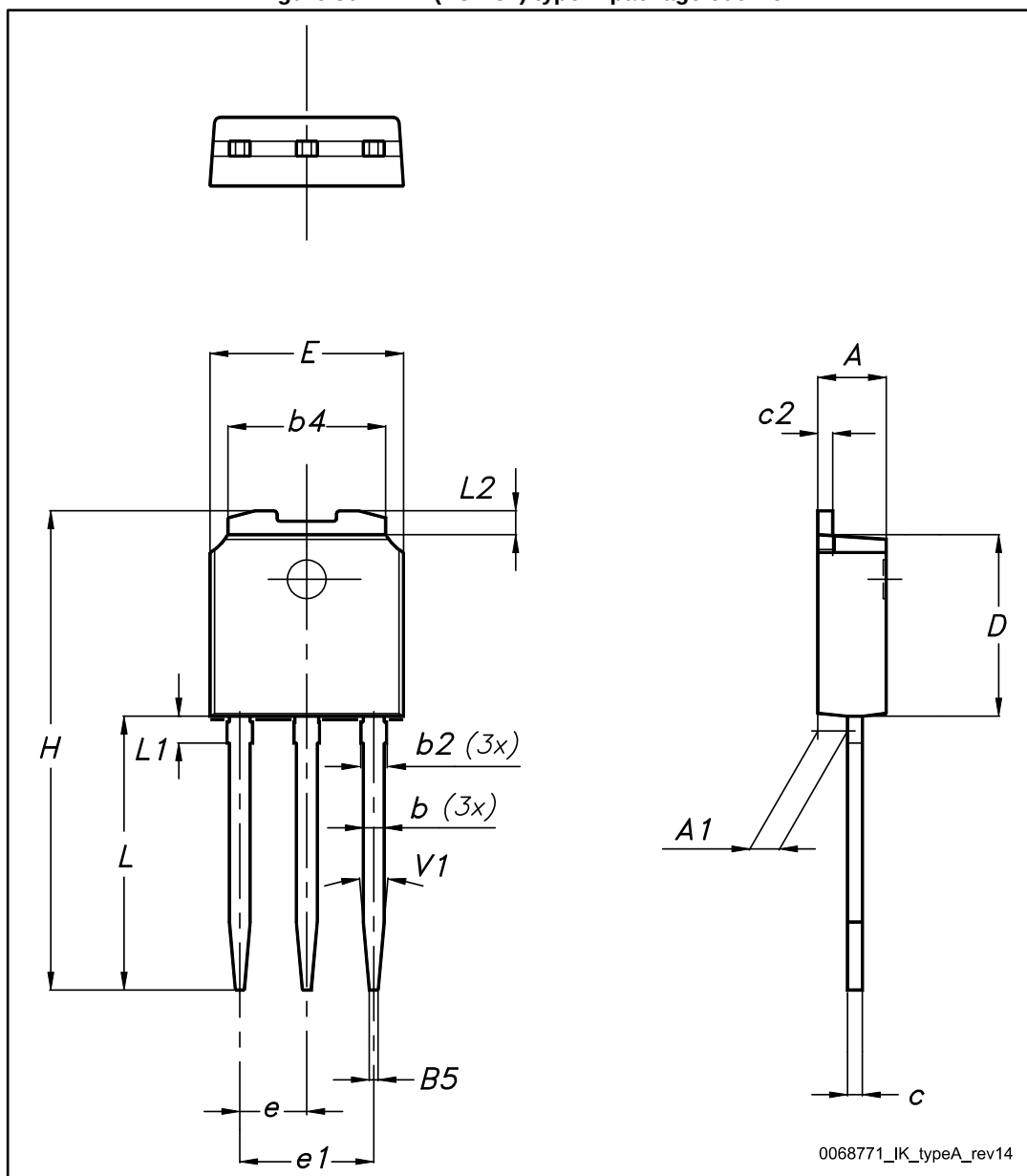


Table 13: IPAK (TO-251) type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
b	0.64		0.90
b2			0.95
b4	5.20		5.40
B5		0.30	
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
E	6.40		6.60
e		2.28	
e1	4.40		4.60
H		16.10	
L	9.00		9.40
L1	0.80		1.20
L2		0.80	1.00
V1		10°	

4.6 IPAK type C package information

Figure 31: IPAK (TO-251) type C package outline

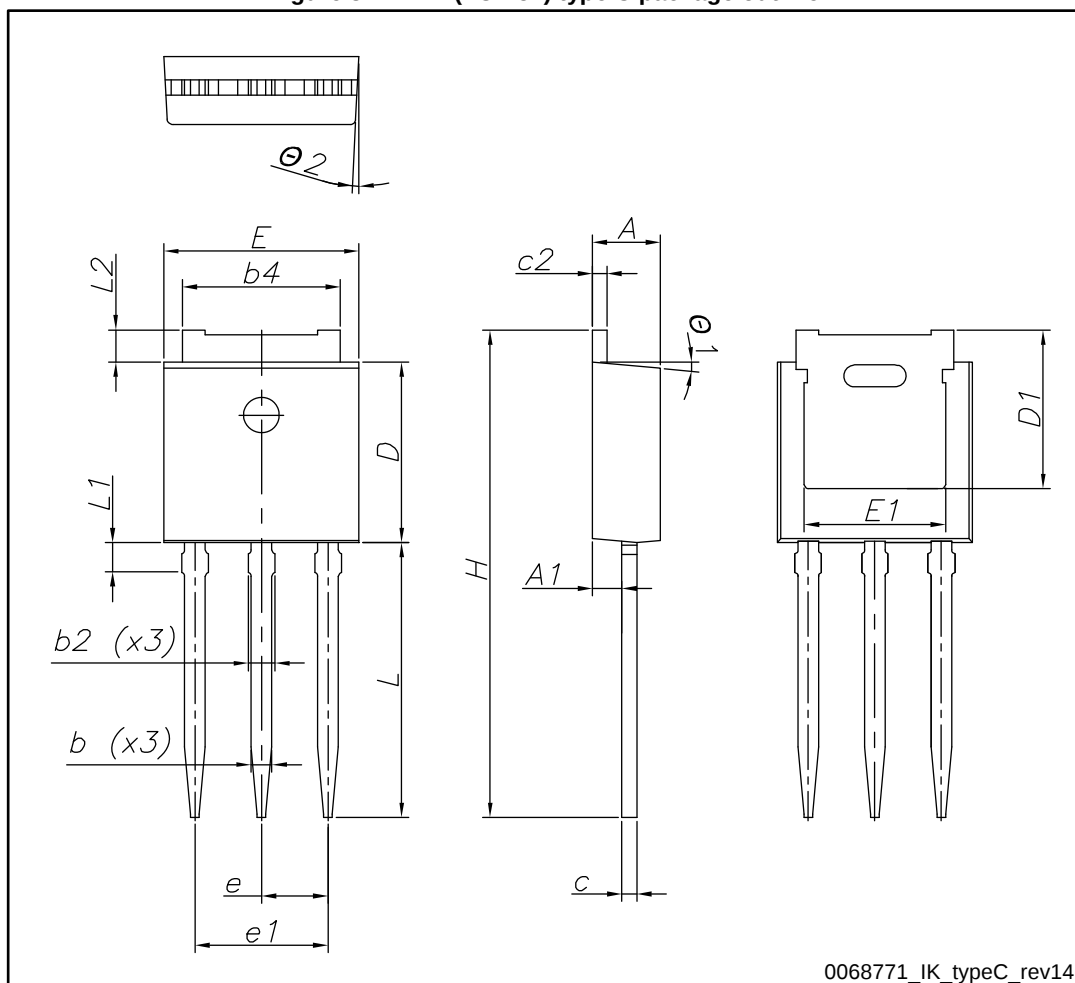


Table 14: IPAK (TO-251) type C package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20	2.30	2.35
A1	0.90	1.00	1.10
b	0.66		0.79
b2			0.90
b4	5.23	5.33	5.43
c	0.46		0.59
c2	0.46		0.59
D	6.00	6.10	6.20
D1	5.20	5.37	5.55
E	6.50	6.60	6.70
E1	4.60	4.78	4.95
e	2.20	2.25	2.30
e1	4.40	4.50	4.60
H	16.18	16.48	16.78
L	9.00	9.30	9.60
L1	0.80	1.00	1.20
L2	0.90	1.08	1.25
θ1	3°	5°	7°
θ2	1°	3°	5°

5 Packing mechanical data

Figure 32: DPAK (TO-252) tape outline

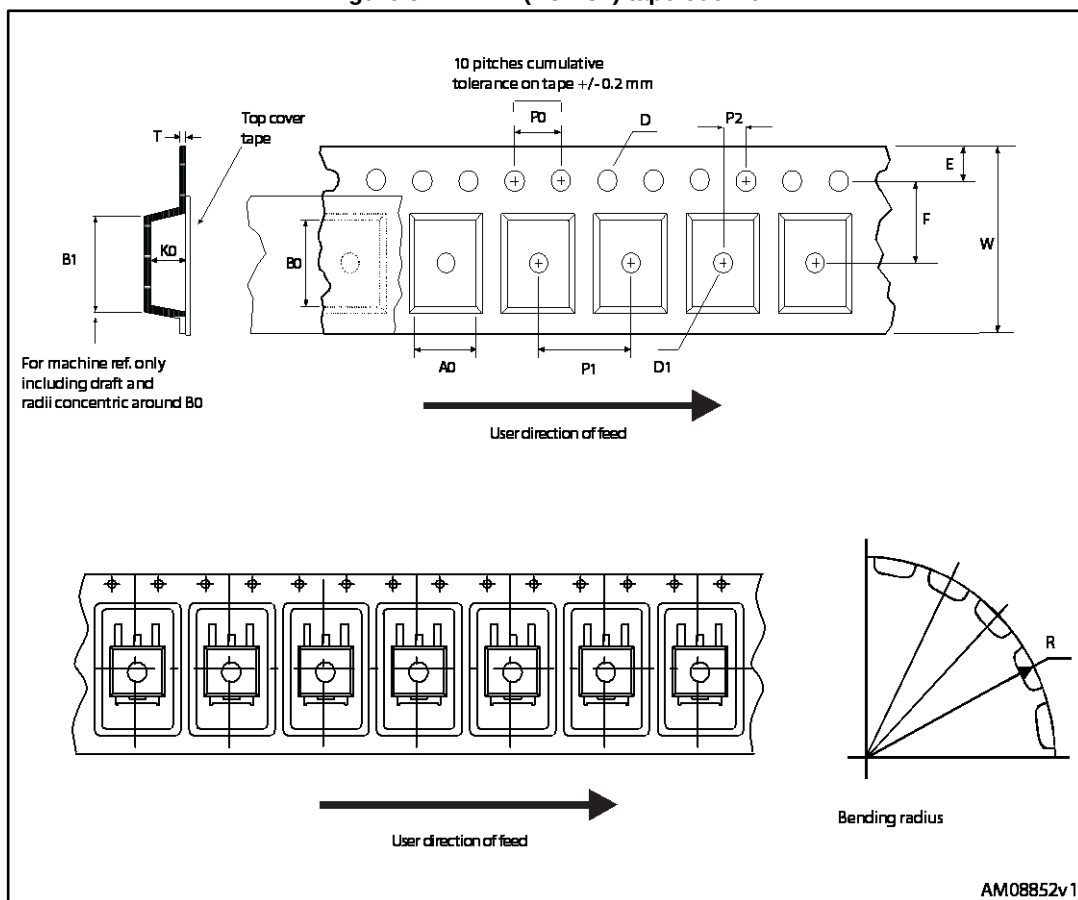


Figure 33: DPAK (TO-252) reel outline

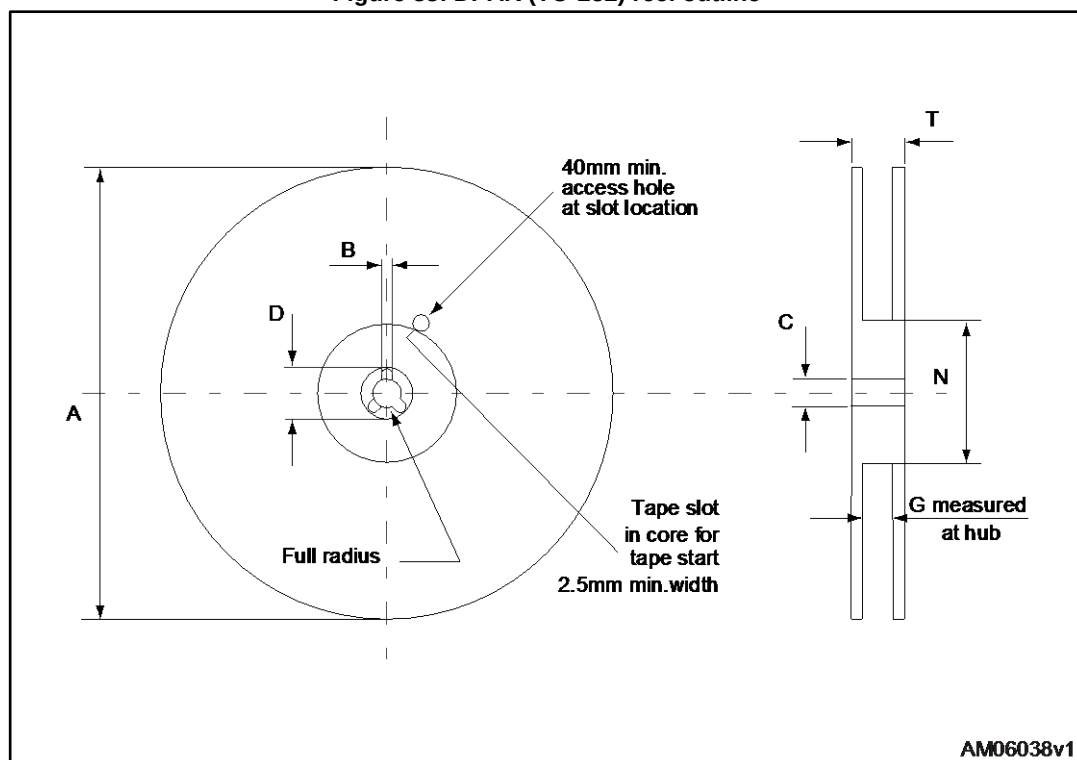


Table 15: DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

6 Revision history

Table 16: Document revision history

Date	Revision	Changes
17-Jul-2012	1	First release.
17-Oct-2012	2	Minor text changes in cover page Modified: title and I _D value in cover page
19-Dec-2012	3	Minor text changes Added: IPAK package Updated: Section 4: Package mechanical data for IPAK
18-Mar-2013	4	Modified: I _{AR} value on Table 2 Updated: Section 4: Package mechanical data only for DPAK package
09-Oct-2013	5	The part number STF7N80K5 has been moved to a separate datasheet Minor text changes
19-May-2017	6	Updated title, description and features in cover page. Updated Table 2: "Absolute maximum ratings" and Table 4: "On/off states" . Updated Section 4: "Package information" . Minor text changes.

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