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LV5212VH

Bi-CMOS IC

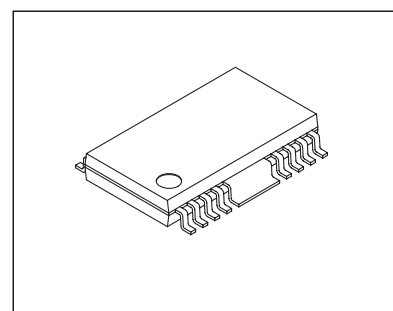
8ch LED Driver

Overview

The LV5212VH is a semiconductor integrated circuit that incorporates a serial input and serial or parallel output 8-stage shift register that features a CMOS structure based on Bi-CMOS process technology. The LV5212VH also contains an n-channel CMOS construction high-withstand-voltage, large-current drive 8-stage parallel output driver.

Function

- Serial input and serial or parallel output
- Enable input for output control
- Serial output enables cascade connection
- Low supply current (0.0μA typ. during standby)
- Serial input/output levels compatible with typical CMOS devices
- High-withstand-voltage LED driver with open drain output
 - High withstand voltage ($V_{DS} < 50V$)
 - High-current drive ($I_O \text{ max} = 300mA$)
- Operating temperature range $T_a = -25$ to $75^\circ C$



HSSOP16(275mil)

Specifications

Absolute Maximum Ratings at $T_a = 25^\circ C$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{CC \text{ max}}$	SV_{CC}	6	V
Output voltage	$V_O \text{ max}$	LEDO1 to LEDO8 off	50	V
Output current	$I_O \text{ max}$		300	mA
Allowable power dissipation	$P_d \text{ max}$	$T_a \leq 25^\circ C$ *	1000	mW
Operating temperature	T_{opr}		-25 to +75	$^\circ C$
Storage temperature	T_{stg}		-40 to +125	$^\circ C$

* Specified board : 114.3mm × 76.1mm × 1.6mm, glass epoxy board.

* The device must be used within the ranges warranted for its specifications so as to ensure its specified ratings (such as maximum ratings and operating condition ranges) are not exceeded even momentarily.

Use of the device in such a way that its ratings are exceeded may cause failures, damage and other problems.

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

ORDERING INFORMATION

See detailed ordering and shipping information on page 10 of this data sheet.

LV5212VH

Recommended Operating Conditions at $T_a = 25^\circ\text{C}$

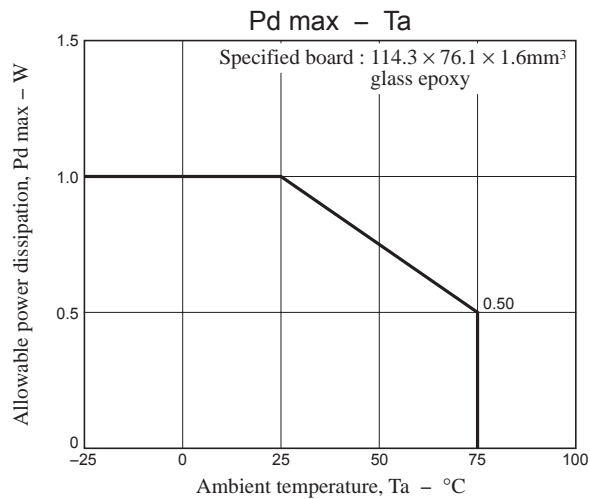
Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V_{CC}	SV_{CC}	5.0	V
Operating supply voltage range	$V_{CC\text{ op}}$	SV_{CC}	3.0 to 5.5	V
Output applied voltage	V_O		50	V
Output current	I_O	Duty = 45% to 55%	300	mA

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

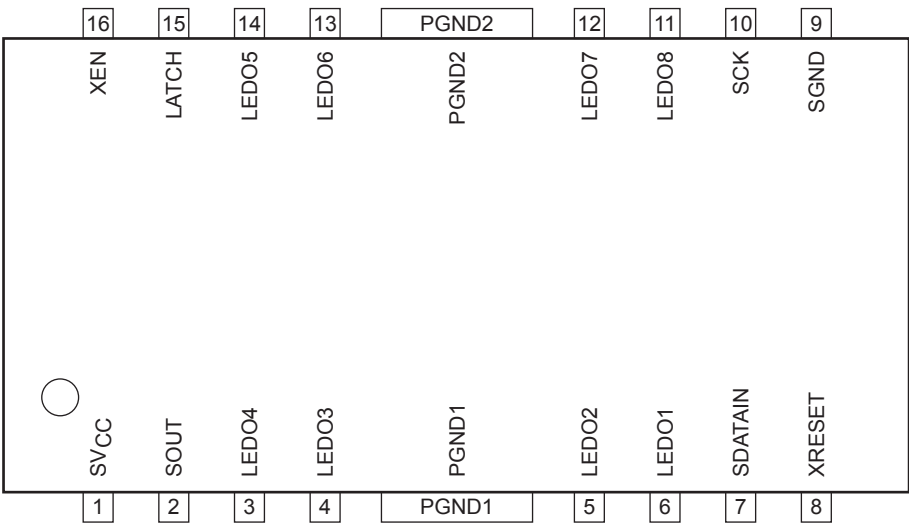
Electrical Characteristics at $T_a = 25^\circ\text{C}$, $V_{CC} = 5\text{V}$

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Quiescent current drain	I_{CC1}	LEDO driver off (standby)		0	5	μA
LEDO output on resistance	R_{on}	$I_O = 100\text{mA}$		3		Ω
OFF leak current	I_{leak}	$V_O = 50\text{V}$		0	10	μA
Control circuit block						
H level 1	V_{INH1}	Input H level	$V_{CC} \times 0.8$			V
L level 1	V_{INL1}	Input L level	0		$V_{CC} \times 0.2$	V
H level 2	V_{OUTH1}	SOUT $I_O = -1\text{mA}$	$V_{CC} - 0.3$			V
L level 2	V_{OUTL1}	SOUT $I_O = 1\text{mA}$	0		0.3	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.



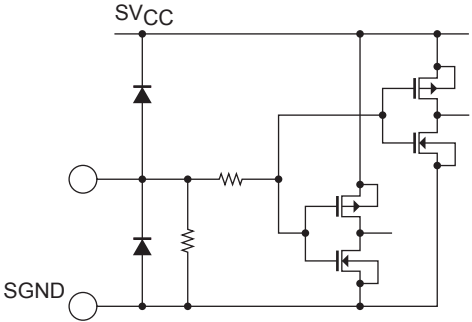
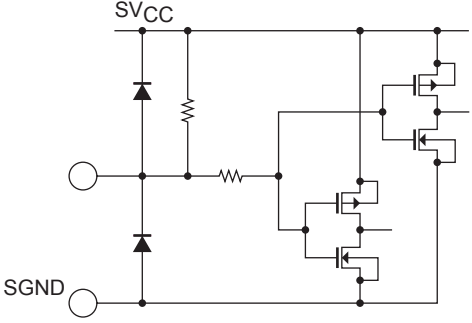
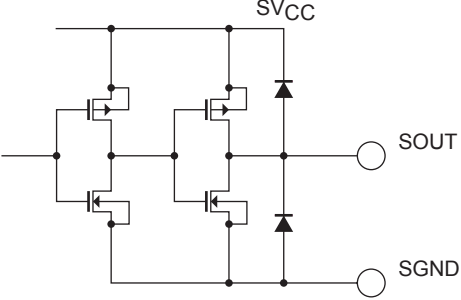
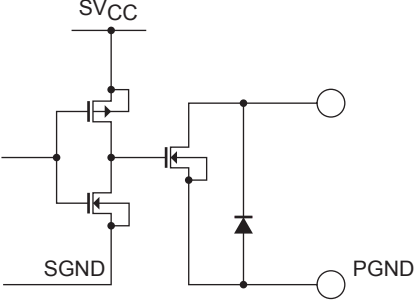
Pin Assignment



Pin Descriptions

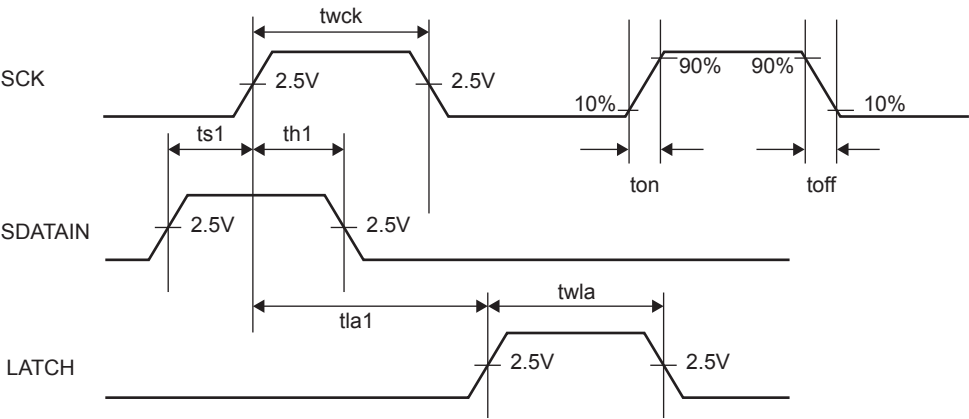
Pin No.	Pin name	I/O	Description
1	SVCC		Power supply
2	SOUT	O	shift register output (final-stage shift register)
3	LEDO4	O	LEDO4 Latch output (LEDO4 of shift register)
4	LEDO3	O	LEDO3 Latch output (LEDO3 of shift register)
5	LEDO2	O	LEDO2 Latch output (LEDO2 of shift register)
6	LEDO1	O	LEDO1 Latch output (LEDO1 of shift register)
7	SDATAIN	I	Serial input
8	XRESET	I	Reset input (shift register and latch)
9	SGND		GND
10	SCK	I	Clock input (for shift register)
11	LEDO8	O	LEDO8 Latch output (LEDO8 of shift register)
12	LEDO7	O	LEDO7 Latch output (LEDO7 of shift register)
13	LEDO6	O	LEDO6 Latch output (LEDO6 of shift register)
14	LEDO5	O	LEDO5 Latch output (LEDO5 of shift register)
15	LATCH	I	Latch input When the latch input is held low, the LED0 output status is retained. When a high-level is input, the LED0 outputs change when the status of the shift register changes.
16	XEN	I	Enable inputs (LEDO1 to LEDO8) When a high-level is input, all the LED0 outputs are turned off. When a low-level is input, the shift register data is output to LED0.
PGND1	PGND1		GND
PGND1	PGND2		GND

Pin Functions

Pin No.	Pin Name	Pin function	Equivalent Circuit
7 10	SDATAIN SCK	Pull-down input	
8 15 16	XRESET LATCH XEN	Pull-up input	
2	SOUT	SOUT output	
3 4 5 6 11 12 13 14	LEDO4 LEDO3 LEDO2 LEDO1 LEDO8 LEDO7 LEDO6 LEDO5	LEDO outputs LEDO1 to LEDO8	

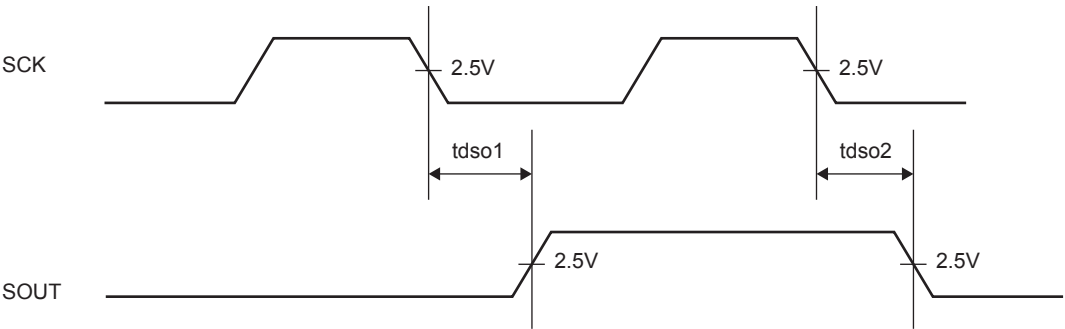
Timing conditions

Parameter	symbol	Conditions	min	typ	max	unit
Clock frequency	fs1	SCK Duty = 50%			10	MHz
Clock pulse width	twck	SCK	50			ns
Latch pulse width	twla	LATCH	50			ns
Data set up time	ts1	SDATAIN setup time relative to the rise of SCK	25			ns
Data hold time	th1	SDATAIN data hold time relative to the rise of SCK	25			ns
Clock latch time	tla1		100			ns
Input conditions 1	ton	SCK and SDATAIN rise time			100	ns
Input conditions 2	toff	SCL and SDATAIN fall time			100	ns



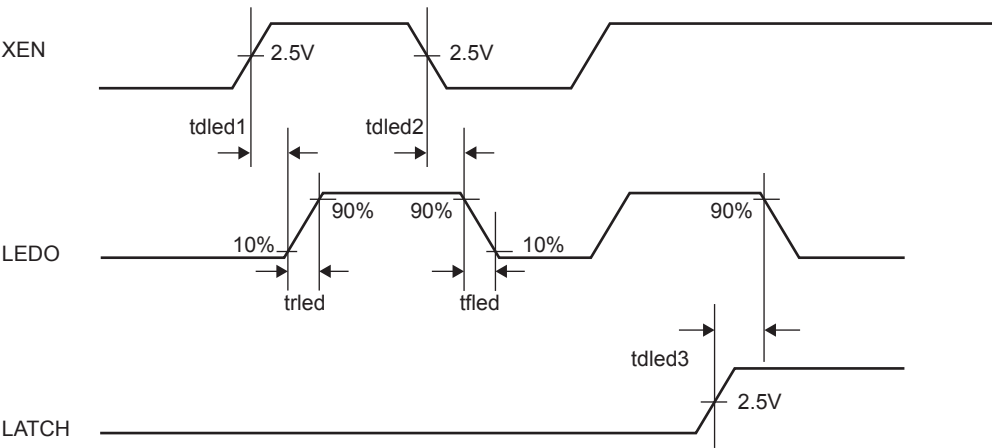
SOUT output timings

Parameter	symbol	Conditions	min	typ	max	unit
SOUT delay time 1	tdso1	The time from a SCK falling edge to SOUT rising edge			50	MHz
SOUT delay time 2	tdso2	The time from a SCK falling edge to SOUT falling edge			50	ns



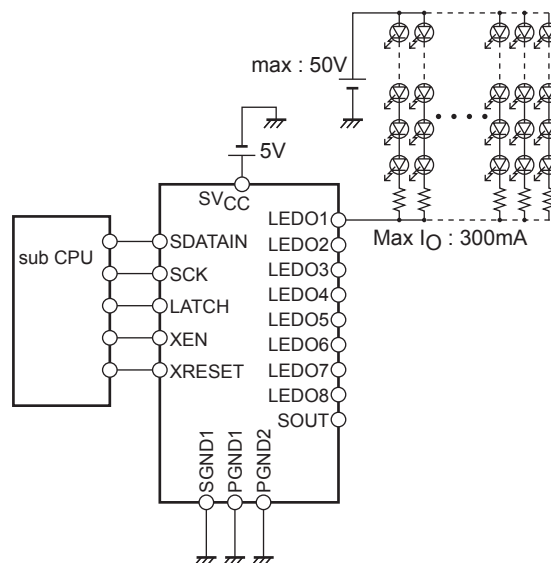
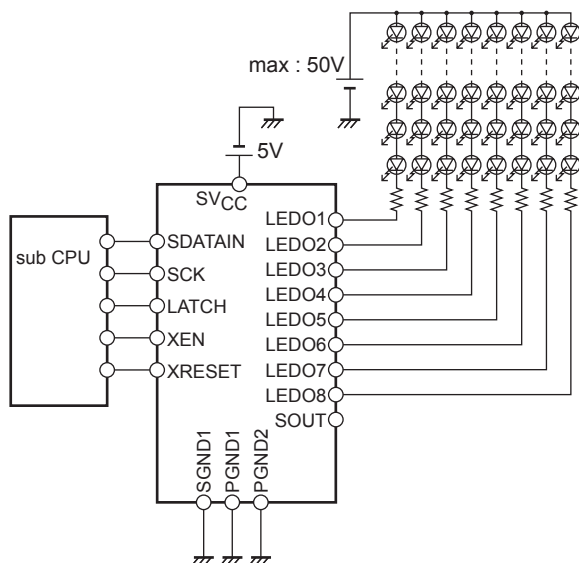
LEDO output timings

Parameter	symbol	Conditions	min	typ	max	unit
LEDO delay time 1	tdled1	The time from an XEN rising edge to LEDO rising edge CL = 30pF, I _O = 100mA, V _O = 30V		100		ns
LEDO delay time 2	tdled2	The time from an XEN falling edge to LEDO falling edge CL = 30pF, I _O = 100mA, V _O = 30V		100		ns
LEDO rise time	trled	LEDO rise time CL = 30pF, I _O = 100mA, V _O = 30V		200		ns
LEDO fall time	tfled	LEDO fall time CL = 30pF, I _O = 100mA, V _O = 30V		200		ns
LEDO delay time 3	tdled3	The time from a LATCH rising edge to LEDO falling edge CL = 30pF, I _O = 100mA, V _O = 30V		200		ns

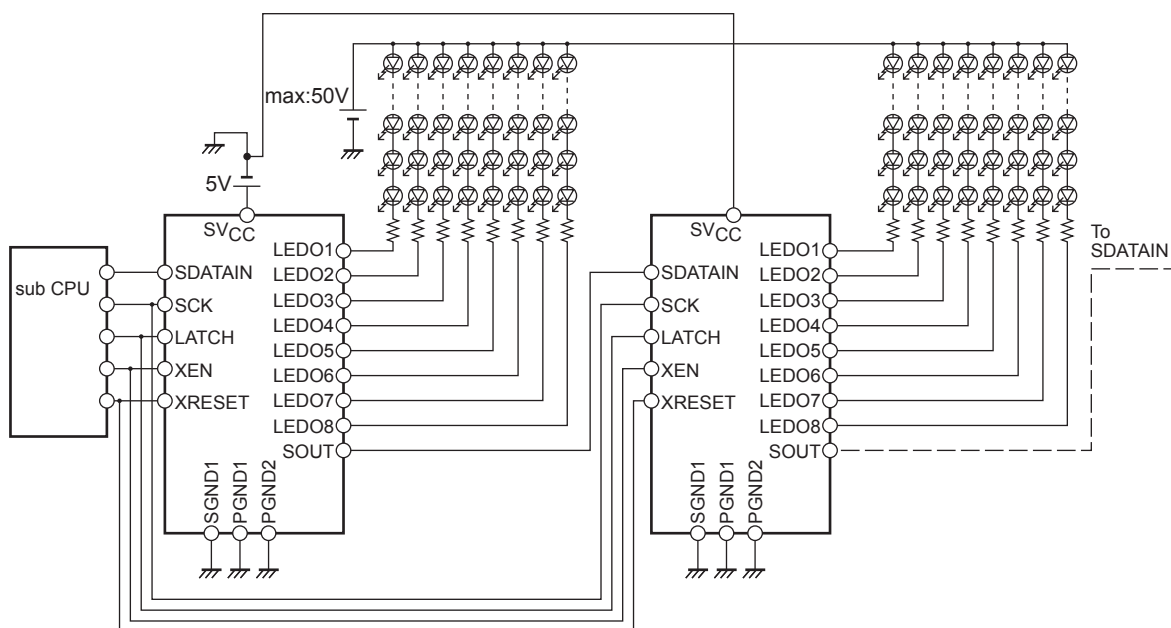


Application Circuit Example

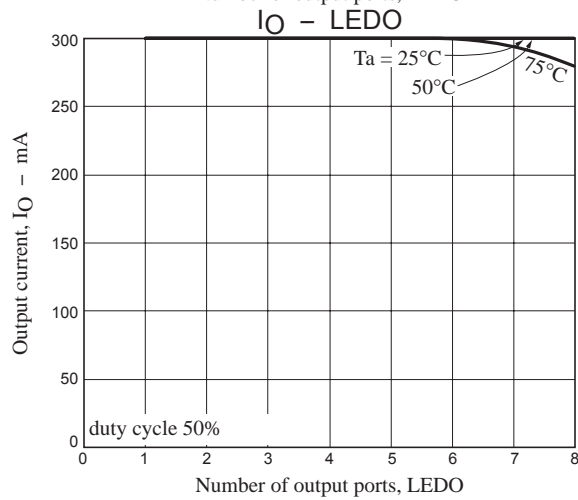
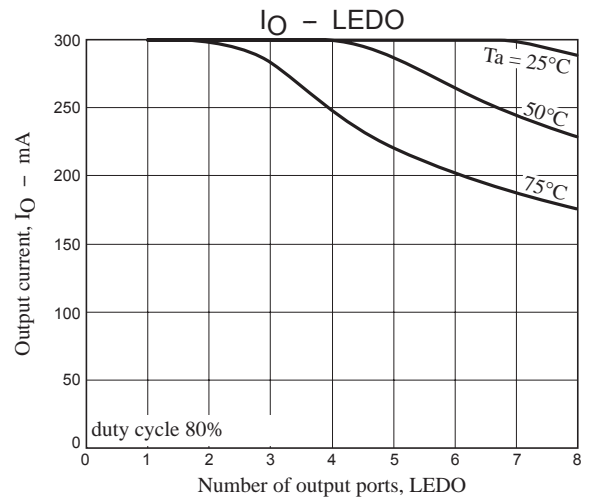
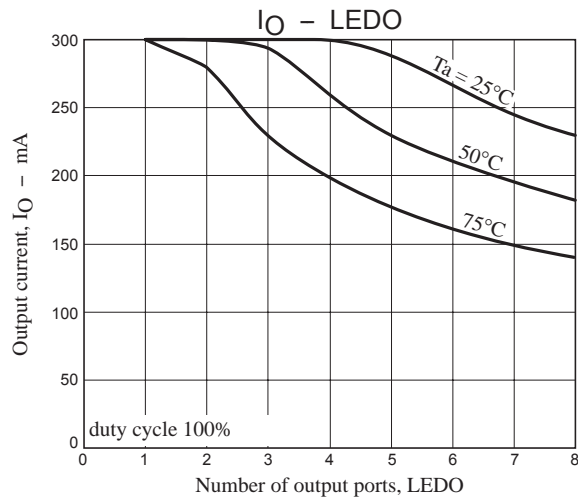
- When parallel output is used



- When serial output is used (SOUT cascade connection)



Allowable output current characteristics



ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
LV5212VH-MPB-H	HSSOP16 (275mil) (Pb-Free / Halogen Free)	48 / Fan-Fold
LV5212VH-TLM-H	HSSOP16 (275mil) (Pb-Free / Halogen Free)	1000 / Tape & Reel

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