TOSHIBA PHOTOCOUPLER GaAℓAs LED & PHOTO-IC

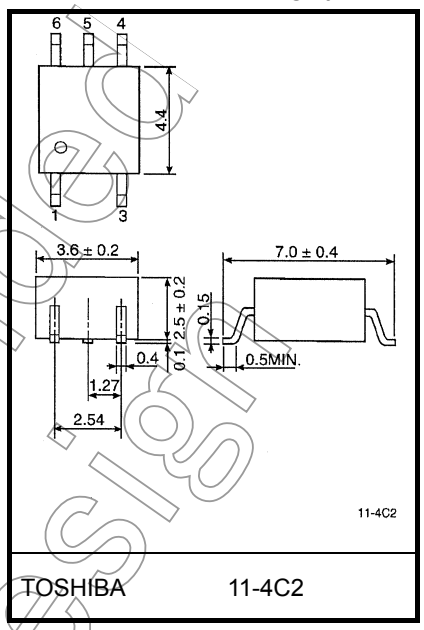
TLP116

PDP(Plasma Display Panel)
High Speed Interface
FA(Factory Automation)

The Toshiba TLP116 consists of a GaAℓAs light-emitting diode and an integrated high-gain, high-speed photodetector.

- Inverter logic (totempole output)
- Package type : MFSOP6
- Guaranteed performance over temperature : -40~100°C
- Power supply voltage : 4.5~5.5V
- Input thresholds current : I_{FHL}=5mA(Max.)
- Propagation delay time (tpHL/tpLH) : 60ns(Max.)
- Switching speed : 20MBd(TYP.)
- Common mode transient immunity : 10kV/us
- Isolation voltage : 3750Vrms
- UL Recognized : UL1577,File No.E67349

Unit in mm

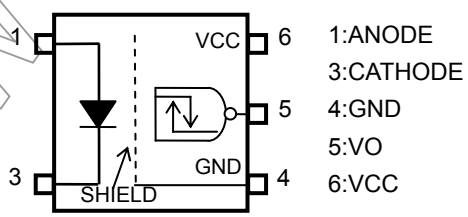


Weight: 0.09 g (typ.)

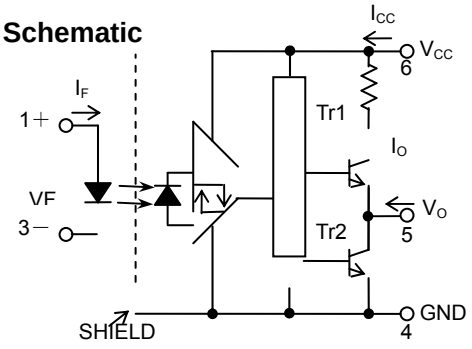
Truth Table

Input	LED	Tr1	Tr2	Output
H	ON	OFF	ON	L
L	OFF	ON	OFF	H

Pin Configuration (Top View)



Schematic



0.1uF bypass capacitor must be connected between pins 6 and 4

Absolute Maximum Ratings (Ta=25°C)

Characteristic		Symbol	Rating	Unit
LED	Forward current	I_F	20	mA
	Forward current derating (Ta≥85°C)	ΔIF/ΔTa	-0.5	mA/°C
	Peak transient forward current (Note1)	I_{FPT}	1	A
	Reverse voltage	V_R	5	V
DETECTOR	Output current	I_O	10	mA
	Output voltage	V_O	6	V
	Supply voltage	V_{CC}	6	V
	Output power dissipation	P_O	40	mW
Operating temperature range		Topr	-40~100	°C
Storage temperature range		Tstg	-55~125	°C
Lead solder temperature(10s)		Tsol	260	°C
Isolation voltage (AC,1min.,R.H.≤60%,Ta=25°C) (Note2)		BVs	3750	Vrms

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Recommended Operating Conditions

Characteristic	Symbol	Min	Typ.	Max	Unit
Input current , ON	$I_{F(ON)}$	8	—	18	mA
Input voltage , OFF	$V_{F(OFF)}$	0	—	0.8	V
Supply voltage (Note3)	V_{CC}	4.5	5.0	5.5	V
Operating temperature	Topr	-40	—	100	°C

Note: Recommended operating conditions are given as a design guideline to obtain expected performance of the device. Additionally, each item is an independent guideline respectively. In developing designs using this product, please confirm specified characteristics shown in this document.

Correlation between Input current , switching speed and drive circuit (reference information).

Input current (IF)	test Circuit	Typical switching speed
12mA	1 (Page 4)	21 – 23 MBd
8mA	1 (Page 4)	18 – 20 MBd
8mA	2 (Page 4,With Speed up capacitor)	23 – 27 MBd

Note1 : Pulse width PW≤1us,300pps.

Note2 : This device is regarded as a two terminal device : pins 1 and 3 are shorted together, as are pins 4,5 and 6.

Note3 : The detector of this product requires a power supply voltage (VCC) of 4.5 V or higher for stable operation. If the VCC is lower than this value, an ICC may increase, or an output may be unstable.
Be sure to use the product after checking the supply current, and the operation of a power-on/-off.

Electrical Characteristics

(Unless otherwise specified, Ta=-40 to 100°C,VCC=4.5~5.5V)

Characteristic	Symbol	Test Circuit	Conditions	Min.	Typ.	Max.	Unit
Input forward voltage	V_F	—	I_F=10mA ,Ta=25°C	—	1.3	1.5	V
Temperature coefficient of forward voltage	$\Delta V_F/\Delta Ta$	—	I_F=10mA	—	-2.0	—	mV/°C
Input reverse current	I_R	—	V_R=5V,Ta=25°C	—	—	10	μA
Input capacitance	C_T	—	V=0,f=1MHz,Ta=25°C	—	70	—	pF
Logic low output voltage	V_{OL}	1	I_{OL}=1.6mA, I_F=12mA,V_{CC}=5V	—	—	0.4	V
Logic high output voltage	V_{OH}	2	I_{OH}=-0.02mA, V_F=1.05V,V_{CC}=5V	4.0	—	—	V
Logic low supply current	I_{CCL}	3	I_F=12mA	—	—	5.0	mA
Logic high supply current	I_{CCH}	4	V_F=0V	—	—	5.0	mA
Input current logic low output	I_{FHL}	—	I_O=1.6mA,V_O<0.4V	—	—	5	mA
Input voltage logic high output	V_{FLH}	—	I_O=-0.02mA,V_O>4.0V	0.8	—	—	V

*All typical values are at Ta=25°C,V_{CC}=5V,I_F(ON)=12mA unless otherwise specified

Isolation Characteristics (Ta = 25°C)

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Capacitance input to output	C_S	V = 0,f = 1MHz (Note 2)	—	0.8	—	pF
Isolation resistance	R_S	R.H. ≤ 60%,V_S = 500V (Note 2)	1×10^{12}	10^{14}	—	Ω
Isolation voltage	BV_S	AC,1 minute	3750	—	—	V_{rms}
		AC,1 second,in oil	—	10000	—	Vdc
		DC,1 minute,in oil	—	10000	—	

Note 4:A ceramic capacitor(0.1 μF) should be connected from pin 6 to pin 4 to stabilize the operation of the high gain linear amplifier. Failure to provide the bypass may impair the switching property.
The total lead length between capacitor and coupler should not exceed 1 cm.

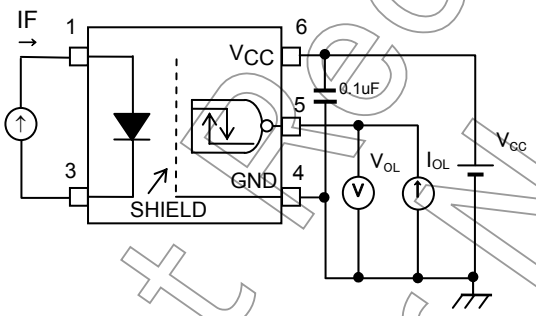
Switching Characteristics
(Unless otherwise specified, Ta=-40 to 100°C, V_{CC}=4.5~5.5V)

Characteristic	Symbol	Test Circuit	Conditions		Min.	Typ.	Max.	Unit
Propagation delay time to logic high output	tpHL	5	I_F=0→12mA	R_{IN}=100Ω C_L=15pF (Note 5)	—	—	60	ns
Propagation delay time to logic low output	tpLH		I_F=12→0mA		—	—	60	ns
Propagation delay time to logic high output	tpHL	6	V_{IN}=0→5V (I_F=0→8mA)	R_{IN}=470Ω C_{IN}=27pF C_L=15pF (Note 5)	—	—	60	ns
Propagation delay time to logic low output	tpLH		V_{IN}=5→0V (I_F=8→0mA)		—	—	60	ns
Switching time dispersion between ON and OFF	|tpHL-tpLH|	5	I_F=12mA , R_{IN}=100Ω , CL=15pF (Note 5)		—	—	30	ns
Output fall time(90-10%)	tf		I_F=0→12mA	R_{IN}=100Ω C_L=15pF (Note 5)	—	15	—	ns
Output rise time(10-90%)	tr		I_F=12→0mA		—	15	—	ns
Common mode transient immunity at high Level output	CM_H	7	V_{CM}=1000Vp-p, I_F=0mA, Vo(Min)=4V, Ta=25°C		10000	—	—	V/us
Common mode transient immunity at low level output	CM_L		V_{CM}=1000Vp-p, I_F=12mA, Vo(Max)=0.4V, Ta=25°C		-10000	—	—	V/us

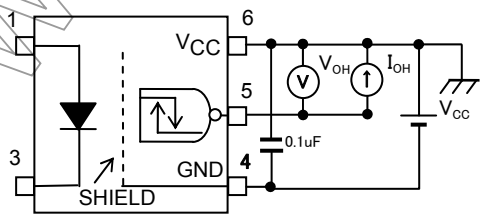
*All typical values are at Ta=25°C

Note 5 : C_L is approximately 15pF which includes probe and Jig/stray wiring capacitance.

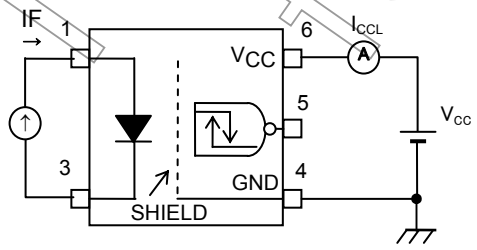
TEST CIRCUIT 1 : V_{OL}



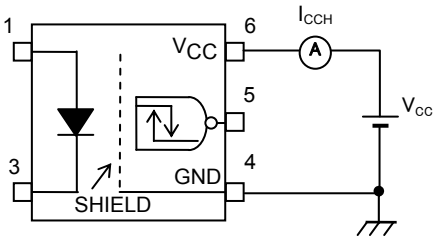
TEST CIRCUIT 2 : V_{OH}



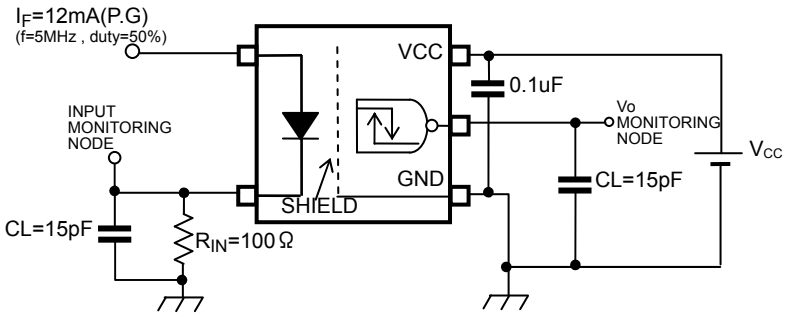
TEST CIRCUIT 3 : I_{CCL}

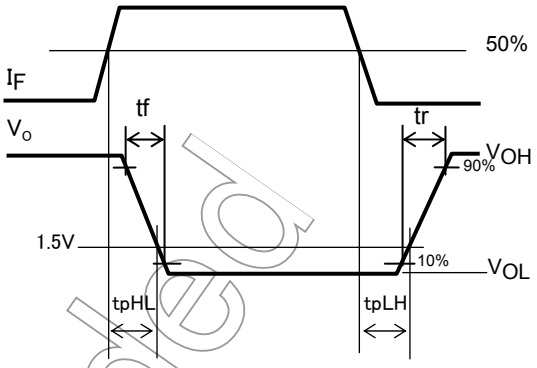


TEST CIRCUIT 4: I_{CCH}



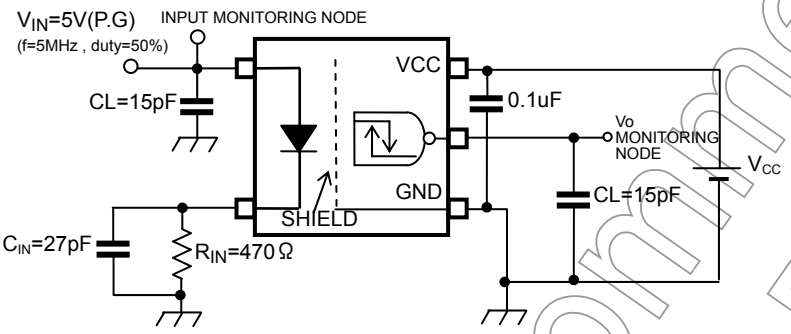
TEST CIRCUIT 5 : tpHL , tpLH

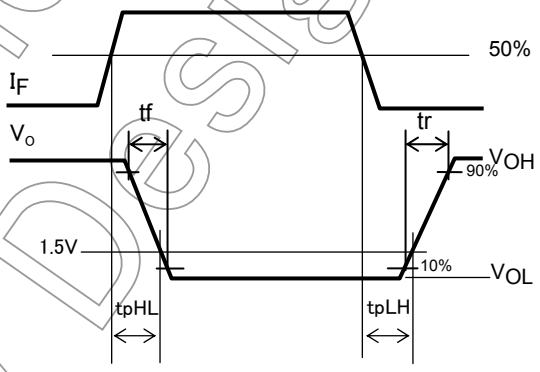




CL is capacitance of the probe and JIG.
(P.G) : Pulse Generator

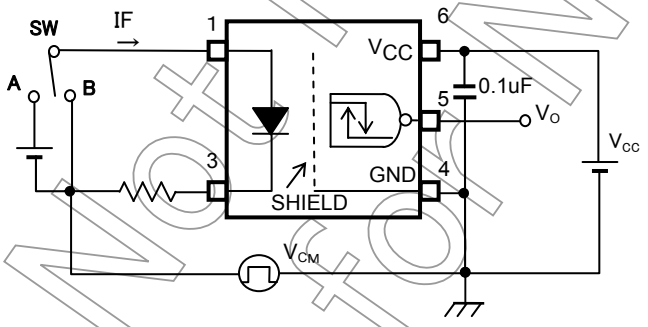
TEST CIRCUIT 6 : tpHL , tpLH

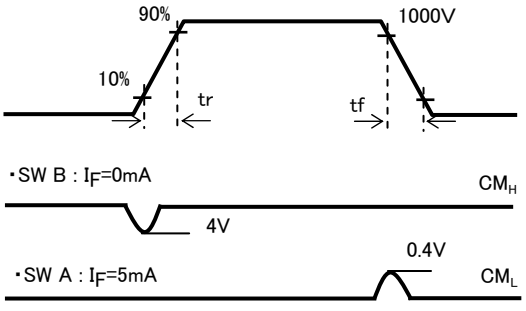




CL is capacitance of the probe and JIG.
(P.G) : Pulse Generator

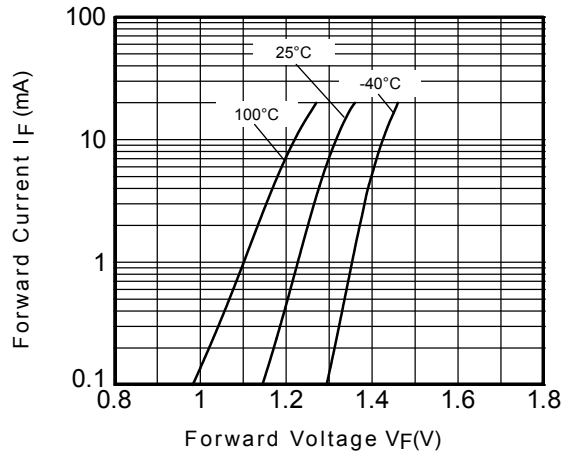
TEST CIRCUIT 7 : Common-Mode Transient Immunity Test Circuit



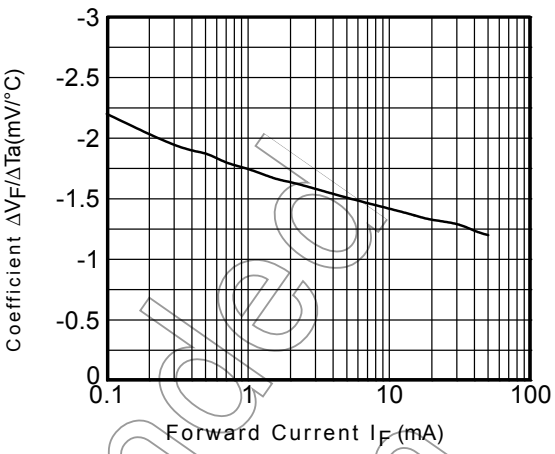


$$CM_H = \frac{800(V)}{t_r(\mu s)} \qquad CM_L = \frac{800(V)}{t_f(\mu s)}$$

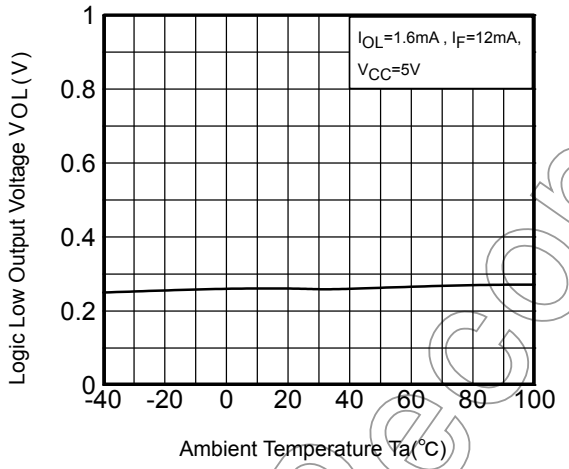
I_F-V_F



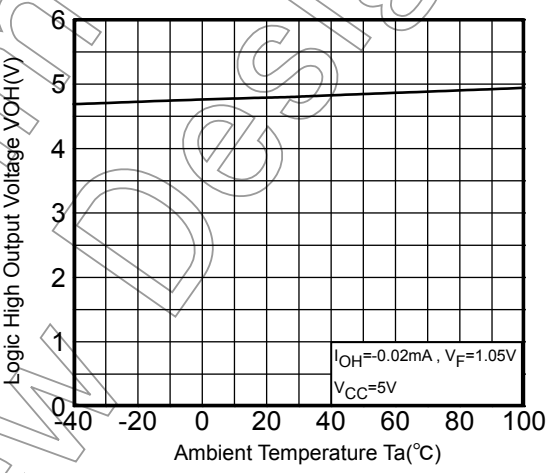
$\Delta V_F/\Delta Ta$-I_F



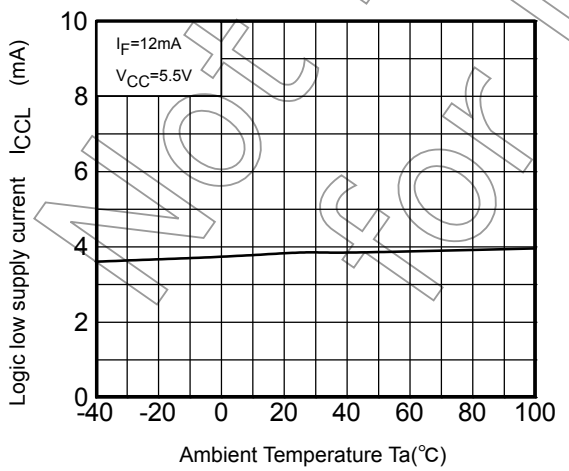
V_{OL}-Ta



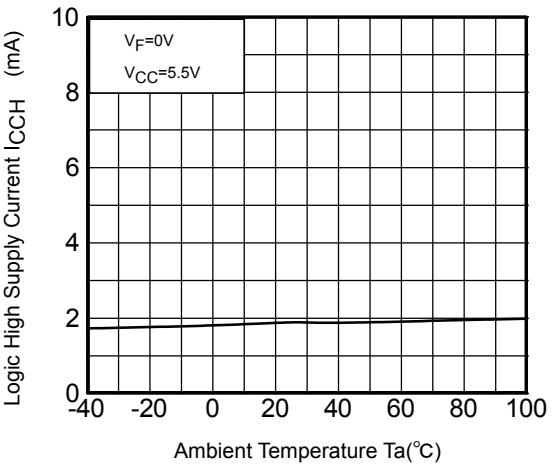
V_{OH}-Ta



I_{CCL}-Ta

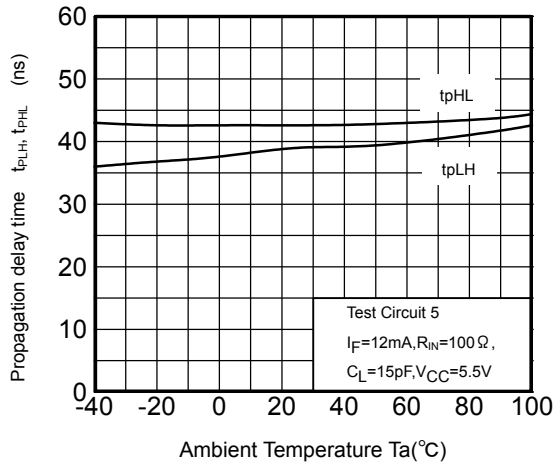


I_{CCH}-Ta

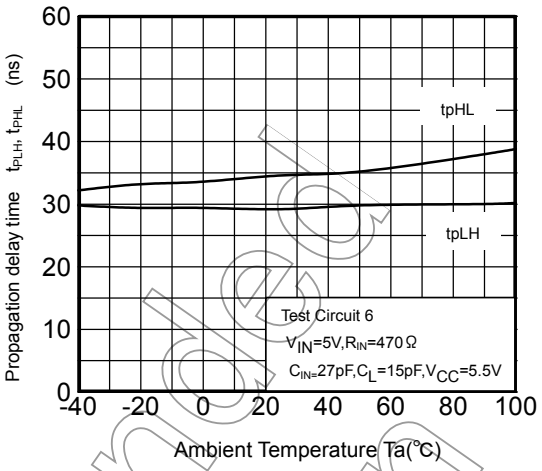


*: The above graphs show typical characteristics.

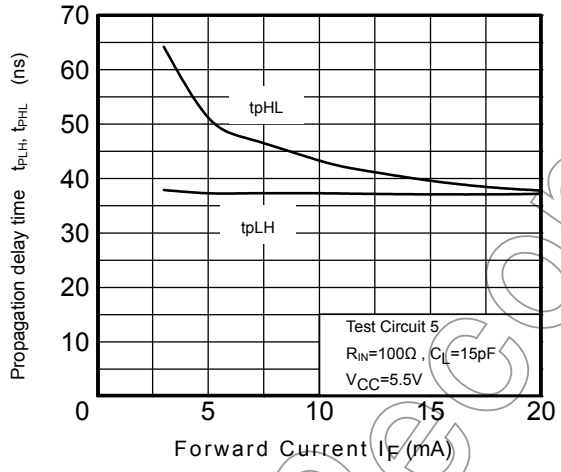
t_{pHL}, t_{pLH}-Ta



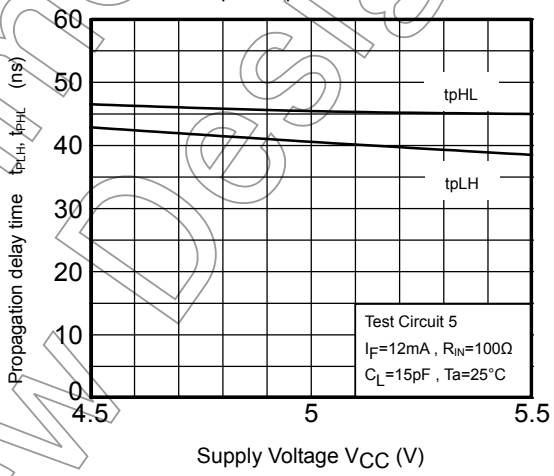
t_{pHL}, t_{pLH}-Ta



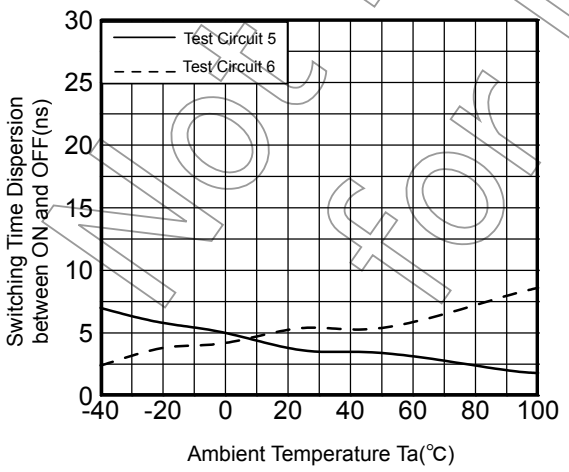
t_{pHL}, t_{pLH}-I_F



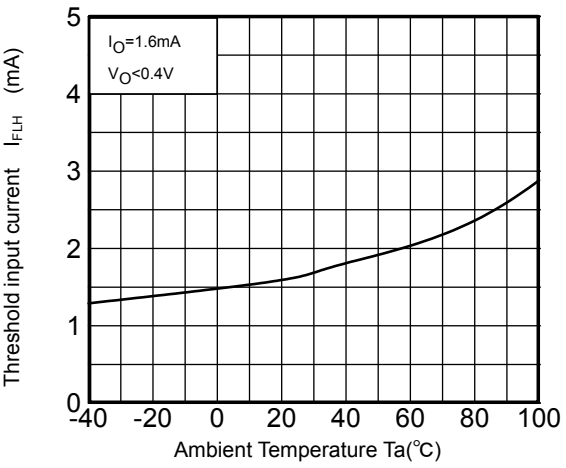
t_{pHL}, t_{pLH}-V_{CC}



|tpHL-tpLH|-Ta



I_{FLH}-Ta



*: The above graphs show typical characteristics.

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