

Double channel high-side driver with analog current sense for automotive applications

Datasheet - production data



Features

Max transient supply voltage	V_{CC}	41 V
Operating voltage range	V_{CC}	4.5 to 28V
Typ on-state resistance (per ch.)	R_{ON}	8 m Ω
Current limitation (typ)	I_{LIMH}	76 A
Off-state supply current	I_S	2 $\mu A^{(1)}$

1. Typical value with all loads connected.

- General:
 - Inrush current active management by power limitation
 - Very low standby current
 - 3.0V CMOS compatible input
 - Optimized electromagnetic emission
 - Very low electromagnetic susceptibility
 - Compliant with European directive 2002/95/EC
 - Proportional load current sense
 - High current sense precision for wide range current
 - Very low current sense leakage
- Diagnostic functions:
 - Off-state open-load detection
 - Current sense disable
 - Thermal shutdown indication
 - Output short to V_{CC} detection
 - Overload and short to ground (power limitation) indication

- Protection:
 - Undervoltage shutdown
 - Overvoltage clamp
 - Load current limitation
 - Self limiting of fast thermal transients
 - Protection against loss of ground and loss of V_{CC}
 - Thermal shut down
 - Reverse battery protection with self switch of the Power MOS

Applications

- All types of resistive, inductive and capacitive loads

Description

The VND5E008AY-E is a device made using STMicroelectronics® VIPower® MO-5 technology. It is intended for driving resistive or inductive loads with one side connected to ground. Active V_{CC} pin voltage clamp protects the device against low energy spikes.

This device integrates an analog current sense which delivers a current proportional to the load current when CS_DIS high leads the current sense pin in high impedance.

Fault conditions such as overload, overtemperature or open-load are reported via the current sense pin

Output current limitation protects the device in overload condition. In case of long overload duration, the device limits the dissipated power to safe level up to thermal shutdown intervention. Thermal shutdown with automatic restart allows the device to recover normal operation as soon as fault condition disappears.

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1 Block diagram and pin description

Figure 1. Block diagram

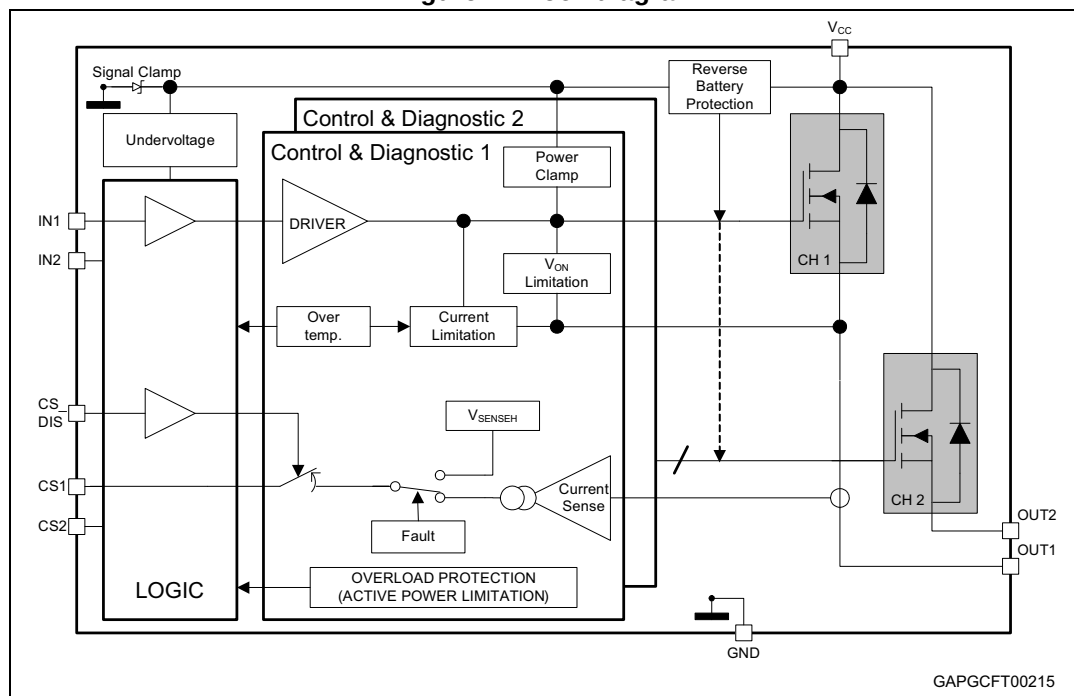


Table 1. Pin function

Name	Function
V _{CC}	Battery connection
OUT _{1,2}	Power output
GND	Ground connection
IN _{1,2}	Voltage controlled input pin with hysteresis, CMOS compatible. Controls output switch state
CS _{1,2}	Analog current sense pin, delivers a current proportional to the load current
CS_DIS	Active high CMOS compatible pin, to disable the current sense pin

Figure 2. Configuration diagram (top view)

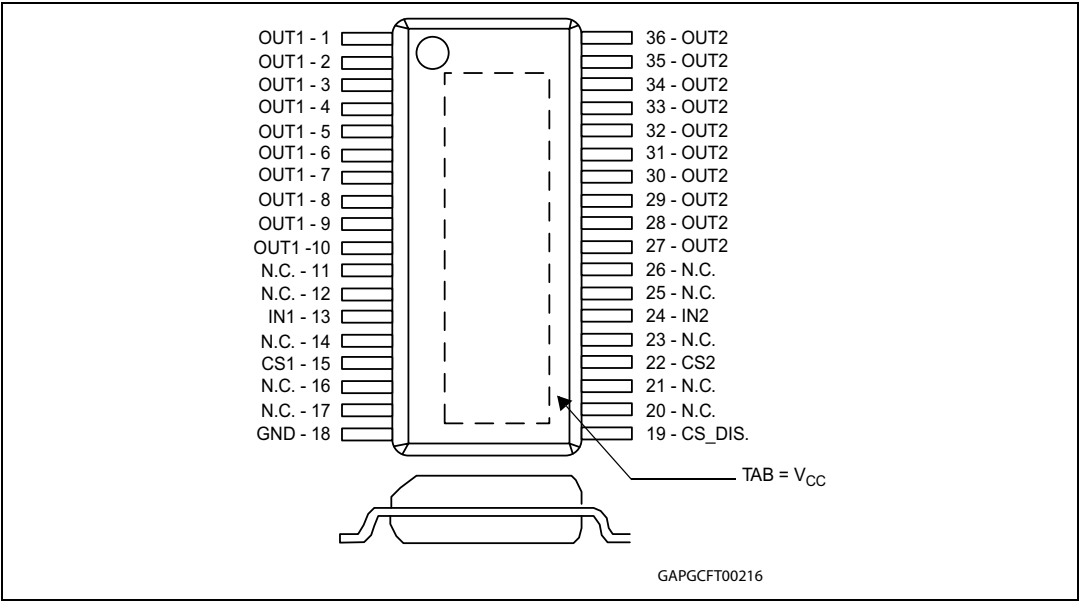
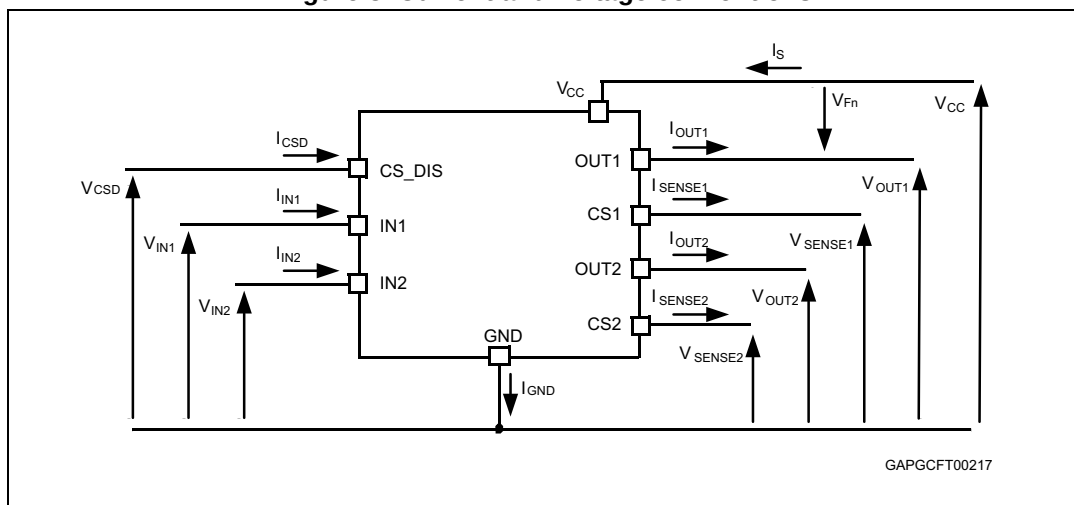


Table 2. Suggested connections for unused and not connected pins

Connection / pin	Current sense	N.C.	Output	Input	CS_DIS
Floating	Not allowed	X	X	X	X
To ground	Through 1 KΩ resistor	X	Not allowed	Through 10 KΩ resistor	Through 10 KΩ resistor

2 Electrical specifications

Figure 3. Current and voltage conventions



2.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	28	V
V_{CCPK}	Transient supply voltage ($T < 400$ ms, $R_{LOAD} > 1 \Omega$)	41	V
$-V_{CC}$	Reverse DC supply voltage	16	V
V_{CC_LSC}	Maximum supply voltage for full protection to short-circuit (acc. AEC-Q100-012)	18	V
$-I_{GND}$	DC reverse ground pin current	200	mA
I_{OUT}	DC output current	Internally limited	A
$-I_{OUT}$	Reverse DC output current	50	A
I_{IN}	DC input current	-1 to 10	mA
I_{CSD}	DC current sense disable input current	-1 to 10	mA
V_{CSENSE}	Current sense maximum voltage	$V_{CC} - 41$ $+V_{CC}$	V V
E_{MAX}	Maximum switching energy (single pulse) ($L = 0.85$ mH; $R_L = 0 \Omega$; $V_{bat} = 13.5$ V; $T_{jstart} = 150$ °C; $I_{OUT} = I_{limL}(Typ.)$)	260	mJ
V_{ESD}	Electrostatic Discharge (Human Body Model: $R = 1.5$ K Ω ; $C = 100$ pF) – V_{CC} , OUTPUT – INPUT, CS_DIS – CURRENT SENSE	5000 4000 2000	V

Table 3. Absolute maximum ratings (continued)

Symbol	Parameter	Value	Unit
V _{ESD}	Charge device model (CDM-AEC-Q100-011)	750	V
T _J	Junction operating temperature	-40 to 150	°C
T _{stg}	Storage temperature	-55 to 150	°C

2.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Max. value	Unit
R _{thj-case}	Thermal resistance junction-case (MAX) (with one channel ON)	0.85	°C/W
R _{thj-amb}	Thermal resistance junction-ambient (MAX)	See Figure 36 in the Thermal section	°C/W

2.3 Electrical characteristics

8 V < V_{CC} < 28 V; -40 °C < T_j < 150 °C, unless otherwise specified

Table 5. Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage		4.5	13	28	V
V_{USD}	Undervoltage shutdown			3.5	4.5	V
$V_{USDhyst}$	Undervoltage shutdown hysteresis			0.5		V
R_{ON}	ON-state resistance	$I_{OUT} = 6\text{ A}$; $T_j = 25\text{ °C}$		8		mΩ
		$I_{OUT} = 6\text{ A}$; $T_j = 150\text{ °C}$			15	mΩ
		$I_{OUT} = 6\text{ A}$; $V_{CC} = 5\text{ V}$; $T_j = 25\text{ °C}$			11	mΩ
$R_{ON REV}$	Reverse battery ON-state resistance	$V_{CC} = -13\text{ V}$; $I_{OUT} = -6\text{ A}$; $T_j = 25\text{ °C}$		8		mΩ
V_{clamp}	Clamp Voltage	$I_S = 20\text{ mA}$	41	46	52	V
I_S	Supply current	Off-state; $V_{CC} = 13\text{ V}$; $T_j = 25\text{ °C}$; $V_{IN} = V_{OUT} = V_{SENSE} = V_{CSD} = 0\text{ V}$		2 ⁽¹⁾	5 ⁽¹⁾	μA
		On-state; $V_{CC} = 13\text{ V}$; $V_{IN} = 5\text{ V}$; $I_{OUT} = 0\text{ A}$		3.5	6.5	mA
$I_{L(off)}$	Off-state output current ⁽²⁾	$V_{IN} = V_{OUT} = 0\text{ V}$; $V_{CC} = 13\text{ V}$; $T_j = 25\text{ °C}$	0	0.01	3	μA
		$V_{IN} = V_{OUT} = 0\text{ V}$; $V_{CC} = 13\text{ V}$; $T_j = 125\text{ °C}$			5	μA

1. PowerMOS leakage included.

2. For each channel.

Table 6. Switching ($V_{CC} = 13\text{ V}$; $T_j = 25\text{ °C}$)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$R_L = 2.2\text{ Ω}$ (see Figure 8)	—	30	—	μs
$t_{d(off)}$	Turn-off delay time	$R_L = 2.2\text{ Ω}$ (see Figure 8)	—	15	—	μs
$(dV_{OUT}/dt)_{on}$	Turn-on voltage slope	$R_L = 2.2\text{ Ω}$	—	See Figure 23	—	V/μs
$(dV_{OUT}/dt)_{off}$	Turn-off voltage slope	$R_L = 2.2\text{ Ω}$	—	See Figure 24	—	V/μs
W_{ON}	Switching energy losses during t_{won}	$R_L = 2.2\text{ Ω}$ (see Figure 8)	—	1.2	—	mJ
W_{OFF}	Switching energy losses during t_{woff}	$R_L = 2.2\text{ Ω}$ (see Figure 8)	—	0.43	—	mJ

Table 7. Current sense (8 V < V_{CC} < 18 V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
K ₀	I _{OUT} /I _{SENSE}	I _{OUT} = 0.25 A; V _{SENSE} = 0.5 V T _j = -40 °C...150 °C	3658	6000	8926	
K ₁	I _{OUT} /I _{SENSE}	I _{OUT} = 6 A; V _{SENSE} = 0.5 V T _j = -40 °C...150 °C T _j = 25 °C...150 °C	3910 4336	6000 6000	8928 8044	
dK ₁ /K ₁ ⁽¹⁾	Current sense ratio drift	I _{OUT} = 6 A; V _{SENSE} = 0.5 V V _{CSD} = 0 V; T _j = -40 °C to 150 °C	-12		12	%
K ₂	I _{OUT} /I _{SENSE}	I _{OUT} = 10 A; V _{SENSE} = 4 V T _j = -40 °C...150 °C T _j = 25 °C...150 °C	4948 5298	6000 6000	7372 6762	
dK ₂ /K ₂ ⁽¹⁾	Current sense ratio drift	I _{OUT} = 10 A; V _{SENSE} = 4 V; V _{CSD} = 0 V; T _j = -40 °C to 150 °C	-7		7	%
K ₃	I _{OUT} /I _{SENSE}	I _{OUT} = 25 A; V _{SENSE} = 4 V T _j = -40 °C...150 °C T _j = 25 °C...150 °C	5455 5535	6000 6000	6762 6282	
dK ₃ /K ₃ ⁽¹⁾	Current sense ratio drift	I _{OUT} = 25 A; V _{SENSE} = 4 V; V _{CSD} = 0V; T _j = -40 °C to 150 °C	-5		5	%
I _{SENSE0}	Analog sense leakage current	I _{OUT} = 0 A; V _{SENSE} = 0 V; V _{CSD} = 5 V; V _{IN} = 0 V; T _j = -40 °C...150 °C	0		1	μA
		V _{CSD} = 0 V; V _{IN} = 5 V; T _j = -40 °C...150 °C	0		2	μA
		I _{OUT} = 6 A; V _{SENSE} = 0 V; V _{CSD} = V _{IN} = 5 V;	0		1	μA
V _{SENSE}	Max analog sense output voltage	I _{OUT} = 15 A; V _{CSD} = 0 V	5			V
V _{SENSEH}	Analog sense output voltage in overtemperature condition ⁽²⁾	V _{CC} = 13 V; R _{SENSE} = 10 KΩ		8		V
I _{SENSEH}	Analog sense output current in overtemperature condition ⁽²⁾	V _{CC} = 13 V; V _{SENSE} = 5 V		9		mA
t _{DSSENSE1H}	Delay Response time from falling edge of CS_DIS pin	V _{SENSE} < 4 V, 1.5 A < I _{OUT} < 25 A I _{SENSE} = 90 % of I _{SENSE} max (see Figure 4)		50	100	μs

Table 7. Current sense (8 V < V_{CC} < 18 V) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t _{DSENSE1L}	Delay Response time from rising edge of CS_DIS pin	V _{SENSE} < 4 V, 1.5 A < I _{OUT} < 25 A I _{SENSE} = 10 % of I _{SENSE max} (see Figure 4)		5	20	μs
t _{DSENSE2H}	Delay Response time from rising edge of INPUT pin	V _{SENSE} < 4 V, 1.5 A < I _{OUT} < 25 A I _{SENSE} = 90 % of I _{SENSE max} (see Figure 4)		70	300	μs
Δt _{DSENSE2H}	Delay response time between rising edge of output current and rising edge of current sense	V _{SENSE} < 4 V, I _{SENSE} = 90 % of I _{SENSEMAX} , I _{OUT} = 90 % of I _{OUTMAX} I _{OUTMAX} = 5 A (see Figure 11)			300	μs
t _{DSENSE2L}	Delay Response time from falling edge of INPUT pin	V _{SENSE} < 4 V, 1.5 A < I _{OUT} < 25 A I _{SENSE} = 10 % of I _{SENSE max} (see Figure 4)		100	250	μs

1. Parameter guaranteed by design; it is not tested.
2. Fault condition includes: power limitation, overtemperature and open load OFF-state detection.

Table 8. Open-load detection (8 V < V_{CC} < 18 V)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V _{OL}	Open-load off-state voltage detection threshold	V _{IN} = 0 V	2	—	4	V
t _{DSTKON}	Output short circuit to V _{CC} detection delay at turn-off	See Figure 5	180	—	1200	μs
I _{L(off2)r}	Off-state output current at V _{OUT} = 4 V	V _{IN} = 0V; V _{SENSE} = 0 V; V _{OUT} rising from 0 V to 4 V	-120	—	90	μA
I _{L(off2)f}	Off-state output current at V _{OUT} = 2 V	V _{IN} = 0V; V _{SENSE} = V _{SENSEH} ; V _{OUT} falling from V _{CC} to 2 V	-50	—	90	μA

Table 9. Protections ⁽¹⁾

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I _{limH}	DC short circuit current	V _{CC} = 13 V	53	76	106	A
		5 V < V _{CC} < 18 V			106	A
I _{limL}	Short circuit current during thermal cycling	V _{CC} = 13 V; T _R < T _j < T _{TSD}		21		A
T _{TSD}	Shutdown temperature		150	175	200	°C
T _R	Reset temperature		T _{RS} +1	T _{RS} +5		°C
T _{RS}	Thermal reset of STATUS		135			°C

Table 9. Protections ⁽¹⁾ (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
T_{HYST}	Thermal hysteresis ($T_{TSD} - T_R$)			7		°C
V_{DEMAG}	Turn-off output voltage clamp	$I_{OUT} = 2\text{ A}$; $V_{IN} = 0$; $L = 6\text{ mH}$	$V_{CC} - 29$	$V_{CC} - 32$	$V_{CC} - 36$	V
V_{ON}	Output voltage drop limitation	$I_{OUT} = 0.4\text{ A}$; $T_j = -40\text{ °C} \dots 150\text{ °C}$ (see Figure 10)		25		mV

1. To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles.

Table 10. Logic input

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input low level voltage				0.9	V
I_{IL}	Low level input current	$V_{IN} = 0.9\text{ V}$	1			μA
V_{IH}	Input high level voltage		2.1			V
I_{IH}	High level input current	$V_{IN} = 2.1\text{ V}$			10	μA
$V_{I(hyst)}$	Input hysteresis voltage		0.25			V
V_{ICL}	Input clamp voltage	$I_{IN} = 1\text{ mA}$	5.5		7	V
		$I_{IN} = -1\text{ mA}$		-0.7		V
V_{CSDL}	CS_DIS low level voltage				0.9	V
I_{CSDL}	Low level CS_DIS current	$V_{CSD} = 0.9\text{ V}$	1			μA
V_{CSDH}	CS_DIS high level voltage		2.1			V
I_{CSDH}	High level CS_DIS current	$V_{CSD} = 2.1\text{ V}$			10	μA
$V_{CSD(hyst)}$	CS_DIS hysteresis voltage		0.25			V
V_{CSCL}	CS_DIS clamp voltage	$I_{CSD} = 1\text{ mA}$	5.5		7	V
		$I_{CSD} = -1\text{ mA}$		-0.7		V

Figure 4. Current sense delay characteristics

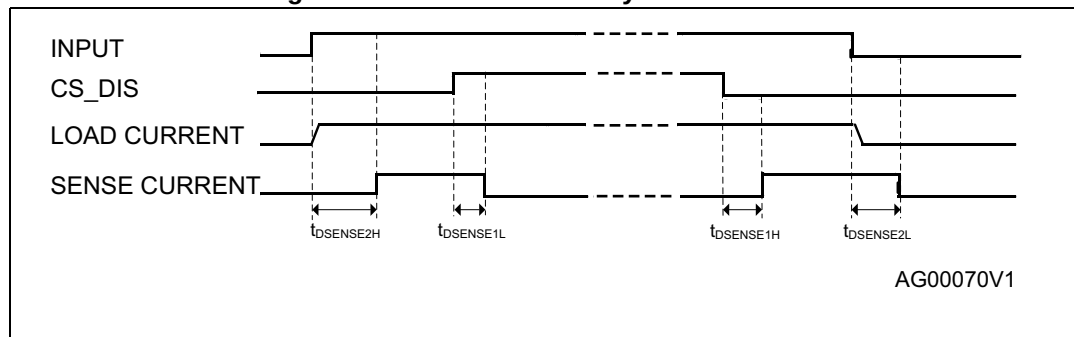


Figure 5. Open-load off-state delay timing

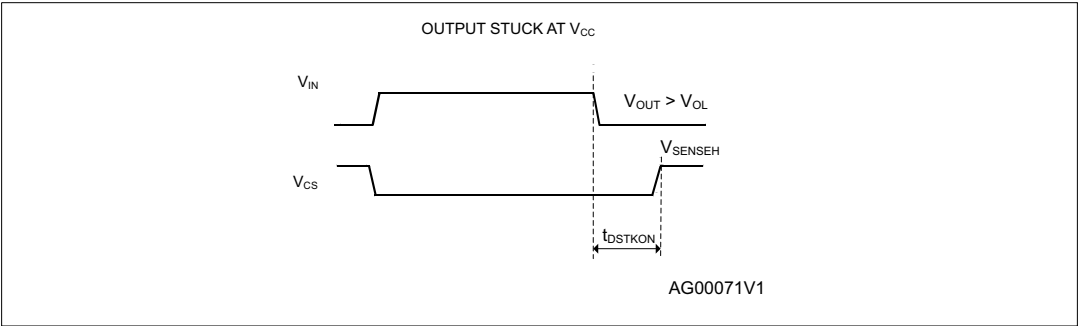


Figure 6. I_{OUT}/I_{SENSE} vs I_{OUT}

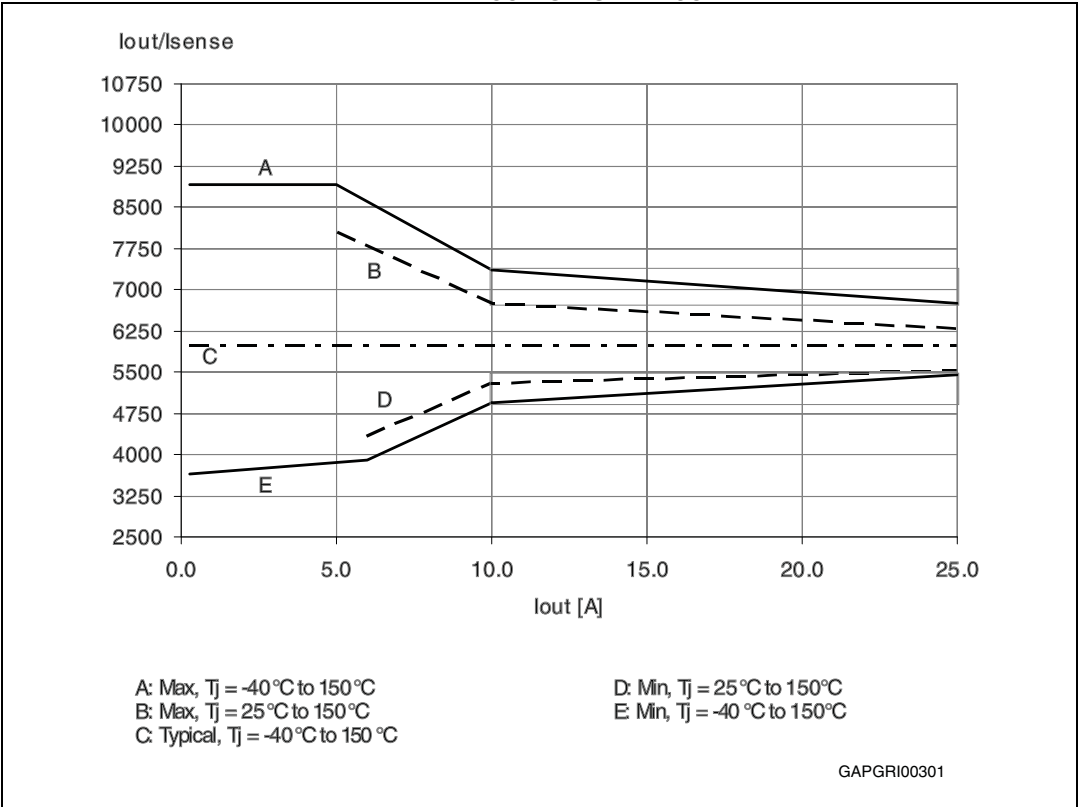


Figure 7. Maximum current sense ratio drift vs load current

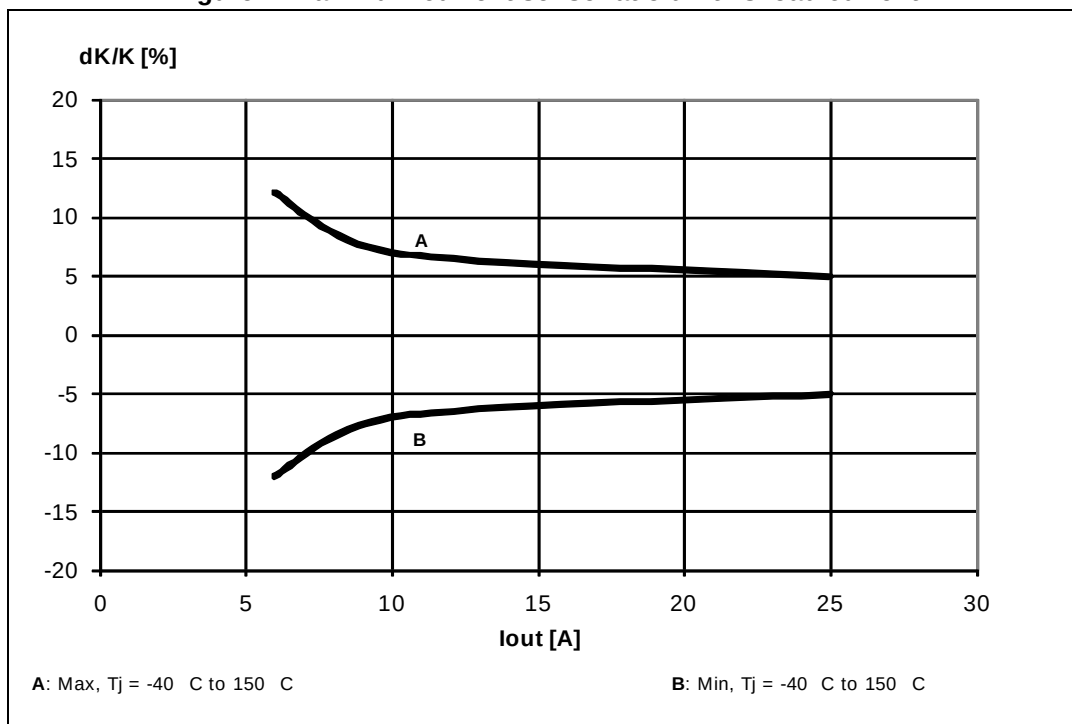
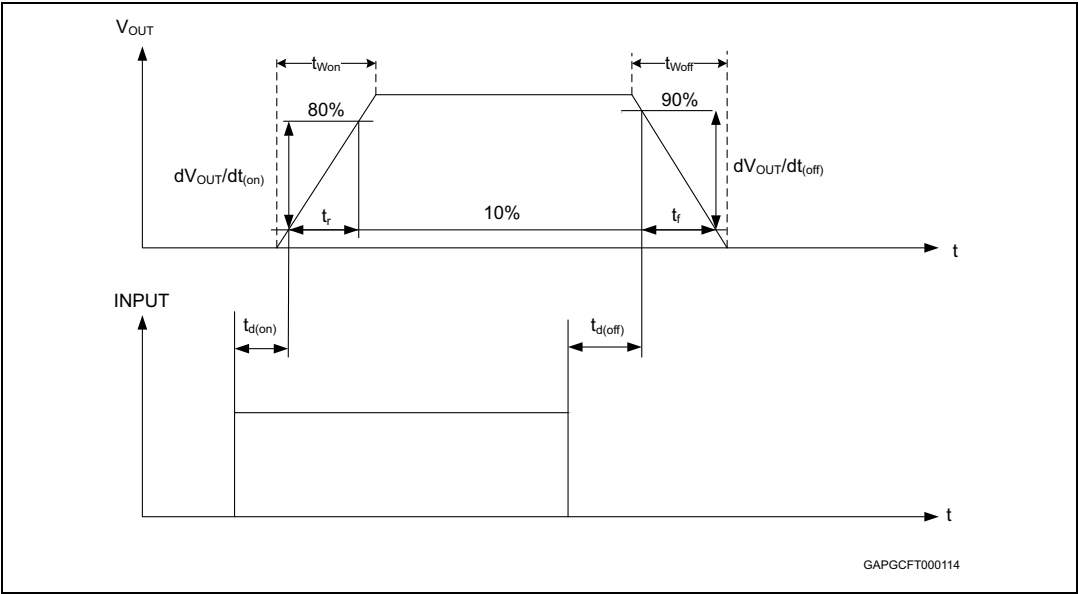


Table 11. Truth table

Conditions	Input	Output	Sense ($V_{CSD} = 0\text{ V}$) ⁽¹⁾
Normal operation	L	L	0
	H	H	Nominal
Overtemperature	L	L	0
	H	L	V_{SENSEH}
Undervoltage	L	L	0
	H	L	0
Overload	H	X	Nominal
	H	(no power limitation)	V_{SENSEH}
		Cycling (power limitation)	
Short circuit to GND (Power limitation)	L	L	0
	H	L	V_{SENSEH}
Open-load off-state (with external pull up)	L	H	V_{SENSEH}
Short circuit to V_{CC} (external pull up disconnected)	L	H	V_{SENSEH}
	H	H	< Nominal
Negative output voltage clamp	L	L	0

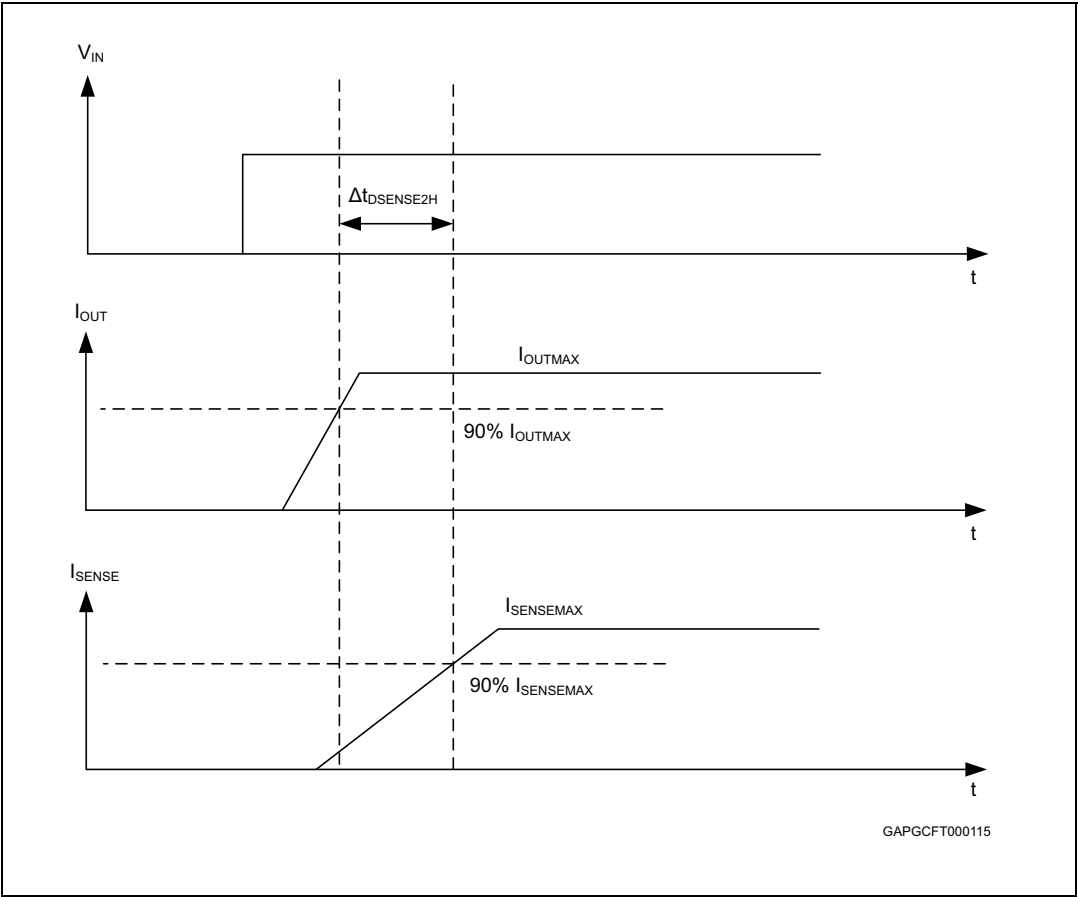
1. If the V_{CSD} is high, the SENSE output is at a high impedance, its potential depends on leakage currents and external circuit.

Figure 8. Switching characteristics



GAPGCFT000114

Figure 9. Delay response time between rising edge of output current and rising edge of current sense (CS enabled)



GAPGCFT000115

Figure 10. Output voltage drop limitation

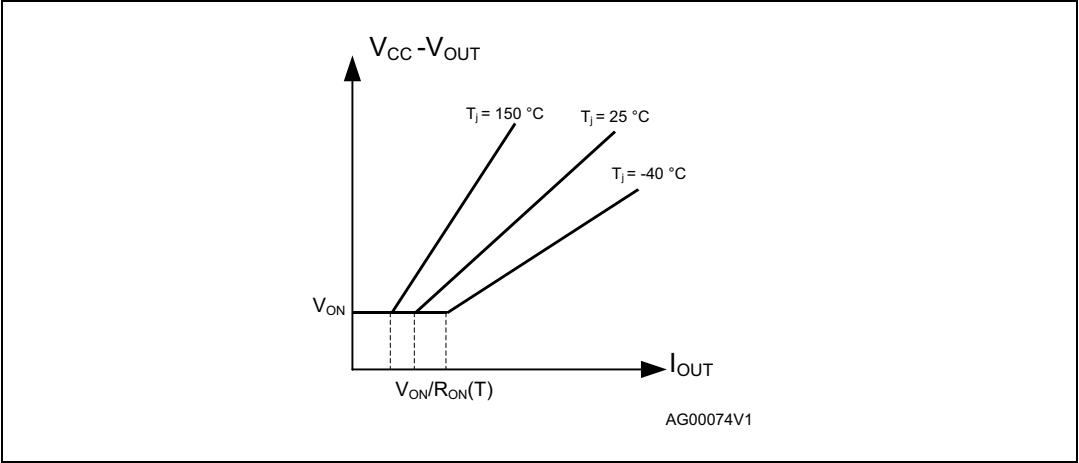


Table 12. Electrical transient requirements (part 1)

ISO 7637-2: 2004(E) Test pulse	Test levels ⁽¹⁾		Number of pulses or test times	Burst cycle/pulse repetition time		Delays and impedance
	III	IV				
1	-75 V	-100 V	5000 pulses	0.5 s	5 s	2 ms, 10 Ω
2a	+37 V	+50 V	5000 pulses	0.2 s	5 s	50 μ s, 2 Ω
3a	-100 V	-150 V	1h	90 ms	100 ms	0.1 μ s, 50 Ω
3b	+75 V	+100 V	1h	90 ms	100 ms	0.1 μ s, 50 Ω
4	-6 V	-7 V	1 pulse			100 ms, 0.01 Ω
5b ⁽²⁾	+65 V	+87 V	1 pulse			400 ms, 2 Ω

1. The above test levels must be considered referred to $V_{CC} = 13.5$ V except for pulse 5b.
2. Valid in case of external load dump clamp: 40V maximum referred to ground. The protection strategy allows PowerMOS to be cyclically switched on during load dump, so distributing the load dump energy along the time and to transfer a part of it to the load.

Table 13. Electrical transient requirements (part 2)

ISO 7637-2: 2004(E) Test pulse	Test level results ⁽¹⁾	
	III	IV
1	C	C
2a	C	C
3a	C	C
3b	C	C
4	C	C
5b ⁽²⁾⁽³⁾	C	C

1. The above test levels must be considered referred to $V_{CC} = 13.5$ V except for pulse 5b.
2. Valid in case of external load dump clamp: 40V maximum referred to ground. The protection strategy allows PowerMOS to be cyclically switched on during load dump, so distributing the load dump energy along the time and to transfer a part of it to the load.
3. Suppressed load dump (pulse 5b) is withstood with a minimum load connected as specified in [Table 3: Absolute maximum ratings](#).

Table 14. Electrical transient requirements (part 3)

Class	Contents
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device are not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the

2.4 Waveforms

Figure 11. Normal operation

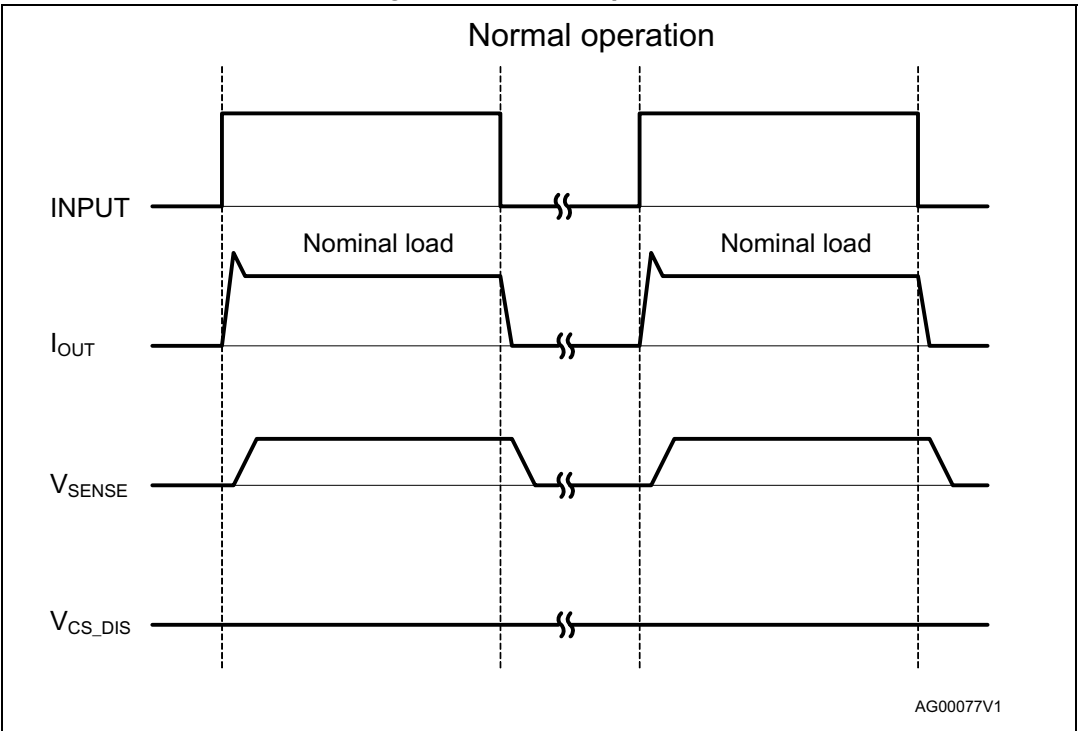


Figure 12. Overload or short to GND

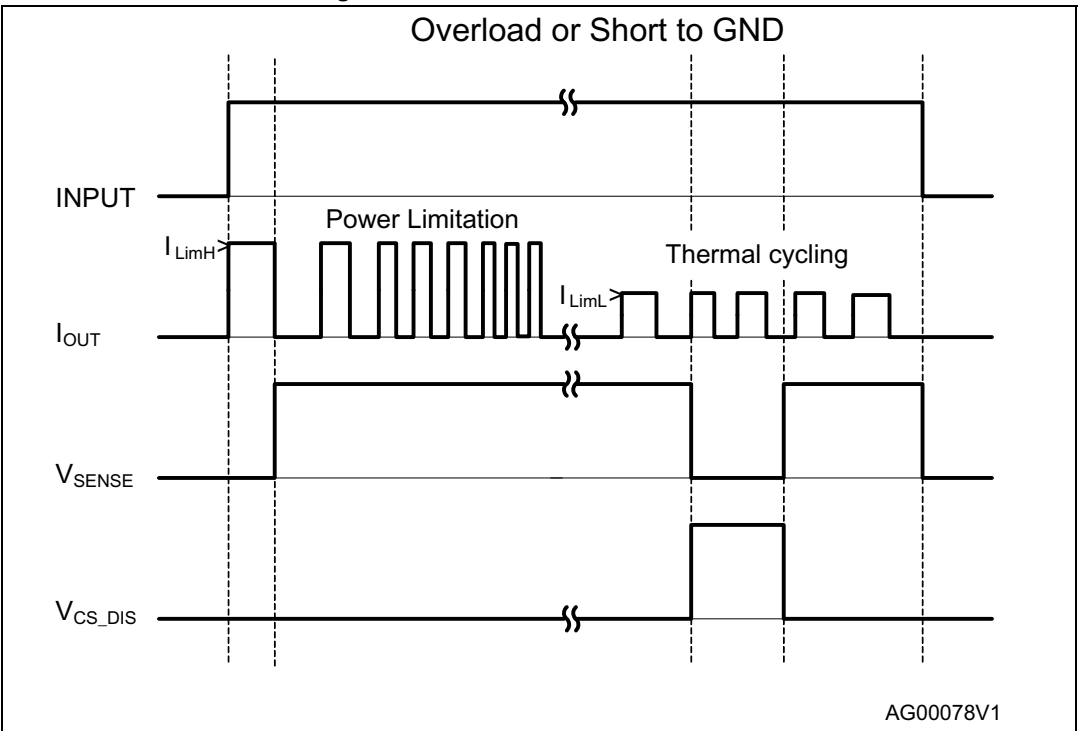


Figure 13. Intermittent overload

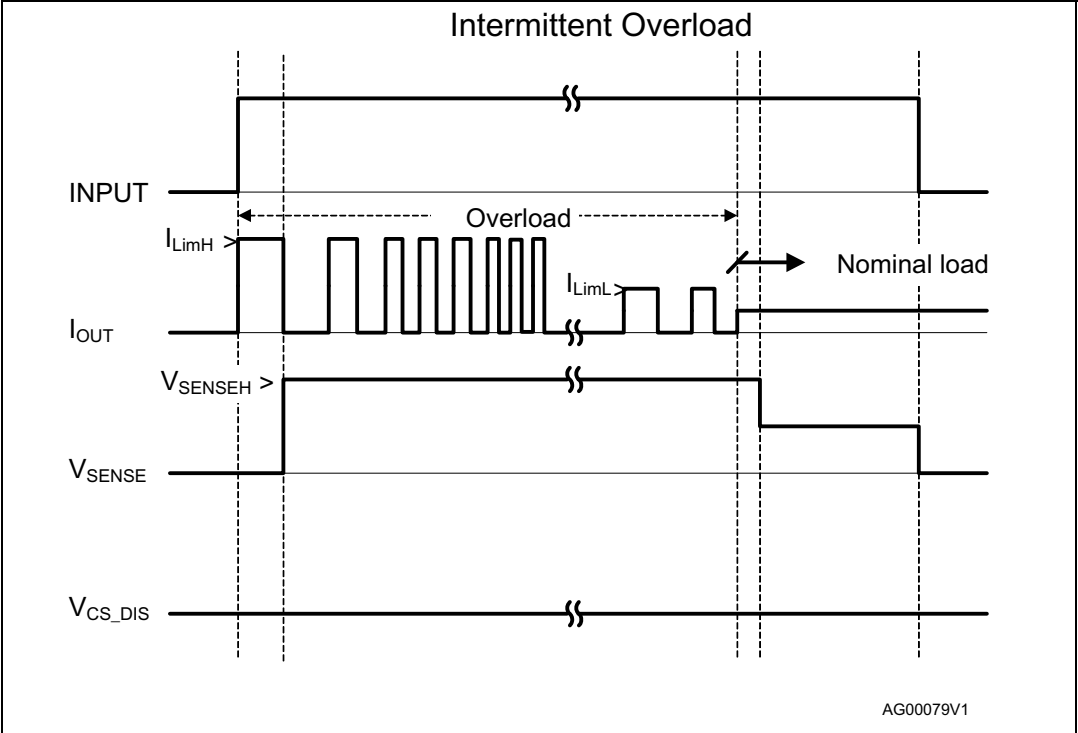


Figure 14. Off-state open-load with external circuitry

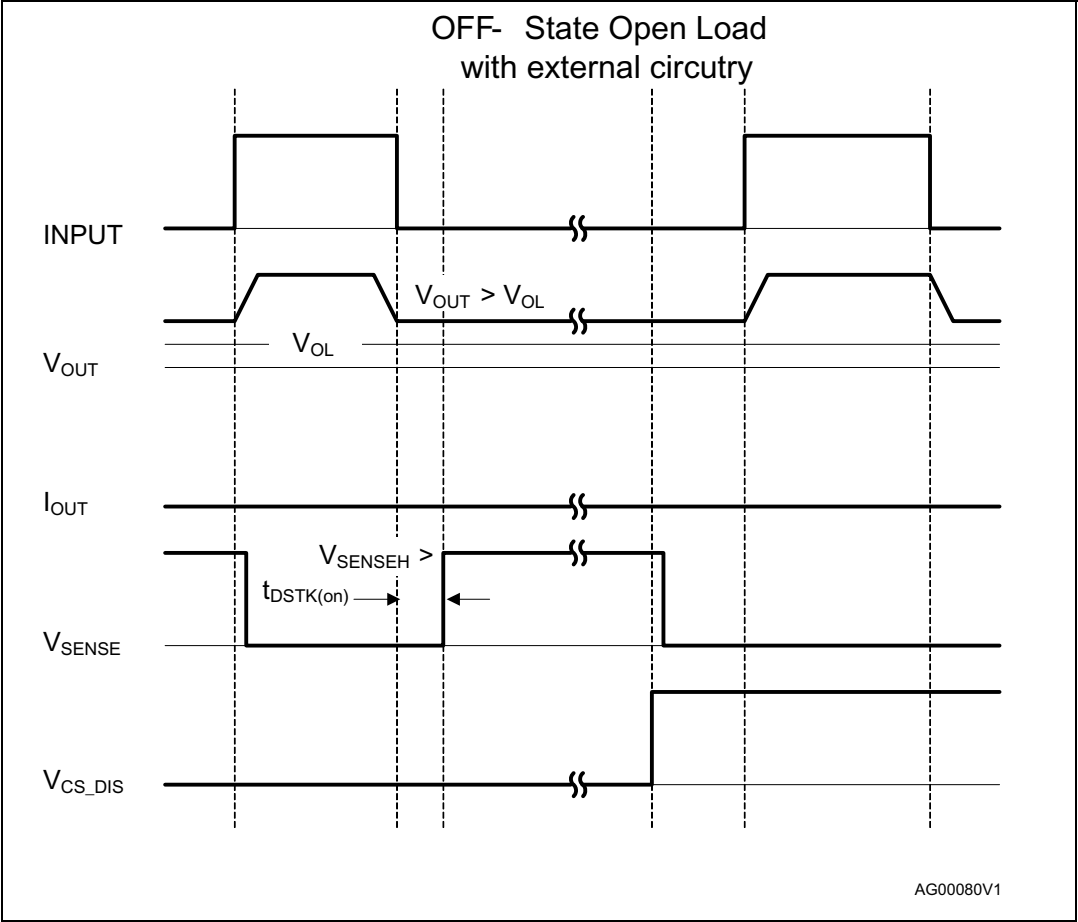


Figure 15. Short to V_{CC}

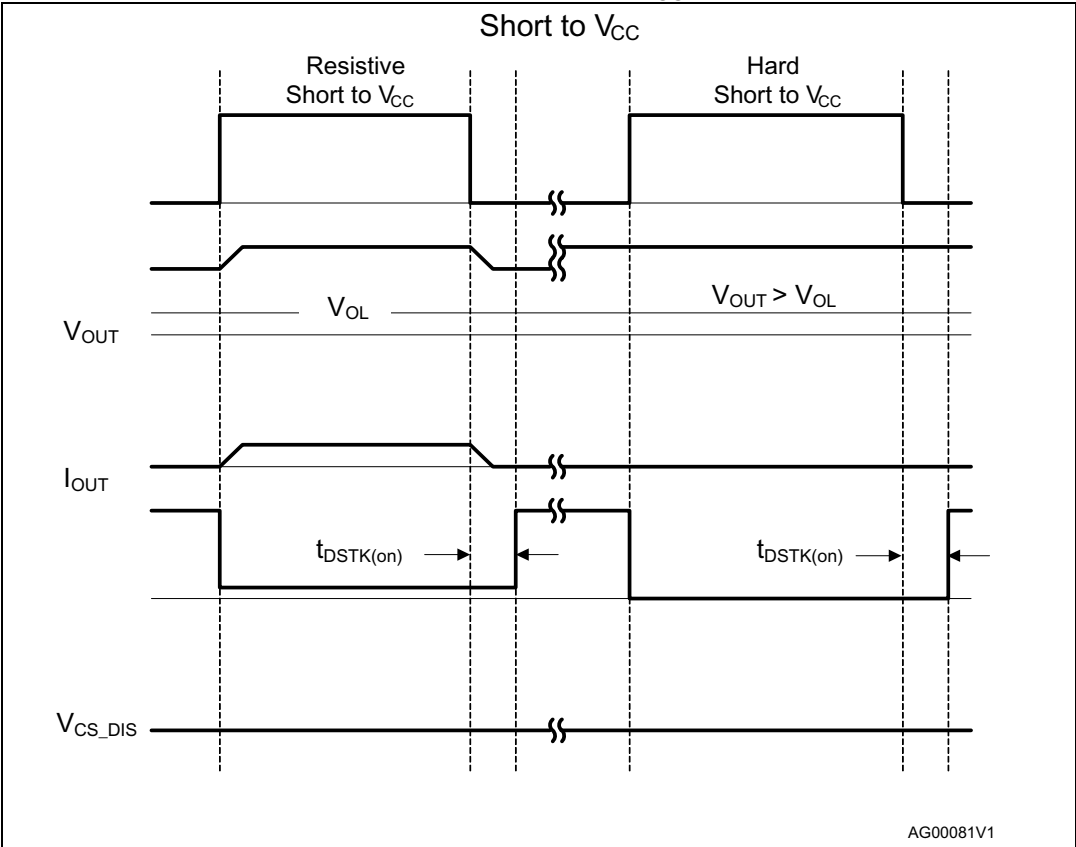
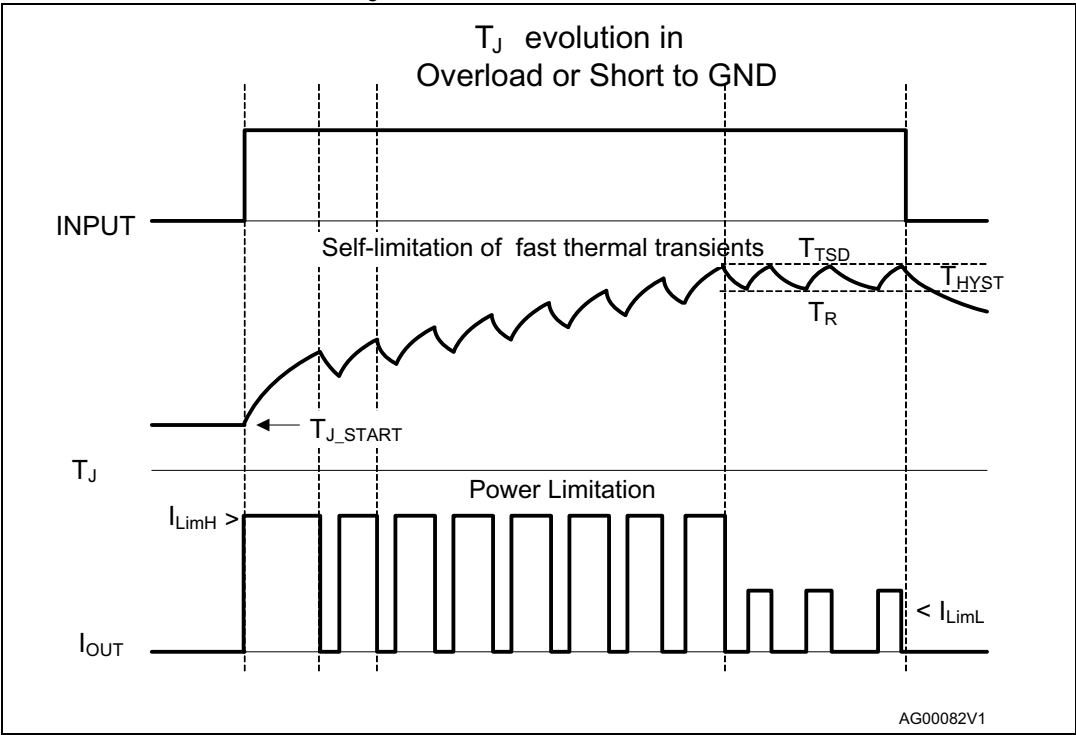


Figure 16. T_J evolution in overload or short to GND



2.5 Electrical characteristics curves

Figure 17. Off-state output current

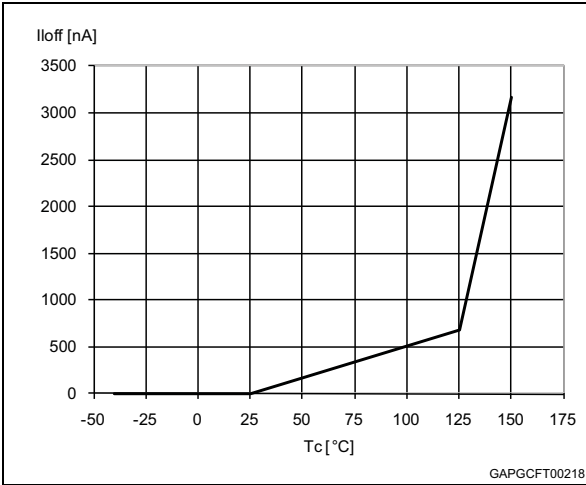


Figure 18. High level input current

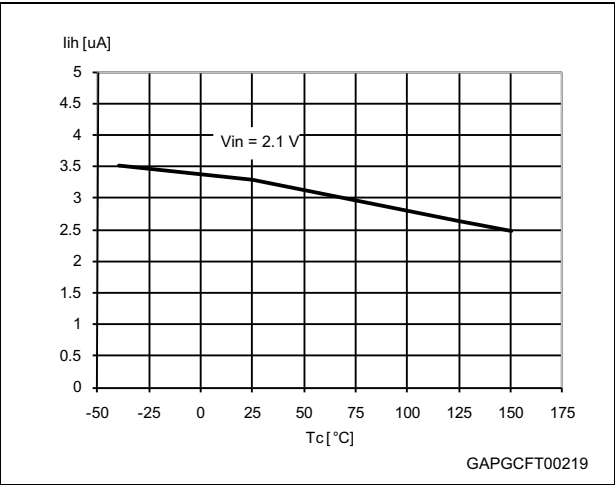


Figure 19. Input clamp voltage

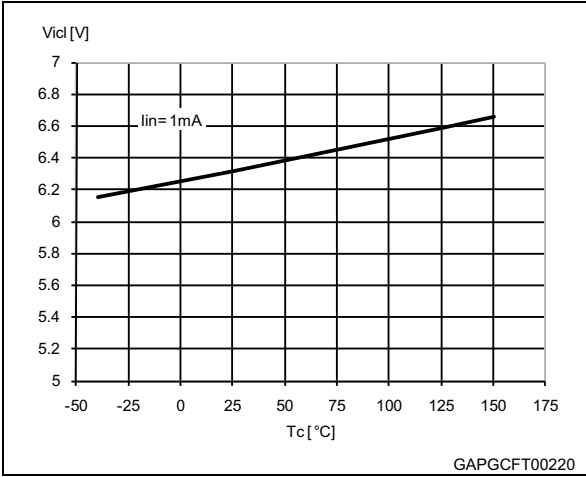


Figure 20. Input high level

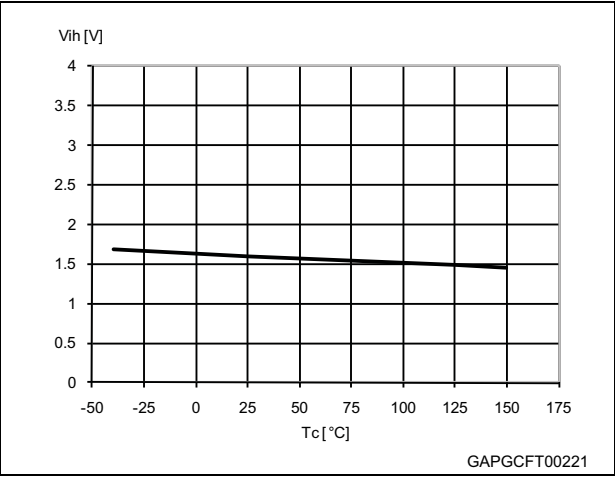


Figure 21. Input low level

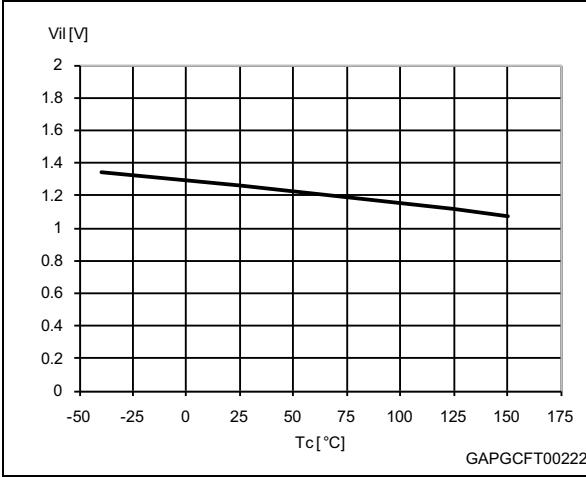


Figure 22. Input hysteresis voltage

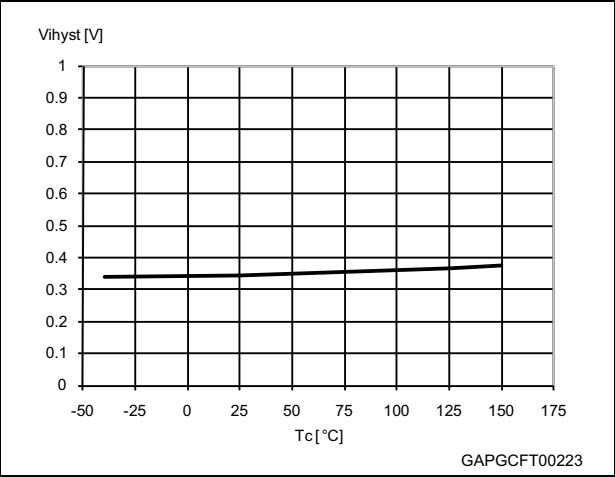


Figure 23. On-state resistance vs T_{case}

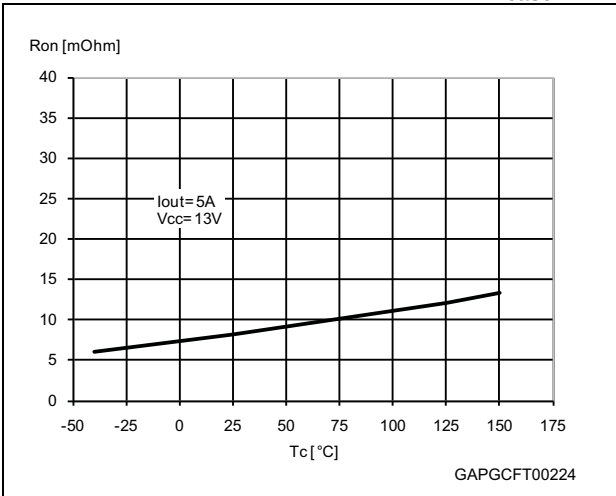


Figure 24. On-state resistance vs V_{CC}

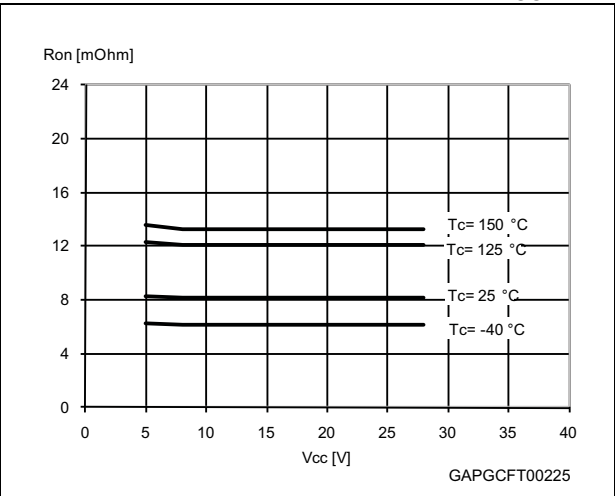


Figure 25. Undervoltage shutdown

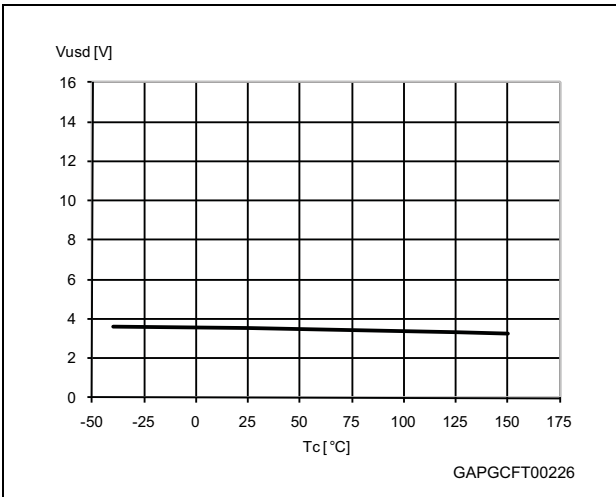


Figure 26. I_{LMH} vs T_{case}

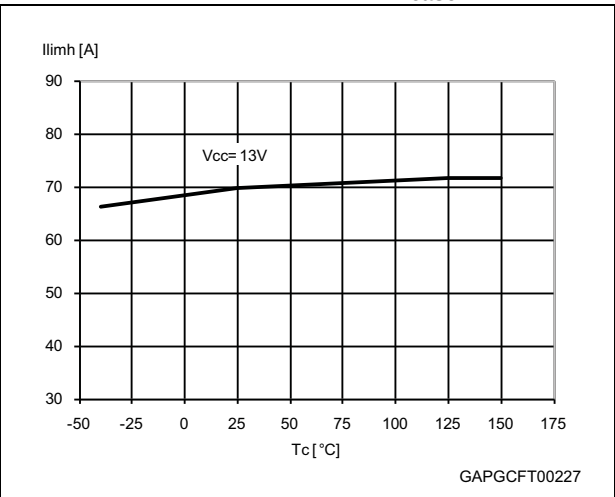


Figure 27. Turn-on voltage slope

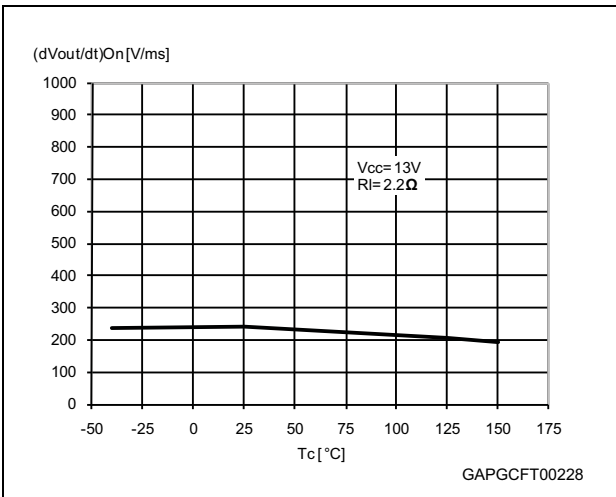


Figure 28. Turn-off voltage slope

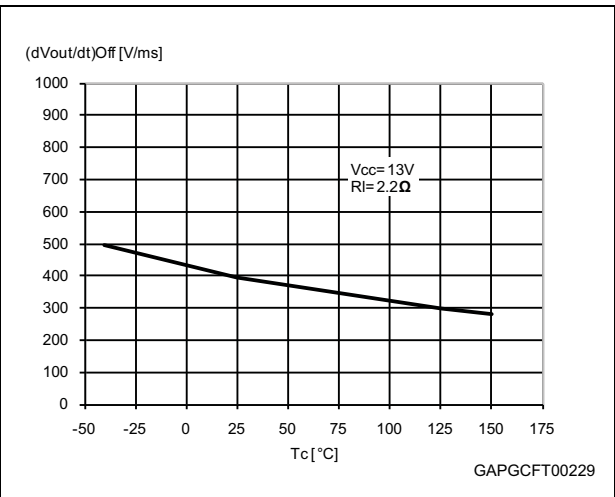


Figure 29. CS_DIS clamp voltage

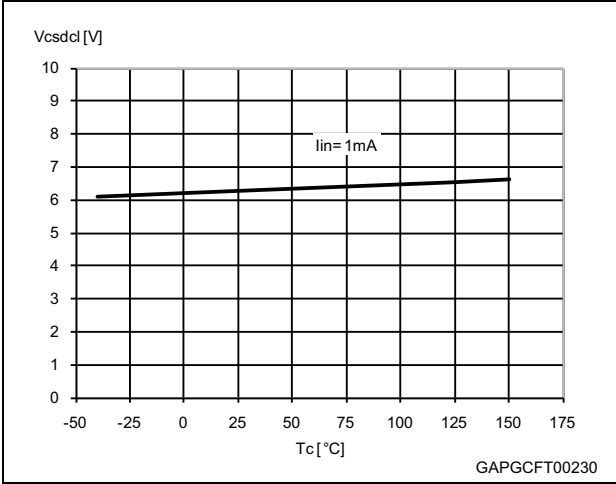


Figure 30. Low level CS_DIS voltage

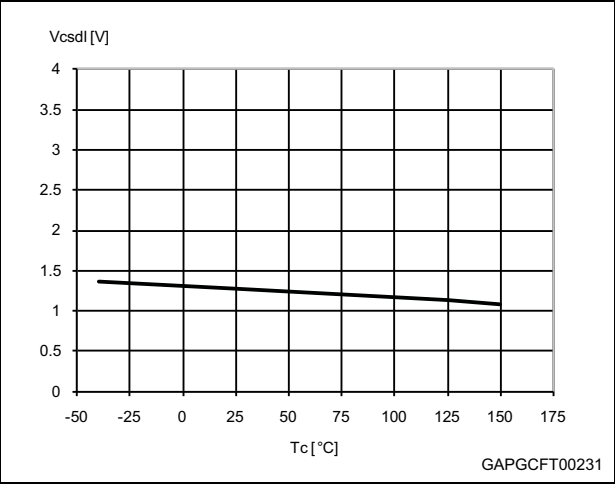
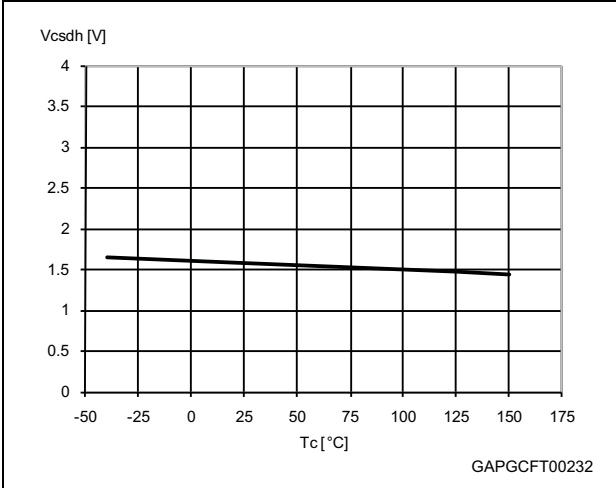
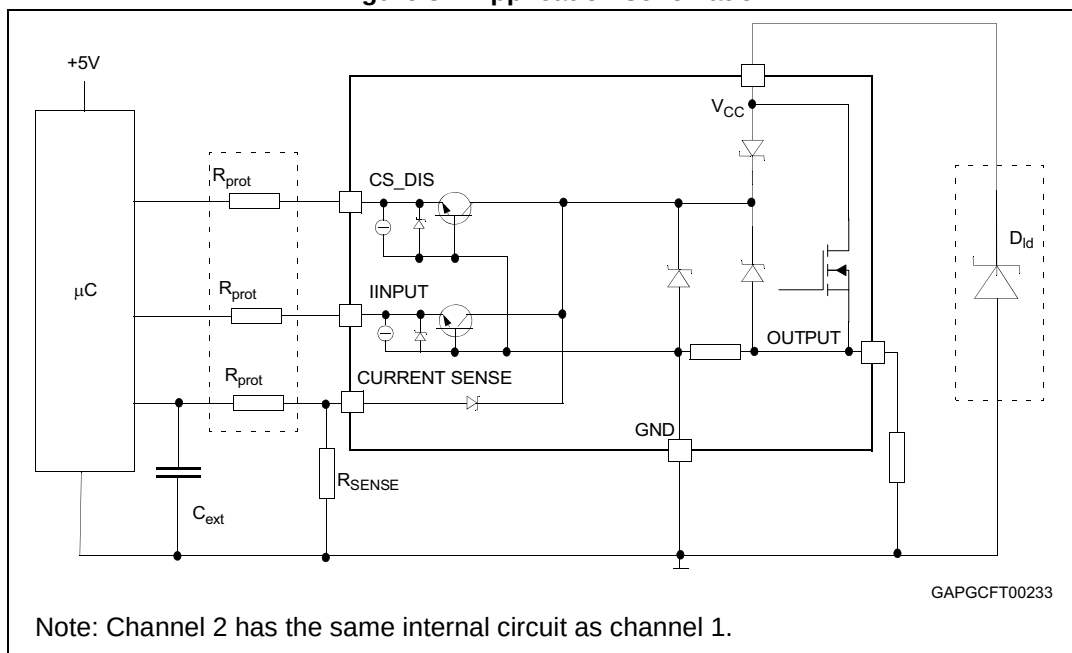


Figure 31. High level CS_DIS voltage



3 Application information

Figure 32. Application schematic



3.1 Load dump protection

D_{ld} is necessary (Voltage Transient Suppressor) if the load dump peak voltage exceeds the V_{CCPK} max rating. The same applies if the device is subject to transients on the V_{CC} line that are greater than the ones shown in the ISO T/R 7637/1 table.

3.2 MCU I/Os protection

When negative transients are present on the V_{CC} line, the control pin is pulled negative to approximately -1.5 V. ST suggests to insert a resistor (R_{prot}) in line to prevent the microcontroller I/O pins from latching-up.

The value of these resistors is a compromise between the leakage current of microcontroller and the current required by the HSD I/Os (input levels compatibility) with the latch-up limit of microcontroller I/Os.

Equation 1:

$$-V_{CCpeak} / I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH}) / I_{IHmax}$$

Calculation example:

$$\text{For } V_{CCpeak} = -1.5 \text{ V; } I_{latchup} \geq 20 \text{ mA; } V_{OH\mu C} \geq 4.5 \text{ V}$$

$$75 \Omega \leq R_{prot} \leq 240 \text{ k}\Omega.$$

Recommended values: $R_{prot} = 10 \text{ k}\Omega$, $C_{EXT} = 10 \text{ nF}$.

3.3 Current sense and diagnostic

The current sense pin performs a double function (see [Figure 33: Current sense and diagnostic](#)):

- **Current mirror of the load current in normal operation**, delivering a current proportional to the load one according to a known ratio K_X .
The current I_{SENSE} can be easily converted to a voltage V_{SENSE} by means of an external resistor R_{SENSE} . Linearity between I_{OUT} and V_{SENSE} is ensured up to 5 V minimum (see parameter V_{SENSE} in [Table 7: Current sense \(8 V < VCC < 18 V\)](#)). The current sense accuracy depends on the output current (refer to current sense electrical characteristics [Table 7: Current sense \(8 V < VCC < 18 V\)](#)).
- **Diagnostic flag in fault conditions**, delivering a fixed voltage V_{SENSEH} up to a maximum current I_{SENSEH} in case of the following fault conditions (refer to [Table 11: Truth table](#)):
 - Power limitation activation
 - Overtemperature
 - Short to V_{CC} in off-state
 - Open-load in off-state with additional external components.

A logic level high on CS_DIS pin sets at the same time all the current sense pins of the device in a high-impedance state, thus disabling the current monitoring and diagnostic detection. This feature allows multiplexing of the microcontroller analog inputs by sharing of sense resistance and ADC line among different devices.

[illegible]

Equation 2:

$$V_{OUT}|_{Pull-up_OFF} = R_{PD} \cdot I_{L(off)2f} < V_{OLmin} = 2V$$

$R_{PD} \leq 22\text{ k}\Omega$ is recommended.

For proper open-load detection in off-state, the external pull-up resistor must be selected according to the following formula:

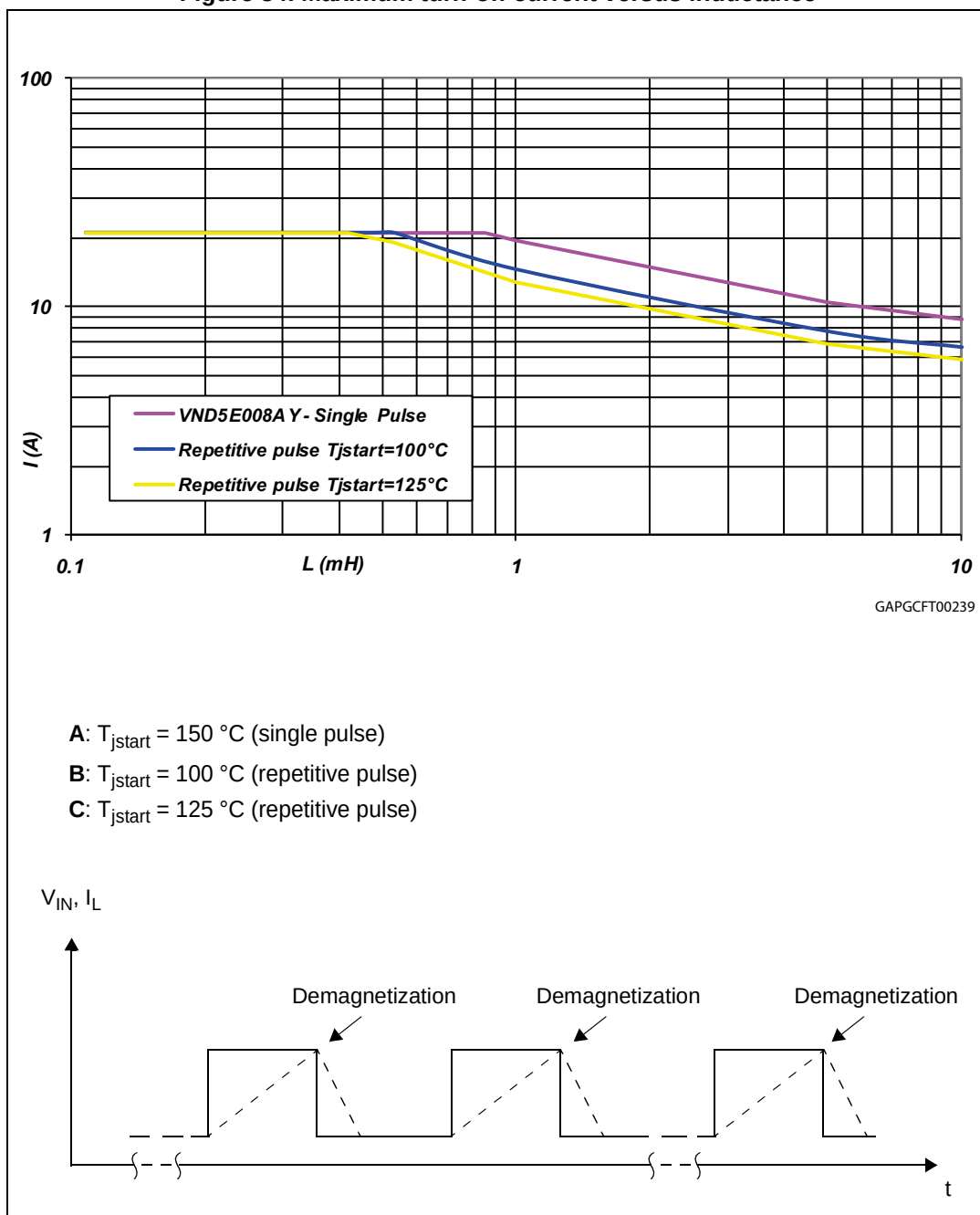
Equation 3:

$$V_{OUT}|_{Pull-up_ON} = \frac{(R_{PD} \cdot V_{PU}) - (R_{PU} \cdot R_{PD} \cdot I_{L(off)2r})}{(R_{PU} + R_{PD})} > V_{OLmax} = 4V$$

For the values of V_{OLmin} , V_{OLmax} , $I_{L(off)2r}$ and $I_{L(off)2f}$ (see [Table 8: Open-load detection \(8 V < VCC < 18 V\)](#)).

3.4 Maximum demagnetization energy ($V_{CC} = 13.5\text{ V}$)

Figure 34. Maximum turn-off current versus inductance



Note:

Values are generated with $R_L = 0\ \Omega$.

In case of repetitive pulses, T_{jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

4 Package and PCB thermal data

4.1 PowerSSO-36 thermal data

Figure 35. PowerSSO-36 PC board

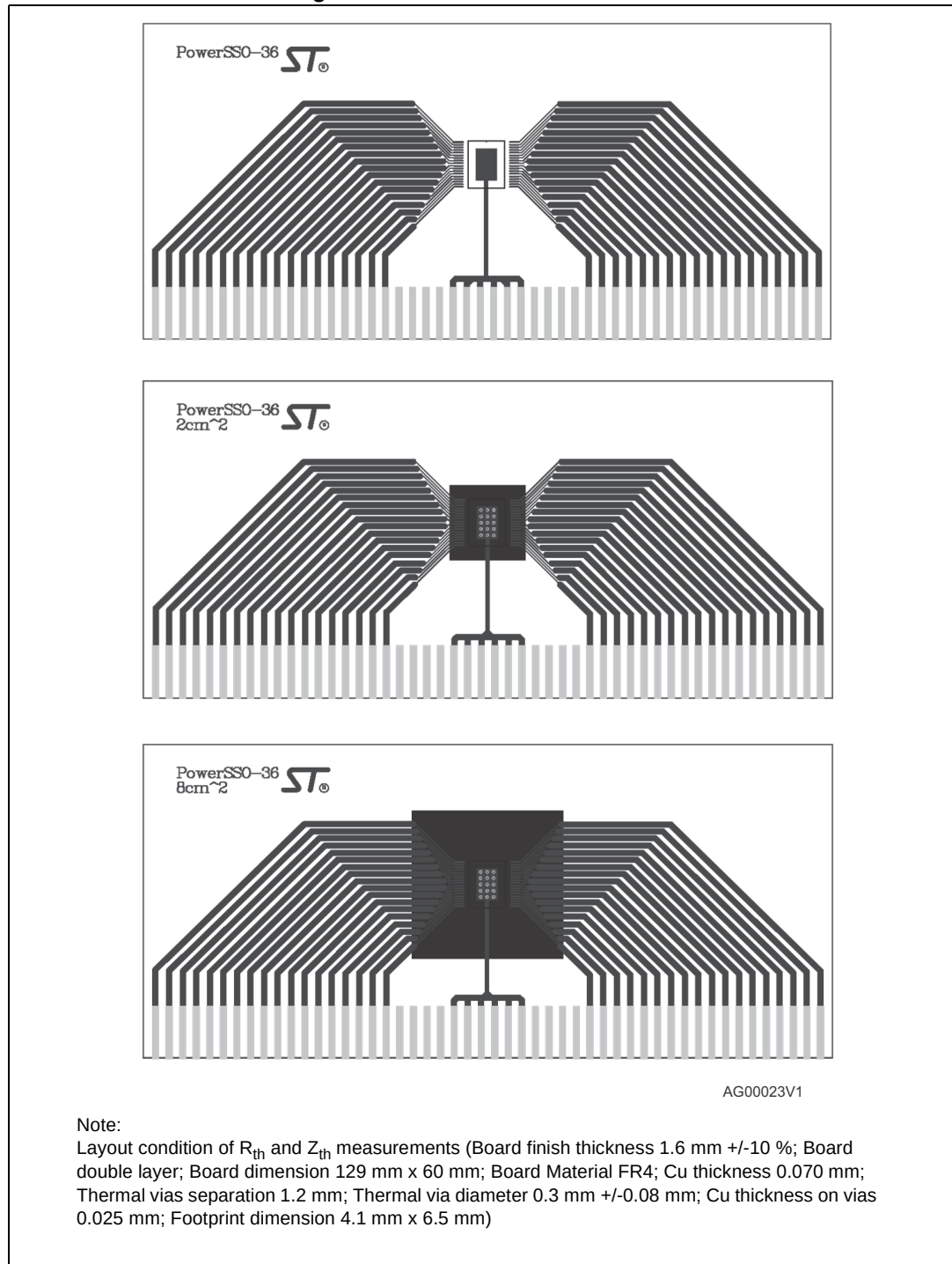


Figure 36. $R_{thj-amb}$ vs PCB copper area in open box free air condition (one channel ON)

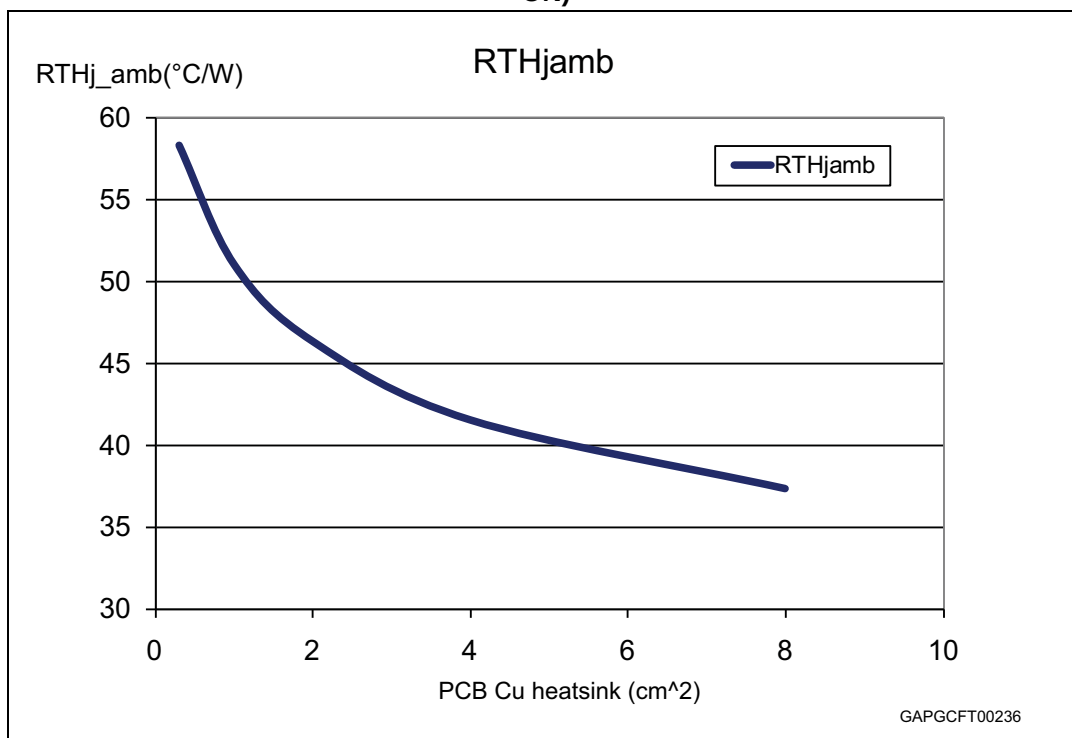


Figure 37. PowerSSO-36 Thermal impedance junction ambient single pulse (one channel ON)

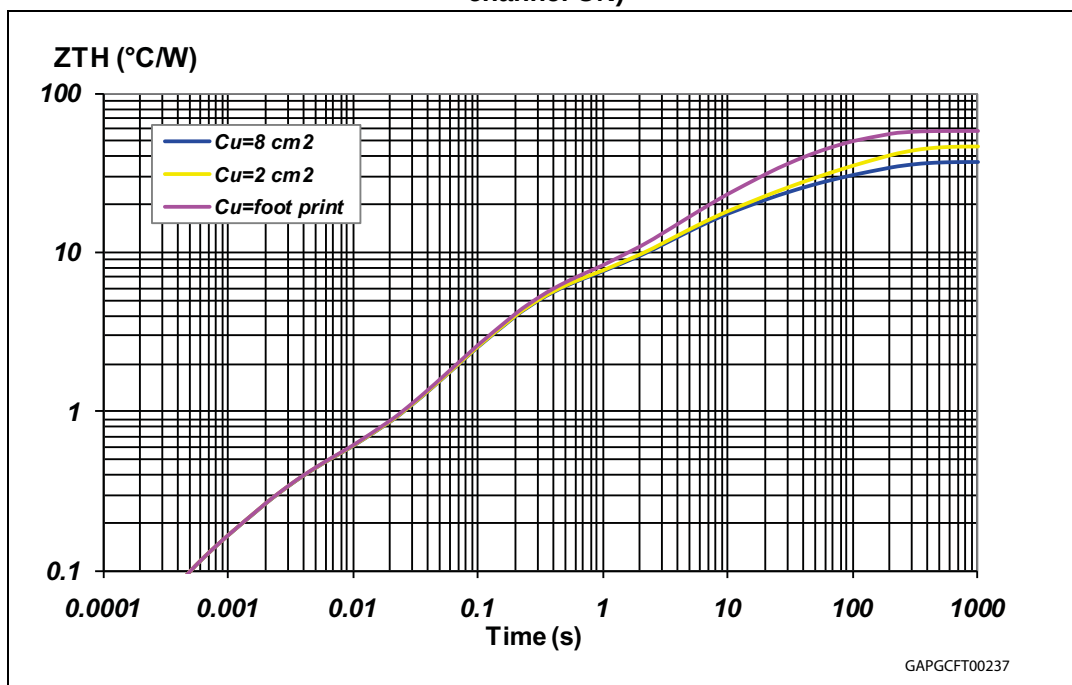
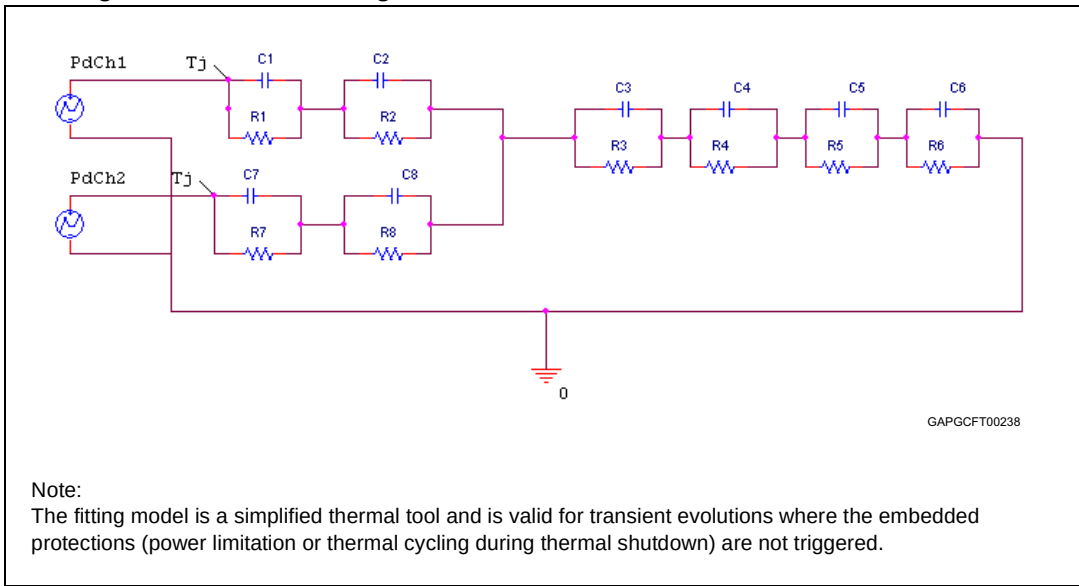


Figure 38. Thermal fitting model of a double channel HSD in PowerSSO-36



Equation 4: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p / T$

Table 15. Thermal parameter

Area/island (cm ²)	Footprint	2	8
R1 = R7 (°C/W)	0.05		
R2 = R8 (°C/W)	0.3		
R3 (°C/W)	5		
R4 (°C/W)	8		
R5 (°C/W)	18	10	10
R6 (°C/W)	27	23	14
C1 = C7 (W.s/°C)	0.004		
C2 = C8 (W.s/°C)	0.008		
C3 (W.s/°C)	0.04		
C4 (W.s/°C)	0.5		
C5 (W.s/°C)	1	2	2
C6 (W.s/°C)	3	6	9

5 Package information

5.1 ECOPACK[®] packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

5.2 PowerSSO-36 mechanical data

Figure 39. PowerSSO-36 package dimensions

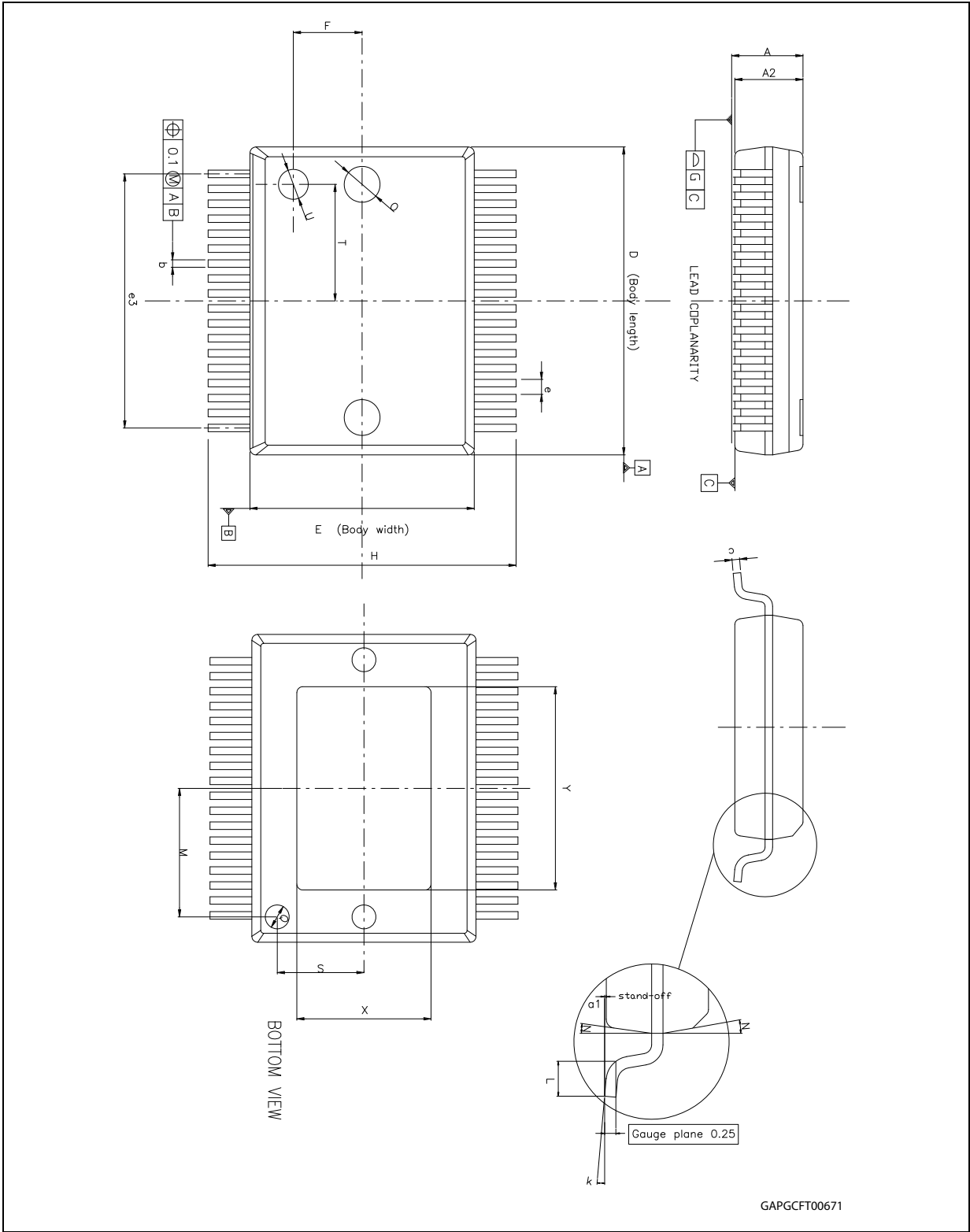


Table 16. PowerSSO-36 mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A	2.15	—	2.47
A2	2.15	—	2.40
a1	0	—	0.075
b	0.18	—	0.36
c	0.23	—	0.32
D	10.10	—	10.50
E	7.4	—	7.6
e	—	0.5	—
e3	—	8.5	—
G	—	—	0.1
G1	—	—	0.06
H	10.1	—	10.5
h	—	—	0.4
L	0.55	—	0.85
N	—	—	10 deg
X	4.1	—	4.7
Y	6.5	—	7.1

5.3 Packing information

Figure 40. PowerSSO-36 tube shipment (no suffix)

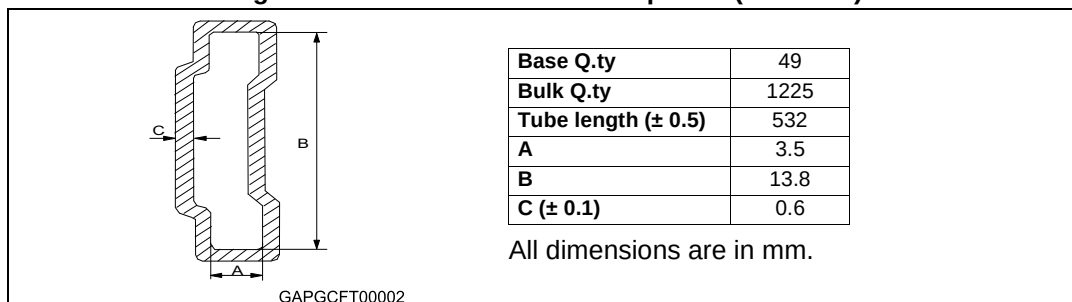
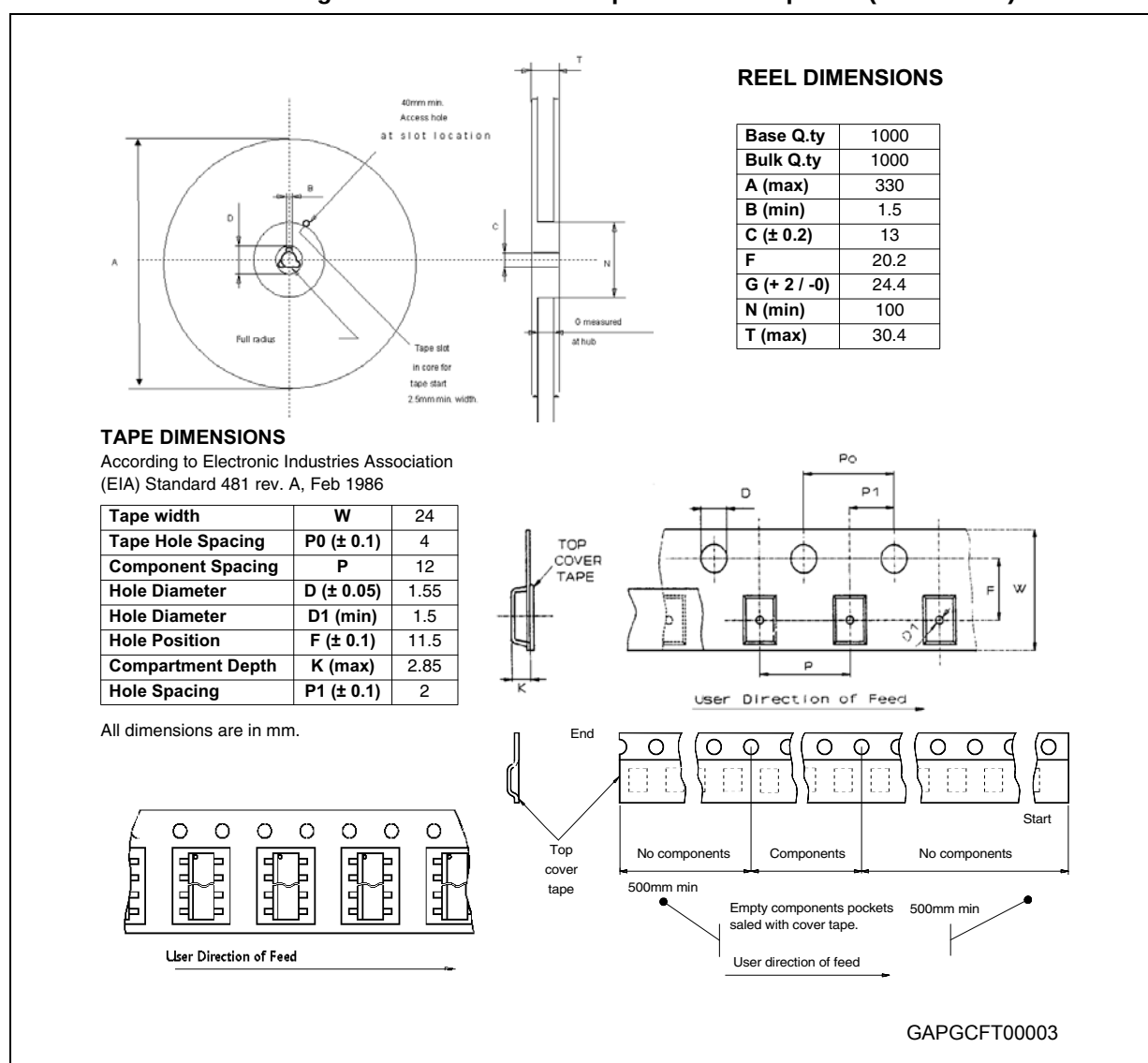


Figure 41. PowerSSO-36 tape and reel shipment (suffix "TR")



6 Order codes

Table 17. Device summary

Package	Order codes	
	Tube	Tape and reel
PowerSSO-36	VND5E008AY-E	VND5E008AYTR-E

7 Revision history

Table 18. Document revision history

Date	Revision	Changes
05-Jun-2007	1	Initial release
20-Apr-2011	2	Updated Features list. Updated following figures: – Figure 1: Block diagram – Figure 2: Configuration diagram (top view) – Figure 3: Current and voltage conventions Inserted following figures: – Figure 6: IOUT/ISENSE vs IOUT – Figure 7: Maximum current sense ratio drift vs load current – Figure 9: Delay response time between rising edge of output current and rising edge of current sense (CS enabled). Updated following tables: – Table 1: Pin function – Table 2: Suggested connections for unused and not connected pins – Table 3: Absolute maximum ratings V_{CCPK}, V_{ESD}: updated parameter V_{CC_LSC}, $-I_{GND}$: added parameter Updated E_{MAX} parameter – Table 4: Thermal data $R_{thj-case}$: added value – Table 5: Power section – Table 6: Switching ($V_{CC} = 13V$; $T_j = 25^{\circ}C$) – Table 7: Current sense ($8V < V_{CC} < 18V$) Updated dK_1/K_1, dK_2/K_2 and dK_3/K_3 minimum and maximum values V_{SENSEH}, I_{SENSEH}: added note – Table 8: Open-load detection ($8V < V_{CC} < 18V$) – Table 9: Protections Updated V_{DEMAG} and I_{LIMH} values – Table 13: Electrical transient requirements (part 2) Added Section 2.4: Waveforms. Updated Section 2.5: Electrical characteristics curves Updated Chapter 3: Application information Updated Chapter 4: Package and PCB thermal data
12-July-2012	3	Updated Figure 39: PowerSSO-36 package dimensions
20-Sep-2013	4	Updated Disclaimer.
25-Oct-2013	5	Updated footnote 2 into the Table 12: Electrical transient requirements (part 1) and Table 13: Electrical transient requirements (part 2) .

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