

FEATURES:

- Low input and output leakage $\leq 1\mu\text{A}$ (max.)
- CMOS power levels
- True TTL input and output compatibility
 - $V_{OH} = 3.3\text{V}$ (typ.)
 - $V_{OL} = 0.3\text{V}$ (typ.)
- Meets or exceeds JEDEC standard 18 specifications
- Military product compliant to MIL-STD-883, Class B and DESC listed (dual marked)
- Std., A, and C speed grades
- Resistor outputs
(-15mA IOH, 12mA IOL Ind.)
(-12mA IOH, 12mA IOL Mil.)
- Reduced system switching noise
- Available in the following packages:
 - Industrial: SOIC, QSOP, TSSOP
 - Military: CERDIP, LCC, CERPACK

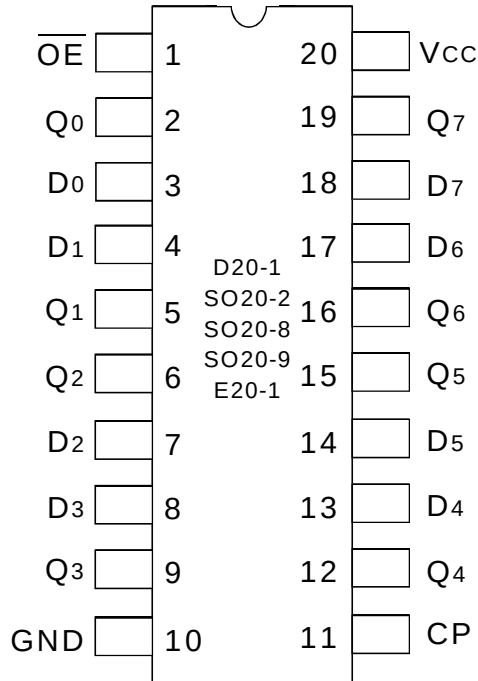
The FCT23741 is an 8-bit register built using an advanced dual metal CMOS technology. These registers consist of eight D-type flip-flops with a buffered common clock and buffered 3-state output control. When the output enable ($\overline{OE}$) input is low, the eight outputs are enabled. When the $\overline{OE}$ input is high, the outputs are in the high-impedance state.

The FCT2374T has balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot and controlled output fall times-reducing the need for external series terminating resistors. FCT2374T parts are plug-in replacements for FCT374T parts.

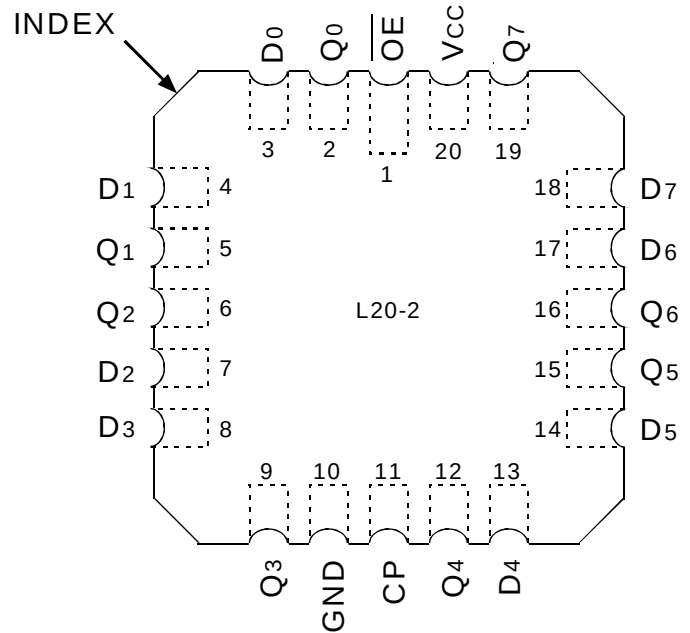
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MAY 2001

PIN CONFIGURATION



CERDIP/ SOIC/ QSOP/ TSSOP/ CERPACK
TOP VIEW



LCC
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Max.	Unit
$V_{TERM}^{(2)}$	Terminal Voltage with Respect to GND	-0.5 to +7	V
$V_{TERM}^{(3)}$	Terminal Voltage with Respect to GND	-0.5 to $V_{CC}+0.5$	V
T_{STG}	Storage Temperature	-65 to +150	°C
I_{OUT}	DC Output Current	-60 to +120	mA

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NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
- Inputs and V_{CC} terminals only.
- Outputs and I/O terminals only.

CAPACITANCE ($T_A = +25^{\circ}\text{C}$, $f = 1.0\text{MHz}$)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0V$	6	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	8	12	pF

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NOTE:

- This parameter is measured at characterization but not tested.

PIN DESCRIPTION

Pin Names	Description
D_N	D flip-flop data inputs
CP	Clock Pulse for the register. Enters data on LOW-to-HIGH transition.
Q_N	3-state outputs (TRUE)
$\overline{Q}_N$	3-state outputs (INVERTED)
$\overline{OE}$	Active LOW 3-state Output Enable input

FUNCTION TABLE (1)

Function	Inputs			Outputs	Internal
	$\overline{OE}$	CP	D_N	Q_N	$\overline{Q}_N$
HI-Z	H	L	X	Z	NC
	H	H	X	Z	NC
LOAD REGISTER	L	↑	L	L	H
	L	↑	H	H	L
	H	↑	L	Z	H
	H	↑	H	Z	L

NOTE:

- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High Impedance
NC = No Change
↑ = LOW-to-HIGH transition

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Industrial : $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 5\%$; Military: $T_A = -55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current ⁽⁴⁾	$V_{CC} = \text{Max.}$	$V_I = 2.7\text{V}$	—	—	± 1	μA
I_{IL}	Input LOW Current ⁽⁴⁾		$V_I = 0.5\text{V}$	—	—	± 1	
I_{OZH}	High Impedance Output Current (3-State Output pins) ⁽⁴⁾	$V_{CC} = \text{Max.}$	$V_O = 2.7\text{V}$	—	—	± 1	
I_{OL}			$V_O = 0.5\text{V}$	—	—	± 1	
I_I	Input HIGH Current ⁽⁴⁾	$V_{CC} = \text{Max.}, V_I = V_{CC} (\text{Max.})$		—	—	± 1	μA
V_{IK}	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18\text{mA}$		—	-0.7	-1.2	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}, V_{IN} = \text{GND or } V_{CC}$		—	0.01	1	mA

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OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
I_{ODL}	Output LOW Current	$V_{CC} = 5\text{V}, V_{IN} = V_{IH} \text{ or } V_{IL}, V_{OUT} = 1.5\text{V}^{(3)}$		16	48	—	mA
I_{ODH}	Output HIGH Current	$V_{CC} = 5\text{V}, V_{IN} = V_{IH} \text{ or } V_{IL}, V_{OUT} = 1.5\text{V}^{(3)}$		-16	-48	—	mA
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -12\text{mA MIL}$ $I_{OH} = -15\text{mA IND}$	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = 12\text{mA}$	—	0.3	0.5	V

NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0\text{V}$, $+25^{\circ}\text{C}$ ambient.
- Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
- The test limit for this parameter is $\pm 5\mu\text{A}$ at $T_A = -55^{\circ}\text{C}$.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(3)}$		—	0.5	2	mA
I_{CCD}	Dynamic Power Supply Current ⁽⁴⁾	$V_{CC} = \text{Max.}$ Outputs Open $\overline{OE} = \text{GND}$ One Input Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	0.06	0.12	mA/ MHz
I_C	Total Power Supply Current ⁽⁶⁾	$V_{CC} = \text{Max.}$ Outputs Open $f_{CP} = 10\text{MHz}$ 50% Duty Cycle $\overline{OE} = \text{GND}$ $f_i = 5\text{MHz}$ 50% Duty Cycle One Bit Toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	0.6	2.2	mA
			$V_{IN} = 3.4$ $V_{IN} = \text{GND}$	—	1.1	4.2	
		$V_{CC} = \text{Max.}$ Outputs Open $f_{CP} = 10\text{MHz}$ 50% Duty Cycle $\overline{OE} = \text{GND}$ Eight Bits Toggling $f_i = 2.5\text{MHz}$ 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	1.5	4 ⁽⁵⁾	
			$V_{IN} = 3.4$ $V_{IN} = \text{GND}$	—	3.8	13 ⁽⁵⁾	

NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0V$, $+25^\circ\text{C}$ ambient.
- Per TTL driven input ($V_{IN} = 3.4V$). All other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
 $I_C = I_{CC} + \Delta I_{CC} D_{HNT} + I_{CCD} (f_{CP}/2 + f_i N_i)$
 $I_{CC} = \text{Quiescent Current}$
 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input } (V_{IN} = 3.4V)$
 $D_H = \text{Duty Cycle for TTL Inputs High}$
 $N_T = \text{Number of TTL Inputs at } D_H$
 $I_{CCD} = \text{Dynamic Current Caused by an Input Transition Pair (HLH or LHL)}$
 $f_{CP} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$
 $f_i = \text{Input Frequency}$
 $N_i = \text{Number of Inputs at } f_i$
 All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE - INDUSTRIAL

Symbol	Parameter	Condition ⁽¹⁾	FCT2374T		FCT2374AT		FCT2374CT		Unit
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
t _{PLH} t _{PHL}	Propagation Delay CP to Q _N	C _L = 50pF R _L = 500Ω	2	10	2	6.5	2	5.2	ns
t _{PZH} t _{PZL}	Output Enable Time		1.5	12.5	1.5	6.5	1.5	5.5	ns
t _{PHZ} t _{PLZ}	Output Disable Time		1.5	8	1.5	5.5	1.5	5	ns
t _{SU}	Set-up Time HIGH or LOW, D _N to CP		2	—	2	—	2	—	ns
t _H	Hold Time HIGH or LOW, D _N to CP		1.5	—	1.5	—	1.5	—	ns
t _w	CP Pulse Width HIGH or LOW ⁽³⁾		7	—	5	—	5	—	ns

SWITCHING CHARACTERISTICS OVER OPERATING RANGE - MILITARY

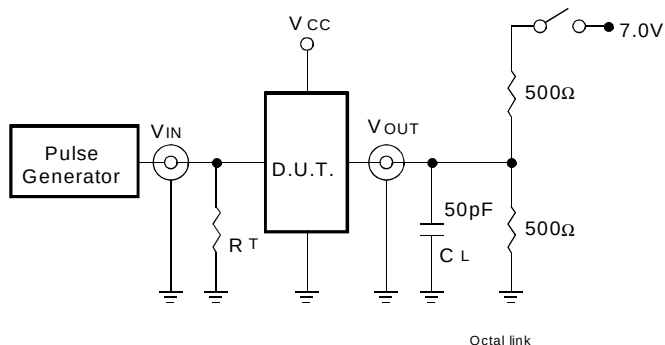
Symbol	Parameter	Condition ⁽¹⁾	FCT2374T		FCT2374AT		FCT2374CT		Unit
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
t _{PLH} t _{PHL}	Propagation Delay CP to Q _N	C _L = 50pF R _L = 500Ω	2	11	2	7.2	2	6.2	ns
t _{PZH} t _{PZL}	Output Enable Time		1.5	14	1.5	7.5	1.5	6.2	ns
t _{PHZ} t _{PLZ}	Output Disable Time		1.5	8	1.5	6.5	1.5	5.7	ns
t _{SU}	Set-up Time HIGH or LOW, D _N to CP		2	—	2	—	2	—	ns
t _H	Hold Time HIGH or LOW, D _N to CP		1.5	—	1.5	—	1.5	—	ns
t _w	CP Pulse Width HIGH or LOW ⁽³⁾		7	—	6	—	6	—	ns

NOTES:

- See test circuit and waveforms.
- Minimum limits are guaranteed but not tested on Propagation Delays.
- This parameter is guaranteed but not tested.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

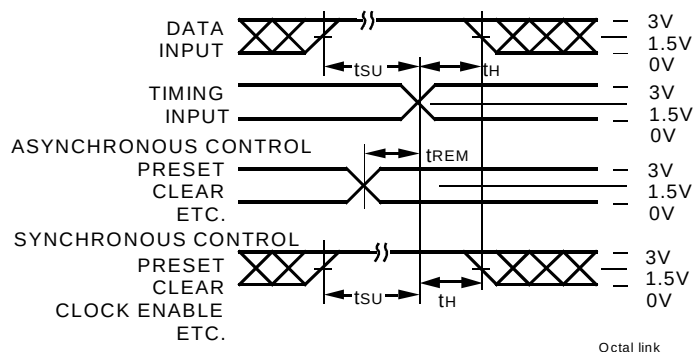
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DEFINITIONS:

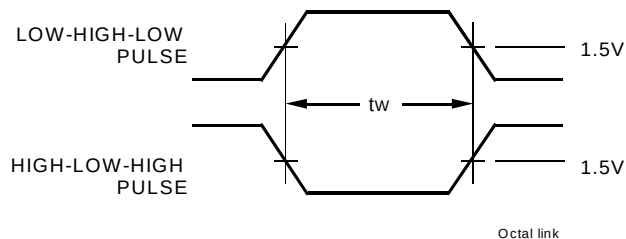
C_L = Load capacitance: includes jig and probe capacitance.

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

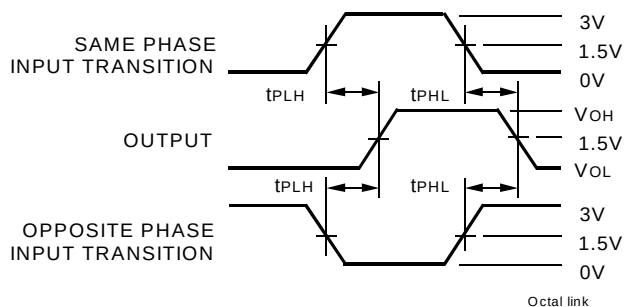
SET-UP, HOLD, AND RELEASE TIMES



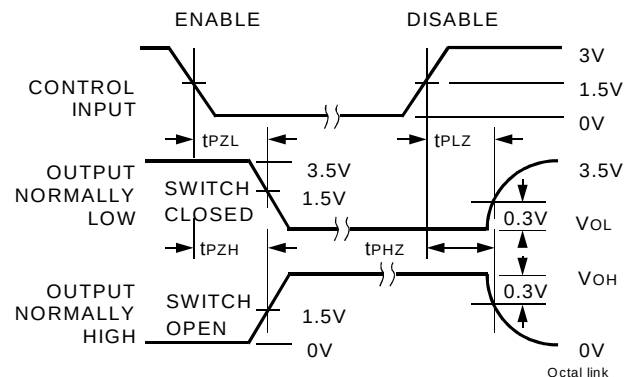
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES



NOTES:

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
- Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; $t_F \leq 2.5\text{ns}$; $t_R \leq 2.5\text{ns}$

ORDERING INFORMATION

IDT	XX	FCT	XXXX	XX	X		
	Temp. Range		Device Type	Package	Process		
					Blank	Industrial	
					B	MIL-STD-883, Class B	
						<u>Industrial Options</u>	
					SO	Small Outline IC (SO20-2)	
					Q	Quarter-size Small Outline Package (SO20-8)	
					PG	Thin Shrink Small Outline Package (SO20-9)	
						<u>Military Options</u>	
					D	CERDIP (D20-1)	
					E	CERPACK (E20-1)	
					L	Leadless Chip Carrier (L20-1)	
					2374T	Octal D Register	
					2374AT		
					2374CT		
					54	– 55°C to +125°C	
					74	– 40°C to +85°C	



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