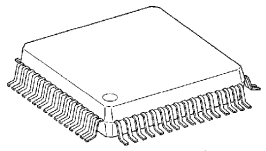
CMOS 8-Bit Microcontroller

TMP86PM72FG

The TMP86PM72 is a OTP type MCU which includes 32-Kbyte one-time PROM. It is a pin compatible with a mask ROM product of the TMP86CH72/CM72. Writing the program to built-in PROM, the TMP86PM72 operates as the same way as the TMP86CH72/CM72. Using the Adapter socket, you can write and verify the data for the TMP86PM72 with a general-purpose PROM programmer same as TC571000D/AD.

Product No.	OTP	RAM	Package	Adapter Socket
TMP86PM72FG	32 K × 8 bits	1 K × 8 bits	P-QFP64-1414-0.80C	BM11707

P-QFP64-1414-0.80C



TMP86PM72FG

030619EBP1

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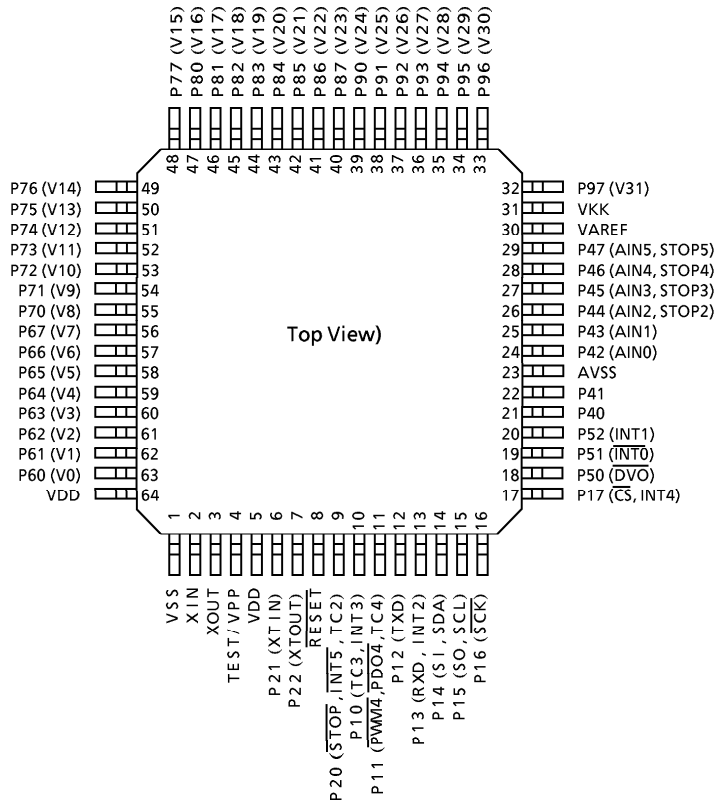
Pin Assignments (Top View)

P-QFP64-1414-0.80C



Note: All VDD terminals are connected externally.

Pin Function

The TMP86PM72 has MCU mode and PROM mode.

(1) MCU mode

In the MCU mode, the TMP86PM72 is a pin compatible with the TMP86CH72/CM72 (Make sure to fix the TEST pin to low level).

(2) PROM mode

Pin name (PROM mode)	Input/Output	Functions	Pin Name (MCU mode)
A16 to A12	Input	Input of Memory address for program	PD4 to PD0
A11 to A8			P53 to P50
A7 to A0			P47 to P40
D7 to D0	I/O	Input/Output of Memory data for program	P17 to P10
$\overline{CE}$	Input	Chip enable	P95
$\overline{OE}$		Output enable	P94
$\overline{PGM}$		Program control	P93
VPP	Power supply	+ 12.75 V/5 V (Power supply of program)	TEST
VDD		+ 6.25 V/5 V	VDD
GND		0 V	VSS
P51, P21	I/O	PROM mode setting pin. Fix to high.	
P50, P20, P22, AVSS, VAREF		PROM mode setting pin. Fix to low.	
$\overline{RESET}$			
XIN	Input	Self oscillation with resonator (10 MHz)	
XOUT	Output		

Operation

This section describes the functions and basic operational blocks of TMP86PM72.
The TMP86PM72 has PROM in place of the mask ROM which is included in the TMP86CH72/CM72.
In addition, TMP86PM72 operates as the single clock mode when releasing reset.
When using the dual clock mode, oscillate a low-frequency clock by [SET (SYSCR2). XTEN] command at the beginning of program.

1. Operating Mode

The TMP86PM72 has MCU mode and PROM mode.

1.1 MCU Mode

The MCU mode is set by fixing the TEST/VPP pin to the low level. (TEST/VPP pin cannot be used open because it has no built-in pull-down resister).

1.1.1 Program Memory

The TMP86PM72 has a 32 Kbyte built-in one time PROM (addresses 8000_H to $FFFF_H$ in the MCU mode, addresses 0000_H to $7FFF_H$ in the PROM mode).
When using TMP86PM72 for evaluation of mask ROM products, the program is written in the program storing area shown in Figure 1-1.

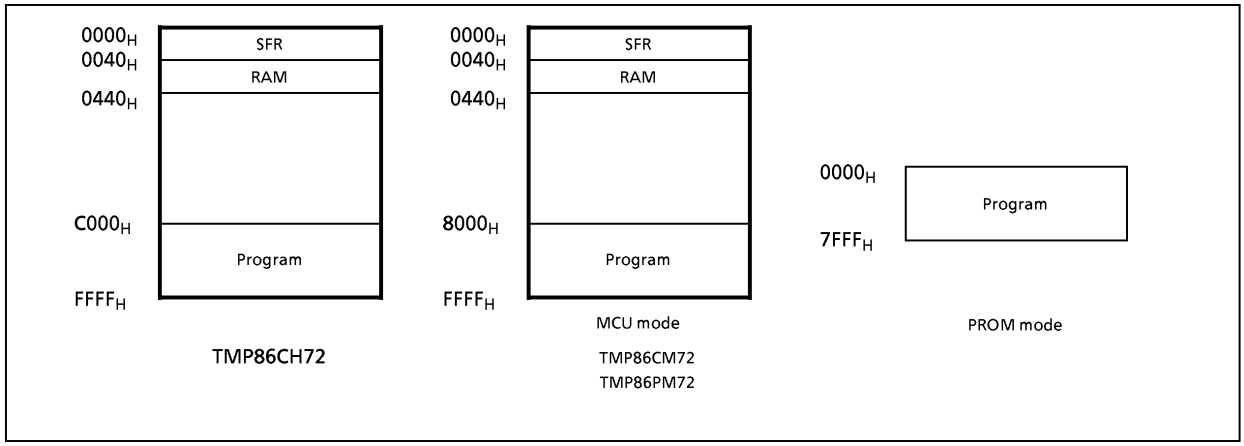


Figure 1-1. Program Memory Area

Note: The area that is not in use should be set data to FFH, or a general-purpose PROM programmer should be set only in the program memory area to access.

Electrical Characteristics

Absolute Maximum Ratings (V_{SS} = 0 V)

Parameter		Symbol	Pins	Rating	Unit
Supply voltage		V_{DD}		– 0.3 to 6.5	V
Program voltage		V_{PP}	TEST/V_{PP}	– 0.3 to 13.0	
Input voltage		V_{IN}		– 0.3 to V_{DD} + 0.3	
Output voltage		V_{OUT1}		– 0.3 to V_{DD} + 0.3	
		V_{OUT2}	Source open drain ports	V_{DD} – 41 to V_{DD} + 0.3	
Output current (per 1 pin)	IOL	I_{OUT1}	P0, P1, P2, P4 (P42~P47), P5 ports	5	mA
		I_{OUT2}	P4 (P40, P41) port	40	
	IOH	I_{OUT3}	P0, P1, P4, P5 ports	– 3	
		I_{OUT4}	P6, P7 ports	– 30	
		I_{OUT5}	P8, P9 ports	– 20	
Output current (total)		ΣI_{OUT1}	P0, P1, P2, P4, P5 ports	120	
		ΣI_{OUT2}	P6, P7, P8, P9 ports	– 120	
Power dissipation [T_{opr} = 25°C]		PD		1200	mW
Soldering temperature (time)		Tsld		260 (10 μ)	°C
Storage temperature		Tstg		– 55 to 125	
Operating temperature		Topr		– 30 to 70	

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

Recommended Operating Condition (V_{SS} = 0 V, Topr = – 30 to 70°C)

Parameter	Symbol	Pins	Condition		Min	Max	Unit
Supply voltage	V_{DD}		fc = 16 MHz	NORMAL1/2 modes	4.5	5.5	V
				IDLE0, 1/2 modes			
			fc = 8 MHz	NORMAL1/2 modes	2.7		
				IDLE0, 1/2 modes			
			fs = 32.768 kHz	SLOW mode			
				SLEEP mode			
				STOP mode			
Output voltage	V_{OUT3}	Source open drain ports			V_{DD} – 38	V_{DD}	
Input high level	V_{IH1}	Except hysteresis input			V_{DD} × 0.70	V_{DD}	
	V_{IH2}	Hysteresis input			V_{DD} × 0.75		
	V_{IH3}	TTL input	$V_{DD} \leqq$ 4.5 V		V_{DD} × 0.90		
Input low level	V_{IL1}	Except hysteresis input			0	V_{DD} × 0.30	
	V_{IL2}	Hysteresis input				V_{DD} × 0.25	
	V_{IL3}	TTL input	$V_{DD} \leqq$ 4.5 V		V_{DD} × 0.10	V_{DD}	
Clock frequency	fc	XIN, XOUT	V_{DD} = 2.7 to 5.5 V		1.0	8.0	MHz
			V_{DD} = 4.5 to 5.5 V			16.0	
	fs	XTIN, XTOUT			30.0	34.0	kHz

Note: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (Supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

DC Characteristics (1) (V_{DD} = 5 V)

[Condition] V_{DD} = 5.0 V ± 10%, V_{SS} = A_{VSS} = 0 V, Topr = −30~70°C
(Typ.: V_{DD} = 5.0 V, Topr = 25°C, Vin = 5.0 V/0 V)

Parameter	Symbol	Pins	Condition		Min	Typ.	Max	Unit
Hysteresis voltage	V_{HS}	Hysteresis input			–	0.9	–	V
Input current	I_{IN1}	TEST	V_{DD} = 5.5 V, V_{IN} = 5.5 V/0 V		–	–	±2	μA
	I_{IN2}	Sink open drain, Tri-st						
	I_{IN3}	RESET, STOP						
Input resistance	R_{IN}	RESET pull-up			100	220	450	kΩ
Pull-down resistance (Note 4)	R_K	Source open drain, Tri-st	V_{DD} = 5.5 V, V_{KK} = −30 V		50	80	120	
Output leakage current	I_{LO1}	Sink open drain, Tri-st	V_{DD} = 5.5 V, V_{OUT} = 5.5 V/0 V		–	–	±2	μA
	I_{LO2}	Source open drain	V_{DD} = 5.5 V, V_{KK} = −32 V		–	–	±2	
Output high voltage	V_{OH}	Tri-st port	V_{DD} = 4.5 V, I_{OH} = −0.7 mA		4.1	–	–	V
Output low voltage	V_{OL1}	Except XOUT and (P40, P41) Port	V_{DD} = 4.5 V, I_{OL} = 1.6 mA		–	–	0.4	
Output high current	I_{OH1}	P6, P7	V_{DD} = 4.5 V, V_{OH} = 2.4 V		−18	−28	–	mA
	I_{OH2}	P8, P9, PD	V_{DD} = 4.5 V, V_{OH} = 2.4 V		−9	−14	–	
Output low current	I_{OL}	High current port (P40, P41)	V_{DD} = 4.5 V, V_{OL} = 1.0 V		–	20	–	
Supply current in NORMAL1/2 modes	I_{DD}		fc = 16.0 MHz fs = 32.768 kHz	AD converter disable (IREF off)	–	12	18	
			fc = 8.0 MHz fs = 32.768 kHz		–	6	9	
Supply current in IDLE0/1/2 modes			fc = 16.0 MHz fs = 32.768 kHz		–	6	9	
			fc = 8.0 MHz fs = 32.768 kHz		–	3	4.5	
Supply current in NORMAL1/2 modes			fc = 16.0 MHz fs = 32.768 kHz	AD converter enable	–	13	19	
			fc = 8.0 MHz fs = 32.768 kHz		–	7	10	
Supply current in STOP mode			Topr = to 50°C	AD converter disable	–	0.5	5	μA
			Topr = to 70°C		–		10	

Note 1: Typical values show those at Topr = 25°C, V_{DD} = 5 V.
Note 2: Input current (I_{IN1}, I_{IN3}): The current through pull-up or pull-down resistor is not included.
Note 3: I_{DD} does not include I_{REF} current.
Note 4: Topr = −10°C to 70°C

DC Characteristics (2) (V_{DD} = 3 V)

[Condition] V_{DD} = 3.0 V ± 10%, V_{SS} = A_{VSS} = 0 V, Topr = – 30 to 70°C
(Typ.: V_{DD} = 3.0 V, Topr = 25°C, Vin = 3.0 V/0 V)

Parameter	Symbol	Pins	Condition		Min	Typ.	Max	Unit
Hysteresis voltage	V_{HS}	Hysteresis input			–	0.4	–	V
Input current	I_{IN1}	TEST	V_{DD} = 3.3 V, V_{IN} = 3.3 V/0 V		–	–	± 2	μA
	I_{IN2}	Sink open drain, Tri-st						
	I_{IN3}	RESET, STOP						
Input resistance	R_{IN}	RESET pull-up			100	220	450	kΩ
Pull-down resistance	R_K	Source open drain, tri-st	V_{DD} = 3.3 V, V_{KK} = – 30 V		45	75	115	
Output leakage current	I_{LO1}	Sink open drain, tri-st	V_{DD} = 3.3 V, V_{OUT} = 3.3 V/0 V		–	–	± 2	μA
	I_{LO2}	Source open drain	V_{DD} = 3.3 V, V_{KK} = – 32 V		–	–	± 2	
Output high voltage	V_{OH}	Tri-st port	V_{DD} = 2.7 V, I_{OH} = – 0.6 mA		2.3	–	–	V
Output low voltage	V_{OL1}	Except XOUT and (P40, P41) Port	V_{DD} = 2.7 V, I_{OL} = 0.9 mA		–	–	0.4	
Output high current	I_{OH1}	P6, P7	V_{DD} = 2.7 V, V_{OH} = 1.5 V		– 5.5	– 8	–	mA
	I_{OH2}	P8, P9, PD	V_{DD} = 2.7 V, V_{OH} = 1.5 V		– 3	– 4.5	–	
Output low current	I_{OL}	High current port (P40, P41) port	V_{DD} = 2.7 V, V_{OL} = 1.0 V		–	6	–	
Supply current in NORMAL1/2 modes	I_{DD}		fc = 8.0 MHz fs = 32.768 kHz	AD converter disable (IREF off)	–	3	4.5	
Supply current in IDLE0/1/2 modes			fc = 8.0 MHz fs = 32.768 kHz		–	2	2.5	
Supply current in NORMAL1/2 modes			fc = 8.0 MHz fs = 32.768 kHz	AD converter enable	–	3.5	5	
Supply current in SLOW1 mode			fs = 32.768 kHz	AD converter disable	–	30	60	μA
Supply current in SLEEP0, 1 mode					–	15	30	
Supply current in STOP mode			Topr = to 50℃		–	0.5	5	
			Topr = to 70℃				10	

Note 1: Typical values show those at Topr = 25°C, V_{DD} = 3 V.
Note 2: Input current (I_{IN1}, I_{IN3}): The current through pull-up or pull-down resistor is not included.
Note 3: I_{DD} does not include I_{REF} current.
Note 4: The supply currents of SLOW2 and SLEEP2 modes are equivalent IDLE0, 1, 2.

AD Conversion Characteristics

(V_{SS} = 0.0 V, 4.5 V ≦ V_{DD} ≦ 5.5 V, Topr = – 30 to 70°C)

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Analog reference voltage	V_{AREF}		V_{DD} – 1.5	–	V_{DD}	V
Analog reference GND	A_{VSS}			V_{SS}		
Analog reference voltage range (Note 4)	$\triangle V_{AREF}$		3.0	–	–	
Analog input voltage	V_{AIN}		V_{SS}	–	V_{AREF}	
Power supply current of analog reference voltage	I_{REF}	V_{DD} = V_{AREF} = 5.5 V V_{SS} = AV_{SS} = 0.0 V	–	0.6	1.0	mA
Non linearity error		V_{DD} = V_{AREF} = 4.5 to 5.0 V, V_{SS} = A_{VSS} = 0.0 V	–	–	± 1	LSB
Zero point error			–	–	± 1	
Full scale error			–	–	± 1	
Total error			–	–	± 2	

(V_{SS} = 0.0 V, 2.7 V ≦ V_{DD} < 4.5 V, Topr = – 30 to 70°C)

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Analog reference voltage	V_{AREF}		V_{DD} – 1.5	–	V_{DD}	V
Analog reference GND	A_{VSS}			V_{SS}		
Analog reference voltage range (Note 4)	$\triangle V_{AREF}$		2.5	–	–	
Analog input voltage	V_{AIN}		V_{SS}	–	V_{AREF}	
Power supply current of analog reference voltage	I_{REF}	V_{DD} = V_{AREF} = 4.5 V V_{SS} = A_{VSS} = 0.0 V	–	0.5	0.8	mA
Non linearity error		V_{DD} = A_{VDD} = 2.7 V to 4.5 V V_{SS} = A_{VSS} = 0.0 V	–	–	± 1	LSB
Zero point error			–	–	± 1	
Full scale error			–	–	± 1	
Total error			–	–	± 2	

Note 1: The total error includes all errors except a quantization error, and is defined as a maximum deviation from the ideal conversion line.
Note 2: Conversion time is different in recommended value by power supply voltage. About conversion time, please refer to "2.11.2 Register Configuration".
Note 3: Please use input voltage to AIN input Pin in limit of V_{AREF} - V_{SS}. When voltage of range outside is input, conversion value becomes unsettled and gives affect to other channel conversion value.
Note 4: Analog Reference Voltage Range: $\triangle V_{AREF} = V_{AREF} - V_{SS}$

AC Characteristics (V_{SS} = 0 V, V_{DD} = 4.5 to 5.5 V, Topr = – 30 to 70°C)

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Machine cycle time	tcy	NORMAL1/2 modes	0.25	–	4	μs
		IDLE1/2 modes				
		SLOW1/2 modes	117.6	–	133.3	
		SLEEP1/2 modes				
High level clock pulse width	twcH	For external clock operation (XIN input) fc = 16 MHz	–	31.25	–	ns
Low level clock pulse width	twcL					
High level clock pulse width	twcH	For external clock operation (XTIN input) fc = 32.768 kHz	–	15.26	–	μs
Low level clock pulse width	twcL					

(V_{SS} = 0 V, V_{DD} = 2.7 to 4.5 V, Topr = – 30 to 70°C)

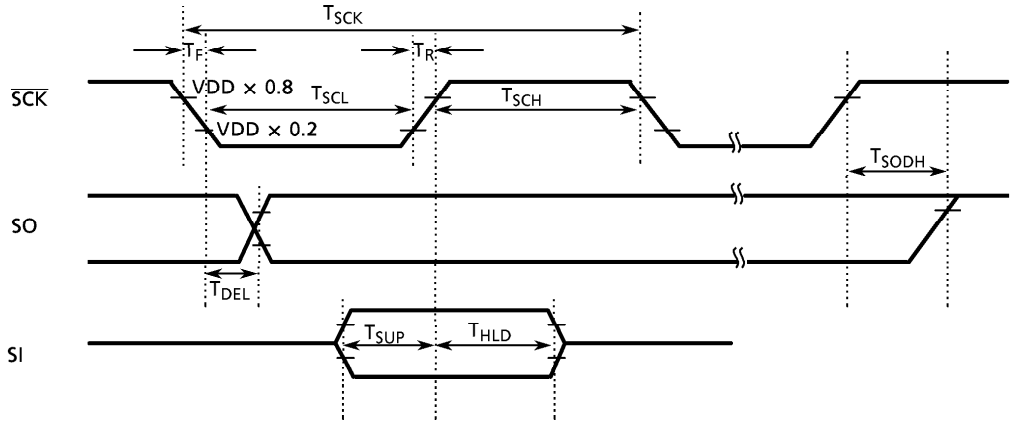
Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Machine cycle time	tcy	NORMAL1/2 modes	0.5	–	8	μs
		IDLE1/2 modes				
		SLOW1/2 modes	117.6	–	133.3	
		SLEEP1/2 modes				
High level clock pulse width	twcH	For external clock operation (XIN input) fc = 8 MHz	–	62.5	–	ns
Low level clock pulse width	twcL					
High level clock pulse width	twcH	For external clock operation (XTIN input) fc = 32.768 kHz	–	15.26	–	μs
Low level clock pulse width	twcL					

HSIO AC Characteristics (V_{SS} = 0 V, 2.7 V ≦ V_{DD} ≦ 5.5 V, Topr = – 30 to 70℃)

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
$\overline{SCK}$ output period (Internal clock)	T_{SCK1}	8 MHz < fc ≦ 16 MHz V_{DD} = 4.5 V to 5.5 V	16/fc	–	–	s
$\overline{SCK}$ output low width (Internal clock)	T_{SCL1}		8/fc – 100ns	–	–	
$\overline{SCK}$ output high width (Internal clock)	T_{SCH1}		8/fc – 100ns	–	–	
$\overline{SCK}$ output period (Internal clock)	T_{SCK2}	4 MHz < fc ≦ 8 MHz V_{DD} = 2.7 V to 5.5 V	8/fc	–	–	
$\overline{SCK}$ output low width (Internal clock)	T_{SCL2}		4/fc – 100ns	–	–	
$\overline{SCK}$ output high width (Internal clock)	T_{SCH2}		4/fc – 100ns	–	–	
$\overline{SCK}$ output period (Internal clock)	T_{SCK3}	fc ≦ 4 MHz V_{DD} = 2.7 V to 5.5 V	4/fc	–	–	
$\overline{SCK}$ output low width (Internal clock)	T_{SCL3}		2/fc – 100ns	–	–	
$\overline{SCK}$ output high width (Internal clock)	T_{SCH3}		2/fc – 100ns	–	–	
$\overline{SCK}$ input period (External clock)	T_{SCK4}	fc ≦ 8 MHz (V_{DD} = 2.7 V to 5.5 V) fc ≦ 16 MHz (V_{DD} = 4.4 V to 5.5 V)	800	–	–	ns
$\overline{SCK}$ input low width (External clock)	T_{SCL4}		300 (Note 1)	–	–	
$\overline{SCK}$ input low width (External clock)	T_{SCH4}		300 (Note 1)	–	–	
SI input setup time	T_{SUP}		150	–	–	ns
SI input hold time	T_{HLD}		150	–	–	
SO output delay time	T_{DEL}		–	–	200	
Rising time	T_R	V_{DD} = 3.0 V, CL = 50pF (Note 2)	–	–	100	
Falling time	T_F		–	–	100	
SO last bit hold time	T_{SODH}		16.5/fc	–	32.5/fc	

Note 1: T_{SCKL}, T_{SCKH} ≧ 2.5/fc (High-frequency clock mode), T_{SCKL}, T_{SCKH} ≧ 2.5/fc (Low-frequency clock mode)

Note 2: CL, external capacitance

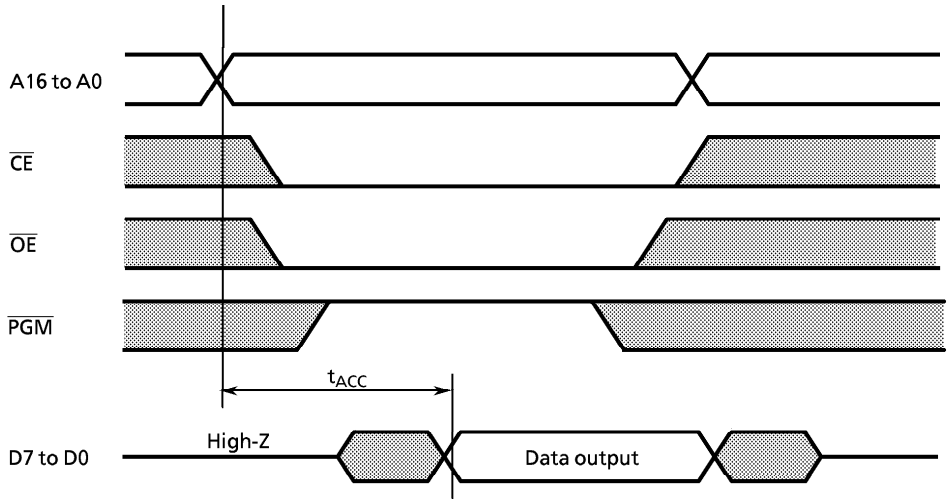


DC Characteristics, AC Characteristics (PROM mode) (V_{SS} = 0 V, Topr = 25 ± 5°C)

(1) Read operation in PROM mode

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
High level input voltage (TTL)	V_{IH3}		2.2	–	V_{DD}	V
Low leve input voltage (TTL)	V_{IL3}		0	–	0.8	
Power supply	V_{DD}		4.75	5.0	5.25	
Power supply of program	V_{PP}					
Address access time	t_{ACC}	V_{DD} = 5.0 ± 0.25 V	–	1.5tcyc + 300	–	ns

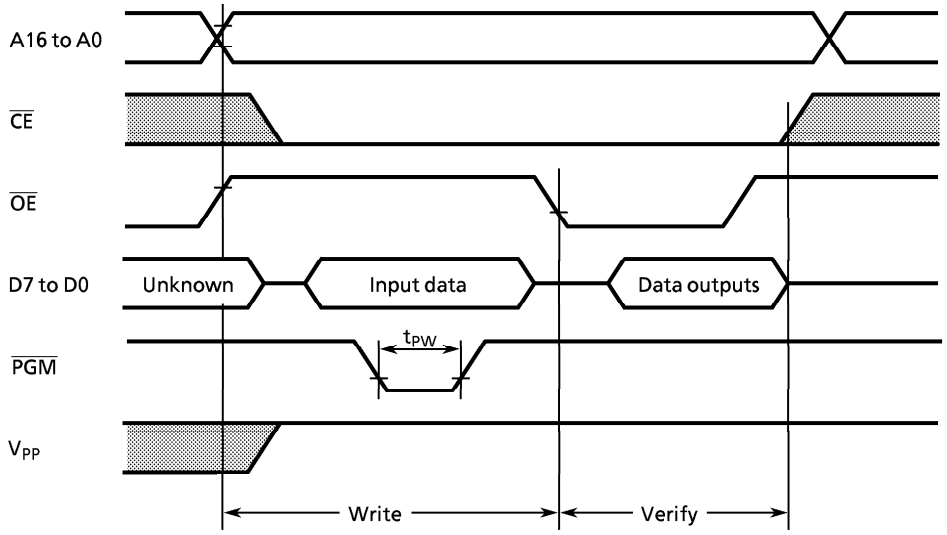
Note: tcyc = 400 ns at 10 MHz



(2) Program operation (High-speed) (Topr = 25 ± 5°C)

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
High level input voltage (TTL)	V_{IH3}		2.2	–	V_{DD}	V
Low leve input voltage (TTL)	V_{IL3}		0	–	0.8	
Power supply	V_{DD}		6.0	6.25	6.5	
Power supply of program	V_{PP}		12.5	12.75	13.0	
Pulse width of initializing program	t_{PW}	V_{DD} = 6.0 V	0.095	0.1	0.105	ms

High-speed program writing



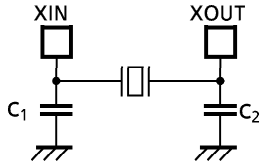
Note 1: The power supply of V_{PP} (12.75 V) must be set power-on at the same time or the later time for a power supply of V_{DD} and must be clear power-on at the same time or early time for a power supply of V_{DD}.

Note2 : The pulling up/down device on the condition of V_{PP} = 12.75 V ± 0.25 V causes a damage for the device. Do not pull up/down at programming.

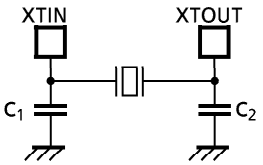
Note3 : Use the recommended adapter and mode.
Using other than the above condition may cause the trouble of the writting.

Recommended Oscillating Conditions (V_{SS} = 0 V, Topr = − 30 to 70°C)

Parameter	Oscillator	Oscillation Frequency	VDD	Recommended Oscillator	Recommended Constant	
					C_1	C_2
High-frequency oscillation	Ceramic resonator	16 MHz	4.5 V to 5.5 V	MURATA CSA16.00MXZ040	10 pF	10 pF
		8 MHz	2.7 V to 5.5 V	MURATA CSA8.00MTZ	30 pF	30 pF
				CST8.00MTW	30 pF (built-in)	30 pF (built-in)
		4.19 MHz	2.7 V to 5.5 V	MURATA CSA4.19MG	30 pF	30 pF
				CST4.19MGW	30 pF (built-in)	30 pF (built-in)
Low-frequency oscillation	Crystal oscillator	32.768 kHz	2.7 V to 5.5 V	SII VT-200	6 pF	6 pF



(1) High-frequency Oscillation



(2) Low-frequency Oscillation

Note 1: An electrical shield by metal shield plate on the surface of IC package is recommended in order to protect the device from the high electric field stress applied from CRT (Cathodic Ray Tube) for continuous reliable operation.

Note2: When using the device (oscillator) in places exposed to high electric fields such as cathode-ray tubes, we recommend electrically shielding the package in order to maintain normal operating condition.

Note 3: The product numbers and specifications of the resonators by Murata Manufacturing Co., Ltd. are subject to change. For up-to-date information, please refer to the following URL; http://www.murata.co.jp/search/index.html