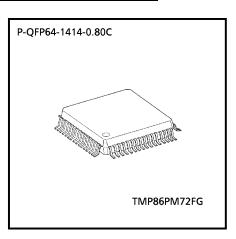
CMOS 8-Bit Microcontroller

## TMP86PM72FG

The TMP86PM72 is a OTP type MCU which includes 32-Kbyte one-time PROM. It is a pin compatible with a mask ROM product of the TMP86CH72/CM72. Writing the program to built-in PROM, the TMP86PM72 operates as the same way as the TMP86CH72/CM72. Using the Adapter socket, you can write and verify the data for the TMP86PM72 with a general-purpose PROM programmer same as TC571000D/AD.

	Product No.	OTP	RAM	Package	Adapter Socket
ſ	TMP86PM72FG	32 K × 8 bits	1 K × 8 bits	P-QFP64-1414-0.80C	BM11707



030619EBP1

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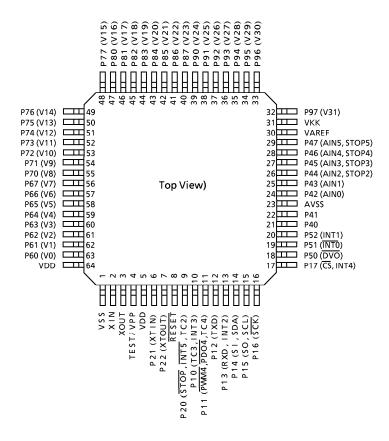


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#### Pin Assignments (Top View)

P-QFP64-1414-0.80C



Note: All VDD terminals are connected externally.

### **Pin Function**

The TMP86PM72 has MCU mode and PROM mode.

## (1) MCU mode

In the MCU mode, the TMP86PM72 is a pin compatible with the TMP86CH72/CM72 (Make sure to fix the TEST pin to low level).

# (2) PROM mode

Pin name (PROM mode)	Input/Output	Functions	Pin Name (MCU mode)			
A16 to A12			PD4 to PD0			
A11 to A8	Input	Input of Memory address for program	P53 to P50			
A7 to A0			P47 to P40			
D7 to D0	1/0	Input/Output of Memory data for program	P17 to P10			
CE		Chip enable	P95			
ŌĒ	Input	Output enable	P94			
PGM		Program control	P93			
VPP		+ 12.75 V/5 V (Power supply of program)	TEST			
VDD	Power supply	+ 6.25 V/5 V	VDD			
GND		0 V	VSS			
P51, P21		PROM mode setting pin. Fix to high.	·			
P50, P20, P22, AVSS, VAREF	1/0	PROM mode setting pin. Fix to low.				
RESET						
XIN	Input	6.16				
XOUT	Output	Self oscillation with resonator (10 MHz)				

#### Operation

This section describes the functions and basic operational blocks of TMP86PM72.

The TMP86PM72 has PROM in place of the mask ROM which is included in the TMP86CH72/CM72.

In addition, TMP86PM72 operates as the single clock mode when releasing reset.

When using the dual clock mode, oscillate a low-frequency clock by [SET (SYSCR2). XTEN] command at the beginning of program.

### 1. Operating Mode

The TMP86PM72 has MCU mode and PROM mode.

### 1.1 MCU Mode

The MCU mode is set by fixing the TEST/VPP pin to the low level. (TEST/VPP pin cannot be used open because it has no built-in pull-down resister).

### 1.1.1 Program Memory

The TMP86PM72 has a 32 Kbyte built-in one time PROM (addresses 8000<sub>H</sub> to FFFF<sub>H</sub> in the MCU mode, addresses 0000<sub>H</sub> to 7FFF<sub>H</sub> in the PROM mode).

When using TMP86PM72 for evaluation of mask ROM products, the program is written in the program storing area shown in Figure 1-1.

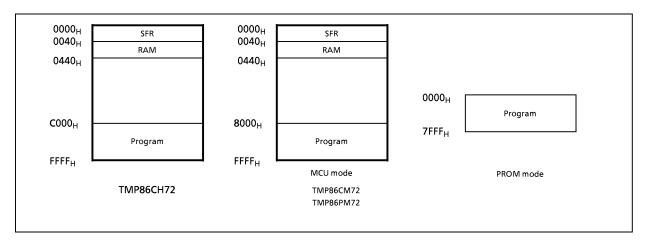


Figure 1-1. Program Memory Area

Note: The area that is not in use should be set data to FFH, or a general-purpose PROM programmer should be set only in the program memory area to access.

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#### **Electrical Characteristics**

Absolute Maximum Ratings  $(V_{SS} = 0 V)$ 

Parameter		Symbol	Pins	Rating	Unit
Supply voltage		$V_{DD}$		- 0.3 to 6.5	
Program voltage		V <sub>PP</sub>	TEST/V <sub>PP</sub>	- 0.3 to 13.0	
Input voltage		V <sub>IN</sub>		- 0.3 to V <sub>DD</sub> + 0.3	v
Output voltage		V <sub>OUT1</sub>		- 0.3 to V <sub>DD</sub> + 0.3	
		V <sub>OUT2</sub>	Source open drain ports	$V_{DD} - 41 \text{ to } V_{DD} + 0.3$	
		I <sub>OUT1</sub>	P0, P1, P2, P4 (P42~P47), P5 ports	5	
	IOL	I <sub>OUT2</sub>	P4 (P40, P41) port	40	
Output current (per 1 pin)		I <sub>OUT3</sub>	P0, P1, P4, P5 ports	- 3	
	ЮН	I <sub>OUT4</sub>	P6, P7 ports	- 30	mΑ
		I <sub>OUT5</sub>	P8, P9 ports	- 20	
Output current (total)		Σl <sub>OUT1</sub>	P0, P1, P2, P4, P5 ports	120	
Output current (total)		Σl <sub>OUT2</sub>	P6, P7, P8, P9 ports	- 120	
Power dissipation $[T_{opr} = 2]$	5℃]	PD		1200	mW
Soldering temperature (time)		Tsld		260 (10 μ)	
Storage temperature		Tstg		– 55 to 125	°c
Operating temperature		Topr		- 30 to 70	

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant.

Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

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**Recommended Operating Condition** 

 $(V_{SS} = 0 \text{ V, Topr} = -30 \text{ to } 70^{\circ}\text{C})$ 

Parameter	Symbol	Pins	C	Condition	Min	Max	Unit	
			6 46 8 411	NORMAL1/2 modes	4.5			
			fc = 16 MHz	IDLE0, 1/2 modes	4.5			
			f- ONALL-	NORMAL1/2 modes				
Supply voltage	V <sub>DD</sub>		fc = 8 MHz	IDLE0, 1/2 modes		5.5		
			fs = SLOW mode		2.7			
			32.768 kHz	SLEEP mode	]			
				STOP mode				
Output voltage	V <sub>OUT3</sub>	Source open drain ports			V <sub>DD</sub> - 38	V <sub>DD</sub>		
	V <sub>IH1</sub>	Except hysteresis input			V <sub>DD</sub> × 0.70			
Input high level	V <sub>IH2</sub>	Hysteresis input			$V_{DD} \times 0.75$	$V_{DD}$		
	V <sub>IH3</sub>	TTL input	$V_{DD} \le 4.5 V$		$V_{DD} \times 0.90$			
	V <sub>IL1</sub>	Except hysteresis input			0	$V_{DD} \times 0.30$		
Input low level	V <sub>IL2</sub>	Hysteresis input			0	$V_{DD} \times 0.25$		
	V <sub>IL3</sub>	TTL input	V	<sub>DD</sub> ≦ 4.5 V	$V_{DD} \times 0.10$	V <sub>DD</sub>		
			$V_{DD} = 2.7 \text{ to } 5.5 \text{ V}$		4.0	8.0		
Clock frequency	fc	XIN, XOUT	V <sub>DD</sub> = 4.5 to 5.5 V		1.0	16.0	MHz	
	fs	XTIN, XTOUT				34.0	kHz	

Note: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (Supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

DC Characteristics (1)

 $(V_{DD} = 5 V)$ 

[Condition]  $V_{DD} = 5.0 \text{ V} \pm 10\%$ ,  $V_{SS} = A_{VSS} = 0 \text{ V}$ , Topr =  $-30 \sim 70 ^{\circ}\text{C}$ 

 $(Typ.: V_{DD} = 5.0 \text{ V}, Topr = 25^{\circ}C, Vin = 5.0 \text{ V}/0 \text{ V})$ 

Parameter	Symbol	Pins	Condi	Condition		Тур.	Max	Unit
Hysteresis voltage	V <sub>HS</sub>	Hysteresis input			_	0.9	_	V
	I <sub>IN1</sub>	TEST						
Input current	I <sub>IN2</sub>	Sink open drain, Tri-st	$V_{DD} = 5.5  V,  V_{IN}$	= 5.5 V/0 V	_	_	± 2	μA
	I <sub>IN3</sub>	RESET, STOP						
Input resistance	R <sub>IN</sub>	RESET pull-up			100	220	450	
Pull-down resistance (Note 4)	R <sub>K</sub>	Source open drain, Tri-st	$V_{DD} = 5.5  V, V_{KK}$	= - 30 V	50	80	120	kΩ
Output leakage current	I <sub>LO1</sub>	Sink open drain, Tri-st	V <sub>DD</sub> = 5.5 V, V <sub>OL</sub>	<sub>JT</sub> = 5.5 V/0 V	-	_	± 2	μA
Output leakage current	I <sub>LO2</sub>	Source open drain	$V_{DD} = 5.5  V, V_{KK}$	$V_{DD} = 5.5 \text{ V}, V_{KK} = -32 \text{ V}$		-	± 2	μΑ
Output high voltage	V <sub>OH</sub>	Tri-st port	V <sub>DD</sub> = 4.5 V, I <sub>OH</sub>	= - 0.7 mA	4.1	İ	_	V
Output low voltage	V <sub>OL1</sub>	Except XOUT and (P40, P41) Port	$V_{DD} = 4.5 \text{ V}, I_{OL} = 1.6 \text{ mA}$		-	-	0.4	\ \ \
Output high current	I <sub>OH1</sub>	P6, P7	$V_{DD} = 4.5  V, V_{OH}$	<sub>I</sub> = 2.4 V	- 18	- 28	_	
Output high current	I <sub>OH2</sub>	P8, P9, PD	$V_{DD} = 4.5 \text{ V, } V_{OH}$	<sub>I</sub> = 2.4 V	- 9	- 14	_	
Output low current	I <sub>OL</sub>	High current port (P40, P41)	$V_{DD} = 4.5  V, V_{OL}$	= 1.0 V	-	20	_	
Supply current in			fc = 16.0 MHz fs = 32.768 kHz		_	12	18	
NORMAL1/2 modes			fc = 8.0 MHz fs = 32.768 kHz	AD converter	_	6	9	mA
Supply current in			fc = 16.0 MHz fs = 32.768 kHz	disable (IREF off)	_	6	9	
IDLE0/1/2 modes			fc = 8.0 MHz fs = 32.768 kHz		_	3	4.5	
Supply current in	I <sub>DD</sub>		fc = 16.0 MHz fs = 32.768 kHz	AD	_	13	19	
NORMAL1/2 modes			fc = 8.0 MHz fs = 32.768 kHz	enable	_	7	10	
Supply current in	in		Topr = to 50°C AD		_		5	
STOP mode			Topr = to 70°C	disable	-	0.5	10	μΑ

Note 1: Typical values show those at Topr =  $25^{\circ}$ C,  $V_{DD} = 5 V$ .

Note 2: Input current ( $I_{IN1}$ ,  $I_{IN3}$ ): The current through pull-up or pull-down resistor is not included.

Note 3: IDD does not include IREF current.

Note 4:  $Topr = -10^{\circ}C$  to  $70^{\circ}C$ 

DC Characteristics (2)

 $(V_{DD} = 3 V)$ 

[Condition]  $V_{DD} = 3.0 \text{ V} \pm 10\%$ ,  $V_{SS} = A_{VSS} = 0 \text{ V}$ , Topr =  $-30 \text{ to } 70^{\circ}\text{C}$ 

 $(Typ.: V_{DD} = 3.0 \text{ V}, Topr = 25^{\circ}C, Vin = 3.0 \text{ V}/0 \text{ V})$ 

Parameter	Symbol	Pins	Condi	tion	Min	Тур.	Max	Unit
Hysteresis voltage	V <sub>HS</sub>	Hysteresis input			-	0.4	-	V
	I <sub>IN1</sub>	TEST						
Input current	I <sub>IN2</sub>	Sink open drain, Tri-st	$V_{DD} = 3.3 \text{ V, } V_{IN}$	= 3.3 V/0 V	_	-	± 2	μA
	I <sub>IN3</sub>	RESET, STOP						
Input resistance	R <sub>IN</sub>	RESET pull-up			100	220	450	
Pull-down resistance	R <sub>K</sub>	Source open drain, tri-st	$V_{DD} = 3.3 \text{ V, } V_{KK}$	= - 30 V	45	75	115	kΩ
Output lealings sument	$I_{LO1}$ Sink open drain, tri-st $V_{DD} = 3.3 \text{ V}, V_{OUT} = 3.3 \text{ V/O V}$		<sub>IT</sub> = 3.3 V/0 V	-	-	± 2		
Output leakage current	I <sub>LO2</sub>	Source open drain	$V_{DD} = 3.3 \text{ V}, V_{KK}$	= -32 V	_	-	± 2	μA
Output high voltage	V <sub>OH</sub>	Tri-st port	$V_{DD} = 2.7 \text{ V}, I_{OH} = -0.6 \text{ mA}$		2.3	-	-	l
Output low voltage	V <sub>OL1</sub>	Except XOUT and (P40, P41) Port	$V_{DD} = 2.7 \text{ V, } I_{OL} = 0.9 \text{ mA}$		-	-	0.4	
	I <sub>OH1</sub>	P6, P7	$V_{DD} = 2.7  V, V_{OH}$	<sub>I</sub> = 1.5 V	- 5.5	-8	-	
Output high current	I <sub>OH2</sub>	P8, P9, PD	$V_{DD} = 2.7 \text{ V}, V_{OH} = 1.5 \text{ V}$		- 3	- 4.5	_	1
Output low current	I <sub>OL</sub>	High current port (P40, P41) port	$V_{DD} = 2.7  V, V_{OL}$	= 1.0 V	_	6	_	1
Supply current in NORMAL1/2 modes			fc = 8.0 MHz fs = 32.768 kHz	AD converter	_	3	4.5	mA
Supply current in IDLE0/1/2 modes			fc = 8.0 MHz fs = 32.768 kHz	disable (IREF off)	_	2	2.5	
Supply current in NORMAL1/2 modes	1		fc = 8.0 MHz fs = 32.768 kHz	AD converter enable	_	3.5	5	
Supply current in SLOW1 mode	- I <sub>DD</sub>		6 22 750 1 11	AD	_	30	60	
Supply current in SLEEPO, 1 mode			fs = 32.768 kHz	converter disable	_	15	30	μA
Supply current in			Topr = to 50°C	1		0.5	5	1
STOP mode			Topr = to 70°C	1	-	0.5	10	1

Note 1: Typical values show those at Topr =  $25^{\circ}$ C,  $V_{DD} = 3 V$ .

Note 2: Input current ( $I_{IN1}$ ,  $I_{IN3}$ ): The current through pull-up or pull-down resistor is not included.

Note 3: IDD does not include IREF current.

Note 4: The supply currents of SLOW2 and SLEEP2 modes are equivalent IDLE0, 1, 2.

# **AD Conversion Characteristics**

# (VSS = 0.0 V, 4.5 V $\leq$ VDD $\leq$ 5.5 V, Topr = - 30 to 70°C)

Parameter	Symbol	Condition	Min	Тур.	Max	Unit
Analog reference voltage	$V_{AREF}$		V <sub>DD</sub> – 1.5	-	$V_{DD}$	
Analog reference GND	A <sub>VSS</sub>			V <sub>SS</sub>		1
Analog reference voltage range (Note 4)	$\triangle v_{AREF}$		3.0	-	_	V
Analog input voltage	V <sub>AIN</sub>		V <sub>SS</sub>	-	V <sub>AREF</sub>	1
Power supply current of analog reference voltage	I <sub>REF</sub>	$V_{DD} = V_{AREF} = 5.5 V$ $V_{SS} = AV_{SS} = 0.0 V$	_	0.6	1.0	mA
Non linearity error			-	-	± 1	
Zero point error		$V_{DD} = V_{AREF} = 4.5 \text{ to } 5.0 \text{ V},$	-	-	± 1	LSB
Full scale error		$V_{SS} = A_{VSS} = 0.0 \text{ V}$	-	-	± 1	LJB
Total error			_	_	± 2	

# (V<sub>SS</sub> = 0.0 V, 2.7 V $\leq$ V<sub>DD</sub> < 4.5 V, Topr = - 30 to 70°C)

Parameter	Symbol	Condition	Min	Тур.	Max	Unit
Analog reference voltage	$V_{AREF}$		V <sub>DD</sub> – 1.5	-	$V_{DD}$	
Analog reference GND	A <sub>VSS</sub>			V <sub>SS</sub>		1
Analog reference voltage range (Note 4)	$\triangle V_{AREF}$		2.5	-	_	V
Analog input voltage	V <sub>AIN</sub>		V <sub>SS</sub>	-	V <sub>AREF</sub>	
Power supply current of analog reference voltage	I <sub>REF</sub>	$V_{DD} = V_{AREF} = 4.5 V$ $V_{SS} = A_{VSS} = 0.0 V$	-	0.5	0.8	mA
Non linearity error			-	-	± 1	
Zero point error		$V_{DD} = A_{VDD} = 2.7 \text{ V to } 4.5 \text{ V}$	-	-	± 1	LSB
Full scale error		$V_{SS} = A_{VSS} = 0.0 V$	-	-	± 1	
Total error			_	-	± 2	

- Note 1: The total error includes all errors except a quantization error, and is defined as a maximum deviation from the ideal
- Note 2: Conversion time is different in recommended value by power supply voltage.
- About conversion time, please refer to "2.11.2 Register Configuration".

  Note 3: Please use input voltage to AIN input Pin in limit of V<sub>AREF</sub> V<sub>SS</sub>.

  When voltage of range outside is input, conversion value becomes unsettled and gives affect to other channel conversion value.

  Note 4: Analog Reference Voltage Range:  $\triangle V_{AREF} = V_{AREF} - V_{SS}$

# **AC Characteristics**

 $(V_{SS} = 0 \text{ V}, V_{DD} = 4.5 \text{ to } 5.5 \text{ V}, Topr = -30 \text{ to } 70^{\circ}\text{C})$ 

Parameter	Symbol Condition		Min	Тур.	Max	Unit
	tcy	NORMAL1/2 modes			_	- μ <b>s</b>
Machine cycle time		IDLE1/2 modes	0.25	_	4	
Machine cycle time		SLOW1/2 modes	447.6	_	133.3	
		SLEEP1/2 modes	117.6			
High level clock pulse width	twcH	For external clock operation (XIN input)			_	ns
Low level clock pulse width	twcL	fc = 16 MHz	_	31.25		
High level clock pulse width	twcH	For external clock operation (XTIN input)		15.26	-	μS
Low level clock pulse width	twcL	fc = 32.768 kHz	_			

$$(V_{SS} = 0 \text{ V}, V_{DD} = 2.7 \text{ to } 4.5 \text{ V}, Topr = -30 \text{ to } 70^{\circ}\text{C})$$

Parameter	Symbol	Condition		Тур.	Max	Unit
	tcy	NORMAL1/2 modes				
Machine cycle time		IDLE1/2 modes	0.5	_	8	
viacnine cycle time		SLOW1/2 modes	117.6	_	133.3	μS
		SLEEP1/2 modes	117.6			
High level clock pulse width	twcH	For external clock operation (XIN input)		62.5	-	ns
Low level clock pulse width	twcL	fc = 8 MHz	_			115
High level clock pulse width	twcH	For external clock operation (XTIN input)		15.26	-	,,c
Low level clock pulse width	twcL	fc = 32.768 kHz	_			μS

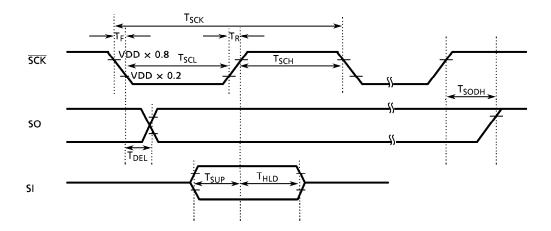
**HSIO AC Characteristics** 

(Vss = 0 V, 2.7 V  $\leqq$  V\_DD  $\leqq$  5.5 V, Topr = – 30 to 70  $^{\circ}\text{C}$  )

Parameter	Symbol	Conditions	Min	Тур.	Max	Unit
SCK output period (Internal clock)	T <sub>SCK1</sub>		16/fc	-	-	
SCK output low width (Internal clock)	T <sub>SCL1</sub>	$8 \text{ MHz} < \text{fc} \le 16 \text{ MHz}$ $V_{DD} = 4.5 \text{ V to } 5.5 \text{ V}$	8/fc - 100ns	-	_	]
SCK output high width (Internal clock)	T <sub>SCH1</sub>	- VDD = 4.5 V to 5.5 V	8/fc - 100ns	-	-	
SCK output period (Internal clock)	T <sub>SCK2</sub>		8/fc	-	-	
SCK output low width (Internal clock)	T <sub>SCL2</sub>	4  MHz < fc ≤ $8  MHzV_{DD} = 2.7 \text{ V to } 5.5 \text{ V}$	4/fc - 100ns	-	-	s
SCK output high width (Internal clock)	T <sub>SCH2</sub>	VDD = 2.7 V to 5.5 V	4/fc – 100ns	-	-	
SCK output period (Internal clock)	T <sub>SCK3</sub>		4/fc	-	-	
SCK output low width (Internal clock)	T <sub>SCL3</sub>	$fc \le 4 \text{ MHz}$ $V_{DD} = 2.7 \text{ V to } 5.5 \text{ V}$	2/fc - 100ns	-	-	
SCK output high width (Internal clock)	T <sub>SCH3</sub>	- VDD - 2.7 V to 3.5 V	2/fc - 100ns	=	-	
SCK input period (External clock)	T <sub>SCK4</sub>	fc ≦ 8 MHz	800	-	-	
SCK input low width (External clock)	T <sub>SCL4</sub>	$(V_{DD} = 2.7 \text{ V to } 5.5 \text{ V})$ fc $\leq 16 \text{ MHz}$	300 (Note 1)	-	-	ns
SCK input low width (External clock)	T <sub>SCH4</sub>	$(V_{DD} = 4.4 \text{ V to } 5.5 \text{ V})$	300 (Note 1)	_	-	
SI input setup time	T <sub>SUP</sub>		150	-	-	
SI input hold time	T <sub>HLD</sub>		150	_	-	1
SO output delay time	T <sub>DEL</sub>		-	_	200	1
Rising time	T <sub>R</sub>	V <sub>DD</sub> = 3.0 V, CL = 50pF	-	_	100	ns
Falling time	T <sub>F</sub>	(Note 2)	-	_	100	1
SO last bit hold time	T <sub>SODH</sub>		16.5/fc	-	32.5/fc	

Note 1:  $T_{SCKL}$ ,  $T_{SCKH} \ge 2.5/fc$  (High-frequency clock mode),  $T_{SCKL}$ ,  $T_{SCKH} \ge 2.5/fc$  (Low-frequency clock mode)

Note 2: CL, external capacitance



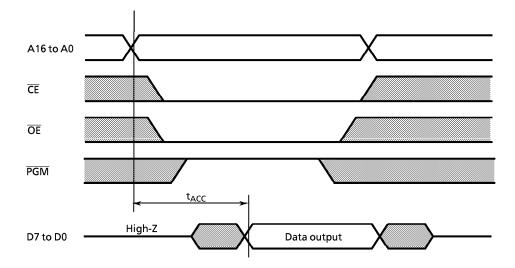
DC Characteristics, AC Characteristics (PROM mode)

 $(V_{SS} = 0 \text{ V, Topr} = 25 \pm 5^{\circ}\text{C})$ 

# (1) Read operation in PROM mode

Parameter	Symbol	Conditions	Min	Тур.	Max	Unit
High level input voltage (TTL)	V <sub>IH3</sub>		2.2	-	V <sub>DD</sub>	
Low leve input voltage (TTL)	V <sub>IL3</sub>		0	_	0.8	,,
Power supply	V <sub>DD</sub>		4.75	5.0	F 2F	V
Power supply of program	$V_{PP}$		4.75	5.0	5.25	
Address access time	t <sub>ACC</sub>	V <sub>DD</sub> = 5.0 ± 0.25 V	_	1.5tcyc + 300	_	ns

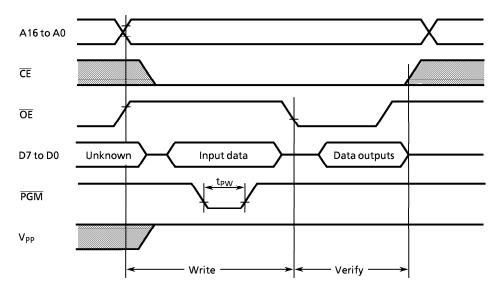
Note: tcyc = 400 ns at 10 MHz



## (2) Program operation (High-speed) (Topr = $25 \pm 5^{\circ}$ C)

Parameter	Symbol	Conditions	Min	Тур.	Max	Unit
High level input voltage (TTL)	V <sub>IH3</sub>		2.2	-	$V_{DD}$	
Low leve input voltage (TTL)	V <sub>IL3</sub>		0	-	0.8	.,
Power supply	$V_{DD}$		6.0	6.25	6.5	V
Power supply of program	V <sub>PP</sub>		12.5	12.75	13.0	
Pulse width of initializing program	t <sub>PW</sub>	V <sub>DD</sub> = 6.0 V	0.095	0.1	0.105	ms

## High-speed program writing



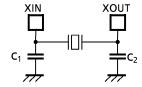
- Note 1: The power supply of  $V_{PP}$  (12.75 V) must be set power-on at the same time or the later time for a power supply of  $V_{DD}$  and must be clear power-on at the same time or early time for a power supply of  $V_{DD}$ .
- Note2: The pulling up/down device on the condition of  $V_{PP} = 12.75 \text{ V} \pm 0.25 \text{ V}$  causes a damage for the device. Do not pull up/down at programming.
- Note3: Use the recommended adapter and mode.

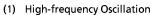
  Using other than the above condition may cause the trouble of the writting.

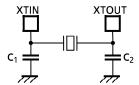
**Recommended Oscillating Conditions** 

$$(V_{SS} = 0 \text{ V}, \text{ Topr} = -30 \text{ to } 70^{\circ}\text{C})$$

Dorometer	Ossillatan	Oscillation	\/DD			Recommended Constant	
Parameter	Oscillator	Frequency VDD		Recommended Oscillator		C <sub>1</sub>	C <sub>2</sub>
High-frequency oscillation	Ceramic resonator	16 MHz	4.5 V to 5.5 V	MURATA CSA16.00MXZ040		10 pF	10 pF
		8 MHz	2.7 V to 5.5 V	MURATA	CSA8.00MTZ CST8.00MTW	30 pF 30 pF (built-in)	30 pF 30 pF (built-in)
		4.19 MHz	2.7 V to 5.5 V	MURATA	CSA4.19MG CST4.19MGW	30 pF 30 pF (built-in)	30 pF 30 pF (built-in)
Low-frequency oscillation	Crystal oscillator	32.768 kHz	2.7 V to 5.5 V	SII	VT-200	6 pF	6 pF







(2) Low-frequency Oscillation

- Note 1: An electrical shield by metal shield plate on the surface of IC package is recommended in order to protect the device from the high electric field stress applied from CRT (Cathodic Ray Tube) for continuous reliable operation.
- Note2: When using the device (oscillator) in places exposed to high electric fields such as cathode-ray tubes, we recommend electrically shielding the package in order to maintain normal operating condition.
- Note 3: The product numbers and specifications of the resonators by Murata Manufacturing Co., Ltd. are subject to change.

  For up-to-date information, please refer to the following URL;

  http://www.murata.co.jp/search/index.html