Low Distortion, Wide Bandwidth Voltage Feedback Clamp Amp

Enhanced Product

AD8037-EP

FEATURES

Superb clamping characteristics
- **3 mV clamp error**
- **1.5 ns overdrive recovery**
- **Minimized nonlinear clamping region**
- **240 MHz clamp input bandwidth**
- **±3.9 V clamp input range**

Wide bandwidth
- **Small signal: 270 MHz**
- **Large signal (4 V p-p): 190 MHz**

Good dc characteristics
- **2 mV offset**
- **10 µV/°C drift**

Ultralow distortion, low noise
- **−72 dBc typical at 20 MHz**
- **4.5 nV/√Hz input voltage noise**

High speed
- **Slew rate 1500 V/µs**
- **Settling 10 ns to 0.1%, 16 ns to 0.01%**

±3 V to ±5 V supply operation

ENHANCED PRODUCT FEATURES

Supports defense and aerospace applications (AQEC standard)
Extended industrial temperature range: −55°C to +105°C
Controlled manufacturing baseline
One assembly/test site
One fabrication site
Product change notification
Qualification data available on request

APPLICATIONS

ADC buffer
IF/RF signal processing
High quality imaging
Broadcast video systems
Video amplifier
Full wave rectifier

FUNCTIONAL BLOCK DIAGRAM

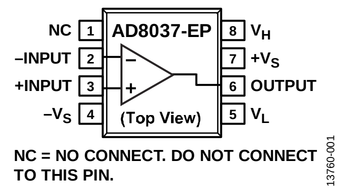

Figure 1.

GENERAL DESCRIPTION

The AD8037-EP is a wide bandwidth, low distortion clamping amplifier. The AD8037-EP is stable at a gain of two or greater. This device allows the designer to specify a high (V_{CH}) and low (V_{CL}) output clamp voltage. The output signal clamps at these specified levels. Utilizing a unique patent pending CLAMPING™ input clamp architecture, the AD8037-EP offers a 10× improvement in clamp performance compared to traditional output clamping devices. In particular, clamp error is typically 3 mV or less and distortion in the clamp region is minimized. This product can be used as a classical op amp or clamp amplifier.

The AD8037-EP, which utilizes a voltage feedback architecture, meets the requirement of many applications which previously depended on current feedback amplifiers. The AD8037-EP exhibits an exceptionally fast and accurate pulse response (16 ns to 0.01%), extremely wide small-signal and large-signal bandwidths and ultralow distortion. The AD8037-EP recovers from 2× clamp overdrive within 1.5 ns. These characteristics position the AD8037-EP ideally for driving as well as buffering flash and high resolution ADCs.

In addition to traditional output clamp amplifier applications, the input clamp architecture supports the clamp levels as additional input to the amplifier. As such, in addition to static dc clamp levels, signals with speeds up to 240 MHz can be applied to the clamp pins. The clamp values can be set to any value within the output voltage range provided that V_H is greater than V_L. Due to these clamp characteristics, the AD8037-EP can be used in nontraditional applications such as a full wave rectifier, a pulse generator, or an amplitude modulator. These novel applications are only examples of some of the diverse applications which can be designed with input clamps.

Additional application and technical information can be found in the AD8037 data sheet.

Rev. 0 **Document Feedback**

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REVISION HISTORY

6/2016—Revision 0: Initial Version

SPECIFICATIONS

V_S = ±5 V, R_L = 100 Ω, gain = +2, V_H, V_L open unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
Bandwidth (–3 dB)					
Small Signal	V_{OUT} ≤ 0.4 V p-p	200	270		MHz
Large Signal[1]	V_{OUT} = 3.5 V p-p	160	190		MHz
Bandwidth for 0.1 dB Flatness	V_{OUT} ≤ 0.4 V p-p, R_F = 274 Ω		130		MHz
Slew Rate, Average ±	V_{OUT} = 4 V step, 10% to 90%	1100	1500		V/μs
Rise/Fall Time	V_{OUT} = 0.5 V step, 10% to 90%		1.2		ns
	V_{OUT} = 4 V step, 10% to 90%		2.2		ns
Setting Time					
To 0.1%	V_{OUT} = 2 V step		10		ns
To 0.01%	V_{OUT} = 2 V step		16		ns
NOISE/HARMONIC PERFORMANCE					
Second Harmonic Distortion	2 V p-p, 20 MHz, R_L = 100 Ω		−52	−45	dBc
	R_L = 500 Ω		−72	−65	dBc
Third Harmonic Distortion	2 V p-p, 20 MHz, R_L = 100 Ω		−70	−63	dBc
	R_L = 500 Ω		−80	−73	dBc
Third-Order Intercept	25 MHz		41		dBm
Noise Figure	R_S = 50 Ω		14		dB
Input Voltage Noise	1 MHz to 200 MHz		4.5		nV/√Hz
Input Current Noise	1 MHz to 200 MHz		2.1		pA/√Hz
Average Equivalent Integrated Input Noise Voltage	0.1 MHz to 200 MHz		60		μV rms
Differential Gain Error (3.58 MHz)	R_L = 150 Ω		0.02	0.04	%
Differential Phase Error (3.58 MHz)	R_L = 150 Ω		0.02	0.04	Degrees
Phase Nonlinearity	DC to 100 MHz		1.1		Degrees
CLAMP PERFORMANCE					
Clamp Voltage Range[1]	V_{CH} or V_{CL}	±3.3	±3.9		V
Clamp Accuracy	2× overdrive, V_{CH} = 2 V, V_{CL} = −2 V		±3	±10	mV
	T_{MIN} to T_{MAX}			±20	mV
Clamp Nonlinearity Range[2]			100		mV
Clamp Input Bias Current (V_H or V_L)	V_H, V_L = ±0.5 V		±50	±70	μA
	T_{MIN} to T_{MAX}			±90	μA
Clamp Input Bandwidth (–3 dB)	V_{CH} or V_{CL} = 2 V p-p	180	270		MHz
Clamp Overshoot	2× overdrive, V_{CH} or V_{CL} = 2 V p-p		1	5	%
Overdrive Recovery	2× overdrive		1.3		ns
DC PERFORMANCE[3], R_L = 150 Ω					
Input Offset Voltage[4]			2	7	mV
	T_{MIN} to T_{MAX}			10	mV
Offset Voltage Drift			±10		μV/°C
Input Bias Current			3	9	μA
	T_{MIN} to T_{MAX}			15	μA
Input Offset Current			0.1	3	μA
	T_{MIN} to T_{MAX}			5	μA
Common-Mode Rejection Ratio	V_{CM} = ±2 V	70	90		dB
Open-Loop Gain	V_{OUT} = ±2.5 V	54	60		dB
	T_{MIN} to T_{MAX}	46			dB

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS					
Input Resistance			500		kΩ
Input Capacitance			1.2		pF
Input Common-Mode Voltage Range			±2.5		V
OUTPUT CHARACTERISTICS					
Output Voltage Range, R_L = 150 Ω		±3.2	±3.9		V
Output Current			70		mA
Output Resistance			0.3		Ω
Short Circuit Current			240		mA
POWER SUPPLY					
Operating Range		±3.0	±5.0	±6.0	V
Quiescent Current			18.5	19.5	mA
	T_{MIN} to T_{MAX}			24	mA
Power Supply Rejection Ratio	T_{MIN} to T_{MAX}	56	66		dB

[1] See the Absolute Maximum Ratings section.
[2] Nonlinearity is defined as the voltage delta between the set input clamp voltage (V_H or V_L) and the voltage at which V_{OUT} starts deviating from V_{IN}.
[3] Measured at A_V = 50.
[4] Measured with respect to the inverting input

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage	12.6 V
Power Dissipation	See Figure 2
Voltage Swing × Bandwidth Product	350 V-MHz
Common-Mode Input Voltage	$\pm V_S$
$\lvert V_H - V_{IN}\rvert$	≤6.3 V
$\lvert V_L - V_{IN}\rvert$	≤6.3 V
Differential Input Voltage	±1.2 V
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−55°C to +105°C
Lead Temperature (Soldering, 10 sec)	300°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

Table 3. Thermal Resistance

Package Type	θ_{JA}	Unit
R-8	155	°C/W

MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated by these devices is limited by the associated rise in junction temperature. The maximum safe junction temperature for plastic encapsulated devices is determined by the glass transition temperature of the plastic, approximately 150°C. Exceeding this limit temporarily may cause a shift in parametric performance due to a change in the stresses exerted on the die by the package. Exceeding a junction temperature of 175°C for an extended period can result in device failure.

Although the AD8037-EP is internally short-circuit protected, this may not be sufficient to guarantee that the maximum junction temperature (150°C) is not exceeded under all conditions. To ensure proper operation, it is necessary to observe the maximum power derating curves.

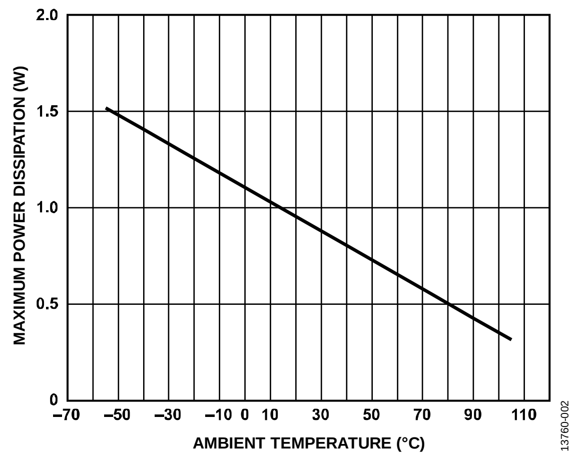

Figure 2. Maximum Power Dissipation vs. Ambient Temperature

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

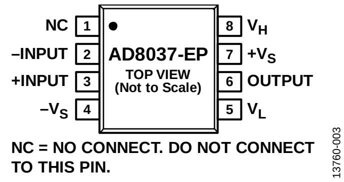

Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	NC	No Connect
2	−INPUT	Inverting Input
3	+INPUT	Noninverting Input
4	$-V_S$	Negative Supply
5	V_L	Low Clamping Voltage
6	OUTPUT	Output
7	$+V_S$	Positive Supply
8	V_H	High Clamping Voltage

TYPICAL PERFORMANCE CHARACTERISTICS

$V_S = \pm 5$ V, $R_L = 150\ \Omega$, $T_A = -55°C$ to $+105°C$, unless otherwise noted.

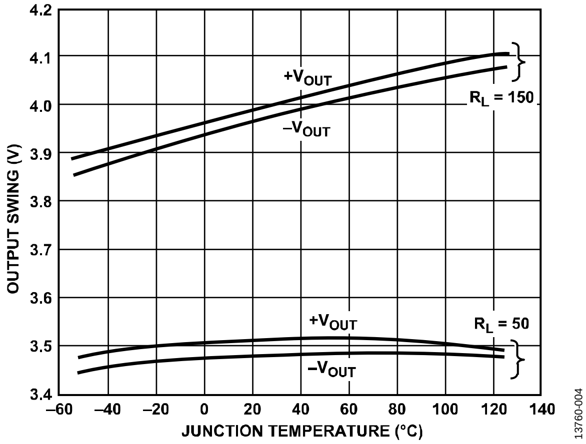

Figure 4. Output Swing vs. Junction Temperature

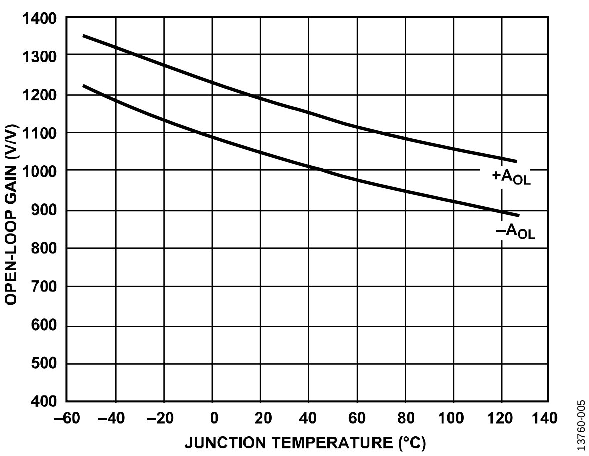

Figure 5. Open-Loop Gain vs. Junction Temperature

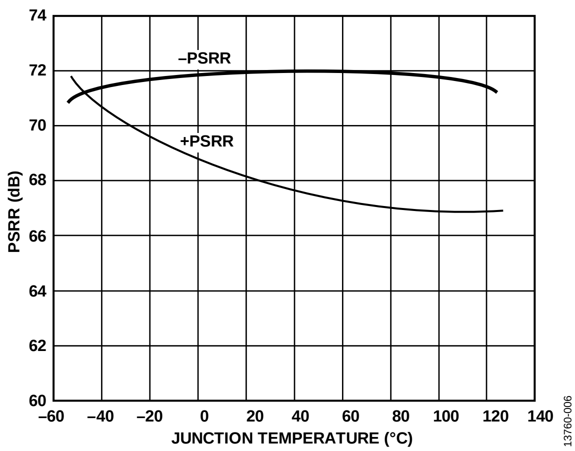

Figure 6. PSRR vs. Junction Temperature

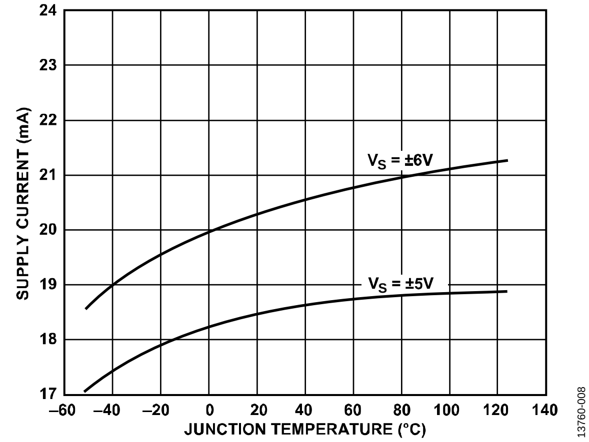

Figure 7. Supply Current vs. Junction Temperature

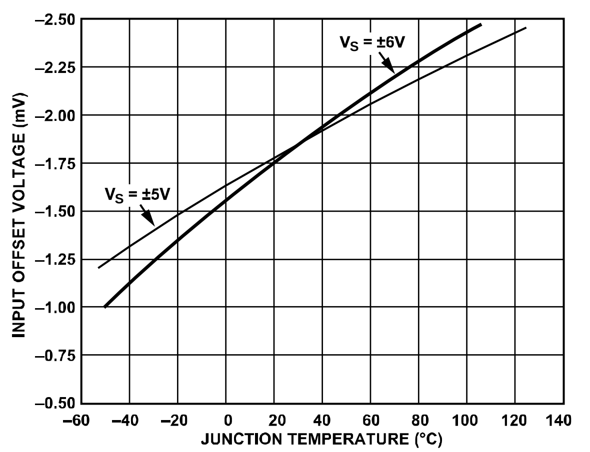

Figure 8. Input Offset Voltage vs. Junction Temperature

OUTLINE DIMENSIONS

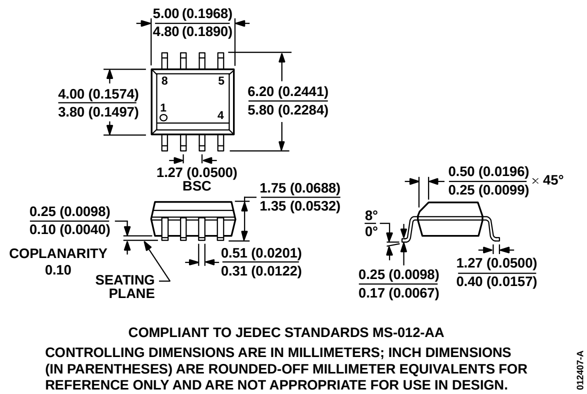

Figure 9. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD8037SRZ-EP	−55°C to +105°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8
AD8037SRZ-EP-R7	−55°C to +105°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8

[1] Z = RoHS Compliant Part.