

# Precision Adjustable Shunt Regulator

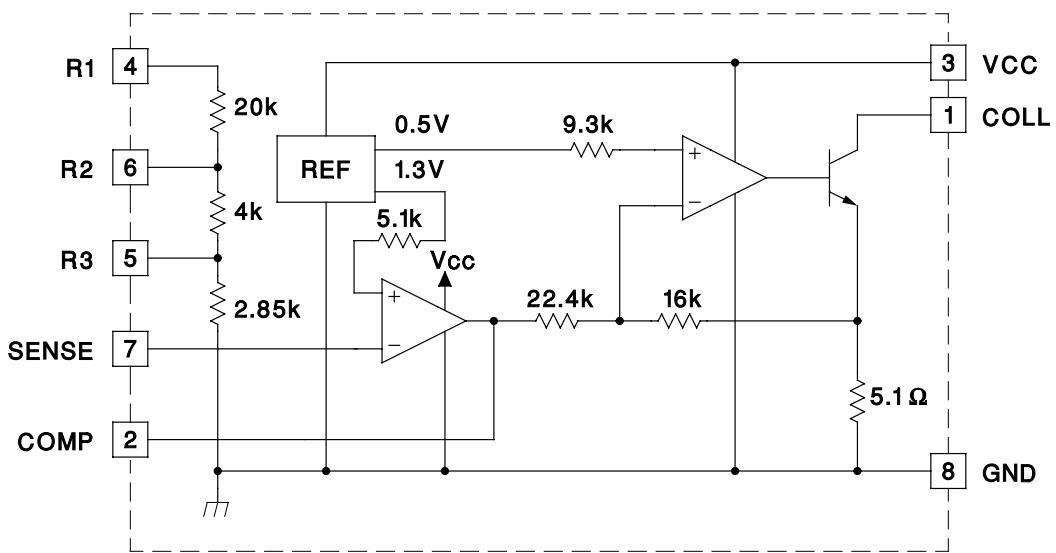
## FEATURES

- Multiple On-Chip Programmable Reference Voltages
- 0.4% Initial Accuracy
- 0.7% Overall Reference Tolerance
- 2.2V to 36.0V Operating Supply Voltage and User Programmable Reference
- 36.0V Operating Supply Voltage
- Reference Accuracy Maintained For Entire Range of Supply Voltage
- Superior Accuracy and Easier Compensation for Optoisolator Application
- Improved Architecture Provides a Known Linear Transconductance with a +5% Typical Tolerance

## DESCRIPTION

The UC39431 is an adjustable shunt voltage regulator with 100mA sink capability. The architecture, comprised of an error amplifier and transconductance amplifier, gives the user separate control of the small signal error voltage frequency response along with a fixed linear transconductance. A minimum 3MHz gain bandwidth product for both the error and transconductance amplifiers assures fast response. In addition to external programming, the IC has three internal resistors that can be connected in six different configurations to provide regulated voltages of 2.82V, 3.12V, 5.1V, 7.8V, 10.42V, and 12.24V. A sister device (UC39432) provides access to the non-inverting error amplifier input and reference, while eliminating the three internal resistors.

## BLOCK DIAGRAM



UC19431  
UC29431  
UC39431  
UC39431B

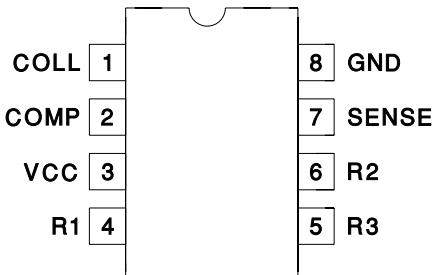
## ABSOLUTE MAXIMUM RATINGS

Supply Voltage: V	36V
Regulated Output: V	36V
Internal Resistors: R1, R2, R3	13V
E/A Input: SENSE	6V
E/A Compensation: COMP	6V
Output Sink Current: I	140mA
Power Dissipation at $T_A \leq 25^\circ\text{C}$ (DIL-8)	1W
Derate 8mW/ $^\circ\text{C}$ for $T_A > 25^\circ\text{C}$	
Storage Temperature Range	$-65^\circ\text{C}$ to $+150^\circ\text{C}$
Junction Temperature	$-55^\circ\text{C}$ to $+150^\circ\text{C}$
Lead Temperature (Soldering, 10 sec.)	$+300^\circ\text{C}$

*Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.*

## CONNECTION DIAGRAM

DIL-8, SOIC-8 (Top View)  
N or J, D Package



**ELECTRICAL CHARACTERISTICS:** Unless otherwise stated, these specifications apply for  $T_A = -55^\circ\text{C}$  to  $+125^\circ\text{C}$  and  $\text{COLL Output} = 2.4\text{V to } 36.0\text{V}$  for the UC19431,  $T_A = -25^\circ\text{C}$  to  $+85^\circ\text{C}$  and  $\text{COLL Output} = 2.3\text{V to } 36.0\text{V}$  for the UC29431, and  $T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$  and  $\text{COLL Output} = 2.3\text{V to } 36.0\text{V}$  for the UC39431/B,  $\text{VCC} = 15\text{V}$ ,  $\text{ICOLL} = 10\text{mA}$ ,  $T_A = T_J$ .

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Reference Voltage Tolerance	$T_A = 25^\circ\text{C}$	19431*	1.295	1.3	1.305
		39431B	1.29	1.3	1.31
Reference Temperature Tolerance	$\text{V}_{\text{COLL}} = 5.0$	19431*	1.291	1.3	1.309
		39431B	1.286	1.3	1.314
Reference Line Regulation	$\text{VCC} = 2.2\text{V to } 36.0\text{V}$ , $\text{V}_{\text{COLL}} = 5\text{V}$	19431*		10	38
Reference Load Regulation		39431B		10	57
$\text{ICOLL} = 10\text{mA to } 50\text{mA}$ , $\text{V}_{\text{COLL}} = 5\text{V}$	19431*		10	mV	
	39431B		10	mV	
Sense Input Current			-0.5	-0.2	$\mu\text{A}$
Minimum Operating Current	$\text{VCC} = 36.0\text{V}$ , $\text{V}_{\text{COLL}} = 5\text{V}$			0.50	0.80
Collector Current Limit	$\text{V}_{\text{COLL}} = \text{VCC} = 36.0\text{V}$ , $\text{Ref} = 1.35\text{V}$			130	145
Collector Saturation	$\text{ICOLL} = 20\text{mA}$		0.7	1.1	1.5
Transconductance (gm)	$\text{VCC} = 2.4\text{V to } 36.0\text{V}$ , $\text{V}_{\text{COLL}} = 3\text{V}$ , $\text{ICOLL} = 20\text{mA}$	19431*	-170	-140	-110
		39431B	-180	-140	-100
5.1V Reference	Internal Divider	19431*	5.05	5.1	5.15
		39431B	5	5.1	5.2
12.24V Reference	Internal Divider	19431*	12	12.24	12.5
		39431B	12	12.24	12.5
Error Amplifier AVOL			60	90	$\text{dB}$
Error Amplifier GBW	(Note 1)		3.0	5	MHz
Transconductance Amplifier GBW				3	MHz

\* Also applies to the UC29431 and UC39431

**Note:** The internal divider can be configured to give six unique references. These references are 2.82V, 3.12V, 5.1V, 7.8V, 10.42V, 12.24V.

**Note 1:** Guaranteed by design. Not 100% tested in production.

## PIN DESCRIPTIONS (cont.)

**COLL:** The collector of the output transistor with a maximum voltage of 36V. This pin is the output of the transconductance amplifier. The overall open loop voltage gain of the transconductance amplifier is  $gm \cdot RL$ , where  $gm$  is designed to be  $-140mS \pm 30mS$  and  $RL$  represents the output load.

**COMP:** The output of the error amplifier and the input to the transconductance amplifier. This pin is available to compensate the high frequency gain of the error amplifier. It is internally voltage limited to approximately 2.0V.

**GND:** The reference and power ground for the device. The power ground of the output transistor is isolated on the chip from the substrate ground used to bias the remainder of the device.

**R1, R2, R3:** Connection points to the three internal resistors.

**SENSE:** The inverting terminal of the error amplifier used as both the voltage sense input to the error amplifier and its other compensation point. The error amplifier uses the SENSE input to compare against the 1.3V on-chip reference.

The SENSE pin is also used as the undervoltage lockout (UVLO). It is intended to keep the chip from operating until the internal reference is properly biased. The threshold is approximately 1V. It is important that once the UVLO is released, the error amplifier can drive the transconductance amplifier to stabilize the loop. If a capacitor is connected between the SENSE and COMP pins to create a pole, it will limit the slew rate of the error amplifier. To increase the bandwidth and ensure startup at low load current, it is recommended to create a zero along with the pole as shown in the shunt regulator application. The error amplifier must slew 2.0V to drive the transconductance amplifier initially on.

**VCC:** The power connection for the device. The minimum to maximum operating voltage is 2.2V to 36.0V. The quiescent current is typically 0.50mA.

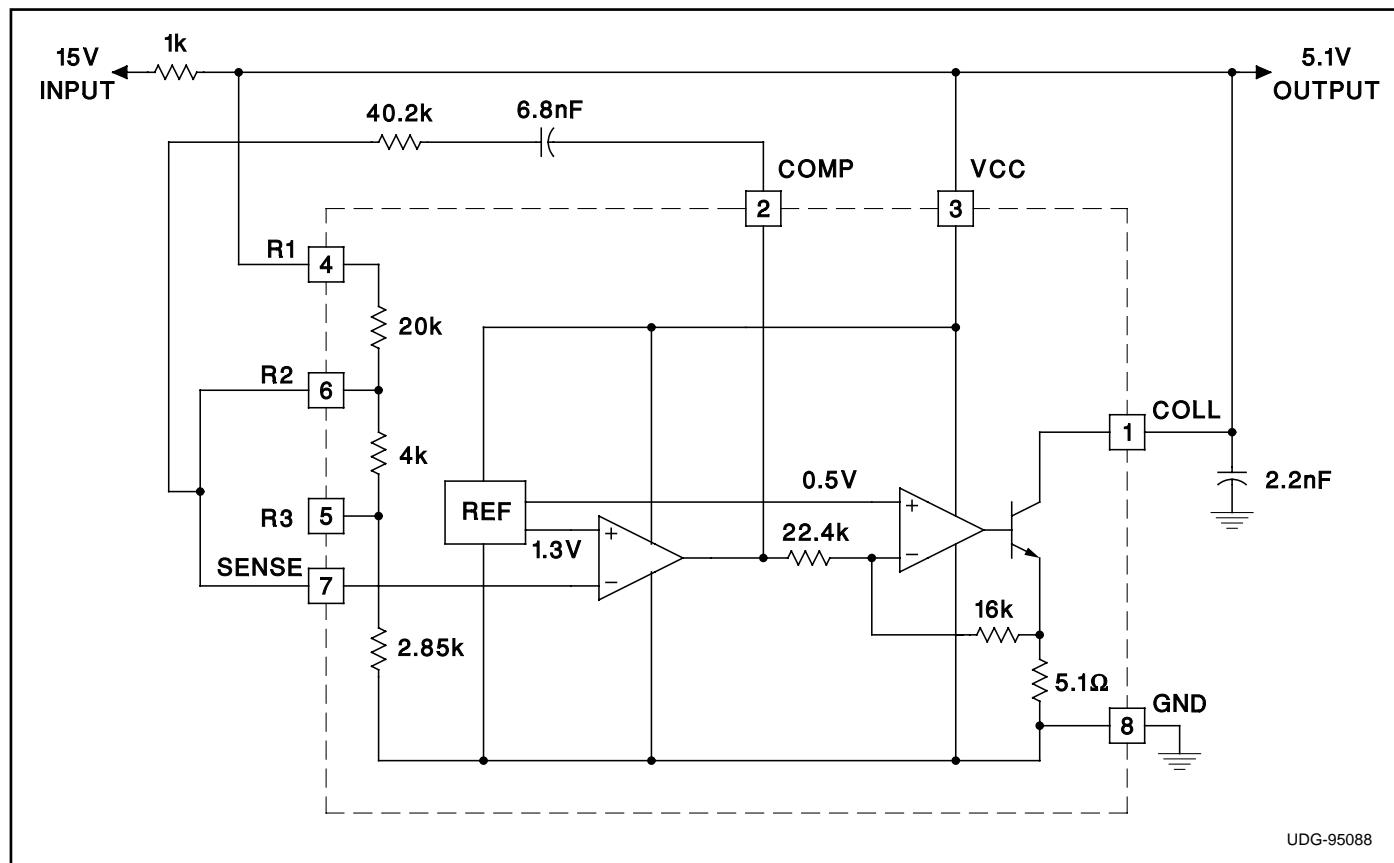


Figure 1. Typical 5.1V shunt regulator application.

## APPLICATION INFORMATION

### Magnetic Amplifier Controller Application

The 0.4% initial reference makes the UC39431 ideal as a programmable shunt regulator. By adding two external resistors, the on-chip 1.3V reference can be gained to any voltage between 2.2V (2.4V for the UC39431) and 36.0V. The input bias current is typically maintained at  $0.2\mu\text{A}$  for the output voltage range. Since the non-inverting error amplifier input is not available, a 5.1k non-inverting input impedance is added to the input of the error amplifier. This allows the user to choose the SENSE pin input impedance to cancel the minimal offset voltage caused by the input bias current.

### Frequency Compensation

The UC39431 shunt regulator is designed with two independent gain stages. The error amplifier provides 90dB of gain with a typical gain bandwidth product of 5MHz. The error amplifier provides sufficient gain in order for the sense voltage to be accurately compared to the 1.3V on-chip reference. Complete control of the frequency response of the error amplifier is accomplished with the COMP pin. By putting negative feedback across

the error amplifier, either a pole or a pole-zero can be added.

The second gain stage is the transconductance (gm) amplifier. The gm amplifier is designed with a known linear 140mS of transconductance. The voltage gain is consequently  $\text{gm} \cdot \text{Ro}$ , where  $\text{Ro}$  is the output impedance at the collector pin. The frequency response of the transconductance amplifier is controlled with the COLL pin. The gain bandwidth product of the gm amplifier is typically 3MHz. A pole or pole-zero can be added to this stage by connecting a capacitor or a series capacitor and resistor between COLL and GND.

The compensation of a control loop containing the UC39431 is made easier due to the independent compensation capability of the error amplifier and gm amplifier. As shown in the applications information, a pole-zero is created with a series resistor and capacitor between SENSE and COMP. The pole created is dominant, while the zero is used to increase the bandwidth and cancel the effects of the pole created by the capacitor between the COLL and GND pins.

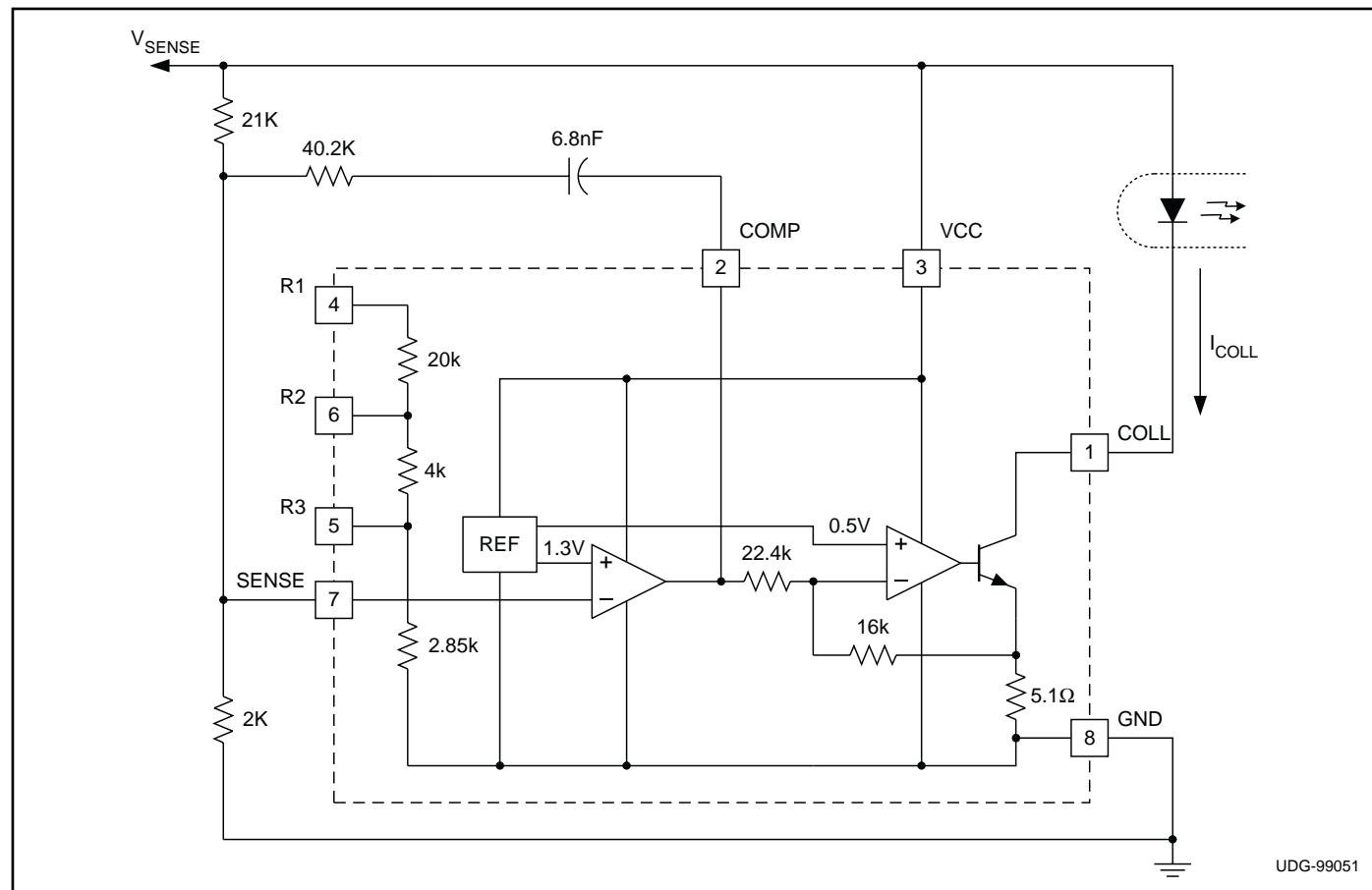


Figure 2. 15.0V optocoupler application.

## APPLICATION INFORMATION (cont.)

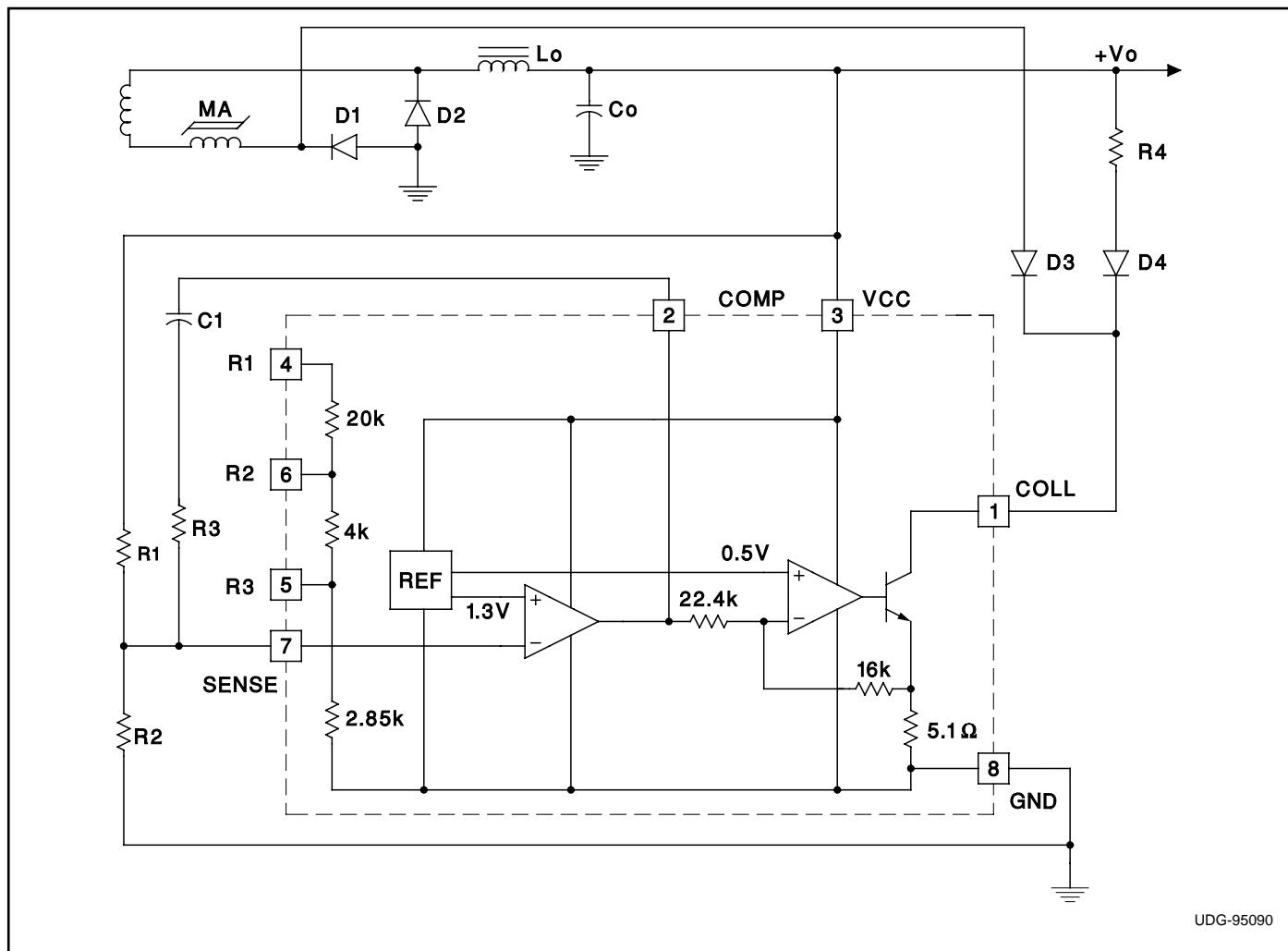
## Optocoupler Application

The two amplifier circuit architecture employed in the UC39431 is most advantageous for the optocoupler application. The error amplifier provides a fixed open loop gain that is available to apply flexible loop compensation of either poles or zeroes. A fixed transconductance amplifier provides a linear current source compared to the typical transistor's exponential output characteristics. It also eliminates the traditional optocoupler's CTR variation.

tions with power supply and voltage, and the need to suffer the additional voltage drop of a series resistor.

## Magnetic Amplifier Controller Application

The UC39431 makes an excellent controller for magnetic amplifier regulated outputs. Working from either a square wave drive or from a PWM signal controlled by another output, a saturable reactor provides highly efficient control, requiring only a reset current which can be generated from its own output.



**Figure 3. Magnetic amplifier controller application.**

Table 1. Resistor divider connection table for shunt applications

REGULATED VOLTAGE	CONNECT R1 TO:	CONNECT R2 TO:	CONNECT R3 TO:
2.82V	SENSE (pin 7)	COLL (pin 1)	SENSE (pin 7)
3.12V	open	COLL (pin 1)	SENSE (pin 7)
5.1V	COLL (pin 1)	SENSE (pin 7)	open
7.8V	COLL (pin 1)	SENSE (pin 7)	GND (pin 8)
10.42V	COLL (pin 1)	SENSE (pin 7)	SENSE (pin 7)
12.24V	COLL (pin 1)	open	SENSE (pin 7)

Note: To obtain the shunt regulated or optocoupler sensed voltage specified in the left column, connect the internal resistors (R1, R2, R3) as indicated. Refer to the shunt regulator application in Fig. 1.

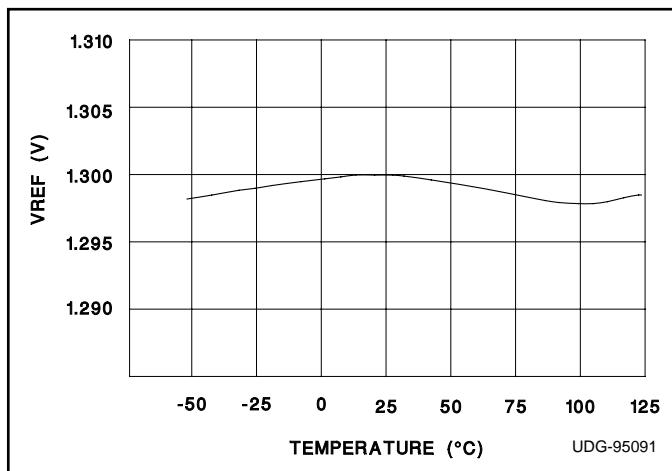


Figure 4. Internal 1.3V vs. temperature.

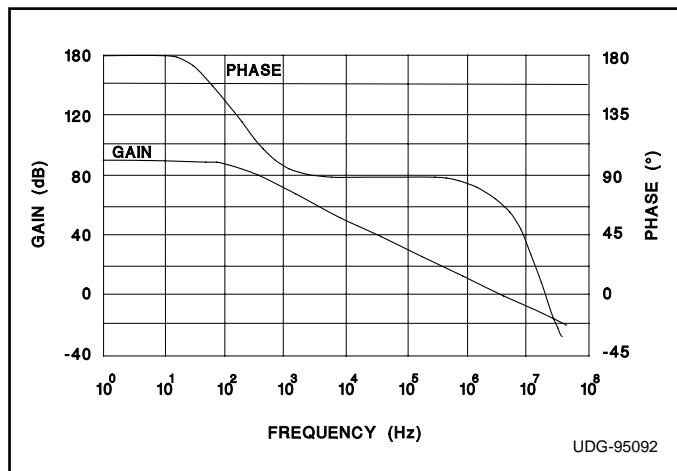


Figure 5. Error amp voltage gain and phase vs. frequency.

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
UC19431J	OBsolete	CDIP	JG	8		TBD	Call TI	Call TI
UC19431J883B	OBsolete	CDIP	JG	8		TBD	Call TI	Call TI
UC29431D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC29431DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC39431D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC39431DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC39431N	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC39431NG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

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**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

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**TBD:** The Pb-Free/Green conversion plan has not been defined.

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**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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