

# High Voltage FET-Input OPERATIONAL AMPLIFIER

## FEATURES

- **WIDE-POWER SUPPLY RANGE:**  
 $\pm 10V$  to  $\pm 45V$
- **HIGH SLEW RATE:**  $15V/\mu s$
- **LOW INPUT BIAS CURRENT:**  $10pA$
- **STANDARD-PINOUT TO-99, DIP, SO-8  
PowerPAD™, AND SO-8 SURFACE-MOUNT  
PACKAGES**

## APPLICATIONS

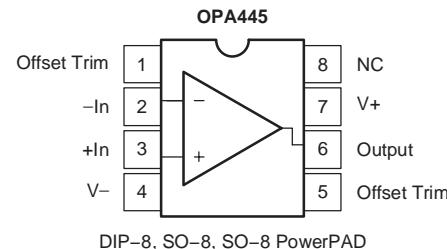
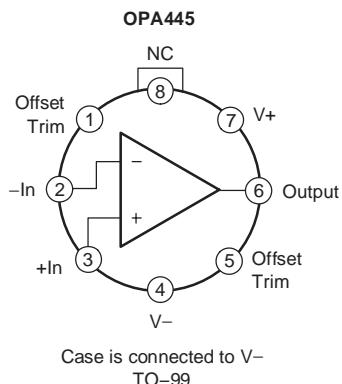
- **TEST EQUIPMENT**
- **HIGH-VOLTAGE REGULATORS**
- **POWER AMPLIFIERS**
- **DATA ACQUISITION**
- **SIGNAL CONDITIONING**
- **AUDIO**
- **PIEZO DRIVERS**

## DESCRIPTION

The OPA445 is a monolithic operational amplifier capable of operation from power supplies up to  $\pm 45V$  and output currents of  $15mA$ . It is useful in a wide variety of applications requiring high output voltage or large common-mode voltage swings.

The OPA445's high slew rate provides wide power-bandwidth response, which is often required for high-voltage applications. FET input circuitry allows the use of high-impedance feedback networks, thus minimizing their output loading effects. Laser trimming of the input circuitry yields low input offset voltage and drift.

The OPA445 is available in standard pinout TO-99, DIP-8, and SO-8 surface-mount packages as well as an SO-8 PowerPAD package for reducing junction temperature. It is fully specified from  $-25^{\circ}C$  to  $+85^{\circ}C$  and operates from  $-55^{\circ}C$  to  $+125^{\circ}C$ . A SPICE macromodel is available for design analysis (from [www.ti.com](http://www.ti.com)).



NC = No internal connection;  
leave NC floating or connect to GND, V+, or V-.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Power Supply	.....	.....	±50V
Differential Input Voltage	.....	.....	±80V
Input Voltage Range	.....	±V <sub>SL</sub>   – 3V	
Storage Temperature Range: M	.....	–65°C to +150°C	
	P, U, DDA	.....	–55°C to +125°C
Operating Temperature Range	.....	–55°C to +125°C	
Output Short-Circuit to Ground (T <sub>J</sub> < +125°C)	.....	Continuous	
Junction Temperature: M	.....	+175°C	
Junction Temperature: P, U, DDA	.....	+150°C	

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## ORDERING INFORMATION<sup>(1)</sup>

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING
OPA445AP	DIP-8	P	OPA445AP
OPA445AU	SO-8 Surface-Mount	D	OPA445AU
OPA445ADDA	SO-8 PowerPAD	DDA	OPA445
OPA445BM	TO-99 8-Pin	LMC	OPA445BM

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).

## ELECTRICAL CHARACTERISTICS

**Boldface** limits apply over the specified temperature range,  $T_A = -25^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ .  $V_S = \pm 40\text{V}$ .

At  $T_A = +25^\circ\text{C}$ ,  $V_S = \pm 40\text{V}$ , and  $R_L = 5\text{k}\Omega$ , unless otherwise noted.

Parameter	Test Conditions	OPA445BM			OPA445AP, AU, ADDA			Units
		Min	Typ	Max	Min	Typ	Max	
<b>OFFSET VOLTAGE</b>								
Input Offset Voltage vs Temperature vs Power Supply	$V_{OS}$ $V_{OS/dT}$ PSRR	$V_{CM} = 0$ , $I_O = 0$ $T_A = -25^\circ\text{C}$ to $+85^\circ\text{C}$ $V_S = \pm 10\text{V}$ to $\pm 45\text{V}$		$\pm 1$ $\pm 10$ 4	$\pm 3$ 100	$\pm 1.5$ *	$\pm 5$ *	$\text{mV}$ $\mu\text{V}/^\circ\text{C}$ $\mu\text{V}/\text{V}$
<b>INPUT BIAS CURRENT(1)</b>								
Input Bias Current <b>Over Specified Temperature Range</b>	$I_B$	$V_{CM} = 0\text{V}$		$\pm 10$	$\pm 50$ $\pm 10$	*	$\pm 100$ $\pm 20$	$\text{pA}$ $\text{nA}$
Input Offset Current <b>Over Specified Temperature Range</b>	$I_{OS}$	$V_{CM} = 0\text{V}$		$\pm 4$	$\pm 20$ $\pm 5$	*	$\pm 40$ $\pm 10$	$\text{pA}$ $\text{nA}$
<b>NOISE</b>								
Input Voltage Noise Density, $f = 1\text{kHz}$ Current Noise Density, $f = 1\text{kHz}$	$e_n$ $i_n$			15 6		*		$\text{nV}/\sqrt{\text{Hz}}$ $\text{fA}/\sqrt{\text{Hz}}$
<b>INPUT VOLTAGE RANGE</b>								
Common-Mode Voltage Range Common-Mode Rejection <b>Over Specified Temperature Range</b>	$V_{CM}$ CMRR	$V_S = \pm 40\text{V}$ $V_{CM} = -35\text{V}$ to $+35\text{V}$	$(V-) + 5$ 80 80	95	$(V+) - 5$	*	*	$\text{V}$ $\text{dB}$ $\text{dB}$
<b>INPUT IMPEDANCE</b>								
Differential Common-Mode				$10^{13} \parallel 1$ $10^{14} \parallel 3$		*		$\Omega \parallel \text{pF}$ $\Omega \parallel \text{pF}$
<b>OPEN-LOOP GAIN, DC</b>								
Open-Loop Voltage Gain <b>Over Specified Temperature Range</b>	$A_{OL}$	$V_O = -35\text{V}$ to $+35\text{V}$	100 97	110		*	*	$\text{dB}$ $\text{dB}$
<b>FREQUENCY RESPONSE</b>								
Gain Bandwidth Product Slew Rate Full Power Bandwidth Rise Time Overshoot Total Harmonic Distortion + Noise	GBW SR	$V_O = 70\text{V}_{\text{PP}}$ $V_O = 70\text{V}_{\text{PP}}$ $V_O = \pm 200\text{mV}$ $G = +1$ , $Z_L = 5\text{k}\Omega \parallel 50\text{pF}$ $f = 1\text{kHz}$ , $V_O = 3.5\text{V}_{\text{rms}}$ , $G = 1$ $f = 1\text{kHz}$ , $V_O = 10\text{V}_{\text{rms}}$ , $G = 1$	5 23	2 15 70 100 35 0.0002 0.00008		*	*	$\text{MHz}$ $\text{V}/\mu\text{s}$ $\text{kHz}$ $\text{ns}$ $\%$ $\%$ $\%$
<b>OUTPUT</b>								
Voltage Output <b>Over Specified Temperature Range</b>	$V_O$		$(V-) + 5$ $(V-) + 5$		$(V+) - 5$ $(V+) - 5$	*	*	$\text{V}$ $\text{V}$
Current Output Output Resistance, Open Loop	$I_O$ $R_O$	$V_O = \pm 28\text{V}$ dc	$\pm 15$	220 $\pm 26$		*	*	$\text{mA}$ $\Omega$
Short Circuit Current Capacitive Load Drive	$I_{SC}$ $C_{LOAD}$				See Typical Characteristic(2)		*	$\text{mA}$
<b>POWER SUPPLY</b>								
Specified Operating Range Operating Voltage Range Quiescent Current	$V_S$ $I_Q$		$\pm 10$	$\pm 40$ $\pm 4.2$	$\pm 45$ $\pm 4.7$	*	*	$\text{V}$ $\text{V}$ $\text{mA}$
<b>TEMPERATURE RANGE</b>								
Specification Range Operating Range Storage Range Thermal Resistance, Junction-to-Ambient TO-99 DIP-8 SO-8 Surface-Mount SO-8 PowerPAD(3)				-25 -55 -65	+85 +125 +125	*	*	$^\circ\text{C}$ $^\circ\text{C}$ $^\circ\text{C}$ $^\circ\text{C}/\text{W}$ $^\circ\text{C}/\text{W}$ $^\circ\text{C}/\text{W}$ $^\circ\text{C}/\text{W}$
Thermal Resistance, Junction-to-Case SO-8 PowerPAD(3)	$\theta_{JA}$ $\theta_{JC}$			200	-55		+125	
						100 150 52		
						10		$^\circ\text{C}/\text{W}$

NOTE: \* Specifications same as OPA445BM.

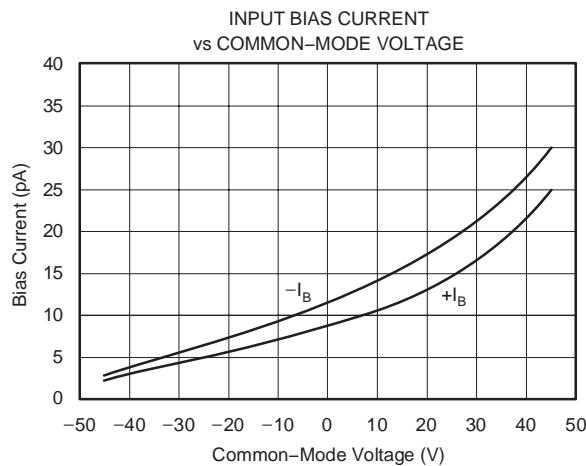
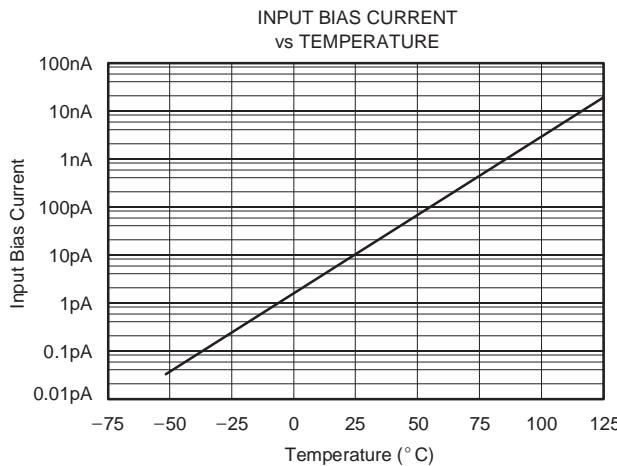
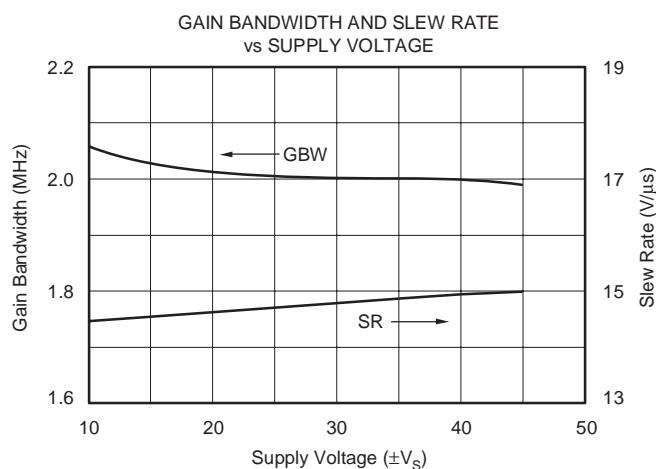
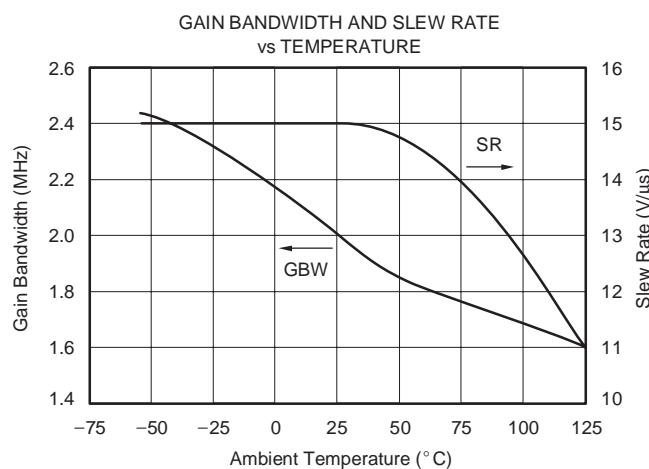
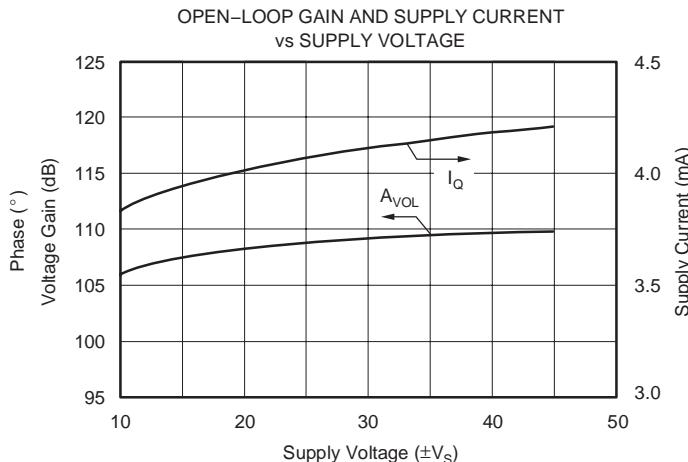
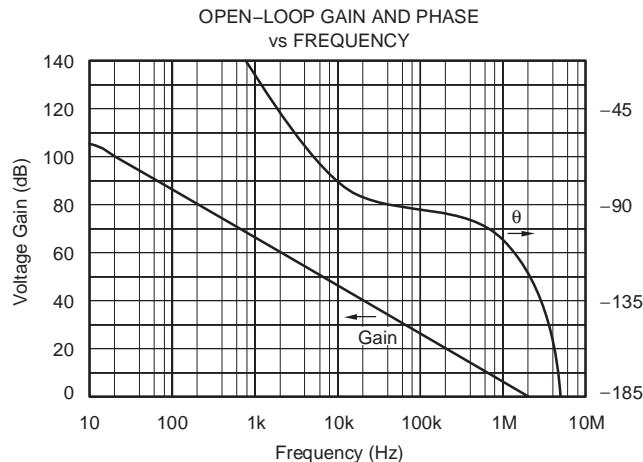
(1) High-speed test at  $T_1 = +25^\circ\text{C}$ .

(2) See *Small-Signal Overshoot vs Load Capacitance* in the Typical Characteristics section.

(3) Test board 1in x 0.5in heat-spreader, 1oz copper.

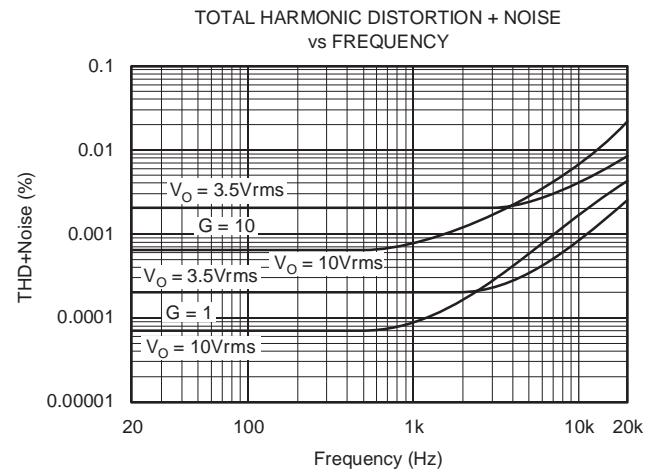
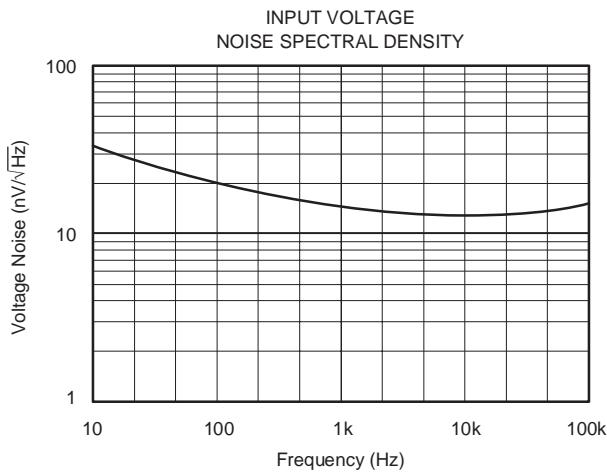
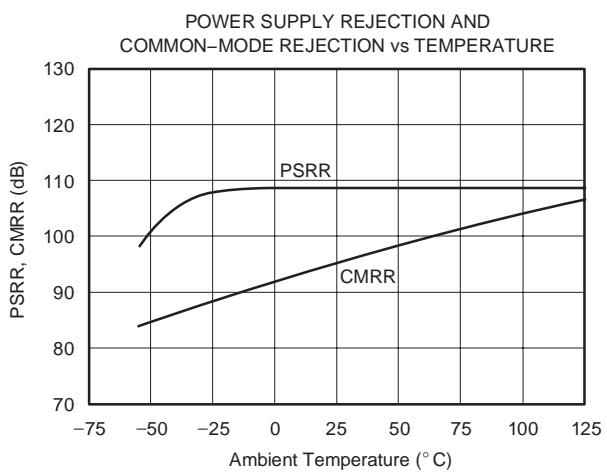
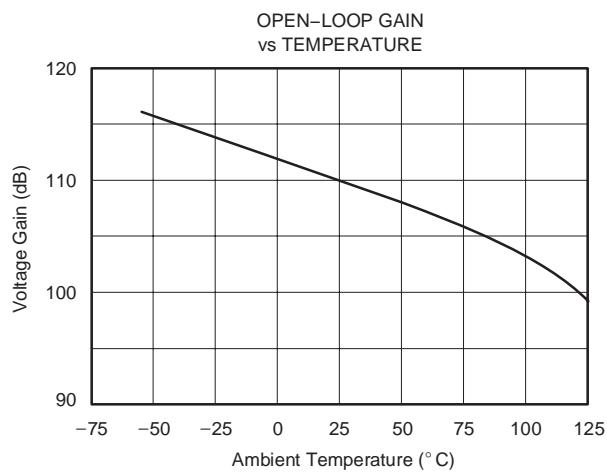
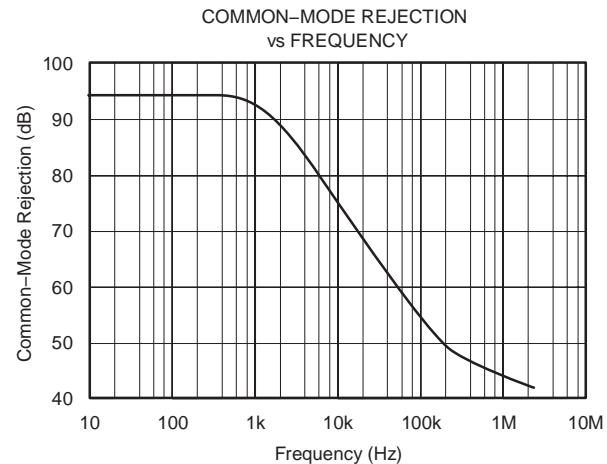
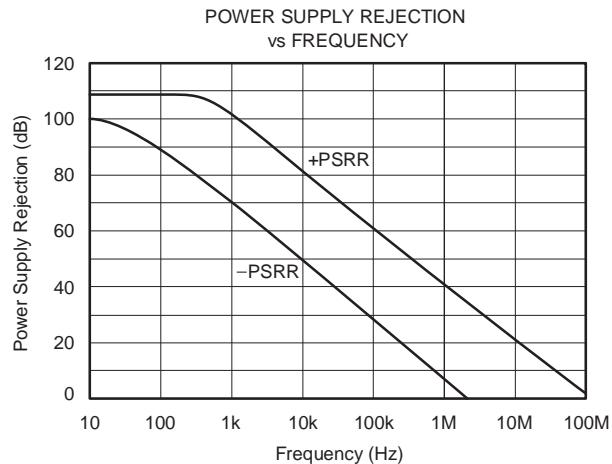
## TYPICAL CHARACTERISTICS

At  $T_A = +25^\circ\text{C}$  and  $V_S = \pm 40\text{V}$ , unless otherwise noted.



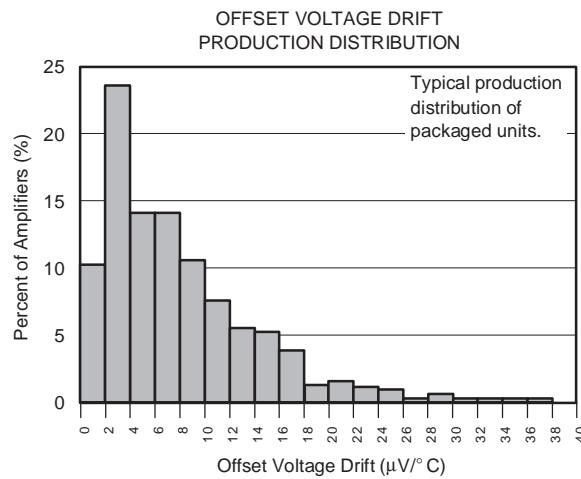
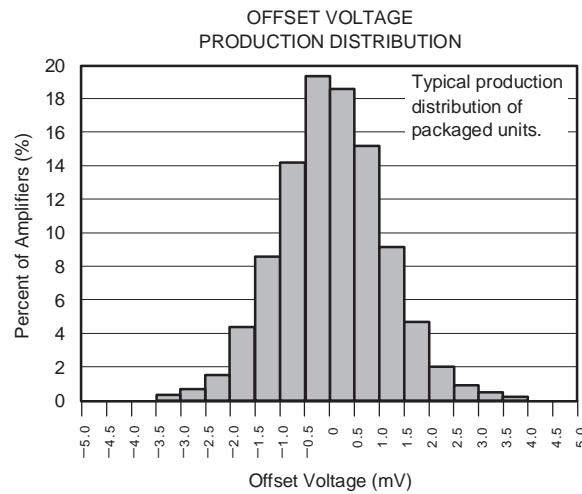
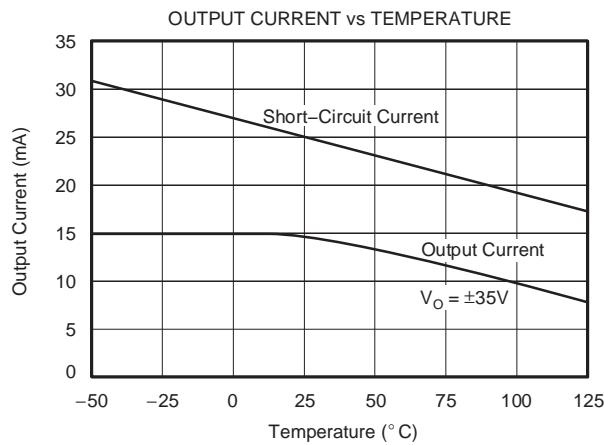
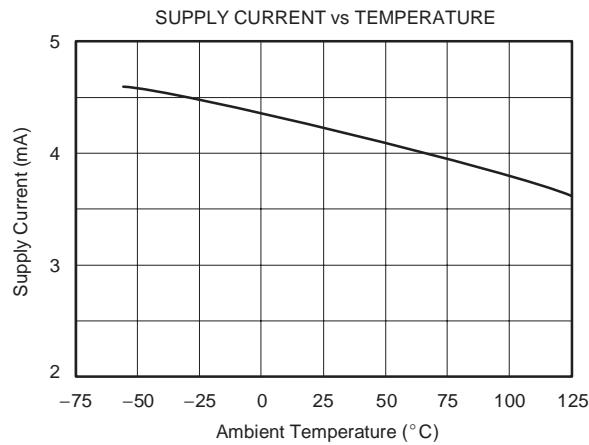
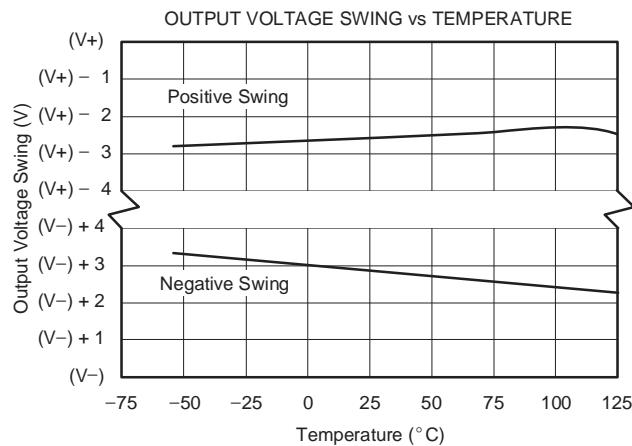
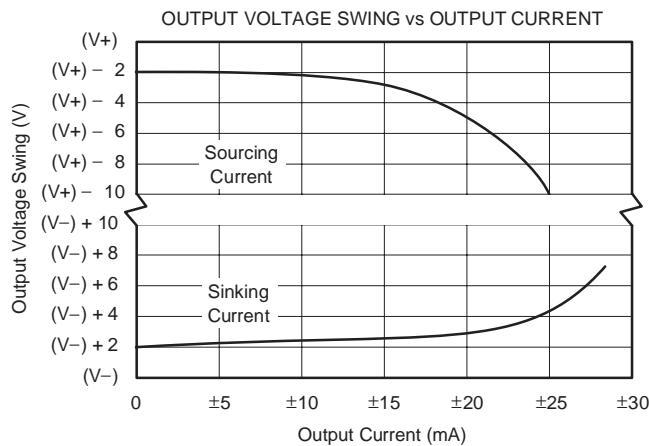
## TYPICAL CHARACTERISTICS (continued)

At  $T_A = +25^\circ\text{C}$  and  $V_S = \pm 40\text{V}$ , unless otherwise noted.



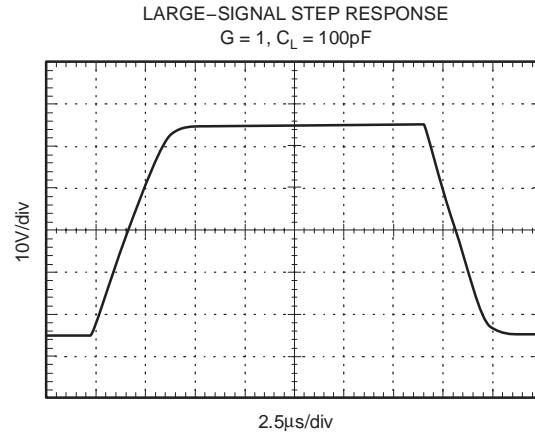
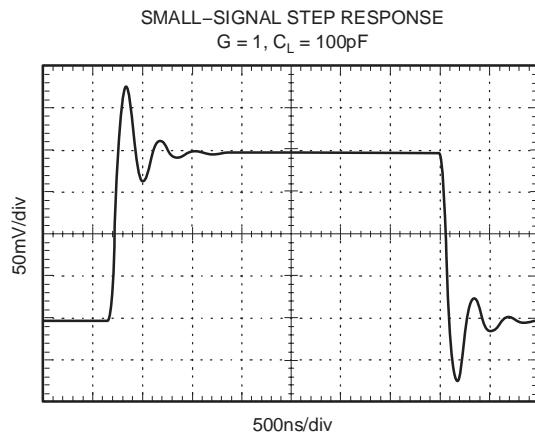
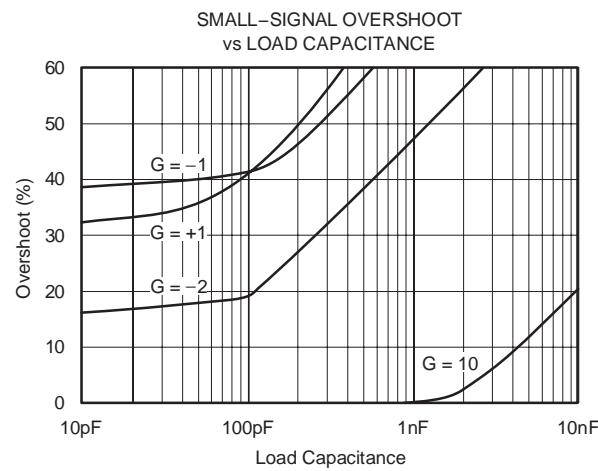
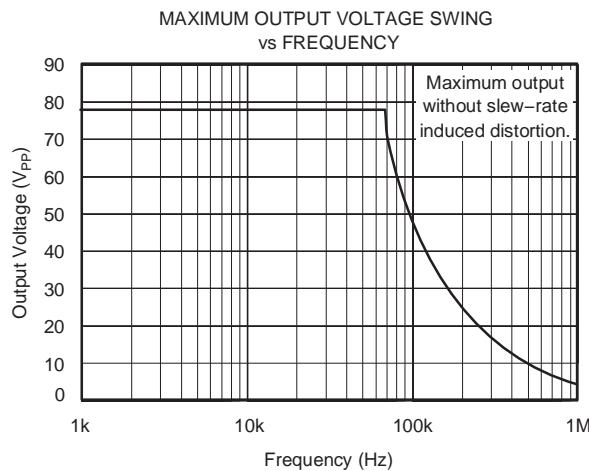
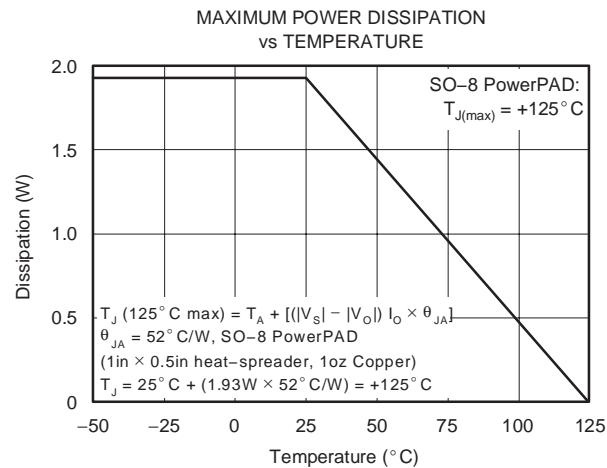
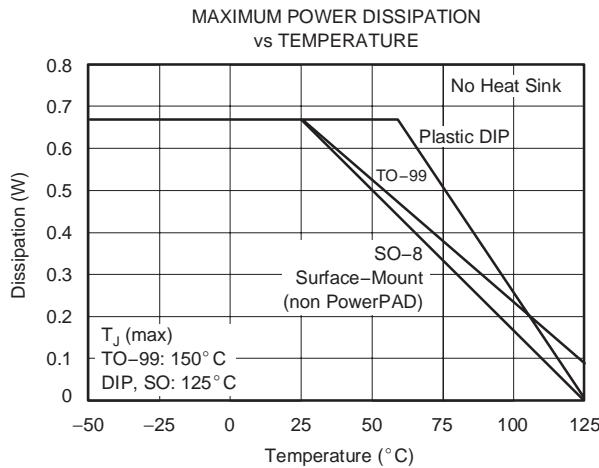
## **TYPICAL CHARACTERISTICS (continued)**

At  $T_A = +25^\circ\text{C}$  and  $V_S = \pm 40\text{V}$ , unless otherwise noted.



## TYPICAL CHARACTERISTICS (continued)

At  $T_A = +25^\circ\text{C}$  and  $V_S = \pm 40\text{V}$ , unless otherwise noted.



## APPLICATIONS

Figure 1 shows the OPA445 connected as a basic noninverting amplifier. The OPA445 can be used in virtually any op amp configuration.

Power-supply terminals should be bypassed with  $0.1\mu\text{F}$  capacitors, or greater, near the power supply pins. Be sure that the capacitors are appropriately rated for the power-supply voltage used.

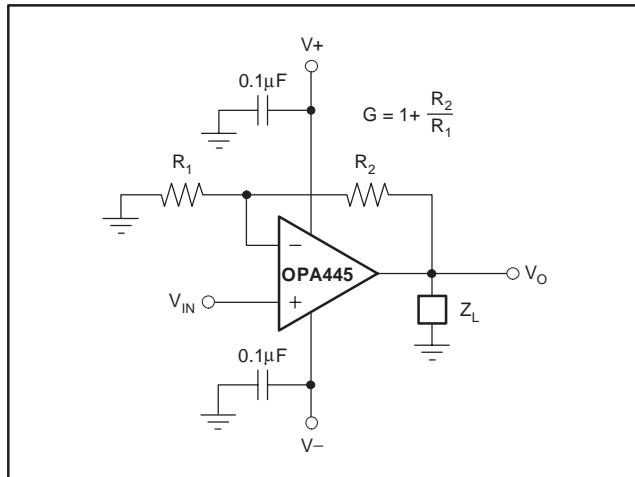


Figure 1. The OPA445 Configured as a Noninverting Amplifier

## POWER SUPPLIES

The OPA445 may be operated from power supplies up to  $\pm 45\text{V}$  or a total of  $90\text{V}$  with excellent performance. Most behavior remains unchanged throughout the full operating voltage range. Parameters which vary significantly with operating voltage are shown in the Typical Characteristics.

Some applications do not require equal positive and negative output voltage swing. Power-supply voltages do not need to be equal. The OPA445 can operate with as little as  $20\text{V}$  between the supplies and with up to  $90\text{V}$  between the supplies. For example, the positive supply could be set to  $80\text{V}$  with the negative supply at  $-10\text{V}$ , or vice-versa.

## INPUT PROTECTION

The inputs of conventional FET-input op amps should be protected against destructive currents that can flow when input FET gate-to-substrate isolation diodes are forward-biased. This can occur if the input voltage exceeds the power supplies or there is an input voltage with  $V_S = 0\text{V}$ . Protection is easily accomplished with a resistor in series with the input. Care should be taken because the resistance in series with the input capacitance may affect stability. Many input signals are inherently current-limited; therefore, a limiting resistor may not be required.

## OFFSET VOLTAGE TRIM

The OPA445 provides offset voltage trim connections on pins 1 and 5. Offset voltage can be adjusted by connecting a potentiometer as shown in Figure 2. This adjustment should be used only to null the offset of the op amp, not to adjust system offset or offset produced by the signal source. Nulling system offset could degrade the offset voltage drift behavior of the op amp. While it is not possible to predict the exact change in drift, the effect is usually small.

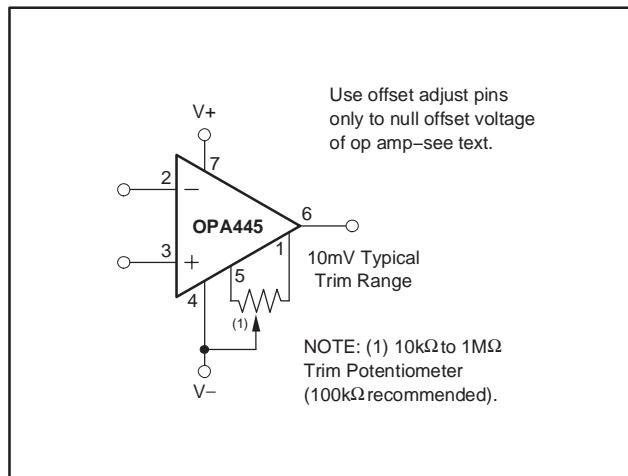
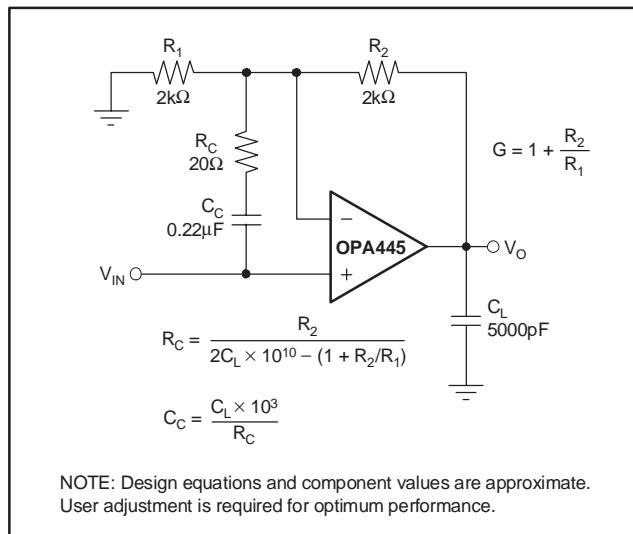


Figure 2. Offset Voltage Trim

## CAPACITIVE LOADS

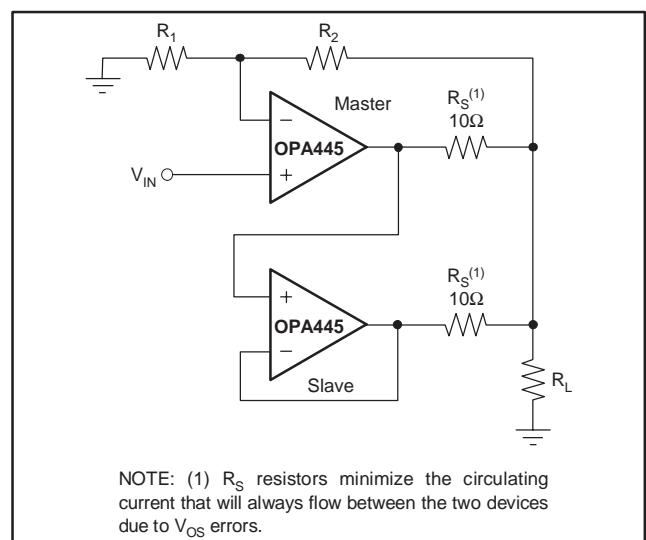
The dynamic characteristics of the OPA445 have been optimized for commonly encountered gains, loads, and operating conditions. The combination of low closed-loop gain and capacitive load will decrease the phase margin and may lead to gain peaking or oscillations. Figure 3 shows a circuit which preserves phase margin with capacitive load. The circuit does not suffer a voltage drop due to load current; however, input impedance is reduced at high frequencies. Consult Application Bulletin SBOA015, available for download at [www.ti.com](http://www.ti.com), for details of analysis techniques and application circuits.



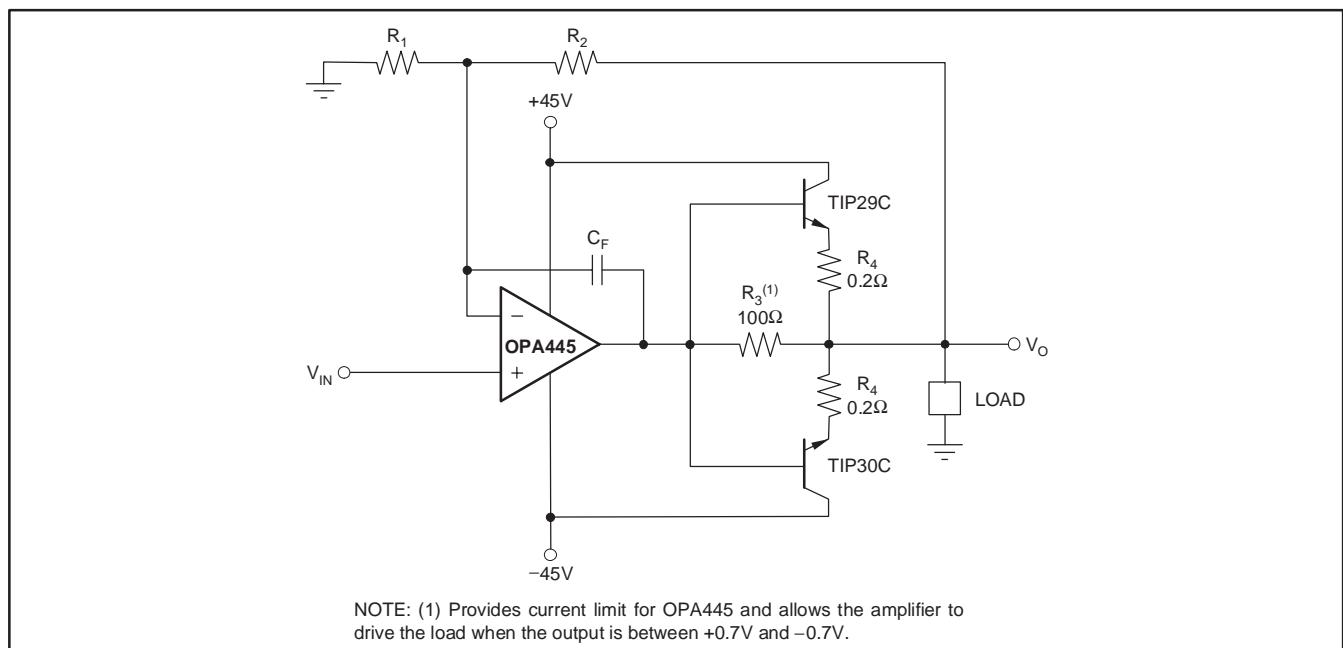
**Figure 3. Driving Large Capacitive Loads**

## INCREASING OUTPUT CURRENT

In those applications where the 15mA of output current is not sufficient to drive the required load, output current can be increased by connecting two or more OPA445s in parallel as shown in Figure 4. Amplifier A1 is the *master* amplifier and may be configured in virtually any op amp circuit. Amplifier A2, the *slave*, is configured as a unity gain buffer. Alternatively, external output transistors can be used to boost output current. The circuit in Figure 5 is capable of supplying output currents up to 1A.



**Figure 4. Parallel Amplifiers Increase Output Current Capability**



**Figure 5. External Output Transistors Boost Output Current Up to 1 Amp**

## SAFE OPERATING AREA

Stress on the output transistors is determined both by the output current and by the output voltage across the conducting output transistors,  $V_S - V_O$ . The power dissipated by the output transistor is equal to the product of the output current and the voltage across the conducting transistor,  $V_S - V_O$ . The Safe Operating Area (SOA) curve, Figure 6 through Figure 10) illustrates the permissible range of voltage and current. The curves shown represent devices soldered to a printed circuit board (PCB) with no heat sink. Increasing printed circuit trace area or the use of a heat sink (TO-99 package) can significantly reduce thermal resistance ( $\theta$ ), resulting in increased output current for a given output voltage (see Figure 11, Figure 12, and the *Heat Sink* section).

The safe output current decreases as  $V_S - V_O$  increases. Output short-circuits are a very demanding case for SOA. A short-circuit to ground forces the full power supply voltage ( $V_+$  or  $V_-$ ) across the conducting transistor and produces a typical output current of 25mA. With  $\pm 40V$  power supplies, this creates an internal dissipation of 1W. This exceeds the maximum rating and is not recommended. If operation in this region is unavoidable, a heat sink is required. For further insight on SOA, consult Application Bulletin SBOA022 (available for download at [www.ti.com](http://www.ti.com)).

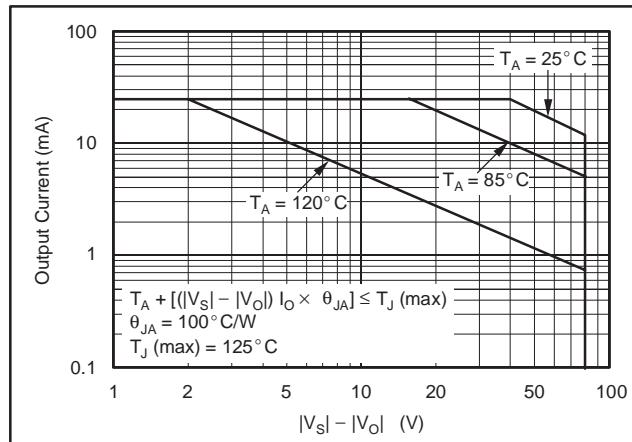


Figure 6. DIP-8 Safe Operating Area

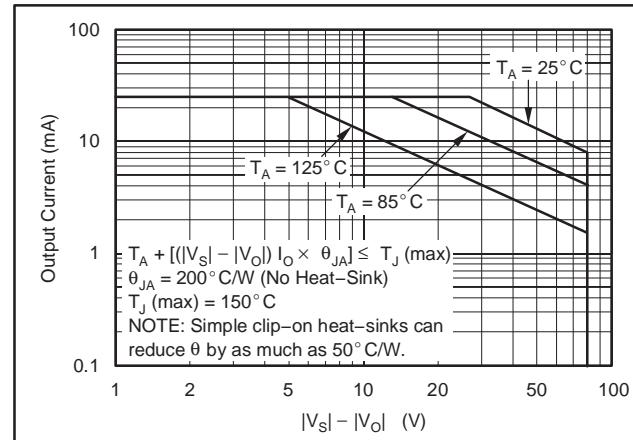


Figure 7. TO-99 Safe Operating Area

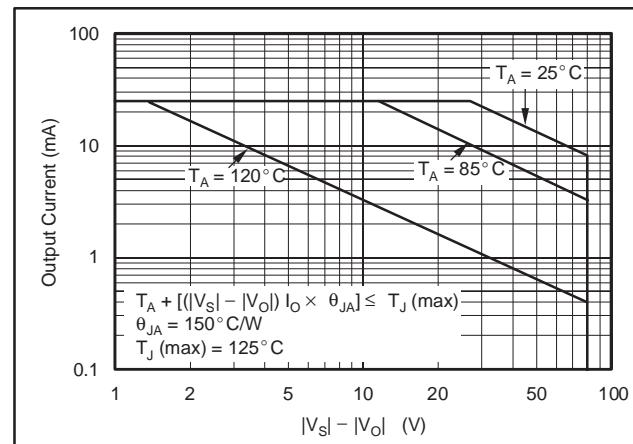


Figure 8. SO-8 (non PowerPAD) Safe Operating Area

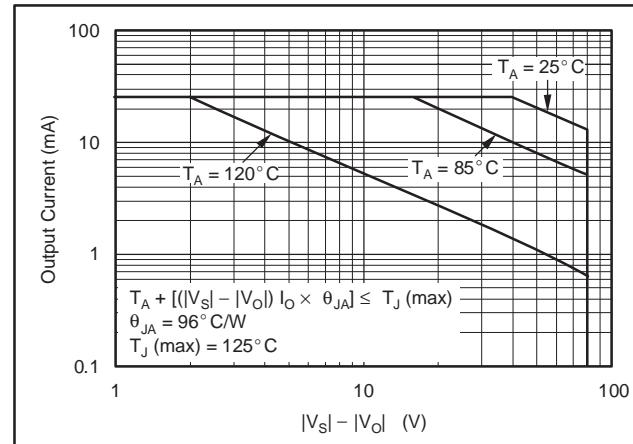
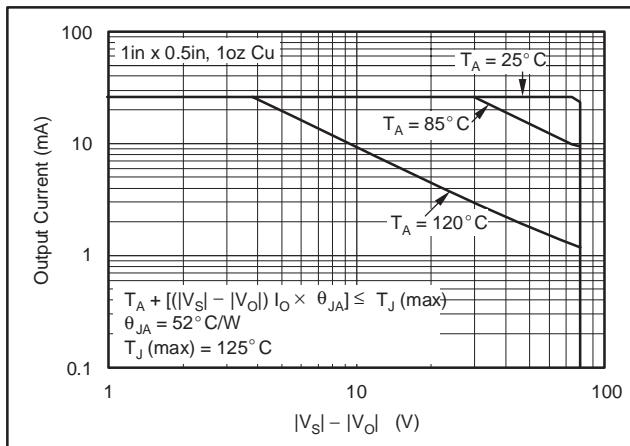
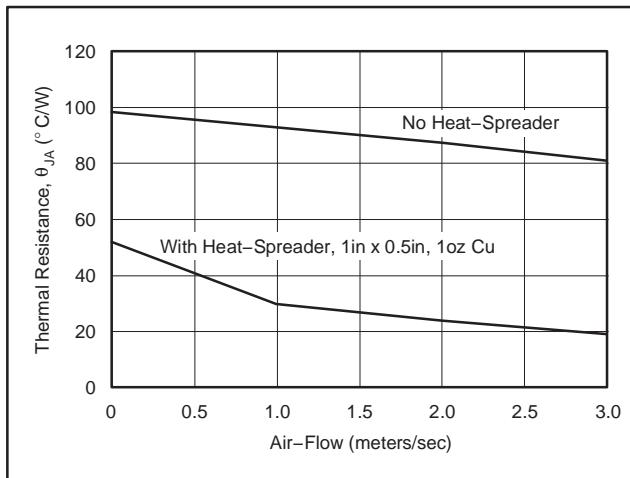


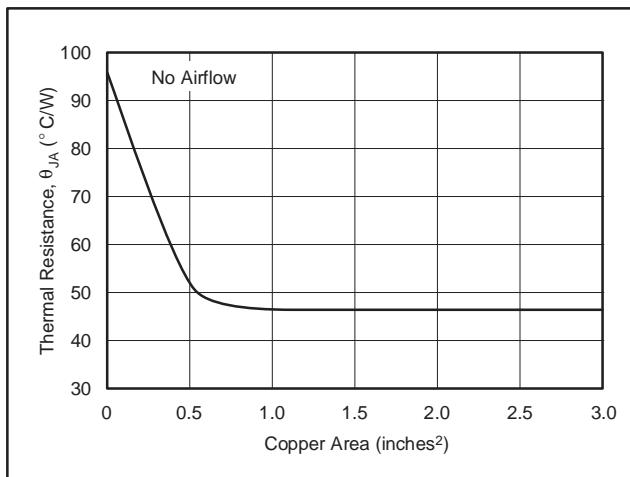
Figure 9. SO-8 PowerPAD Safe Operating Area (no heat-spreader, no airflow)



**Figure 10. SO-8 PowerPAD Safe Operating Area (with heat-spreader, no airflow)**



**Figure 11. SO-8 PowerPAD Thermal Resistance (with and without heat-spreader)**



**Figure 12. Thermal Resistance vs Circuit Board Copper Area**

## POWER DISSIPATION

Power dissipation depends on power supply, signal, and load conditions. For dc signals, power dissipation is equal to the product of the output current times the voltage across the conducting output transistor,  $P_D = I_L (V_S - V_O)$ . Power dissipation can be minimized by using the lowest possible power-supply voltage necessary to assure the required output voltage swing.

For resistive loads, the maximum power dissipation occurs at a dc output voltage of one-half the power supply voltage. Dissipation with ac signals is lower. Application Bulletin SBOA022 explains how to calculate or measure dissipation with unusual loads or signals.

The OPA445 can supply output currents of 15mA and larger. This would present no problem for a standard op amp operating from  $\pm 15V$  supplies. With high supply voltages, however, internal power dissipation of the op amp can be quite large. Operation from a single power supply (or unbalanced power supplies) can produce even larger power dissipation since a large voltage is impressed across the conducting output transistor. Applications with large power dissipation may require a heat-sink.

## HEAT SINKING

Power dissipated in the OPA445 will cause the junction temperature to rise. For reliable operation junction temperature should be limited to  $125^\circ\text{C}$ , maximum ( $150^\circ\text{C}$  for TO-99 package). Some applications will require a heat-sink to assure that the maximum operating junction temperature is not exceeded. In addition, the junction temperature should be kept as low as possible for increased reliability. Junction temperature can be determined according to the following equation:

$$T_J = T_A + P_D \theta_{JA} \quad (1)$$

Package thermal resistance,  $\theta_{JA}$ , is affected by mounting techniques and environments. Poor air circulation and use of sockets can significantly increase thermal resistance. Best thermal performance is achieved by soldering the op amp into a circuit board with wide printed circuit traces to allow greater conduction through the op amp leads. Simple clip-on heat sinks (such as a Thermalloy 2257) can reduce the thermal resistance of the TO-99 metal package by as much as  $50^\circ\text{C/W}$ . The SO-8 PowerPAD package will provide lower thermal resistance, especially with a simple heat-spreader—even lower with a heat-sink. For additional information on determining heat-sink requirements, consult Application Bulletin SBOA021.

## PowerPAD THERMALLY-ENHANCED PACKAGE

In addition to the SO-8, DIP-8, and TO-99 packages, the OPA445 also comes in an SO-8 PowerPAD. The SO-8 PowerPAD is a standard-size SO-8 package where the exposed leadframe on the bottom of the package can be soldered directly to the PCB to create an extremely low thermal resistance. This architecture enhances the OPA445's power dissipation capability significantly and eliminates the use of bulky heatsinks and slugs traditionally used in thermal packages. This package can be easily mounted using standard PCB assembly techniques. NOTE: Since the SO-8 PowerPAD is pin-compatible with standard SO-8 packages, the OPA445 can directly replace operational amplifiers in existing sockets. Soldering the PowerPAD to the PCB is always required, even with applications that have low power dissipation. Soldering the device to the PCB provides the necessary thermal and mechanical connection between the leadframe die pad and the PCB.

The PowerPAD package is designed so that the leadframe die pad (or thermal pad) is exposed on the bottom of the IC; see Figure 13. This design provides an extremely low thermal resistance ( $\theta_{JC}$ ) path between the die and the exterior of the package. The thermal pad on the bottom of the IC can then be soldered directly to the PCB, using the PCB as a heatsink. In addition, plated-through holes (vias) provide a low thermal resistance heat flow path to the back side of the PCB.

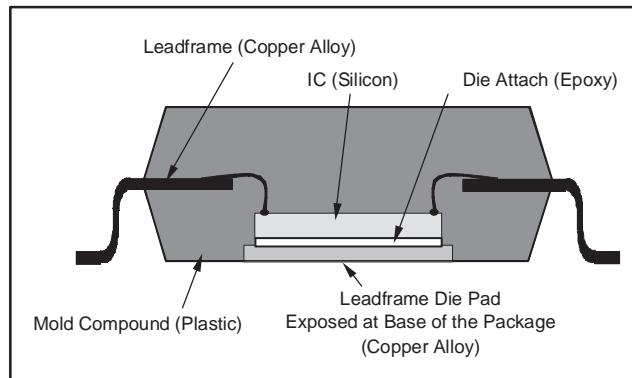


Figure 13. Section View of a PowerPAD Package

## GENERAL PowerPAD LAYOUT GUIDELINES

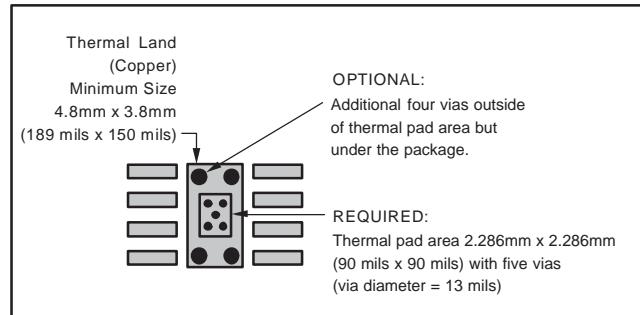
The OPA445 is available in a thermally-enhanced PowerPAD package. This package is constructed using a downset leadframe upon which the die is mounted. This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package. This thermal pad has direct thermal contact with the die; thus, excellent thermal performance is achieved by providing a good thermal path away from the thermal pad.

The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad must be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat-dissipating device. Soldering the PowerPAD to the PCB is always required, even with applications that have low power dissipation. Follow these steps:

1. The PowerPAD must be connected to the most negative supply voltage on the device, V-.
2. Prepare the PCB with a top-side etch pattern. There should be etching for the leads as well as etch for the thermal pad.
3. Place recommended holes in the area of the thermal pad. Recommended thermal land size and thermal via patterns for the SO-8 DDA package is shown in Figure 14. These holes should be 13 mils in diameter. Keep them small, so that solder wicking through the holes is not a problem during reflow. The minimum recommended number of holes for the SO-8 PowerPAD package is five.
4. Additional vias may be placed anywhere along the thermal plane outside of the thermal pad area. These vias help dissipate the heat generated by the OPA445 IC. These additional vias may be larger than the 13-mil diameter vias directly under the thermal pad. They can be larger because they are not in the thermal pad area to be soldered; thus, wicking is not a problem.
5. Connect all holes to the internal power plane of the correct voltage potential (V-).
6. When connecting these holes to the plane, do not use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations, making the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the OPA445 PowerPAD package should make the connections to the internal plane with a complete connection around the entire circumference of the plated-through hole.
7. The top-side solder mask should leave the terminals of the package and the thermal pad area exposed. The bottom-side solder mask should cover the holes of the thermal pad area. This masking prevents solder from being pulled away from the thermal pad area during the reflow process.
8. Apply solder paste to the exposed thermal pad area and all of the IC terminals.

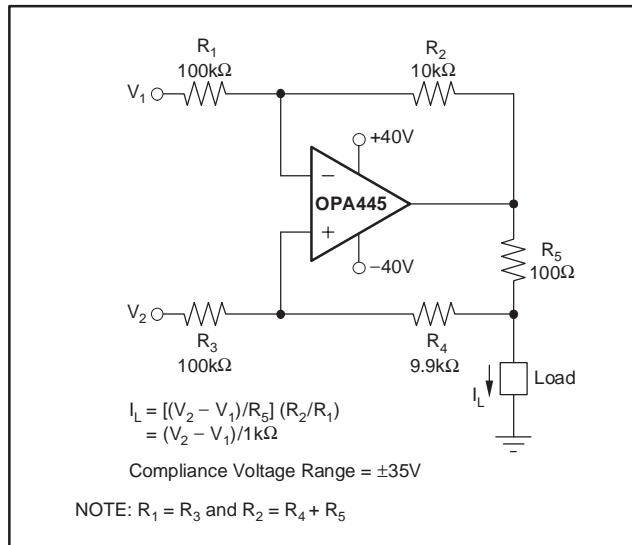
9. With these preparatory steps in place, the PowerPAD IC is simply placed in position and run through the solder reflow operation as any standard surfacemount component. This preparation results in a properly installed part.

For detailed information on the PowerPAD package, including thermal modeling considerations and repair procedures, see technical brief SLMA002 *PowerPAD Thermally-Enhanced Package* available for download at [www.ti.com](http://www.ti.com).

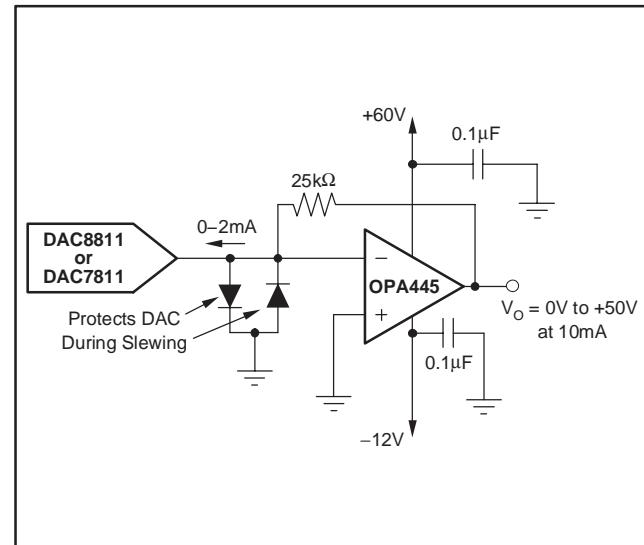


**Figure 14. 8-Pin PowerPAD PCB Etch and Via Pattern**

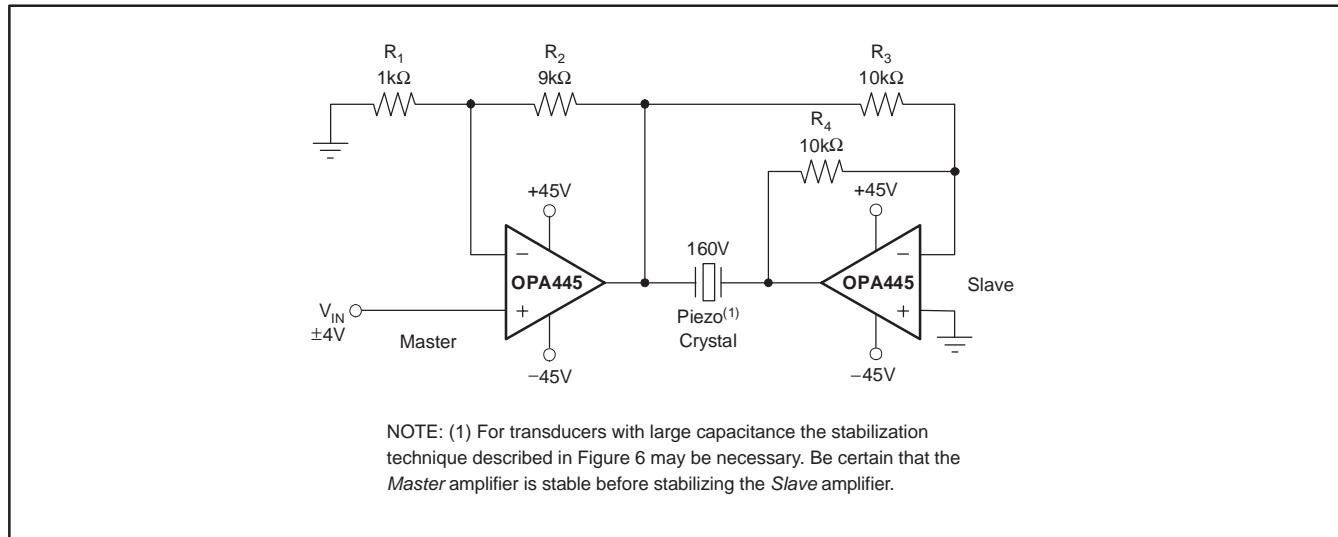
## TYPICAL APPLICATIONS



**Figure 15. Voltage-to-Current Converter**



**Figure 16. Programmable Voltage Source**



**Figure 17. Bridge Circuit Doubles Voltage for Piezo Crystals**

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">OPA445ADDA</a>	Active	Production	SO PowerPAD (DDA)   8	75   TUBE	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-55 to 125	OPA445
OPA445ADDA.A	Active	Production	SO PowerPAD (DDA)   8	75   TUBE	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-55 to 125	OPA445
<a href="#">OPA445ADDR</a>	Active	Production	SO PowerPAD (DDA)   8	2500   LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-55 to 125	OPA445
OPA445ADDR.A	Active	Production	SO PowerPAD (DDA)   8	2500   LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-55 to 125	OPA445
<a href="#">OPA445AP</a>	Active	Production	PDIP (P)   8	50   TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	OPA445AP
OPA445AP.A	Active	Production	PDIP (P)   8	50   TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	OPA445AP
<a href="#">OPA445AU</a>	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-50 to 125	OPA 445AU
OPA445AU.A	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-50 to 125	OPA 445AU
<a href="#">OPA445AU/2K5</a>	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	OPA 445AU
OPA445AU/2K5.A	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	OPA 445AU
<a href="#">OPA445BM</a>	Active	Production	TO-99 (LMC)   8	20   TUBE	Yes	AU	N/A for Pkg Type	-	OPA445BM
OPA445BM.A	Active	Production	TO-99 (LMC)   8	20   TUBE	Yes	AU	N/A for Pkg Type	-55 to 125	OPA445BM

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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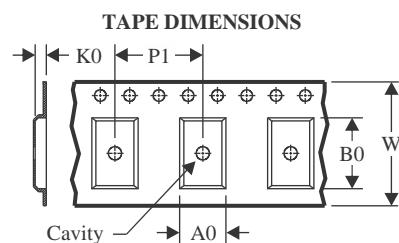
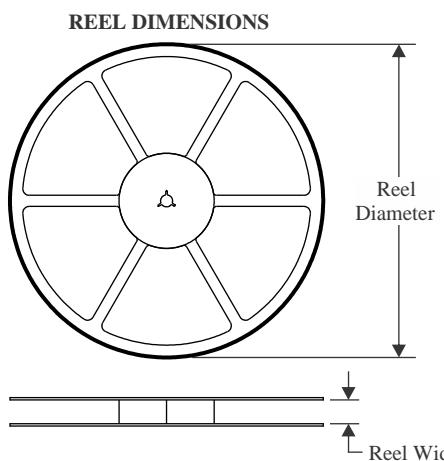
<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

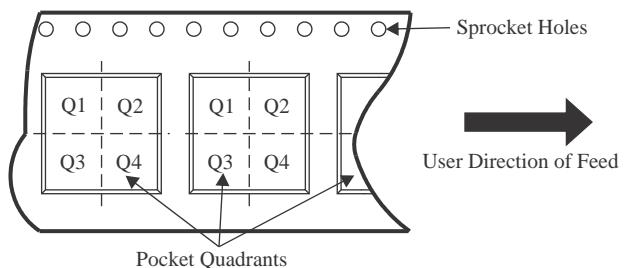
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**TAPE AND REEL INFORMATION**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


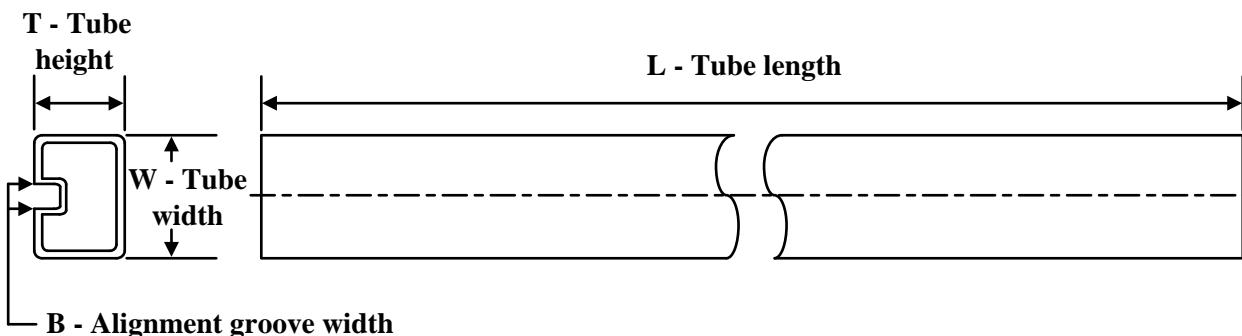
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA445ADDR	SO PowerPAD	DDA	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA445AU/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA445ADDAR	SO PowerPAD	DDA	8	2500	353.0	353.0	32.0
OPA445AU/2K5	SOIC	D	8	2500	353.0	353.0	32.0

**TUBE**


\*All dimensions are nominal

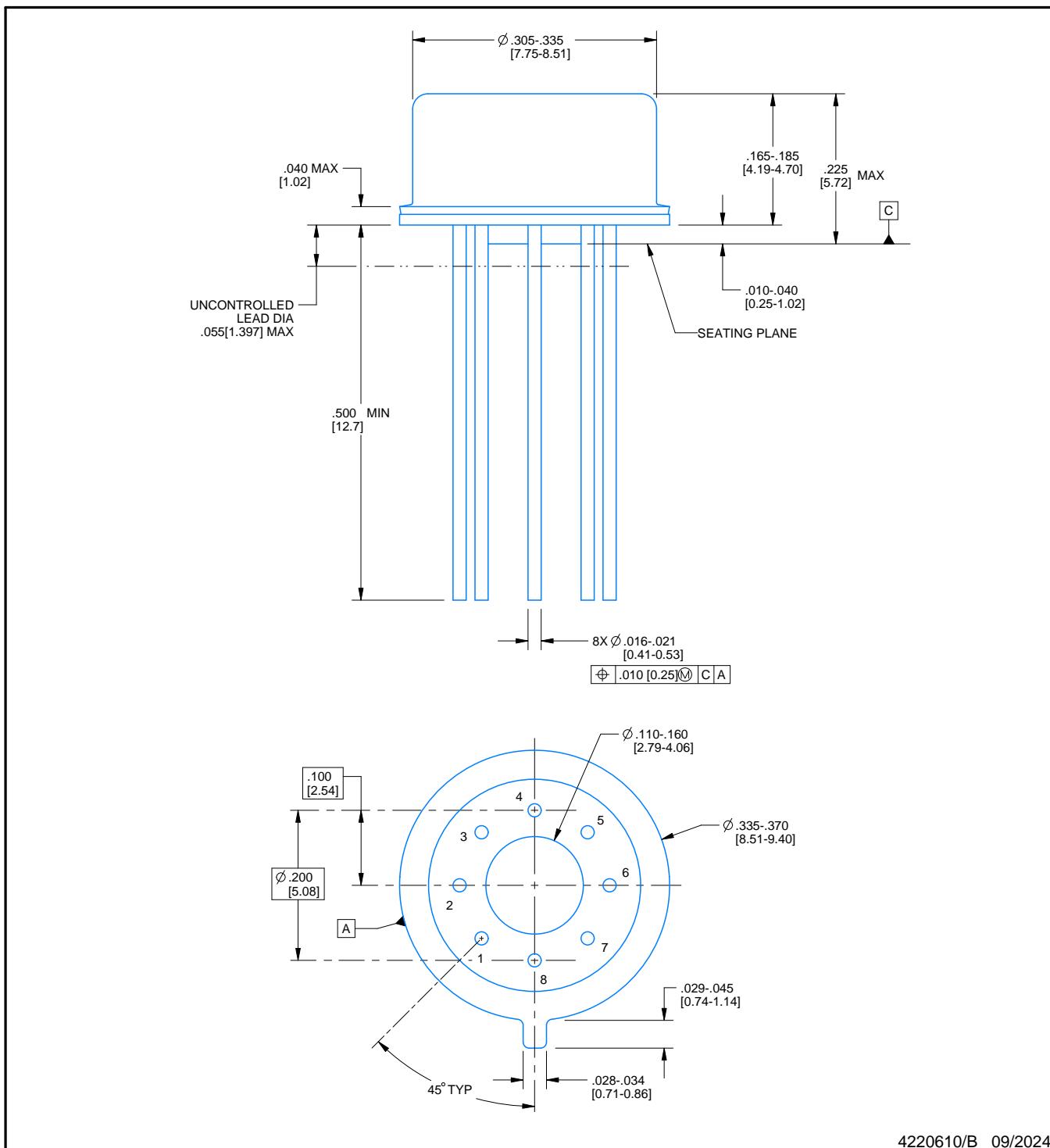
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
OPA445ADDA	DDA	HSOIC	8	75	506.6	8	3940	4.32
OPA445ADDA.A	DDA	HSOIC	8	75	506.6	8	3940	4.32
OPA445AP	P	PDIP	8	50	506	13.97	11230	4.32
OPA445AP.A	P	PDIP	8	50	506	13.97	11230	4.32
OPA445AU	D	SOIC	8	75	506.6	8	3940	4.32
OPA445AU.A	D	SOIC	8	75	506.6	8	3940	4.32
OPA445BM	LMC	TO-CAN	8	20	532.13	21.59	889	NA
OPA445BM.A	LMC	TO-CAN	8	20	532.13	21.59	889	NA

# PACKAGE OUTLINE

LMC0008A

TO-CAN - 5.72 mm max height

TRANSISTOR OUTLINE



4220610/B 09/2024

## NOTES:

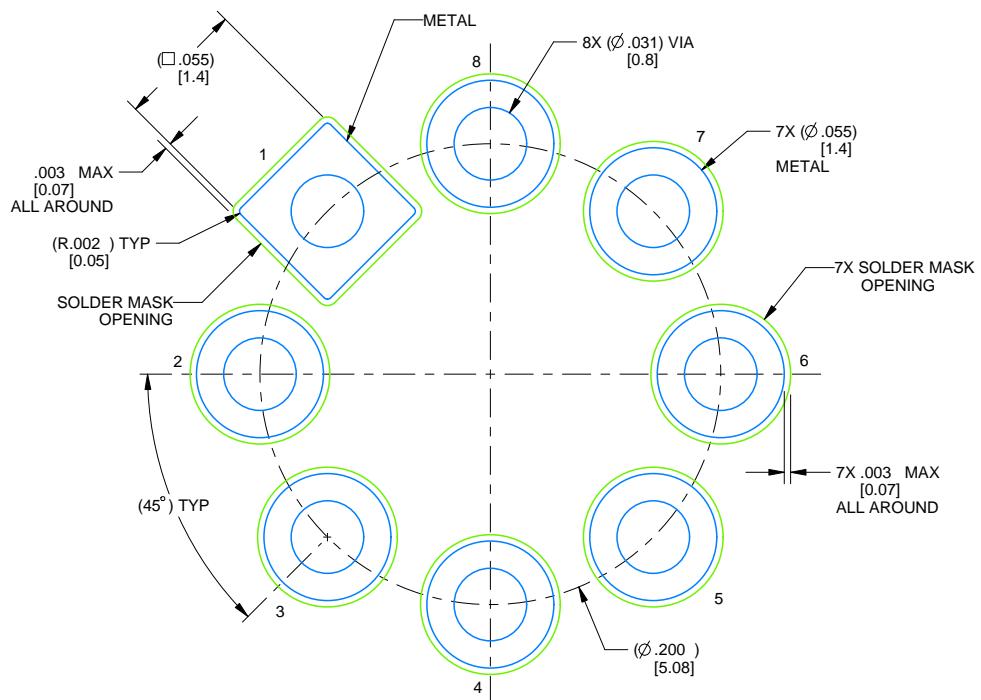
1. All linear dimensions are in inches [millimeters]. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Pin numbers shown for reference only. Numbers may not be marked on package.
4. Reference JEDEC registration MO-002/TO-99.

# EXAMPLE BOARD LAYOUT

LMC0008A

TO-CAN - 5.72 mm max height

TRANSISTOR OUTLINE



LAND PATTERN EXAMPLE  
NON-SOLDER MASK DEFINED  
SCALE: 12X

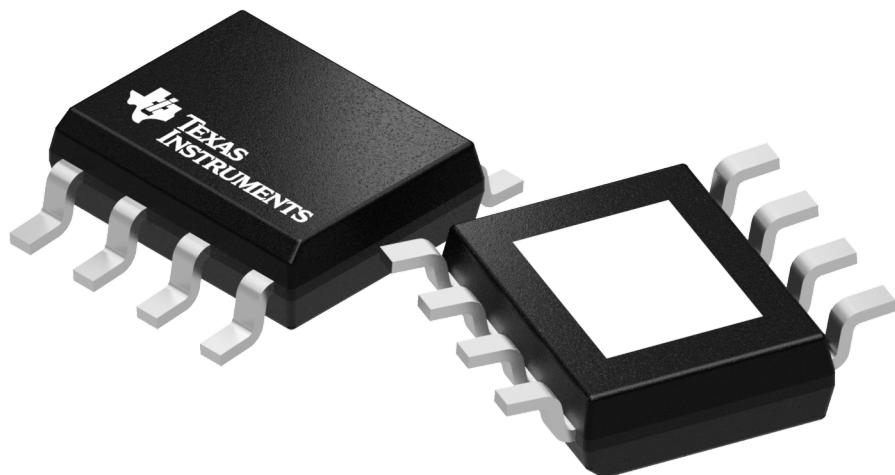
4220610/B 09/2024

## GENERIC PACKAGE VIEW

DDA 8

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4202561/G

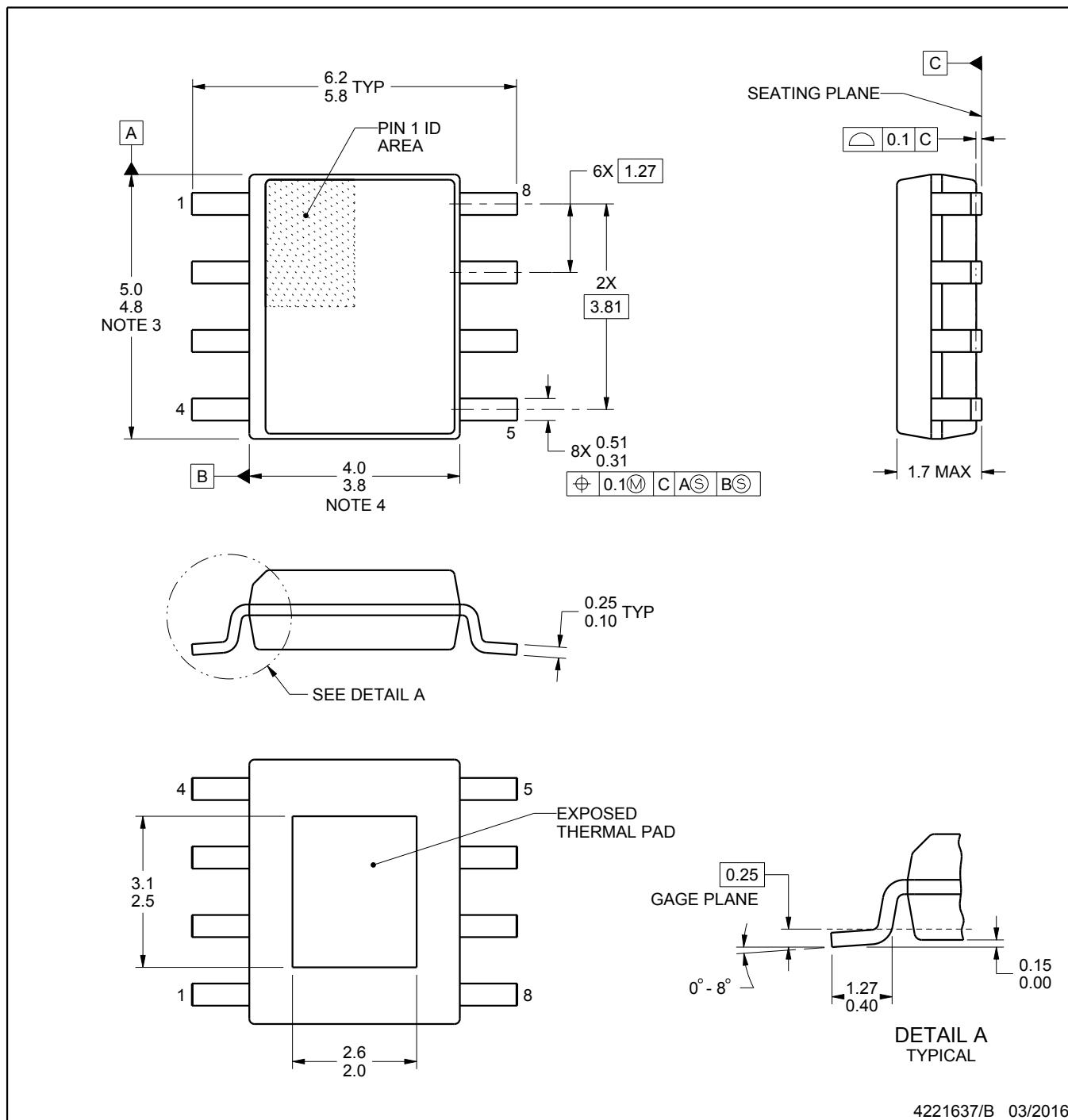
## PACKAGE OUTLINE

DDA0008J



## PowerPAD™ SOIC - 1.7 mm max height

## PLASTIC SMALL OUTLINE



4221637/B 03/2016

PowerPAD is a trademark of Texas Instruments.

## NOTES:

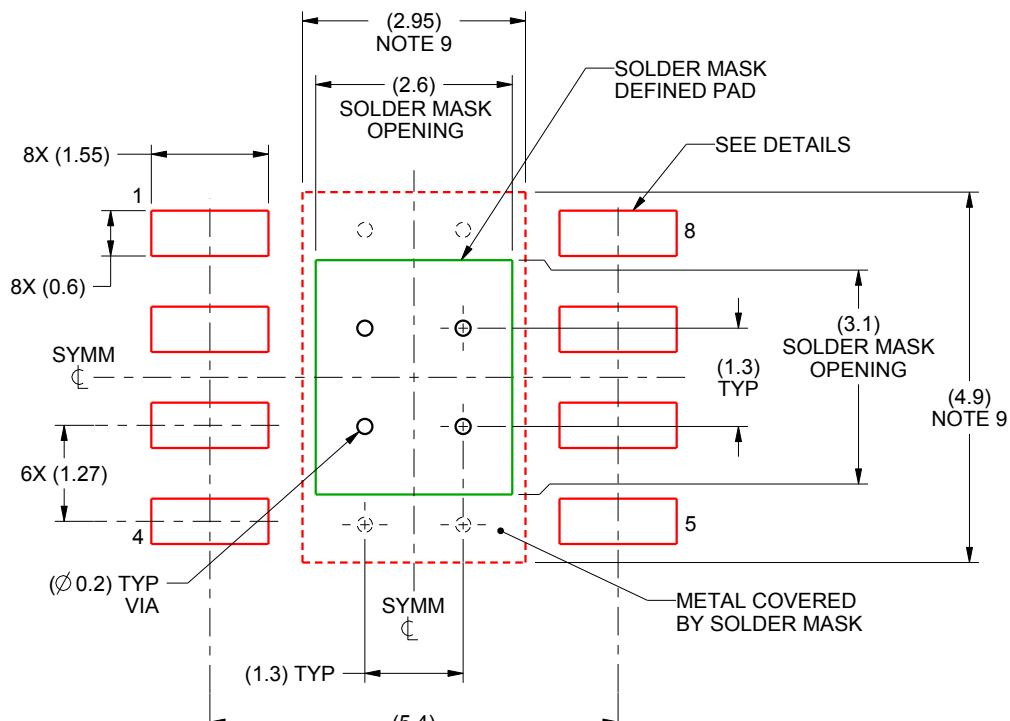
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012, variation BA.

# EXAMPLE BOARD LAYOUT

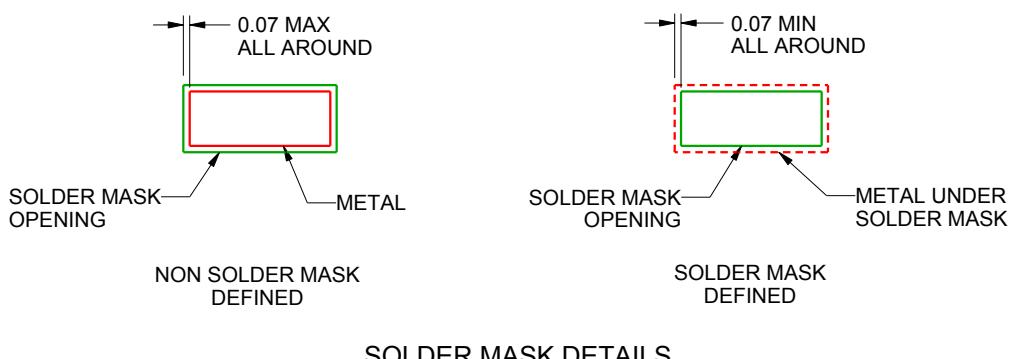
DDA0008J

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE  
SCALE:10X



SOLDER MASK DETAILS

4221637/B 03/2016

NOTES: (continued)

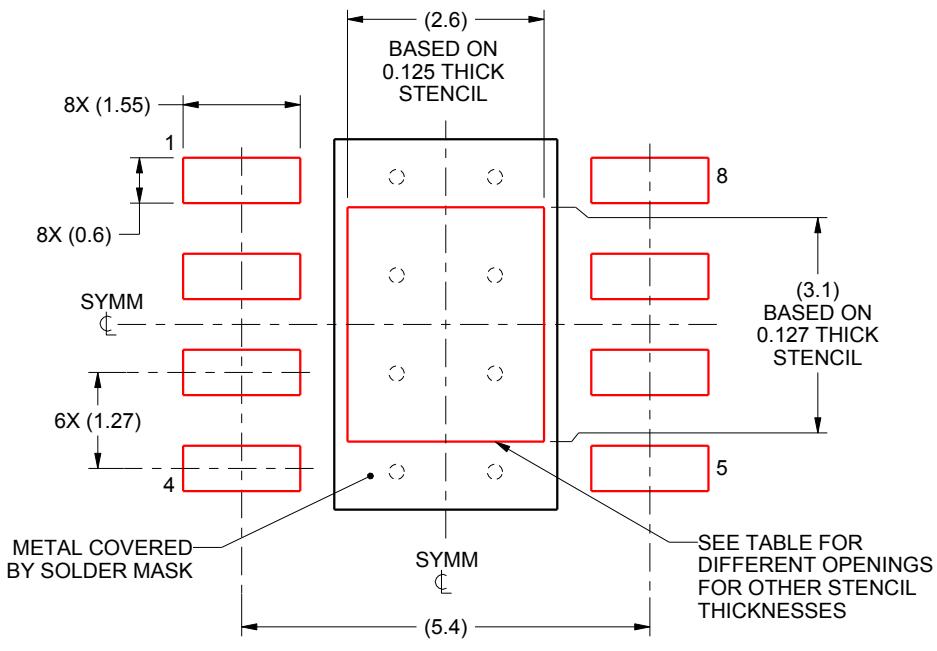
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 ([www.ti.com/lit/slma002](http://www.ti.com/lit/slma002)) and SLMA004 ([www.ti.com/lit/slma004](http://www.ti.com/lit/slma004)).
9. Size of metal pad may vary due to creepage requirement.

## EXAMPLE STENCIL DESIGN

**DDA0008J**

## PowerPAD™ SOIC - 1.7 mm max height

## PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE  
EXPOSED PAD  
100% PRINTED SOLDER COVERAGE BY AREA  
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.91 X 3.47
0.125	2.6 X 3.1 (SHOWN)
0.150	2.37 X 2.83
0.175	2.20 X 2.62

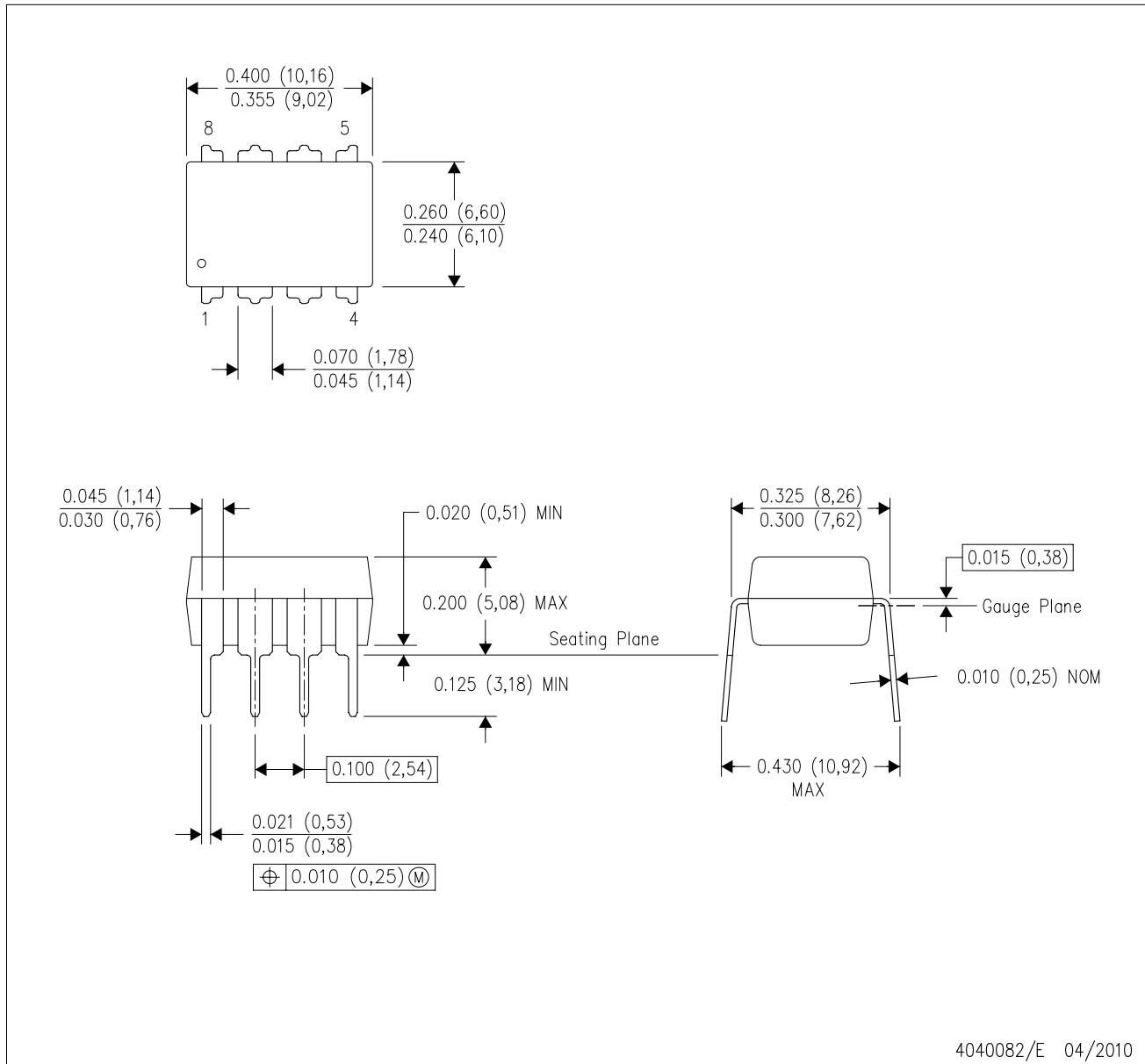
4221637/B 03/2016

#### NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Falls within JEDEC MS-001 variation BA.

4040082/E 04/2010

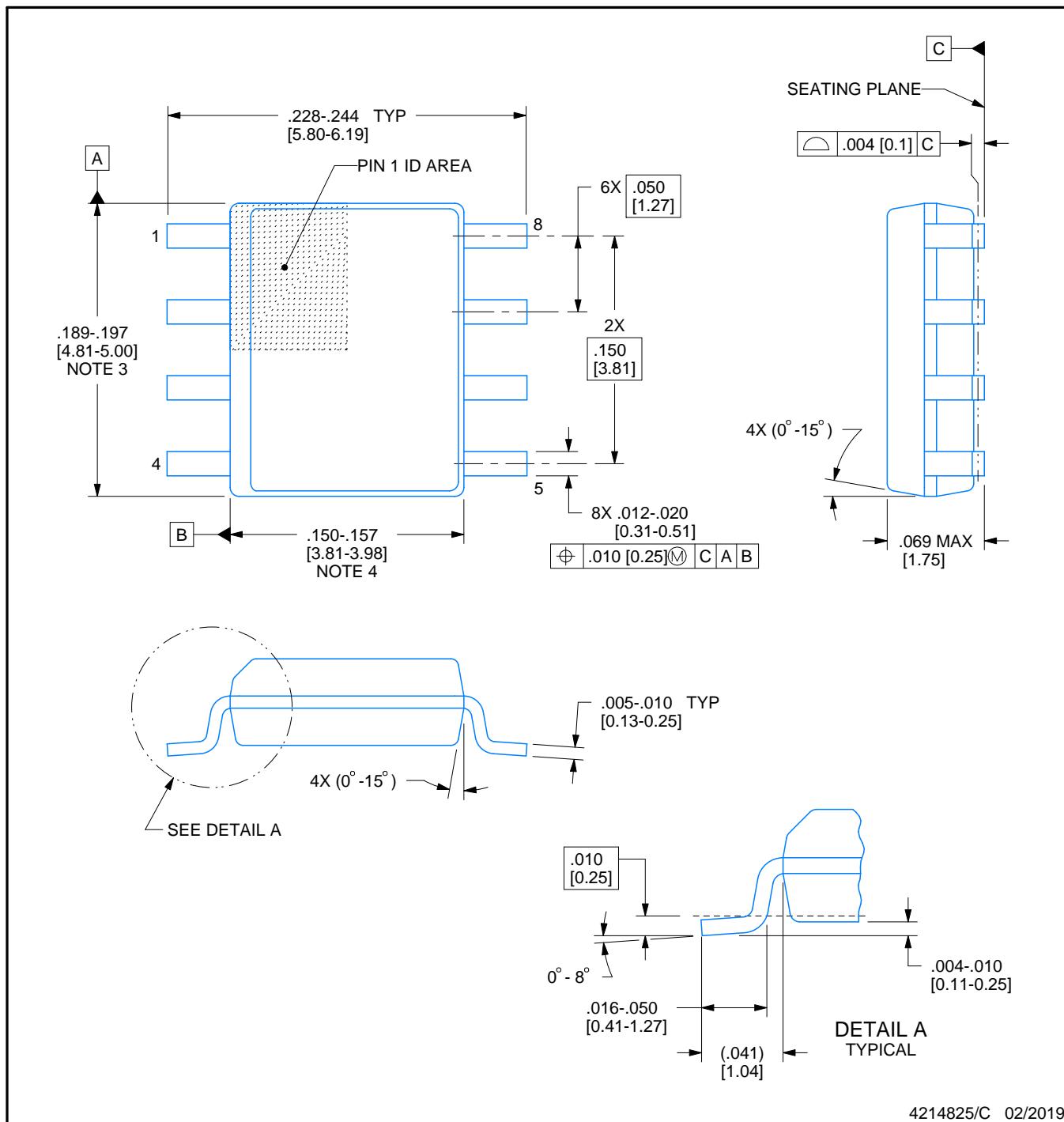


# PACKAGE OUTLINE

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



## NOTES:

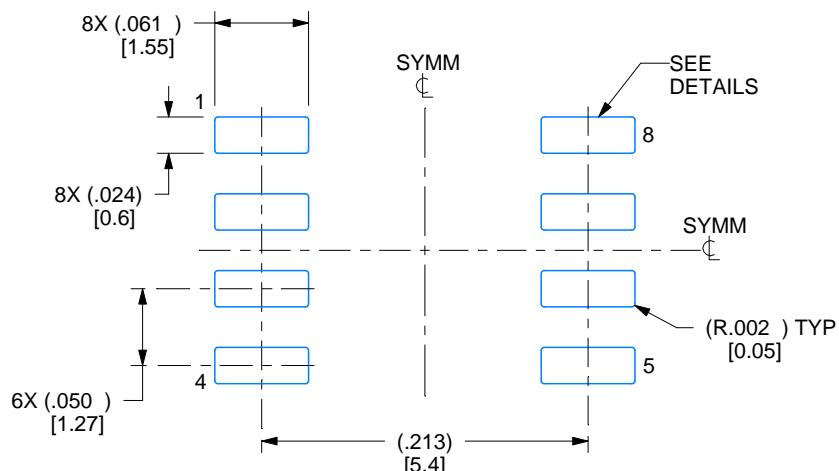
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

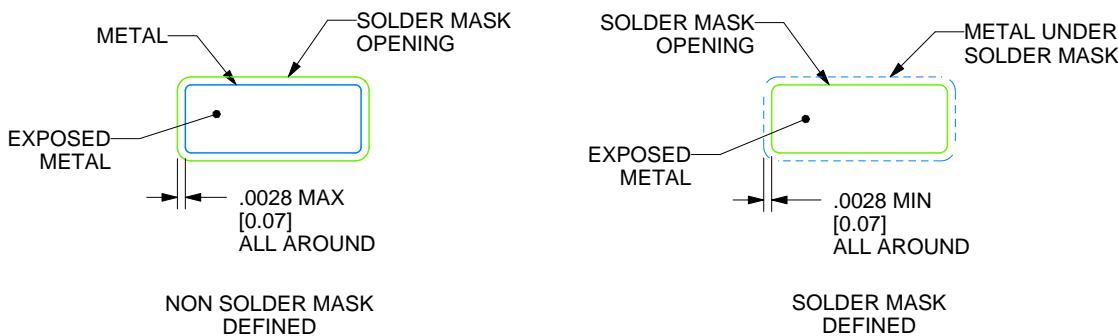
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

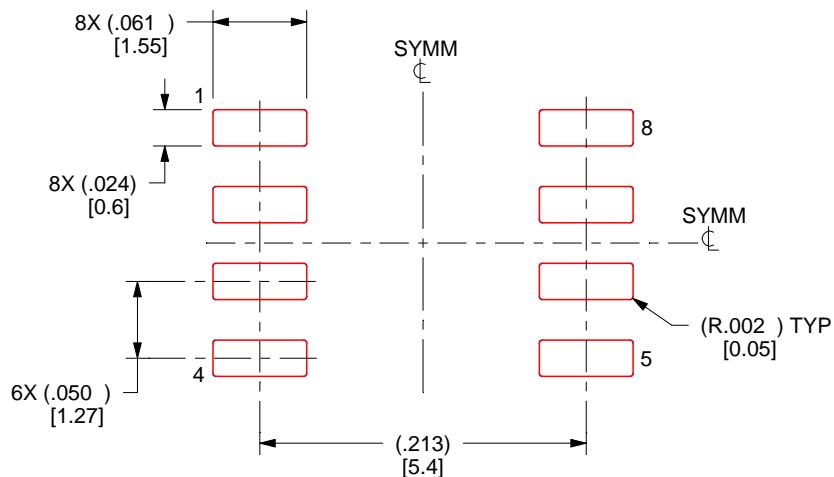
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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