SIEMENS

Data Communications ICs

High-Level Serial Communication Controller Extended (HSCX)
SAB 82525; SAB 82526
SAF 82525; SAF 82526

User's Manual 10.94

SAB 82525; SAF 82525; SAB 82526; SAF 82526 Revision History: 10.94	
Previous Releases: 01.92	
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	Update

Data Classification

Maximum Ratings

Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

Characteristics

The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at T_A = 25 °C and the given supply voltage.

Operating Range

In the operating range the functions given in the circuit description are fulfilled.

For detailed technical information about "**Processing Guidelines**" and "**Quality Assurance**" for ICs, see our "**Product Overview**".

Edition 10.94

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Table of Contents **Page**

1 Features ... 6
1.1 Pin Definitions and Functions ... 10
1.2 System Integration ... 17
1.3 Functional Description ... 22
2 Operating Modes ... 24
2.1 Auto-Mode (MODE: MDS1, MDS0 = 00) ... 24
2.2 Non-Auto Mode (MODE: MDS1, MDS0 = 01) ... 24
2.3 Transparent Mode 1 (MODE: MDS1, MDS0, ADM = 101) ... 25
2.4 Transparent Mode 0 (MODE: MDS1, MDS0, ADM = 100) ... 25
2.5 Extended Transparent Modes 0; 1 (MODE: MDS1, MDS0 = 11) ... 25
2.6 Receive Data Flow (Summary) ... 26
2.7 Transmit Data Flow ... 27
3 Procedural Support (Layer-2 Functions) ... 28
3.1 Full-Duplex LAPB/LAPD Operation ... 28
3.2 Half-Duplex SDLC-NRM Operation ... 34
3.3 Error Handling ... 38
4 CPU Interface ... 38
4.1 Register Set ... 38
4.2 Data Transfer Modes ... 38
4.3 Interrupt Interface ... 39
4.4 DMA Interface ... 43
4.5 FIFO Structure ... 47
5 Serial Interface (Layer-1 Functions) ... 49
5.1 Clock Modes ... 49
5.2 Clock Recovery (DPLL) ... 57
5.3 Bus Configuration ... 60
5.4 Data Encoding ... 63
5.5 Modem Control Functions (RTS/CTS, CD) ... 63
6 Special Functions ... 65
6.1 Fully Transparent Transmission and Reception ... 65
6.2 Cyclic Transmission (Fully Transparent) ... 65
6.3 Continuous Transmission (DMA Mode only) ... 66
6.4 Receive Length Check Feature ... 66
6.5 One Bit Insertion ... 67
6.6 Data Inversion ... 67

Table of Contents **Page**

6.8 Test Mode 68
6.7 Special RTS Function 68
7 Operational Description 69
7.1 RESET 69
7.2 Initialization 70
7.3 Operational Phase 71
7.4 Data Transmission 71
7.5 Data Reception 75
8 Detailed Register Description 79
8.1 Register Address Arrangement 79
8.2 Register Definitions 80
9 Electrical Characteristics 108
10 Quartz Specifications 118
11 Package Outlines 125

The SAB 82525 is a High-Level Serial Communication Controller compatible to the SAB 82520 HSCC with extended features and functionality (HSCX).

The SAB 82526 is pin and software compatible to the SAB 82525, realizing one HDLC channel (channel B).

The HSCX has been designed to implement high-speed communication links using HDLC protocols and to reduce the hardware and software overhead needed for serial synchronous communications.

Due to its 8-bit demultiplexed adaptive bus interface it fits perfectly into every Siemens/Intel or Motorola 8- or 16-bit microcontroller or microprocessor system. The data through-put from/to system memory is optimized transferring blocks of data (usually 32 bytes) by means of DMA or interrupt request. Together with the storing capacity of up to 64 bytes in on-chip FIFO's, the serial interfaces are effectively decoupled from the system bus which drastically reduces the dynamic load and reaction time of the CPU.

The HSCX directly supports the X.25 LAPB, the ISDN LAPD, and SDLC (normal response mode) protocols and is capable of handling a large set of layer-2 protocol functions independently from the host processor.

Furthermore, the HSCX opens a wide area for applications which use time division multiplex methods (e.g. time-slot oriented PCM systems, systems designed for packet switching, ISDN applications) by its programmable telecom-specific features.

The HSCX is fabricated using Siemens advanced ACMOS 3 technology and available in a P-LCC-44 pin package.

The data link controller handles all functions necessary to establish and maintain an HDLC data link, such as

– Flag insertion and detection,
– Bit stuffing,
– CRC generation and checking,
– Address field recognition.

Associated with each serial channel is a set of independent command and status registers (SP-REG) and 64-byte deep FIFO's for transmit and receive direction.

DMA capability has been added to the HSCX by means of a 4-channel DMA interface (SAB 82525) with one DMA request line for each transmitter and receiver of both channels.

General

- Advanced CMOS technology
- Low power consumption: active 25 mW at 4 MHz
  standby 4 mW

SIEMENS

SAB 82525
SAB 82526
SAF 82525
SAF 82526

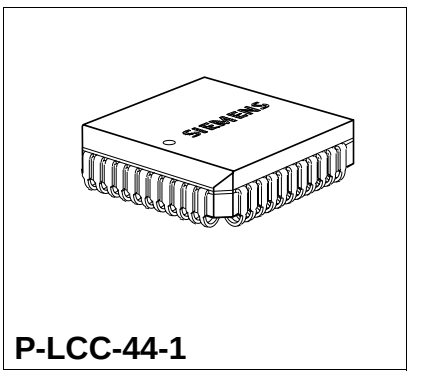
High-Level Serial Communications Controller Extended (HSCX)

Preliminary Data **CMOS IC**

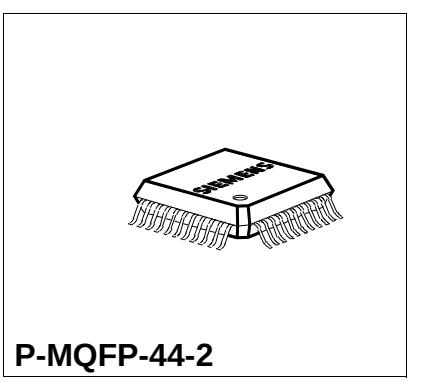
1 Features

Serial Interface

- Two independent full-duplex HDLC channels (SAB 82526: one channel)
  - On chip clock generation or external clock source
  - On chip DPLL for clock recovery for each channel
  - Two independent baudrate generators (SAB 82526: one baudrate generator)
  - Independent time-slot assignment for each channel with programmable time-slot length (1-256 bit)
- Different modes of data encoding
- Modem control lines (RTS, CTS, CD)
- Support of bus configuration by collision resolution
- Programmable bit inversion
- Transparent receive/transmit of data bytes without HDLC framing
- Continuous transmission of 1 to 32 bytes possible
- Data rate up to 4 Mbit/s



P-LCC-44-1



P-MQFP-44-2

Type	Ordering Code	Package
SAB 82525 N	Q67100-H6486	P-LCC-44-1 (SMD)
SAB 82526 N	Q67100-H6512	P-LCC-44-1 (SMD)
SAF 82525 N	Q67100-H6504	P-LCC-44-1 (SMD)
SAF 82526 N	Q67100-H6511	P-LCC-44-1 (SMD)
SAB 82525 H	Q67101-H6482	P-MQFP-44-2 (SMD)

Features (cont'd)

Protocol Support

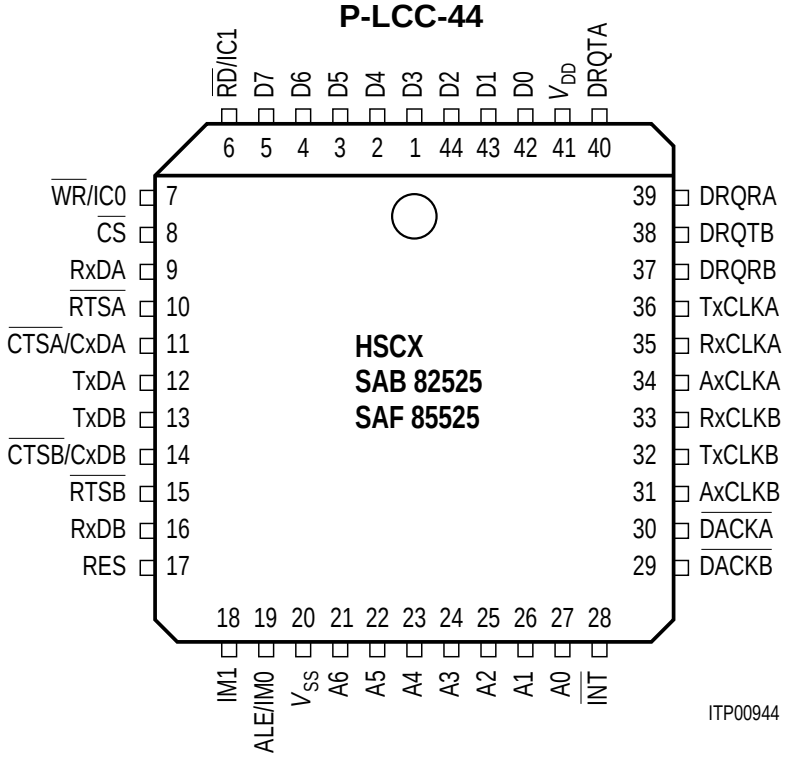
- Various types of protocol support depending on operating mode
  - Auto-mode
  - Non-auto mode
  - Transparent mode
- Handling of bit oriented functions in all modes
- Support of LAPB/LAPD/SDLC/HDLC protocol in auto-mode (I- and S-frame handling)
- Modulo 8 or modulo 128 operation
- Programmable time-out and retry conditions
- Programmable maximum packet size checking

µP Interface

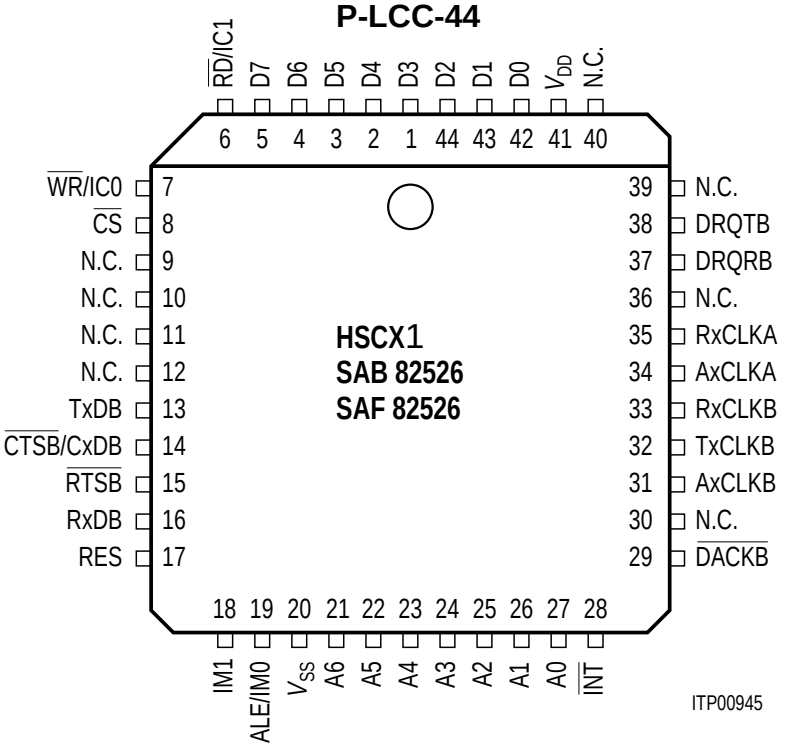
- 64 byte FIFO's per channel and direction
- Storage capacity of up to 17 short frames in receive direction
- Efficient transfer of data blocks from/to system memory by DMA or interrupt request
- 8-bit demultiplexed or multiplexed bus interface
- Intel or Motorola type µP interface

Pin Configurations
(top view)

P-LCC-44

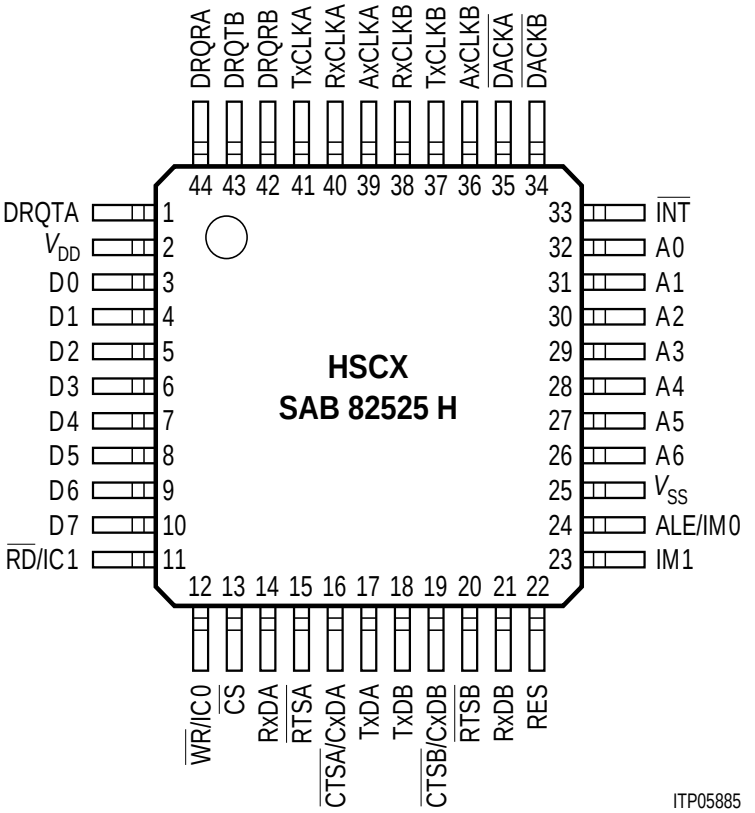


P-LCC-44



Pin Configurations
(top view)

P-MQFP-44-2



1.1 Pin Definitions and Functions

Pin No. P-LCC	Pin No. P-MQFP	Symbol	Input (I) Output (O)	Function
42 43 44 1 2 3 4 5	3 4 5 6 7 8 9 10	D0 D1 D2 D3 D4 D5 D6 D7	I/O	**Data Bus** The data bus lines are bidirectional threestate lines which interface with the system's data bus. These lines carry data and command/status to and from the HSCX.
6	11	$\overline{RD}$/IC1	I	**Read**, Intel bus mode, IM1 connected to low This signal indicates a read operation. When the HSCX is selected via $\overline{CS}$ the read signal enables the bus drivers to put data from an internal register addressed via A0-A6 on the data bus. When the HSCX is selected for DMA transfers via DACK, the RD signal enables the bus driver to put data from the respective receive FIFO on the data bus. Inputs to A0-A6 are ignored. **Input Control 1**, Motorola bus mode IM1 connected to high. If Motorola bus mode has been selected this pin serves either as E = Enable, active high (IM0 tied to low) or DS = Data Strobe, active low (IM0 tied to high) input (depending on the selection via IM0) to control read/ write operations.
7	12	$\overline{WR}$/IC0	I	**Write**, Intel bus mode This signal indicates a write operation. When $\overline{CS}$ is active the HSCX loads an internal register with data provided via the data bus. When DACK is active for DMA transfers the HSCX loads data from the data bus on the top of the respective transmit FIFO. **Input Control** Motorola bus mode In Motorola bus mode, this pin serves as the R/$\overline{W}$ input to distinguish between read or write operations.
8	13	$\overline{CS}$	I	**Chip Select** A low signal selects the HSCX for a read/write operation.

Pin Definitions and Functions (cont'd)

Pin No. P-LCC	Pin No. P-MQFP	Symbol	Input (I) Output (O)	Function
9 16	14 21	RXDA RXDB	I	**Receive Data** (channel A/channel B) Serial data is received on these pins at standard TTL or CMOS levels.
10 15	15 20	$\overline{\text{RTSA}}$ $\overline{\text{RTSB}}$	O	**Request to Send** (channel A/channel B) When the RTS bit in the mode register is set, the RTS signal goes low. When the RTS is reset, the signal goes high if the transmitter has finished and there is no further request for a transmission. In a bus configuration, this pin can be programmed via CCR2 to: – go low during the actual transmission of a frame shifted by one clock period, excluding collision bits – go low during the reception of a data frame – stay always high (RTS disabled).
11 14	16 19	$\overline{\text{CTSA}}$/ CXDA $\overline{\text{CTSB}}$/ CXDB	I	**Clear to Send** (channel A/channel B) A low on the CTS inputs enables the respective transmitter. Additionally, an interrupt may be issued if a state transition occurs at the CTS pin (programmable feature). If no "Clear To Send" function is required, the CTS inputs can be connected directly to V_{SS}. **Collision Data** (channel A/channel B) In a bus configuration, the external serial bus must be connected to the respective C × D pin for collision detection.
12 13	17 18	TXDA TXDB	O	**Transmit Data** (channel A/channel B) Transmit data is shifted out via these pins at standard TTL or CMOS levels. These pins can be programmed to work either as push-pull, or open drain outputs supporting bus configurations.
17	22	RES	I	**RESET** A high signal on this input forces the HSCX into the reset state. The HSCX is in power-up mode during reset and in power-down mode after reset. The minimum pulse width is 1.8 µs.

Pin Definitions and Functions (cont'd)

Pin No. P-LCC	Pin No. P-MQFP	Symbol	Input (I) Output (O)	Function
18	23	IM1	I	**Input Mode 1** Connecting this pin to either V_{SS} or V_{DD} the bus interface can be adapted to either Siemens/Intel or Motorola environment. IM1 = LOW: Intel bus mode IM1 = HIGH: Motorola bus mode
19	24	ALE/ IM0	I	**Address Latch Enable** (Intel bus mode) A high on this line indicates an address on the external address/data bus, which will select one of the HSCX's internal registers. The address is latched by the HSCX with the falling edge of ALE. This allows the HSCX to be directly connected to a CPU with multiplexed address/data bus compatible to SAB 82520 HSCC. The address input pins A0-A6 must be externally connected to the data bus pins (D0-D6 for 8-bit CPU's, D1-D7 for 16-bit CPU's, i.e. multiply all internal register addresses by 2). This pin should be connected to high for a de-multiplexed bus. **Input Mode 0**, Motorola bus mode In Motorola Bus Mode, the level at this pin determines the function of the IC1 pin (see description of pin 6).
20	25	V_{SS}	I	**Ground**
27 26 25 24 23 22 21	32 31 30 29 28 27 26	A0 A1 A2 A3 A4 A5 A6	I	**Address Bus** These inputs interface with seven bits of the system's address bus to select one of the internal registers for read or write. They are usually connected at A0-A6 in 8-bit systems or at A1-A7 in 16-bit systems.

Pin Definitions and Functions (cont'd)

Pin No. P-LCC	Pin No. P-MQFP	Symbol	Input (I) Output (O)	Function
28	33	$\overline{\text{INT}}$	oD	**Interrupt Request** The signal is activated, when the HSCX requests an interrupt. The CPU may determine the particular source and cause of the interrupt by reading the HSCX's interrupt status registers. (ISTA, EXIR). $\overline{\text{INT}}$ is an open drain output, thus the interrupt requests outputs of several HSCX's can be connected to one interrupt input in a "wired-or" combination. This pin must be connected to a pull-up resistor.
30 29	35 34	$\overline{\text{DACKA}}$ $\overline{\text{DACKB}}$	I	**DMA Acknowledge** (channel A/channel B) When low, this input signal from the DMA controller notifies, the HSCX, that the requested DMA cycle controlled via DRQxx (pins 37–40) is in progress, i.e. the DMA controller has achieved bus mastership from the CPU and will start data transfer cycles (either read or write). Together with $\overline{\text{RD}}$, if DMA has been requested from the receiver, or with $\overline{\text{WR}}$, if DMA has been requested from the transmitter, this input works like $\overline{\text{CS}}$ to enable a data byte to be read from or written to the top of the receive or transmit FIFO of the specified channel. If $\overline{\text{DACKn}}$ is active, the input on pins A0–A6 is ignored and the FIFOs are implicitly selected. If the $\overline{\text{DACKn}}$ signals are not used, these pins must be connected to V_{DD}.
34 31	39 36	AxCLK A AxCLK B	I	**Alternative Clock** (channel A/channel B) These pins realize several input functions. Depending on the selected clock mode, they may supply either a – CD (= Carrier Detect) modem control or general purpose input. This pin can be programmed to functions as receiver enable if the "auto start" feature is selected (CAS bit in XBCH set). The state at this pin can be read from VSTR register, – or a receive strobe signal (clock mode 1) – or a frame synchronization signal in time-slot oriented operation mode (clock mode 5) – or, together with RxCLK, a crystal connection for the internal oscillator (clock mode 4, 6, 7, AxCLK A only).

Pin Definitions and Functions (cont'd)

Pin No. P-LCC	Pin No. P-MQFP	Symbol	Input (I) Output (O)	Function
36 32	41 37	TxCLK A TxCLK B	I/O	**Transmit Clock** (channel A/channel B) The functions of these pins depend on the programmed clock mode, provided that the TSS bit in the CCR2 register is reset. Programmed as inputs (if the TIO bit in CCR2 is reset), they may supply either – the transmit clock for the respective channel (clock mode 0, 2, 6), – or a transmit strobe signal (clock mode 1). Programmed as outputs (if the TIO bit in CCR2 is set), the TxCLK pins supply either the – transmit clock of the respective channel which is generated either ● from the baudrate generator (clock mode 2, 6; TSS bit in CCR2 set), ● or from the DPLL circuit (clock mode 3, 7), ● or from the crystal oscillator (clock mode 4) – or a tristate control signal indicating the programmed transmit time-slot (clock mode 5).
35 33	40 38	RxCLK A RxCLK B	I	**Receive Clock** (channel A/channel B) The functions of these pins also depend on the programmed clock mode. In each channel, RxCLK may supply either – the receive clock (clock mode 0) – or the receive and transmit clock (clock mode 1, 5) – or the clock for the baudrate generator (clock mode 2, 3), – or a crystal connection for the internal oscillator (clock mode 4,6,7, RxCLK A/B together with AxCLK A)
39 37	44 42	DRQRA DRQRB	O	**DMA Request Receiver** (channel A/channel B) The receiver of the HSCX requests a DMA data transfer by activating this line. The DRQRn remains high as long as the receive FIFO requires data transfers, thus always blocks of data (32, 16, 8 or 4 bytes) are transferred. DRQRn is deactivated immediately following the falling edge of the last read cycle.

Pin Definitions and Functions (cont'd)

Pin No. P-LCC	Pin No. P-MQFP	Symbol	Input (I) Output (O)	Function
40 38	1 43	DRQTA DRQTB	O	**DMA Request Transmitter** (channel A/channel B) The transmitter of the HSCX requests a DMA data transfer by activating this line. The DRQTn remains high as long as the transmit FIFO requires data transfers. The amount of data bytes to be transferred from system memory to the HSCX (= byte count) must be written first to the XBCH, XBCL registers. Always blocks of data (n x 32 bytes + REST, n = 0, 1,…) are transferred till the byte count is reached. DRQTn is deactivated immediately following the falling edge of the last $\overline{WR}$ cycle.
41	2	V_{DD}	I	Power supply + 5 V.

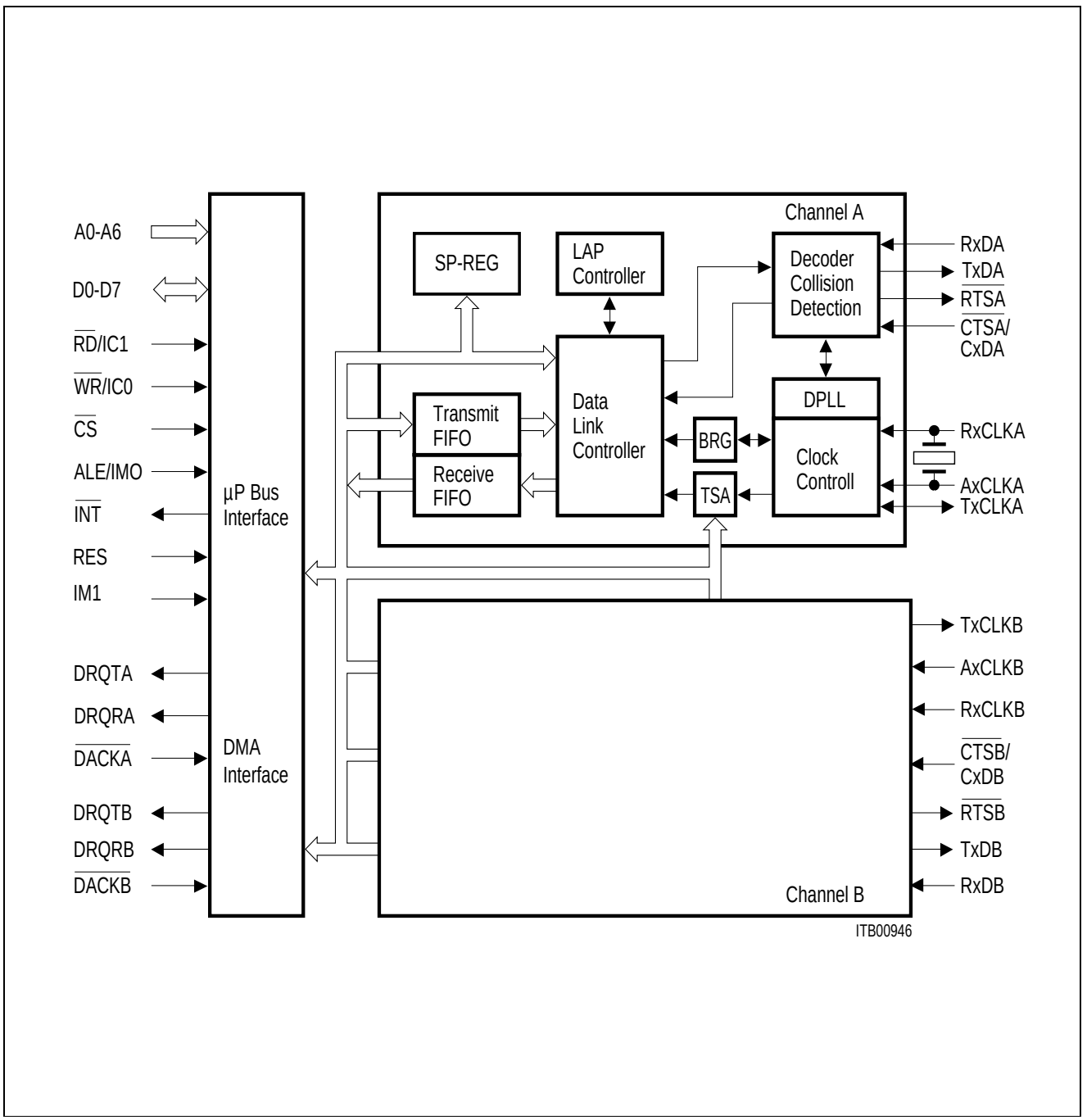


Figure 1
Block Diagram SAB 82525/SAB 82526

The HSCX SAB 82526 comprises one (channel B), the SAB 82525 two completely independent full-duplex HDLC channels (channel A and channel B), supporting various layer-1 functions by means of internal oscillator, Baud Rate Generator (BRG), Digital Phase Locked Loop (DPLL), and Time-Slot Assignment (TSA) circuits.

Furthermore, layer-2 functions are performed by an on-chip LAP (Link Access Procedure, e.g. LAPB or LAPD) controller.

1.2 System Integration

General Aspects

Figure 2 gives a general overview of the system integration of HSCX.

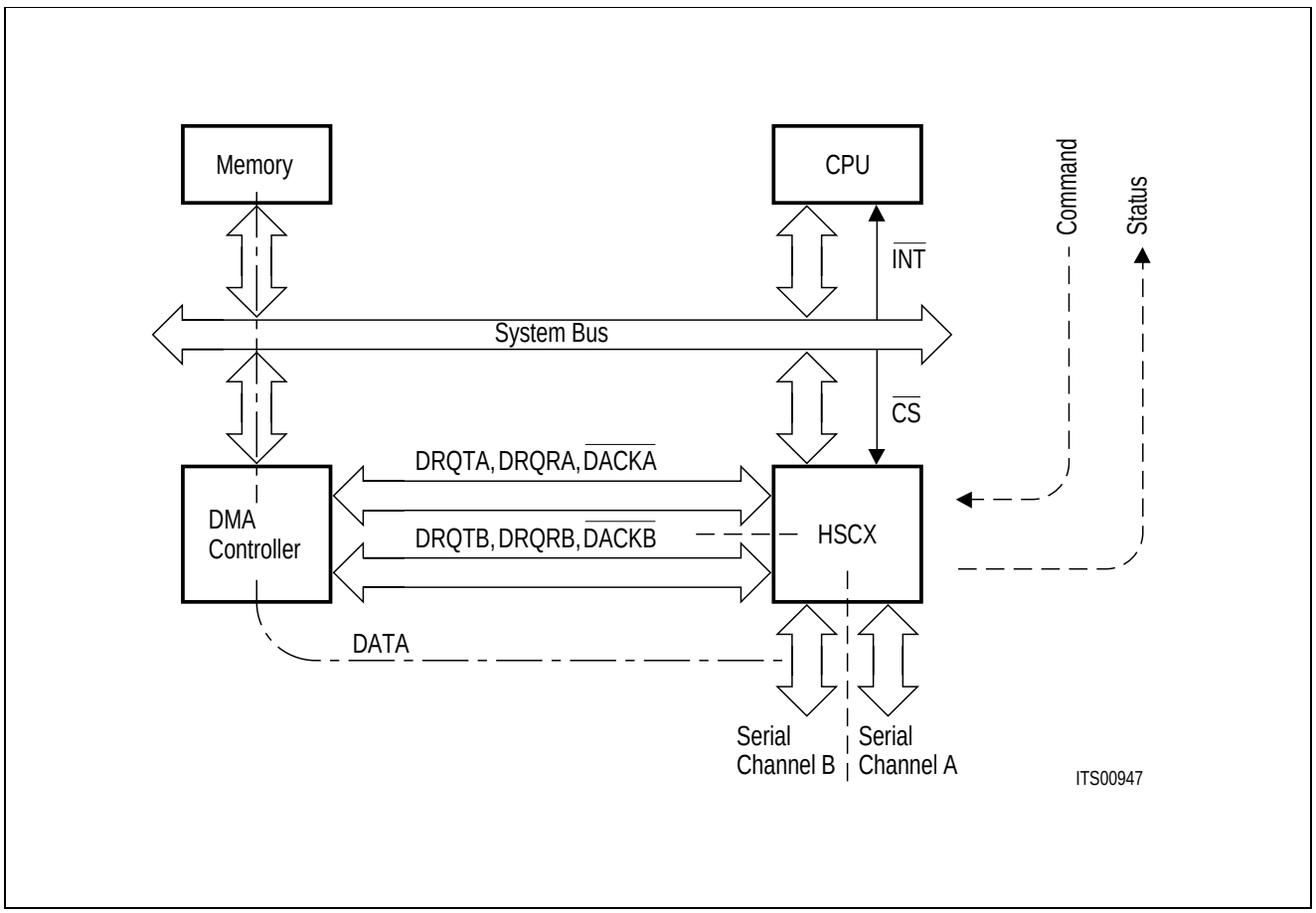


Figure 2
General System Integration of HSCX

The HSCX bus interface consists of an 8-bit bidirectional data bus (D0–D7), seven address line inputs (A0–A6), three control inputs ($\overline{RD}$/DS, $\overline{WR}$/R/$\overline{W}$, $\overline{CS}$), one interrupt request output ($\overline{INT}$) and a 4-channel DMA interface (DRQTA, DRQRA, $\overline{DACKA}$, DRQTB, DRQRB, $\overline{DACKB}$). Mode input pins (strapping options) allow the bus interface to be configured for either Siemens/ Intel or Motorola environment.

Generally, there are two types of transfers occurring via the system bus:

– command/status transfers, which are always controlled by the CPU. The CPU sets the operation mode (initialization), controls function sequences and gets status information by writing or reading the HSCX's registers (via $\overline{CS}$, $\overline{WR}$ or $\overline{RD}$, and register address via A0-A6).
– data transfers, which are effectively performed by DMA without CPU interaction using the HSCX's DMA interface (DMA mode). Optionally, interrupt controlled data transfer can be done by the CPU (interrupt mode).

Specific Applications

HSCX with SAB 8051 Microcontroller

For cost-sensitive applications, the HSCX can be interfaced with a small SAB 8051 microcontroller system (without DMA support) very easily as shown in **figure 3**.

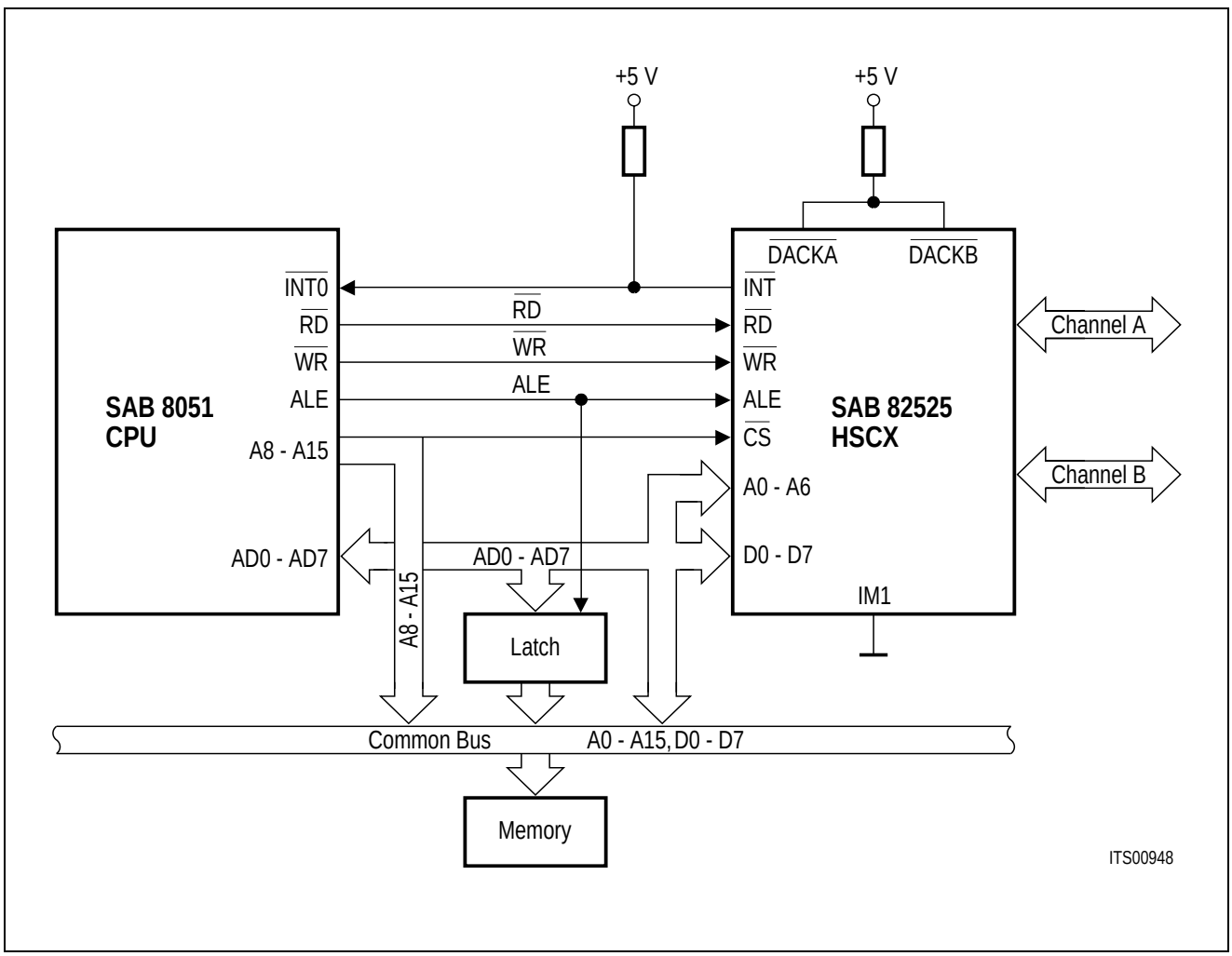


Figure 3
HSCX with 8051 CPU

Although the HSCX provides a demultiplexed bus interface, it can optionally be connected directly to the local multiplexed bus of SAB 8051 because of the internal address latch function (via ALE, compatibility to SAB 82520 HSCC).

The address lines A0 … A6 must be wired externally to the data lines D0 … D6 (direct connection) in this case.

Intel bus mode is selected connecting IM1 pin to low (V_{SS}). Since data transfer is controlled by interrupt, the DMA acknowledge inputs ($\overline{DACKA}$, $\overline{DACKB}$) are connected to V_{DD} (+ 5 V).

HSCX with SAB 80188 Microprocessor

A system with minimized additional hardware expense can be with a SAB 80188 microprocessor as shown in **figure 4.**

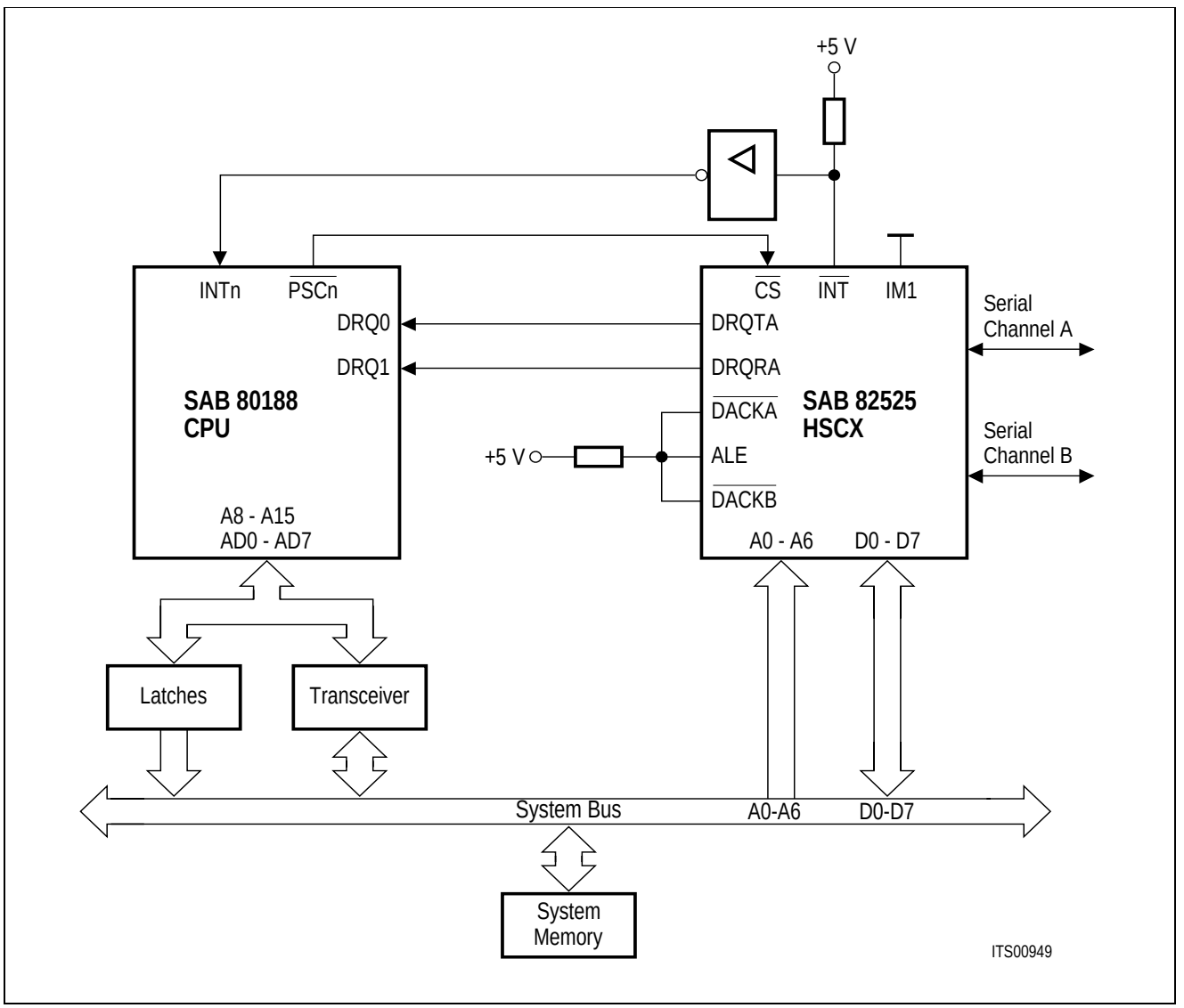


Figure 4
HSCX with SAB 80188 CPU

The HSCX is connected to the demultiplexed system bus. Data transfer for one serial channel can be done by the 2-channel on-chip DMA controller of the SAB 80188, the other channel is serviced by interrupt. Since the SAB 80188 does not provide DMA acknowledge outputs, data transfer from/to HSCX is controlled via $\overline{CS}$, $\overline{RD}$ or $\overline{WR}$ address information (A0 … A6) and the $\overline{DACKA}$, $\overline{DACKB}$ inputs are not used.

This solution supports applications with a high speed data rate in one serial channel with minimum hardware expense making use of the on-chip peripheral functions of the SAB 80188 (chip select logic, interrupt controller, DMA controller).

HSCX with SAB 80186 Microprocessor and SAB 82258 Advanced DMA Controller (ADMA)

In applications, where two high-speed channels are required, a 16-bit system with SAB 80186 CPU and SAB 82258 ADMA is suitable. This is shown in **figure 5.**

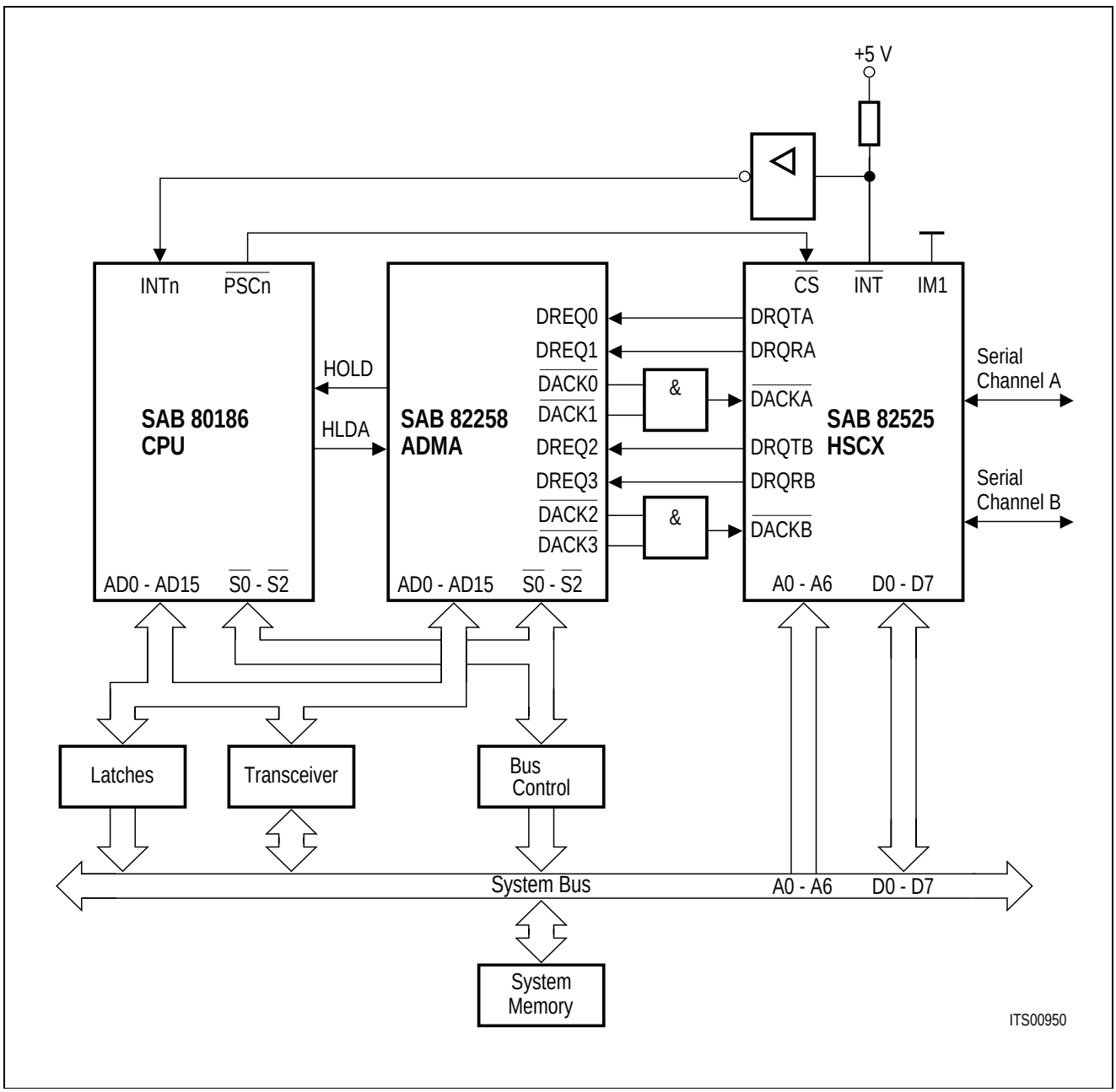


Figure 5
HSCX with SAB 80186 CPU/SAB 82258 ADMA

The four selector channels of ADMA are used for serving the four DMA request sources of HSCX, allowing very high data rates at both the system bus and the serial channels.

Another big advantage of the ADMA is it's data chaining feature, providing an optimized memory management for receive and transmit data. Recording the HSCX, a linked chain of 32 byte deep buffers can be set up, which are subsequently filled with the contents of the HSCX's FIFOs during reception. Not used buffers can be saved and linked to another buffer chain reserved for the reception of the next frame.

As a result, it's not necessary to reserve a very large space in system memory, determined by the maximum frame length of every received frame.

In this example, the ADMA works directly at the CPU's local bus and shares the same bus interface logic (address latches, transceivers, bus controller) with the SAB 80186. Since one DMA acknowledge line is provided for each DMA request, two DACK outputs must be ANDed together for input to the HSCX.

The HSCX's data lines are connected to the lower half of the system data bus (D0 … D7) and the address lines to A1 … A7, thus (from the CPU's point of view) all internal register addresses must be multiplied by two (even register addresses only).
e.g. CMDR register: HSCX address 61_H < = > system address $C2_H$.

1.3 Functional Description

General

The HSCX distinguishes from other low level HDLC devices by its advanced characteristics. The most important are:

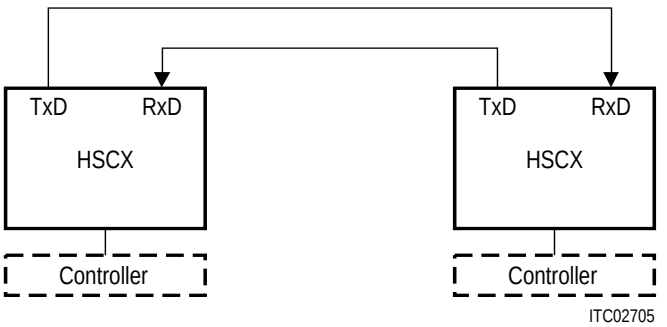
- Enlarged support of link configurations.

Beyond the point-to-point configurations, the HSCX directly enables point-to-multipoint or multimaster configurations without additional hardware or software expense.

In point-to-multipoint configurations, the HSCX can be used as a master as well as a slave station. Even when working as slave station, the HSCX can initiate the transmission of data at any time. An internal function block provides means of idle and collision detection and collision resolution, which are necessary if several stations start transmitting simultaneously.

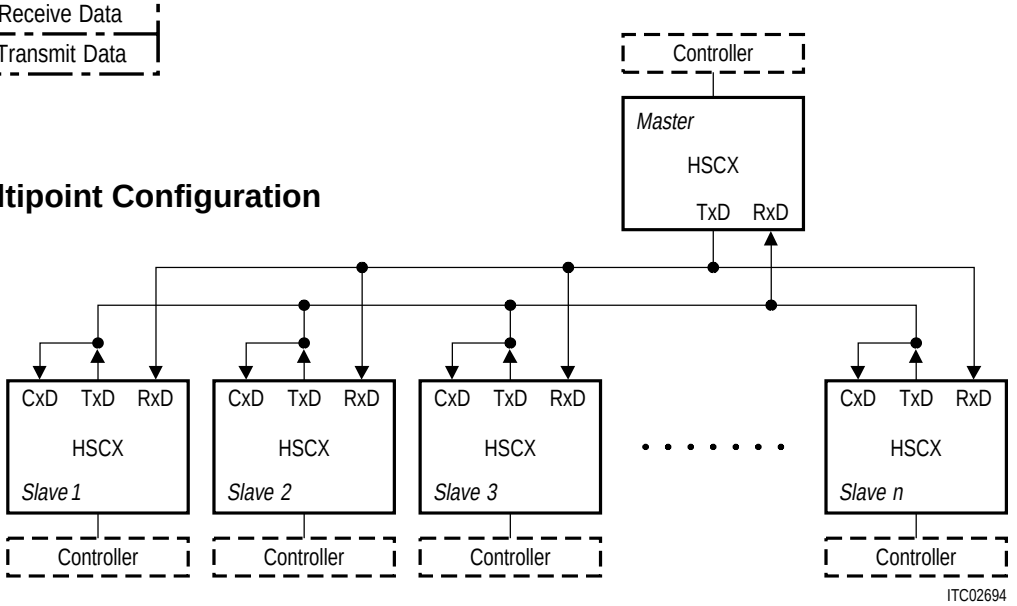
These features were integrated to support multimaster configurations.

Point-to-Point Configuration



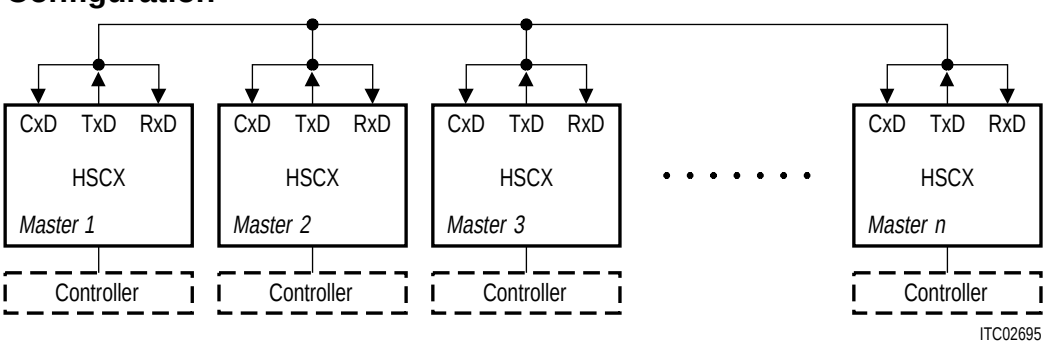
RxD - Receive Data
TxD - Transmit Data

Point-to-Multipoint Configuration



RxD - Receive Data
CxD - Collision Data
TxD - Transmit Data

Multimaster Configuration



RxD - Receive Data
CxD - Collision Data
TxD - Transmit Data

Figure 6
Link Configuration

- Support of layer-2 functions by HSCX

Beside those bit-oriented functions usually supported with the HDLC protocol, such as bit stuffing, CRC check, flag and address recognition, the HSCX provides a high degree of procedural support. In a special operating mode (auto-mode), the HSCX processes the information transfer and the procedure handshaking (I-, and S-frames of HDLC protocol) autonomously. The only restriction is, that the window size (= number of outstanding unacknowledged frames) is limited to 1, which will be sufficient in most applications. The communication procedures are mainly processed between the communication controllers and not between the processors. Thus the dynamic load of the CPU and the software expense is largely reduced.

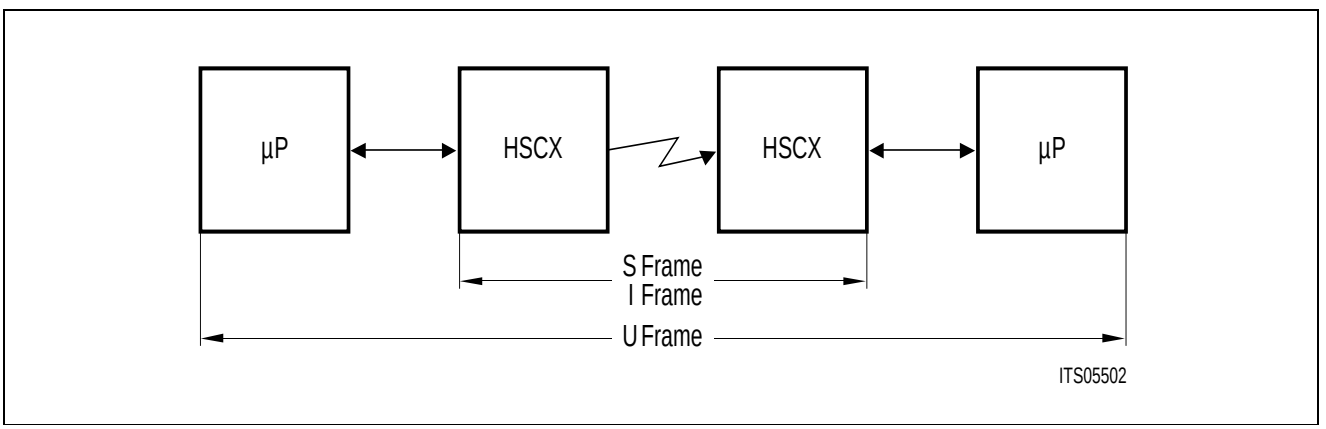


Figure 7
Procedural Support in Auto-Mode

The CPU is informed about the status of the procedure and has to manage the receive and transmit data mainly. In order to maintain cost effectiveness and flexibility, such functions as link setup/disconnection and error recovery in case of protocol errors (U-frames of HDLC protocols) are not implemented in hardware and must be done by user's software.

- Telecom specific features

In a special operating mode, the HSCX can transmit or receive data packets in one of up to 64 time-slots of programmable width (clock mode 5). Furthermore, the HSCX can transmit or receive variable data portions within a defined window of one or more clock cycles, which has to be selected by an external strobe signal (clock mode 1). These features make the HSCX especially suitable for all applications using time division multiplex methods, such as time-slot oriented PCM systems, systems designed for packet switching, or in ISDN applications.

- FIFO buffers to efficient transfer of data packets.

A further speciality of HSCX are the FIFO buffers used for the temporary storage of data packets transferred between the serial communications interface and the parallel system bus. Also because of the overlapping input/output operation (dual-port behaviour), the maximum message length is not limited by the size of the buffer. Together with the DMA capability, the dynamic load of the CPU is drastically reduced by transferring the data packets block by block via direct memory access. The CPU only has to initiate the data transmission by the HSCX and determine the status in case of completely received frames, but is not involved in data transfers.

2 Operating Modes

The HDLC controller of each channel can be programmed to operate in various modes, which are different in the treatment of the HDLC frame in receive direction. Thus, the receive data flow and the address recognition features can be effected in a very flexible way, which satisfies most requirements.

There are 6 different operating modes which can be set via the MODE register.

2.1 Auto-Mode (MODE: MDS1, MDS0 = 00)

Characteristics: Window size 1, arbitrary message length, address recognition.

The HSCX processes autonomously all numbered frames (S-, I-frames) of an HDLC procedure.

The HDLC control field, data in the I-field of the frames and an additional status byte is temporarily stored in the RFIFO. The HDLC control field as well as additional information can also be read from special registers (RHCR, RSTA).

According to the selected address mode, the HSCX can perform a 2-byte or 1-byte address recognition. If a 2-byte address field is selected, the high address byte is compared with the fixed value FE_H or FC_H (group address) as well as with two individually programmable values in RAH1 and RAH2 registers. According to the ISDN LAPD protocol, bit 1 of the high byte address will be interpreted as COMMAND/RESPONSE bit (C/R), dependent on the setting of the CRI bit in RAH1, and will be excluded from the address comparison.

Similary, two compare values can be programmed in special registers (RAL1, RAL2) for the low address byte. A valid address will be recognized in case the high and low byte of the address field correspond to one of the compare values. Thus, the HSCX can be called (addressed) with 6 different address combinations, however, only the logical connection identified through the address combination RAH1, RAL1 will be processed in the auto-mode, all others in the non-auto mode. HDLC frames with address fields that do not match with any of the address combinations, are ignored by the HSCX.

In case of a 1-byte address, RAL1 and RAL2 will be used as compare registers. According to the X.25 LAPB protocol, the value in RAL1 will be interpreted as COMMAND and the value in RAL2 as RESPONSE.
After receiving a frame it takes 5 clock cycles to generate the response frame and to start transmission.

2.2 Non-Auto Mode (MODE: MDS1, MDS0 = 01)

Characteristics: address recognition, arbitrary window size.

All frames with valid addresses (address recognition identical to auto-mode) are forwarded directly to the system memory.

The HDLC control field, data in the I-field and an additional status byte are temporarily stored in the RFIFO. The HDLC control field and additional information can also be read from special registers (RHCR, RSTA).

In non-auto mode, all frames are treated similarly.

2.3 Transparent Mode 1 (MODE: MDS1, MDS0, ADM = 101)

Characteristics: address recognition high byte

Only the high byte of a 2-byte address field will be compared. The whole frame except the first address byte will be stored in RFIFO. RAL1 contains the second and RHCR the third byte following the opening flag.

2.4 Transparent Mode 0 (MODE: MDS1, MDS0, ADM = 100)

Characteristics: no address recognition

No address recognition is performed and each frame will be stored in the RFIFO. RAL1 contains the first and RHCR the second byte following the opening flag.

2.5 Extended Transparent Modes 0; 1 (MODE: MDS1, MDS0 = 11)

Characteristics: fully transparent

In extended transparent modes, fully transparent data transmission/reception without HDLC framing is performed, i.e. without FLAG generation/recognition, CRC generation/check, bit-stuffing mechanism. This allows user specific protocol variations or the usage of Character Oriented Protocols (such as IBM BISYNC).

Data transmission is always performed out of the XFIFO. In extended transparent mode 0 (ADM = 0), data reception is done via the RAL1 register, which always contains the actual data byte assembled at the RxD pin. In extended transparent mode 1 (ADM = 1), the receive data are additional shifted into the RFIFO.
Also refer to chapter 6.1 and 6.2.

2.6 Receive Data Flow (Summary)

The following figure gives an overview of the management of the received HDLC frames as affected by different operating modes.

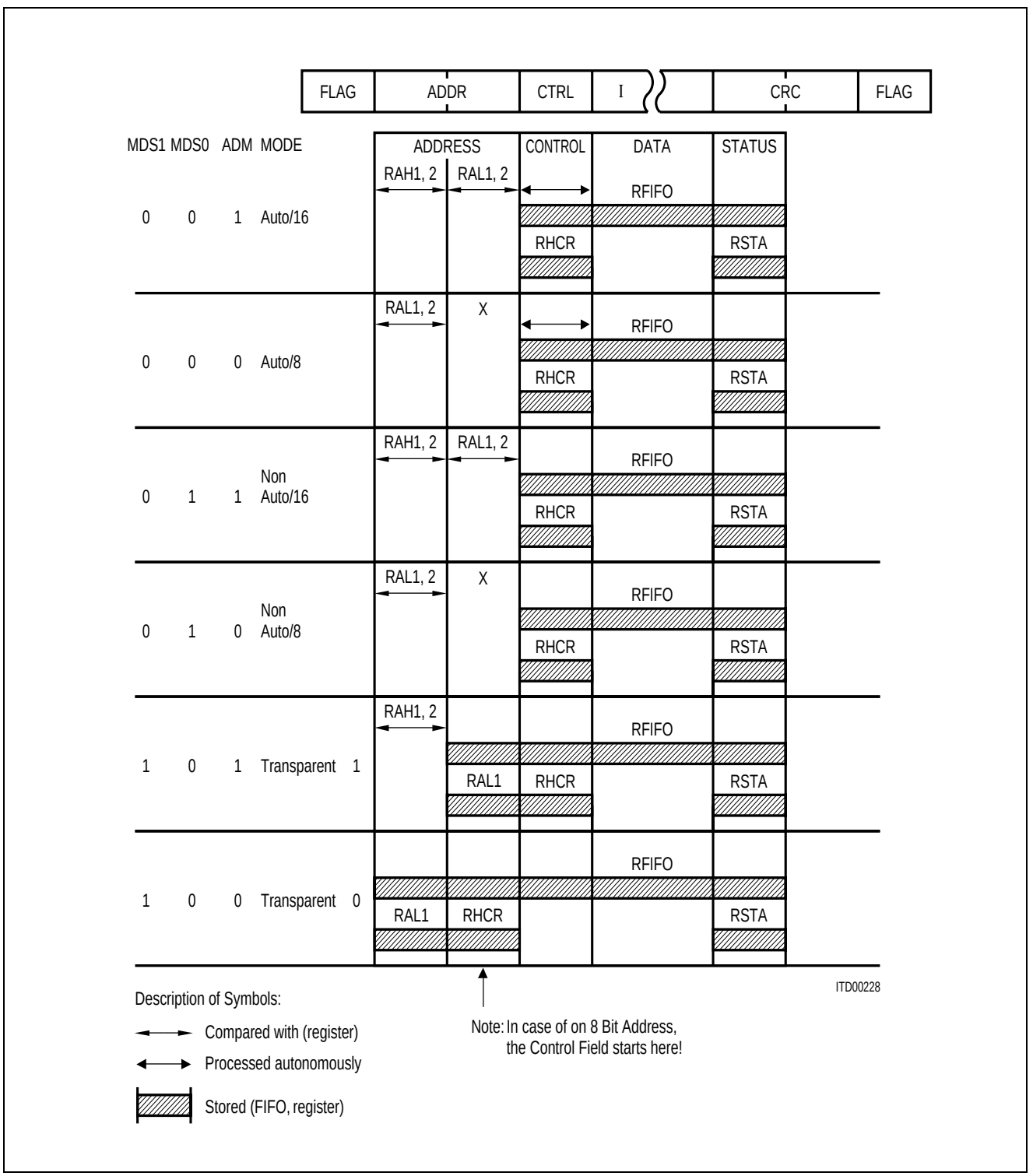


Figure 8
Receive Data Flow of HSCX

2.7 Transmit Data Flow

Two different types of frames can be transmitted:

– I-frames and

– transparent frames

as shown below.

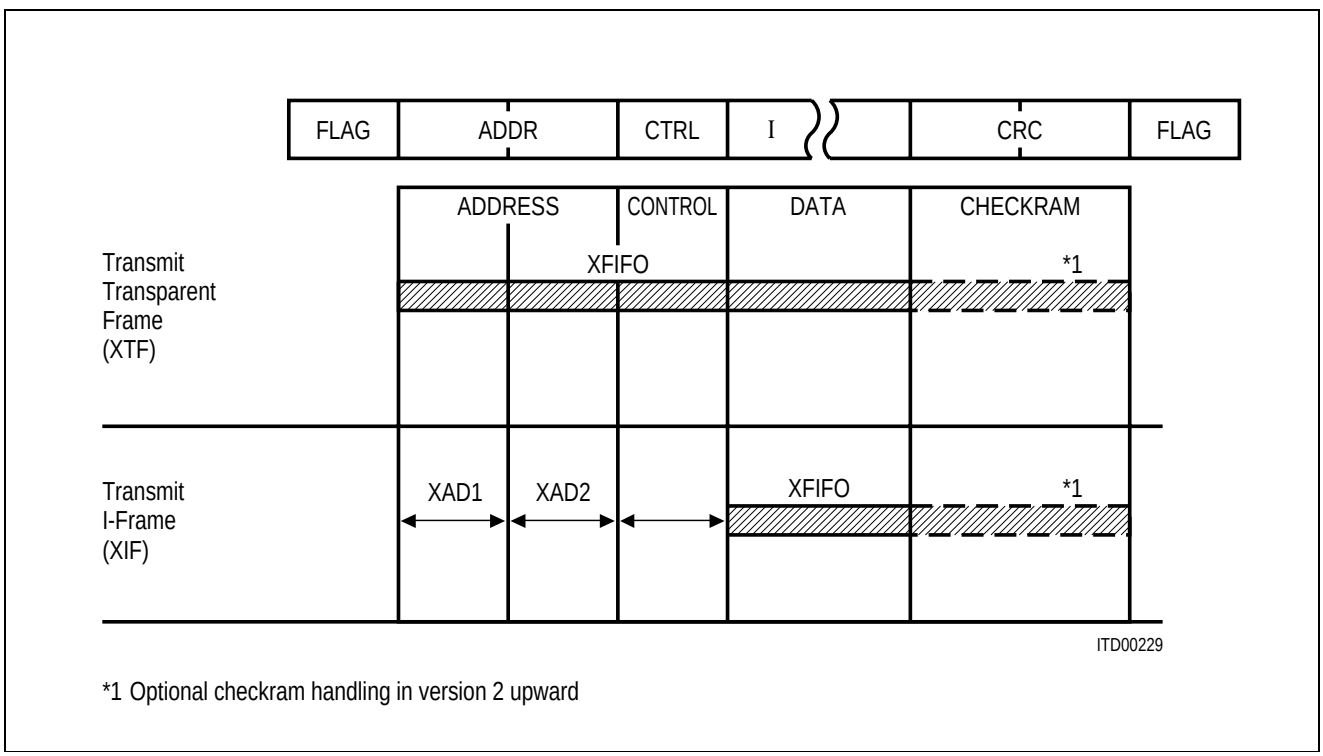


Figure 9
Transmit Data Flow of HSCX

For I-frames (command XIF via CMDR register), the address and control fields are generated autonomously by the HSCX and the data in the XFIFO is entered into the information field of the frame. This is possible only, if the HSCX is operated in the auto-mode.

For transparent frames (command XTF via CMDR register), the address and the control fields have to be entered in the XFIFO as well. This is possible in all operating modes and used also in auto-mode for sending U-frames.

3 Procedural Support (Layer-2 Functions)

When operating in the auto-mode, the HSCX offers a high degree of procedural support. In addition to address recognition, the HSCX autonomously processes all (numbered) S- and I-frames (prerequisite window size 1) with either normal or extended control field format (modulo 8 or modulo 128 sequence numbers – selectable via RAH2 register).

The following functions will be performed:

- updating of transmit and receive counter
- evaluation of transmit and receive counter
- processing of S commands
- flow control with RR/RNR
- generation of responses
- recognition of protocol errors
- transmitting of S commands, if acknowledgement is missing
- continuous status query of opposite termination after RNR has been received
- programmable timer/repeater functions.

In addition, all unnumbered frames are forwarded directly to the processor.

Additional logic connections can be operated in parallel by software. The logic link can be initialized by software at any time (RHR).

3.1 Full-Duplex LAPB/LAPD Operation

Initially (i.e. after RESET), the LAP controllers of the two serial channels are configured to function as a combined station, where they autonomously perform a subset of the X.25 LAPB/ ISDN LAPD protocol.

Reception of Frames

The logic processing of received S-frames is performed by the HSCX without interrupting the µC. The µC is merely informed by interrupt with respect to status changes in the opposite station (receive ready/not receive ready) and protocol errors (unacceptable N(R) or S-frame with I field).

I-frames are also processed autonomously and checked for protocol errors. The I-frame will not be accepted in the case of N(s) error (no interrupt is forwarded to the µC), but is immediately confirmed by an S response. If the µC sets the HSCX into a "receive not ready" status, an I-frame will not be accepted (no interrupt) and an RNR response is transmitted. U-frames are always stored in the RFIFO and forwarded directly to the µC. The logic sequence and the reception of a frame in the auto-mode is illustrated in **figure 10.**

Note: The state variables N(S), N(R) are evaluated within the window size, i.e. the HSCX checks only the lsb of the receive and transmit counter regardless of the selected modulo count.

Transmission of Frames

The HSCX autonomously transmits S commands and S responses in the auto-mode. Either transparent or I-frames can be transmitted by the user. The software timer has to be operated in the internal timer mode to transmit I-frames. After the frame has been transmitted, the timer is self-started, the XFIFO is inhibited, and the HSCX waits for the arrival of a positive acknowledgement. This acknowledgement can be provided by means of an S- or I-frame.

If no positive acknowledgement is received during time t_1, the HSCX transmits an S command (p = 1), which must be followed by an S response (f = 1). If the S response is omitted, the process is performed n1 times before it is terminated.

Upon the arrival of an acknowledgement or after the completion of this poll procedure the XFIFO is enabled and an interrupt is forwarded to the µC. Interrupts may be triggered by the following:

- message has been acknowledged as positive (XPR interrupt)
- message must be repeated (XMR interrupt)
- response has not been received (TIN interrupt)

Upon arrival of an RNR frame, the software timer is started and the status of the opposite station is polled periodically after expiration of t_1, until the status "receive ready" has been detected. The user is informed accordingly via interrupt. If no response is received after n1 times an interrupt will be generated (TIN interrupt). As a result, the process will be terminated as illustrated in **figure 11**.

Note: The internal timer mode should only be used in the auto-mode.

Transparent frames can be transmitted in all operating modes. After the transmission of a transparent frame the XFIFO is immediately enabled, which is confirmed by interrupt (XPR). In this case, time monitoring can be performed with the timer in the external timer mode.

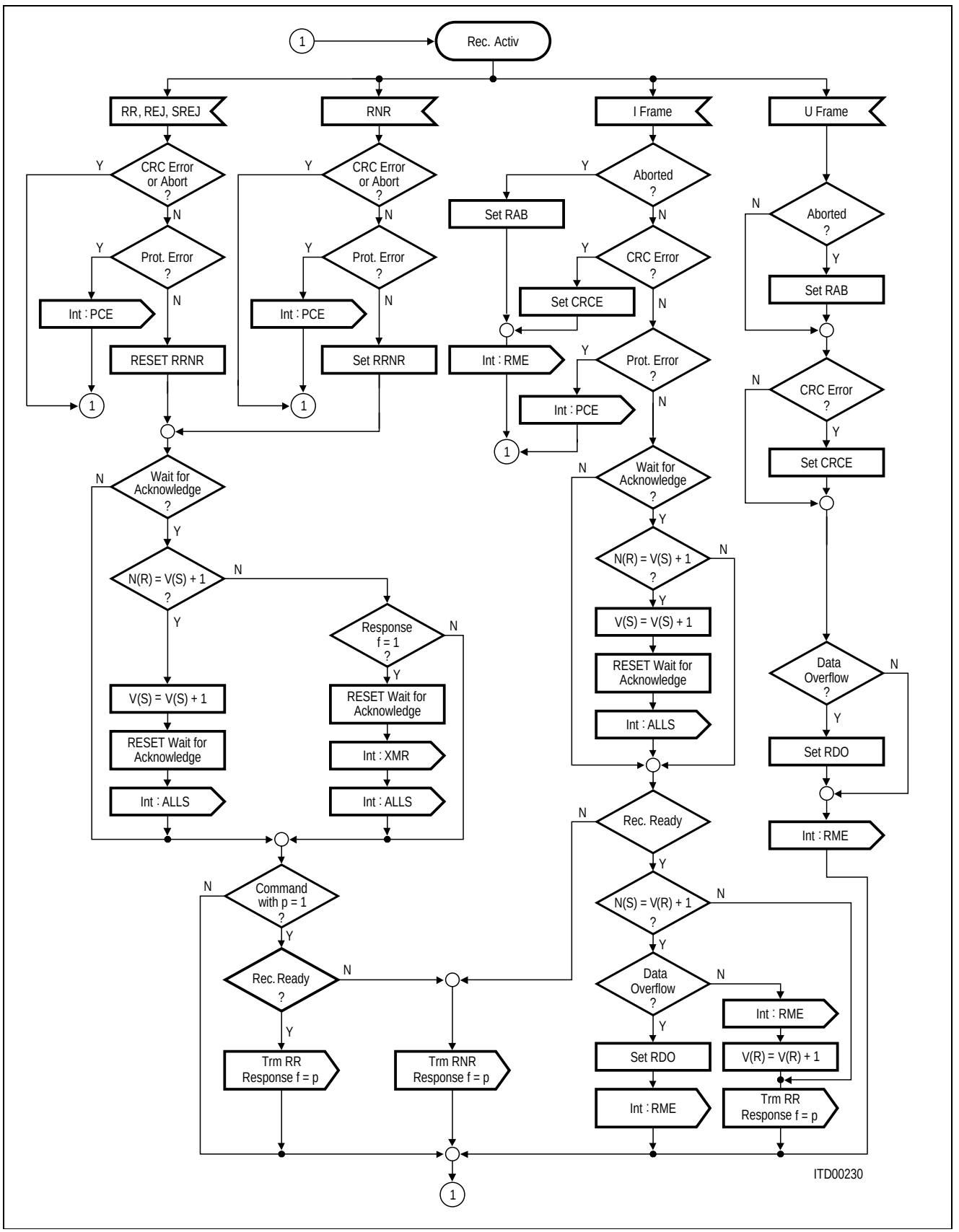


Figure 10
Processing of Received Frames in Auto-Mode

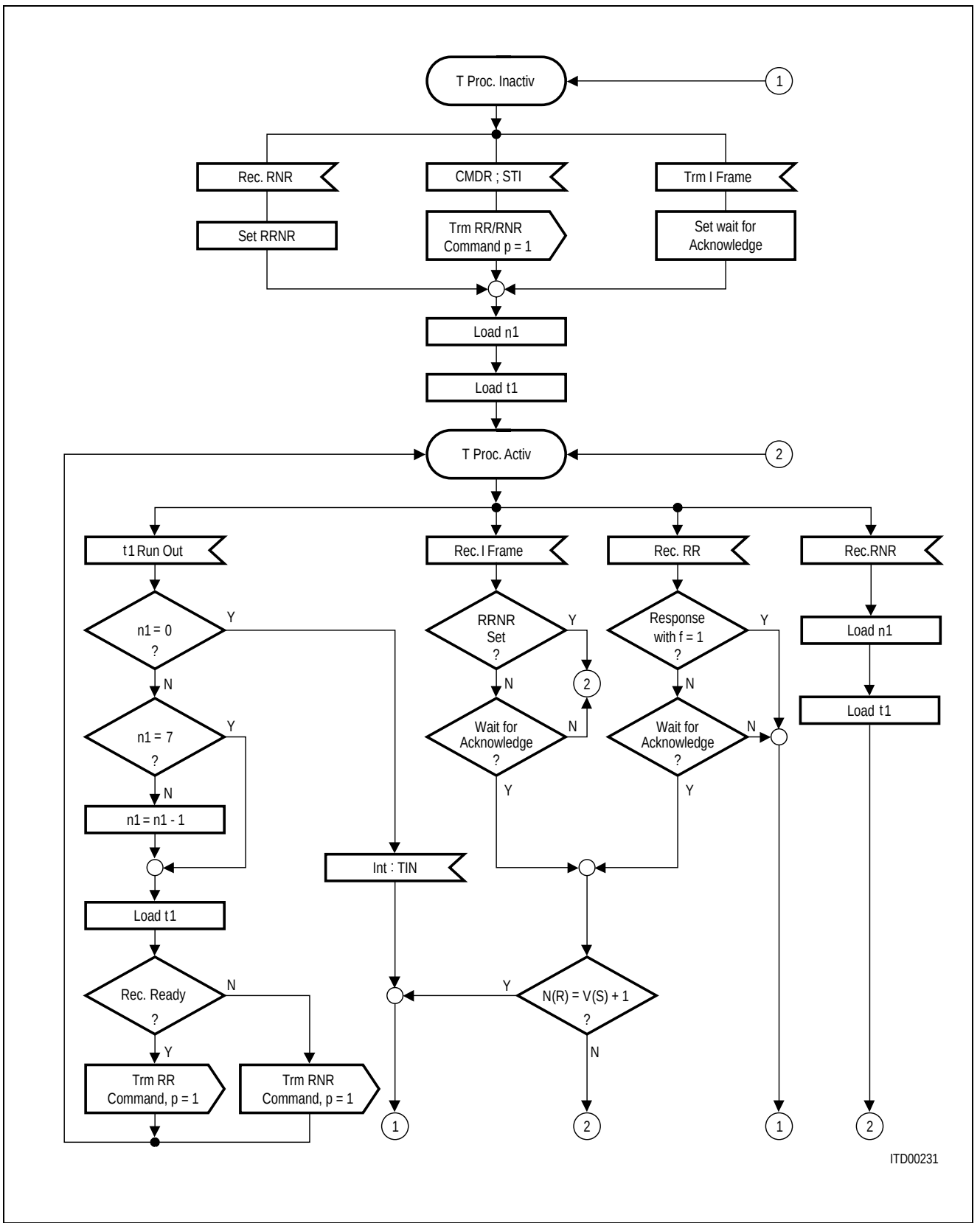


Figure 11
Timer Procedure/Poll Cycle

Examples

The interaction between the HSCX and the CPU during the transmission and reception of I-frames is illustrated in **figure 12,** the flow control with RR/RNR during the reception of I-frames in **figure 13,** and during the transmission of I-frames in **figure 14.** Both the sequence of the poll cycle and protocol errors are illustrated in **figure 15**.

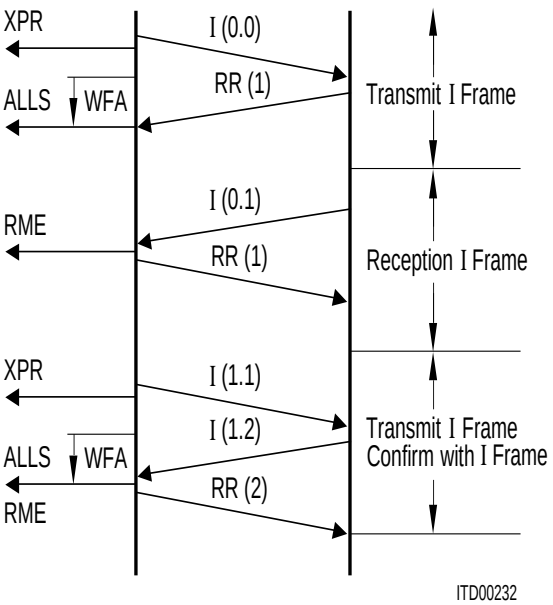


Figure 12
Transmission/Reception I-Frames

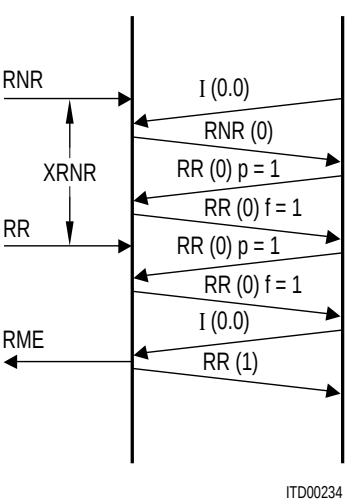


Figure 13
Flow Control/Reception

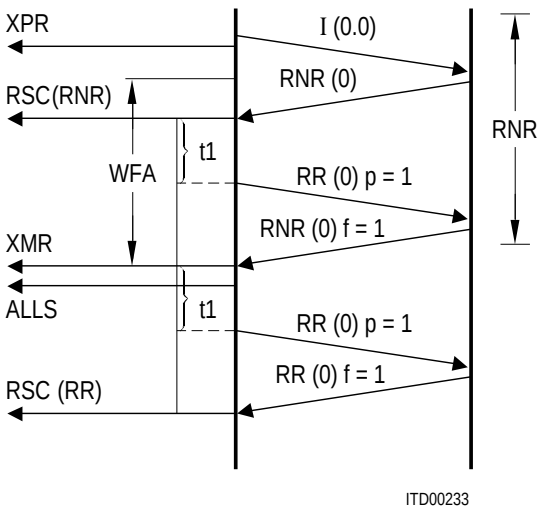


Figure 14
Flow Control/Transmission

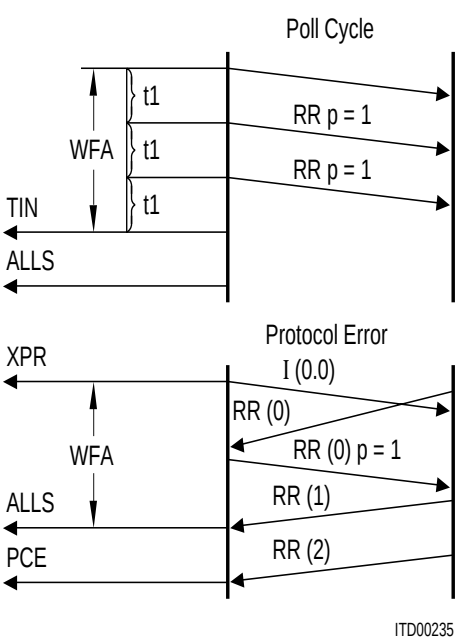


Figure 15
S Commands/Protocol Error

3.2 Half-Duplex SDLC-NRM Operation

The LAP controllers of the two serial channels can be configured to function in a half-duplex Normal Response Mode (NRM), where they will operate as a slave (secondary) station, by setting the NRM bit in the XBCH register of the respective channel.

In contrast to the full-duplex LAPB/LAPD operation, where the combined (primary + secondary) station transmits both commands and responses and may transmit data at any time, the NRM mode allows only responses to be transmitted **and** the secondary station may transmit only when instructed to do so by the master (primary) station.

The HSCX gets the permission to transmit a frame from the primary by an S-, or I-frame with the poll bit (p) **set!**

The NRM mode can be profitably used in a point-to-multipoint configuration with a fixed master-slave relationship and avoids collisions on the common transmit line. It's the responsibility of the master station to poll the slaves periodically and to process the error recovery.

Prerequisite for NRM operation is:

- auto-mode with 8-bit address field selected

MODE: MDS0, MDS1, ADM = 000

- external timer mode

MODE: TDM = 0

- same transmit and receive addresses, since only responses can be transmitted, i.e.

XAD1 = XAD2 = RAL1 = RAL2	← (address of secondary)

Note: The broadcast address may be programmed in RAL2 if broadcasting is required.

Reception of Frames

The reception of frames functions equally to the LAPB/LAPD operation.

Transmission of Frames

The HSCX does **not** transmit S-, or I-frames if not instructed to do so by the primary station sending an S-, or I-frame with the poll bit set.

The HSCX can be prepared to send an I-frame by the CPU issuing an XIF command (via CMDR) at any time. The transmission of the frame, however, will not be initiated by the HSCX prior to the reception of either a

- RR, or
- I-frame

with a poll bit set (p = 1).

After the frame has been transmitted (with the final bit set), the XFIFO is inhibited and the HSCX waits for the arrival of a positive acknowledgement.

Since the on-chip timer of the HSCX must be operated in the external mode (a secondary may not poll the primary for acknowledgements), time supervisory must be done by the primary station.

Upon the arrival of an acknowledgement the XFIFO is enabled and an interrupt is forwarded to the CPU, either the

– message has been acknowledged as positive (XPR interrupt), or the

– message must be repeated (XMR interrupt).

Additionally, the timer can be used **under CPU control** to provide timer recovery of the secondary if no acknowledgements are received at all.

Note: The transmission of transparent frames is possible only if the permission to send is achieved by an S-frame (p = 1) or I-frame.

Examples

A few examples of HSCX/CPU interaction in case of NRM mode are provided in **figure 16 to figure 19.**

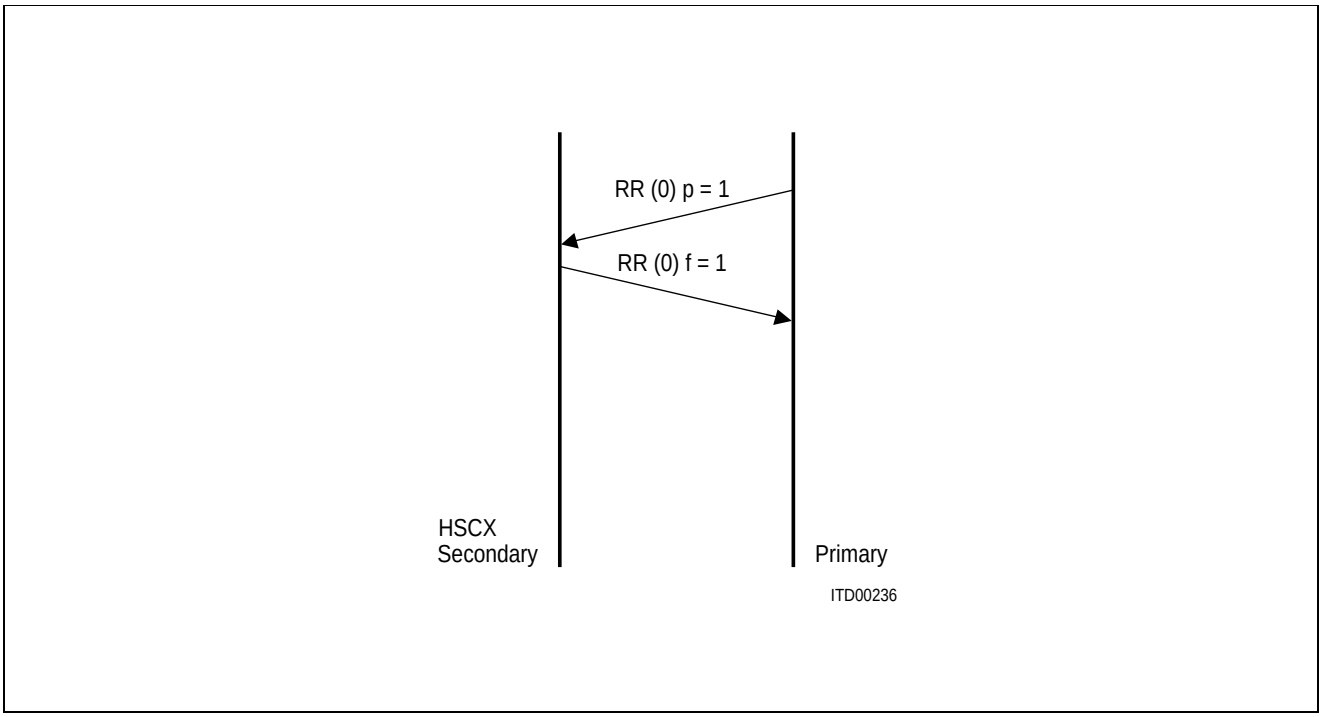


Figure 16
No Data to Send

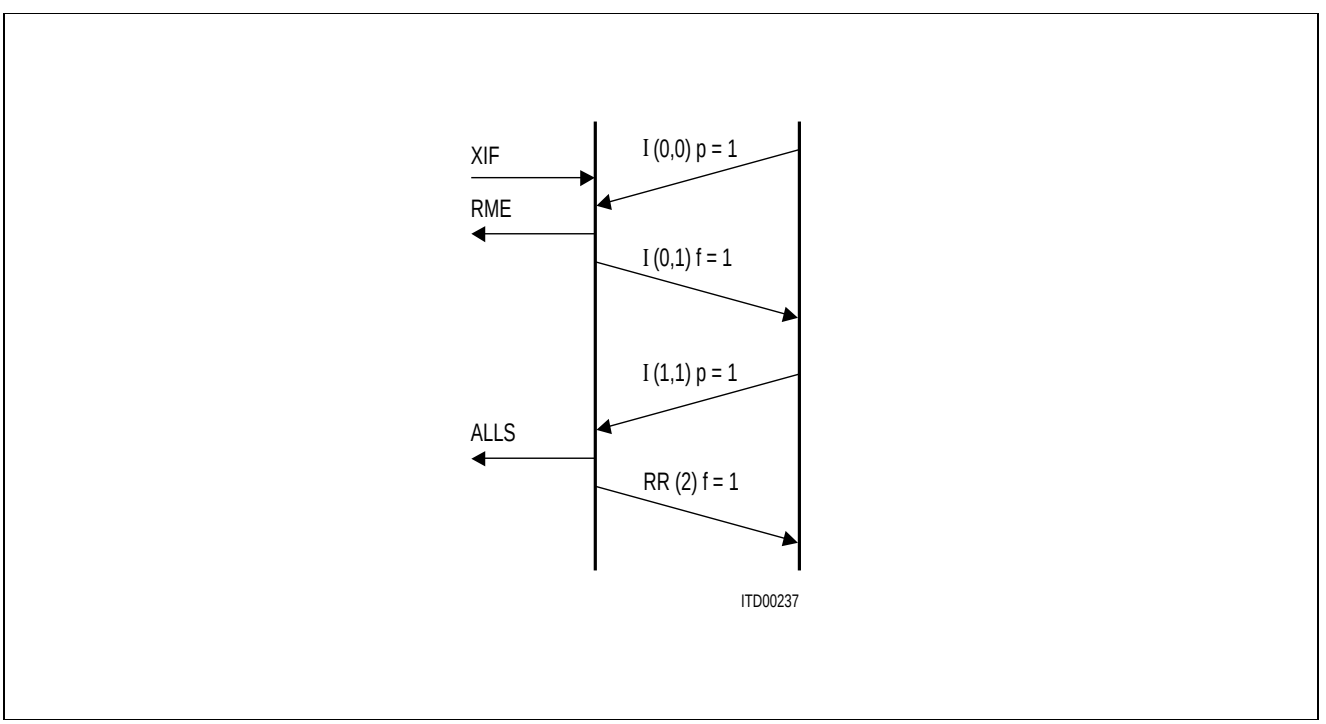


Figure 17
Data Reception/Transmission

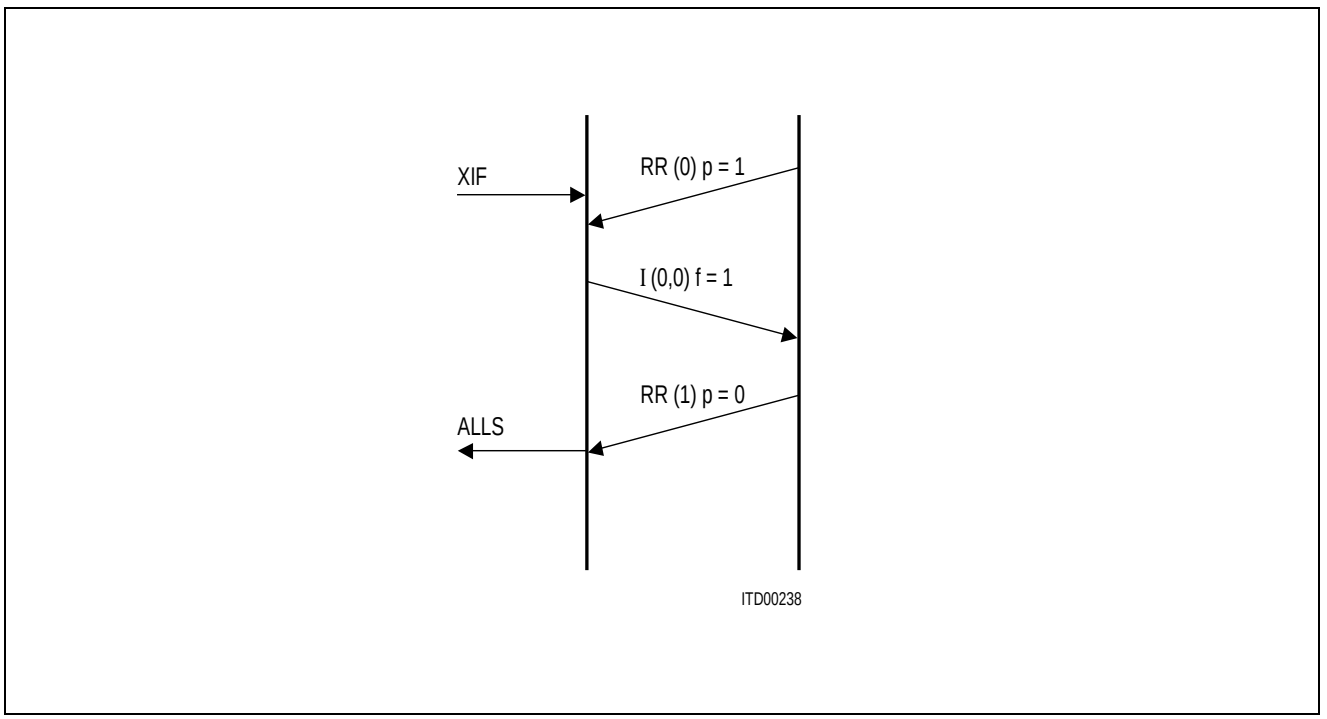


Figure 18
Data Transmission (no Error)

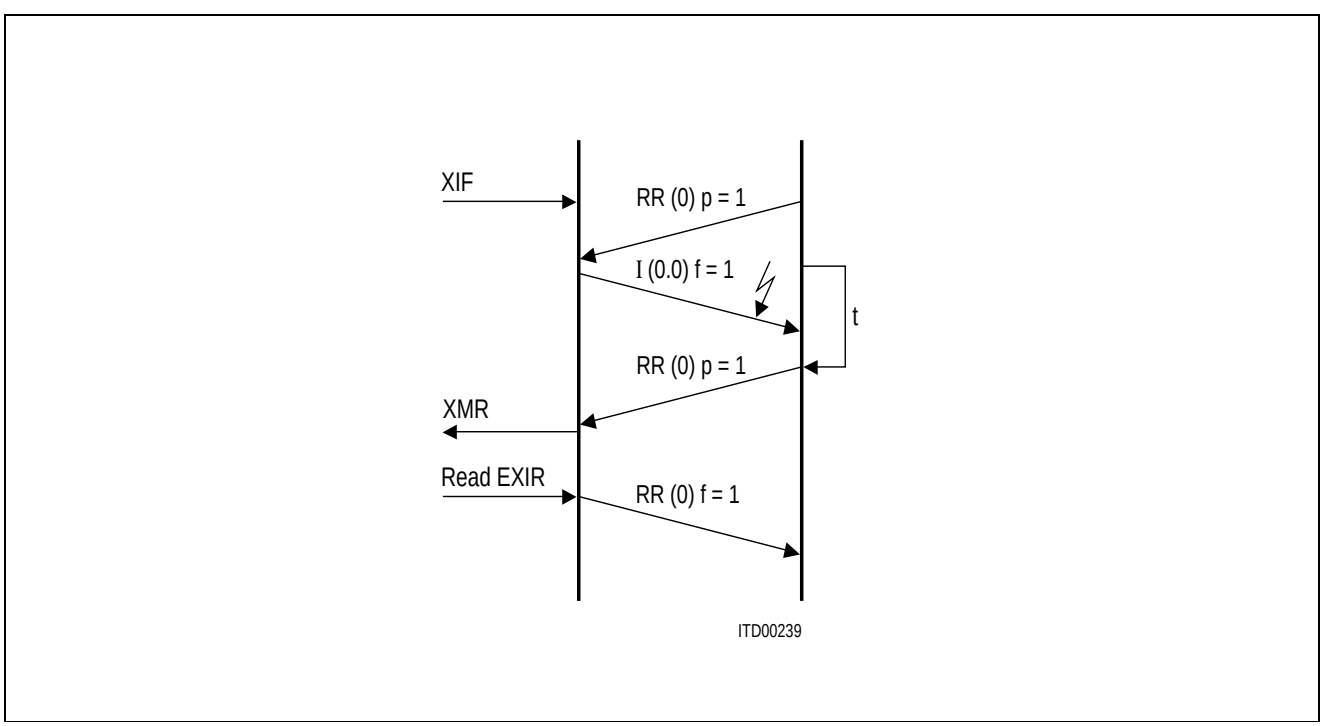


Figure 19
Data Transmission (Error)

3.3 Error Handling

Depending on the error type, erroneous frames are handled according **table 1.**

Table 1
Error Handling

Frame Type	Error Type	Generated Response	Generated Interrupt	Rec. Status
I	CRC error aborted unexpec. N(S) unexpec. N(R)	– – S-frame –	RME RME – PCE	CRC error abort –
S	CRC error aborted unexpec. N(R) with I-field	– – – –	– – PCE PCE	– –

Note: The station variables (V(S), V(R)) are not changed.

4 CPU Interface

4.1 Register Set

The communication between the CPU and the HSCX is done via a set of directly accessible 8-bit registers. The CPU sets the operating modes, controls function sequences, and gets status information by writing or reading these registers (Command/Status transfer). Complete information concerning the register functions is provided in detailed register description. The most important functions programmable via these registers are:

- setting of operating and clocking modes
- layer-2 functions
- data transfer modes (Interrupt, DMA)
- bus mode
- DPLL mode
- baudrate generator
- test loop

Each of two serial channels of HSCX is controlled via an equal, but totally independent register file (channel A and channel B).

4.2 Data Transfer Modes

Data transfer between the system memory and the HSCX for both transmit and receive direction is controlled by either interrupts (Interrupt Mode), or independently from CPU interaction using the HSCX's 4-channel DMA interface (DMA Mode).

After RESET, the HSCX operates in Interrupt Mode, where data transfer must be done by the CPU. The user selects the DMA Mode by setting the DMA bit in the XBCH register. Both channels can be independently operated in either Interrupt or DMA Mode (e.g. Channel A-DMA, Channel B-Interrupt).

4.3 Interrupt Interface

Special events in the HSCX are indicated by means of a single interrupt output, which requests the CPU to read status information from the HSCX, or, if Interrupt Mode is selected, transfer data from/to HSCX.

Since only one $\overline{\text{INT}}$ request output is provided, the cause of an interrupt must be determined by the CPU reading the HSCX's interrupt status registers (ISTA, EXIR).
The structure of the interrupt status registers is shown in **figure 20.**

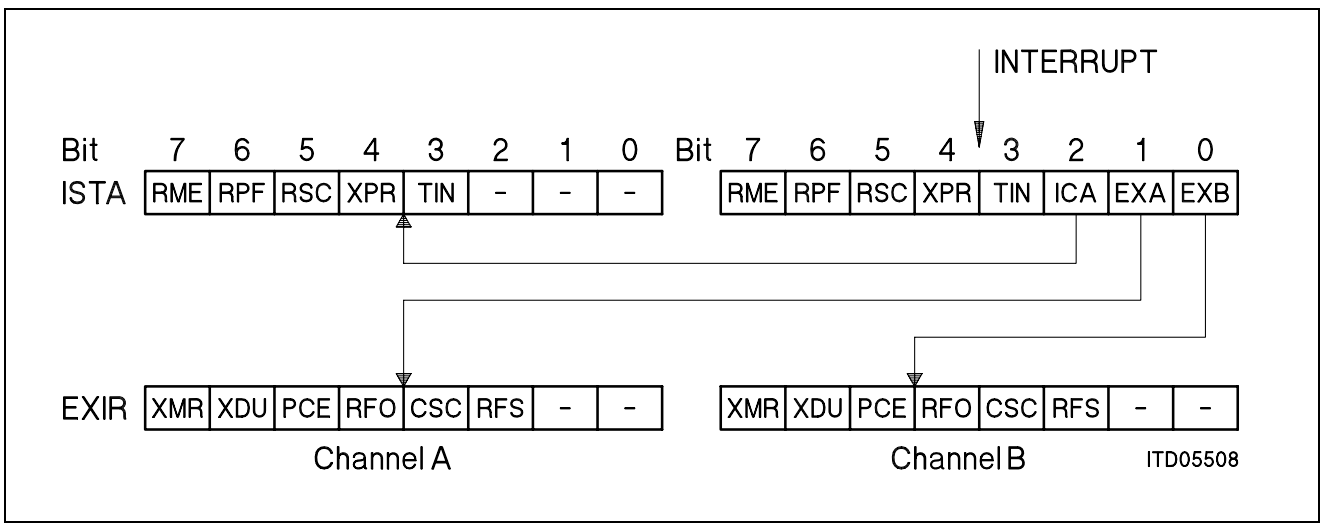


Figure 20
HSCX Interrupt Status Registers

Five interrupt indications can be read directly from the ISTA register and another six interrupt indications from the extended interrupt register (EXIR).

After the HSCX has requested an interrupt by setting its $\overline{INT}$ pin to low, the CPU must first read the interrupt status register of channel B (ISTA-B) in the associated interrupt service routine. The three lowest order bits (bit 2-0) of ISTA-B (ICA, EXA, EXB) point are set to those registers in which the actual interrupt source is indicated. It is possible that several interrupt sources are indicated referring to one interrupt request (e.g. if the ICA bit is set, at least one interrupt is indicated in the ISTA register of channel A).

An interrupt source from channel B is implicitly indicated by bits 7-3 of ISTA-B; therefore these bits must also always be checked.

The $\overline{INT}$ pin of the HSCX remains active until all interrupt sources are cleared by reading the corresponding interrupt register. Therefore it is possible that the $\overline{INT}$ pin is still active when the interrupt service routine is finished.

For some interrupt controllers or CPUs it might be necessary to generate a new edge on the interrupt line to recognize pending interrupts. This can be done by masking all interrupts at the end of the interrupt service routine (writing FF_H into the MASK register) and write back the old mask to the MASK register.

The HSCX interrupt sources can be logically grouped into

– receive interrupts,

– transmit interrupts, and

– special condition interrupts.

Each interrupt indication of the ISTA registers can be selectively masked by setting the respective bit in the MASK register.

The following tables give a complete overview of the individual interrupt indications and the cause of their activation as well as specific restrictions (marked with ”*”).

Table 2
Receive Interrupts

RECEIVE INTERRUPTS		
RPF	Receive Pool Full (ISTA)	*Only activated in Interrupt Mode! Activated as soon as 32-bytes are stored in the RFIFO but the message is not yet completed.
RME	Receive Message End (ISTA)	**Interrupt Mode:** Activated if either one message up to 32 bytes or the last part of a message with more than 32 bytes is stored in the RFIFO, i.e. after the reception of the CRC and closing flag sequence. **DMA Mode:** Activated **after** the complete message has been read out by the DMA controller.
RFO	Receive Frame Overflow (EXIR)	Activated if a complete frame could not be stored due to occupied RFIFO, i.e. the RFIFO is full and the HSCX has detected the start of a new frame.
RFS	Receive Frame Start (EXIR)	*Only activated if enabled by setting the RIE bit in CCR2 register. Activated after the **start** of a valid frame has been detected, i.e. after a valid address check in operation modes providing address recognition, otherwise after the opening flag (transparent mode 0), delayed by two bytes. After an RFS interrupt, the contents of – RHCR – RAL1 – RSTA – bit 3-0 are valid and can be read by the CPU.

Table 3
Transmit Interrupts

TRANSMIT INTERRUPTS		
XPR	Transmit Pool Ready (ISTA)	Activated whenever a 32-byte FIFO pool is empty and accessible to the CPU, i.e. – following a XRES command via CMDR. **Interrupt Mode:** Repeatedly during frame transmission started by XTF or XIF command, and no end of message indication (XME command) has been issued yet by the CPU, – after the end-of-message indication when frame transmission of a transparent frame is completed (i.e. CRC and closing flag sequence are shifted out), **Auto-Mode:** If an I-frame has been positively acknowledged by the opposite station.
XMR	Transmit Message Repeat (EXIR)	**Auto-Mode:** Activated if the last transmitted I-frame has to be repeated due to the reception of a negative acknowledgement (S-, or I-frame with unaccording receive sequence number) of the opposite station. **Bus Configuration:** A collision has occurred after sending the 32nd data byte of a message. **Point-to-Point Configuration:** $\overline{\text{CTS}}$ has been withdrawn after sending the 32nd data byte.
XDU	Transmit Data Underrun (EXIR)	Activated if the XFIFO holds no further data, i.e. all data has been shifted out via the serial T×D pin, but no End Of Message (EOM) indication has been detected by the HSCX. The EOM indication is supplied either – by a XME command from the CPU in **Interrupt Mode,** – or by checking the pre-programmed transmit byte count (via XBCH, XBCL) against the actual amount of data bytes shifted out in **DMA Mode.**

Table 4
Special Condition Interrupts

SPECIAL CONDITION INTERRUPTS

Layer 2-Specific * Activated only if the "Auto" operating mode has been selected via MODE register)

RSC	Receive Status Change	Activated after a status change of the opposite stations receiver has been detected (Receiver Ready/Receiver Not Ready) due to the reception of a – RR frame, if receiver was not ready, or – RNR frame, if receiver was ready.
PCE	Protocol Error	Activated if a protocol violation has been detected due to the reception of – an S-, or I-frame with incorrect N(R), – an S-frame containing an I-field.

Internal Timer

TIN	Timer Interrupt (ISTA)	Activated if the internal timer and repeat counter has been expired (see description of TIMR register in **chapter 8).**

External Pin

CSC	CTS Status Change (EXIR)	* Only activated if enabled by setting the CIE bit in the CCR2 register.

4.4 DMA Interface

The HSCX comprises a 4-channel DMA interface for fast and effective data transfers.

For both serial channels, a separate DMA Request Output for Transmit (DRQT) and receive direction (DRQR) as well as a DMA Acknowledgement ($\overline{\text{DACK}}$) input is provided.

The HSCX activates the DRQ line as long as data transfers are needed from/to the specific FIFO (level triggered demand transfer mode of DMA controller).

It's the responsibility of the DMA controller to perform the correct amount of bus cycles. Either read cycles will be performed if the DMA transfer has been requested from the receiver, or write cycles if DMA has been requested from the transmitter. If the DMA controller provides a DMA acknowledge signal (input to the HSCX's $\overline{\text{DACK}}$ pin), each bus cycle implicitly selects the top of the specific FIFO and neither address (via A0-A6) nor chip select need to be supplied (I/O to Memory transfers). If no $\overline{\text{DACK}}$ signal is supplied, normal read/write operations (providing addresses) must be performed (memory to memory transfers).

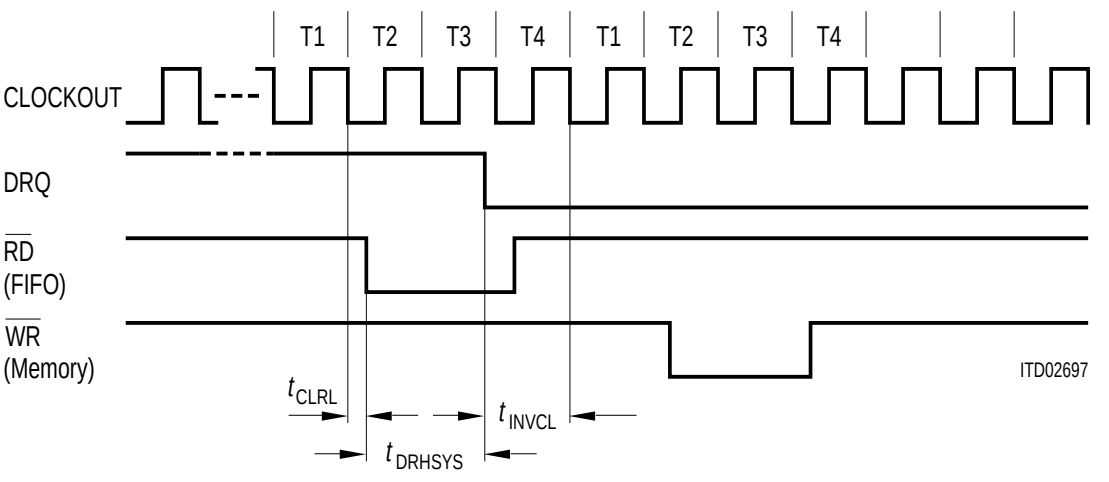
The HSCX deactivates the DRQ line immediately after the last read/write cycle of the data transfer has started.

HSCX supports target synchronous as well as source synchronous DMA transfer. In source synchronous DMA transfer mode a DMA cycle is started when an active level occurs an the DMA request line. This request is controlled by the source (transfer peripheral device → memory).

First of all the data is read out of the peripheral device. During the second clock cycle it is written into the memory according to the target address.

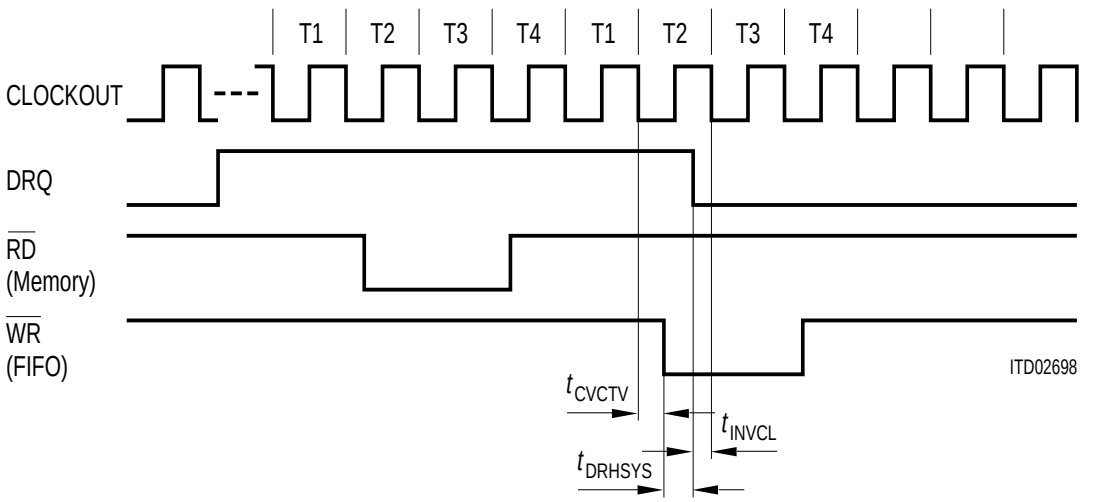
If there is target synchronous DMA transfer the DMA cycle is started when there is an active level on the DMA request line. The request is controlled by the target (transfer memory → peripheral).

First of all the data is read from the memory. During the second clock cycle it is written into the peripheral IC. The DMA request line continues being activated until it is reset by a write cycle to a peripheral device IC.



$t_{DRHSYS\,max}$ = T2 + T3 + T4 - t_{CLRL} - t_{INVCL} = 3 x t_{CLCL} - t_{CLRL} - t_{INVCL}

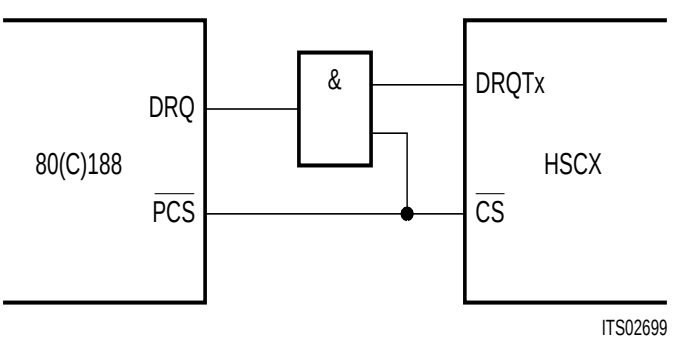
f_{CLKOUT}	t_{CLCL}	t_{CLRL}	t_{INVCL}	$t_{DRHSYS\,max}$
8 MHz	125 ns	44 ns	15 ns	316 ns
12.5 MHz	80 ns	37 ns	15 ns	188 ns
16 MHz	62.5 ns	31 ns	15 ns	141.5 ns



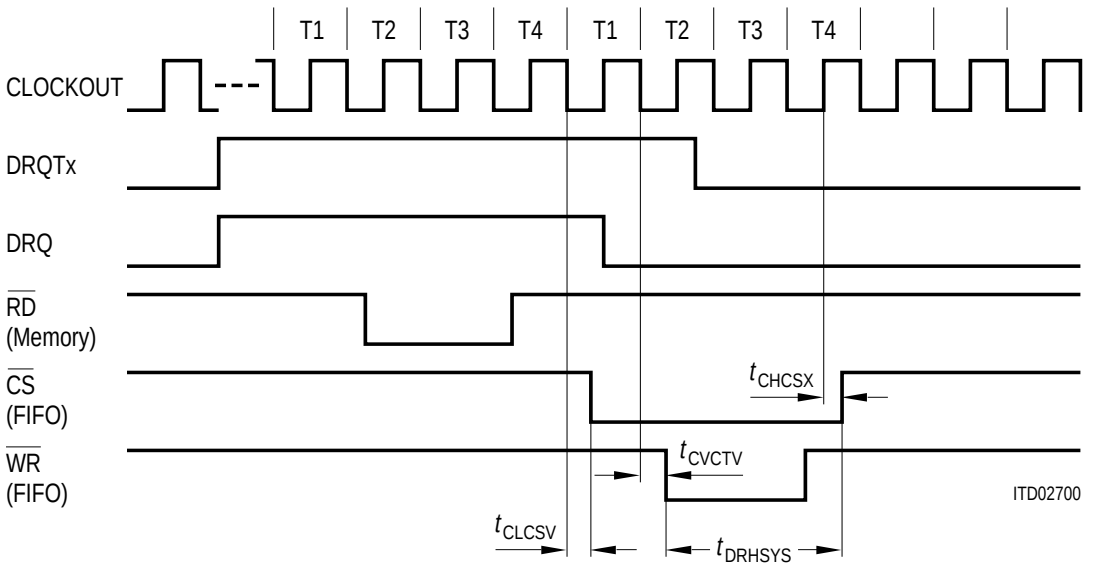
$t_{DRHSYS\,max} = T2 - t_{CVCTV} - t_{INVCL}$

f_{CLKOUT}	t_{CLCL}	t_{CVCTV}	t_{INVCL}	$t_{DRHSYS\,max}$
8 MHz	125 ns	56 ns	15 ns	54 ns
12.5 MHz	80 ns	47 ns	15 ns	18 ns
16 MHz	62.5 ns	31ns	15 ns	16.5 ns

If you use the write signal instead of the chip select signal in order to reset the DMA request you gain some time. The extra circuit is just an AND gate. The first input of the AND gate is connected to the DMA request line of the peripheral IC; the second input is connected to the chip select line. The AND gate's output is the DMA request signal for the 80(C)188.



Theoretically, the request line of an 80(C)188, for example, would still be active when the determination is made and DMA cycles would be performed permanently. Therefore the decision of the DMA request line is delayed; it is already made two clock cycles before the end of the write cycle. If no wait-states are inserted the decision is made at the end of the T2 clock cycle. Due to the fact that the write signal will be valid at the beginning of T2 there is only little time left for resetting the DMA request line.



$t_{DRHSYS\,max}$ = T2 + T3 + T4/2 - t_{CVCTV} + t_{CHCSX}

f_{CLKOUT}	t_{CLCL}	t_{CVCTV}	t_{CHCSX}	$t_{DRHSYS\,max}$
8 MHz	125 ns	56 ns	5 ns	261 ns
12.5 MHz	80 ns	47 ns	5 ns	158 ns
16 MHz	62.5 ns	31 ns	5 ns	130 ns

The circuit mentioned above results in a slower data transfer with the HSCX. HSCX usually performs block transfers. The block length is up to 32 bytes. The DMA request line of the IC remains active as long as more data are needed. Having transmitted the last byte the DMA request is being reset. Using the additional circuit the DMA request line will be active at least shortly before T4. So the next DMA cycle will be started four (instead of two) clock cycles later. Therefore the maximum transmission rate is reduced from 1.25 Mbyte/s to 1.04 Mbyte/s (clock rate: 12.5 MHz).

For more information refer to **chapter 7.2** (Data Transmission: DMA Mode), **chapter 7.3** (Data Reception: DMA mode), and Appendix C (Application Example HSCX with 80(C)188 using DMA).

4.5 FIFO Structure

In both transmit and receive direction 64-byte deep FIFO's are provided for the intermediate storage of data between the serial interface and the CPU interface. The FIFO's are divided into two halves of 32-bytes, where only one half is accessible to the CPU or DMA controller at any time.

The organization of the Receive FIFO (RFIFO) is such, that in the case of a frame at most 64 bytes long, the whole frame may be stored in the RFIFO. After the first 32 bytes have been received, the HSCX prompts to read the 32-byte block by means of interrupt or DMA request (RPF interrupt or activation of DRQR line). This block remains in the RFIFO until a confirmation is given to the HSCX acknowledging the transfer of the data block. This confirmation is either a RMC (Receive Message Complete) command via the CMDR register in Interrupt Mode, or is implicitly achieved in DMA mode after 32-bytes have been read from the RFIFO. As a result, it's possible in Interrupt Mode, to read out the data block any number of times until the RMC command is issued.
The configuration of the RFIFO prior to and after acknowledgement is shown in **figure 21.**

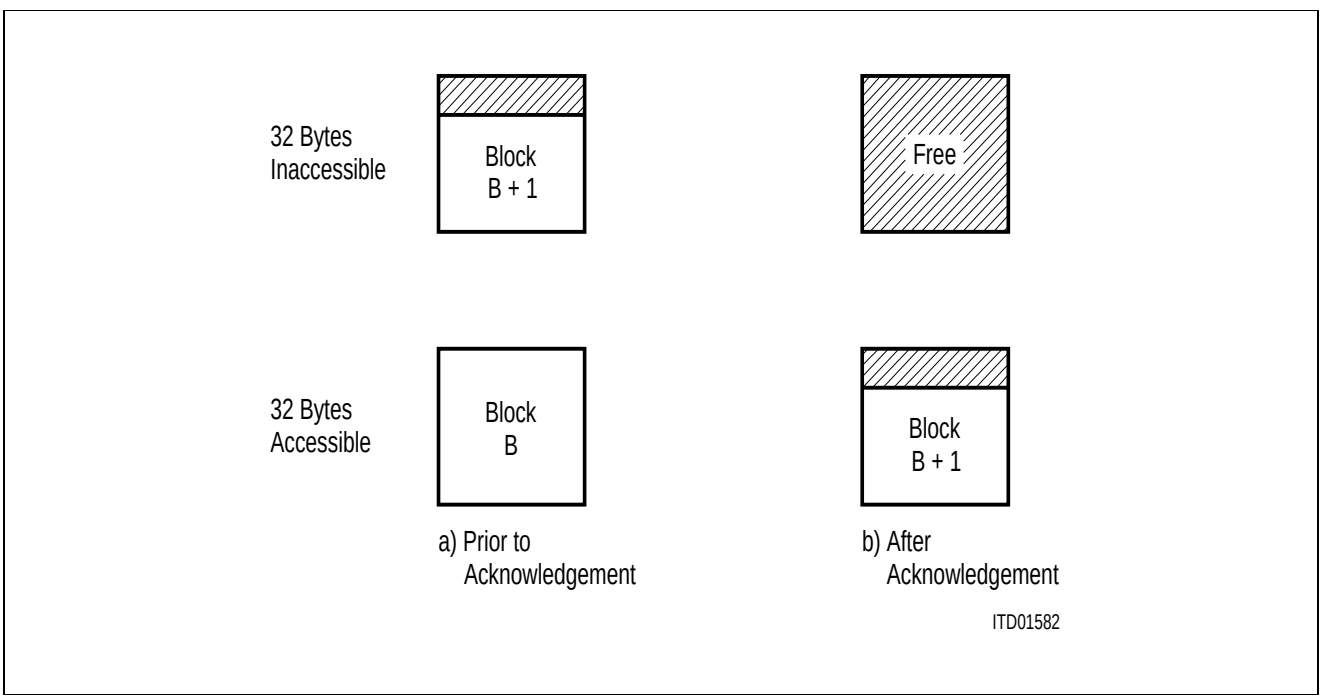


Figure 21
Configuration of RFIFO (Long Frames)

If frames longer than 64 bytes are received, the device will repeatedly prompt to read out 32-byte data blocks via interrupt or DMA.

In the case of several shorter frames, up to 17 may be stored in the HSCX.

If the accessible half of the RFIFO contains a frame i (or the last part of frame i), up to 16 short frames may be stored in the other half (i + 1,. . ., i + n) meanwhile, prior to frame i being fetched from the RFIFO.

This is illustrated in **figure 22.**

For a description of a transmit and receive sequence in both Interrupt or DMA Mode, please refer to **chapter 7.2 and 7.3.**

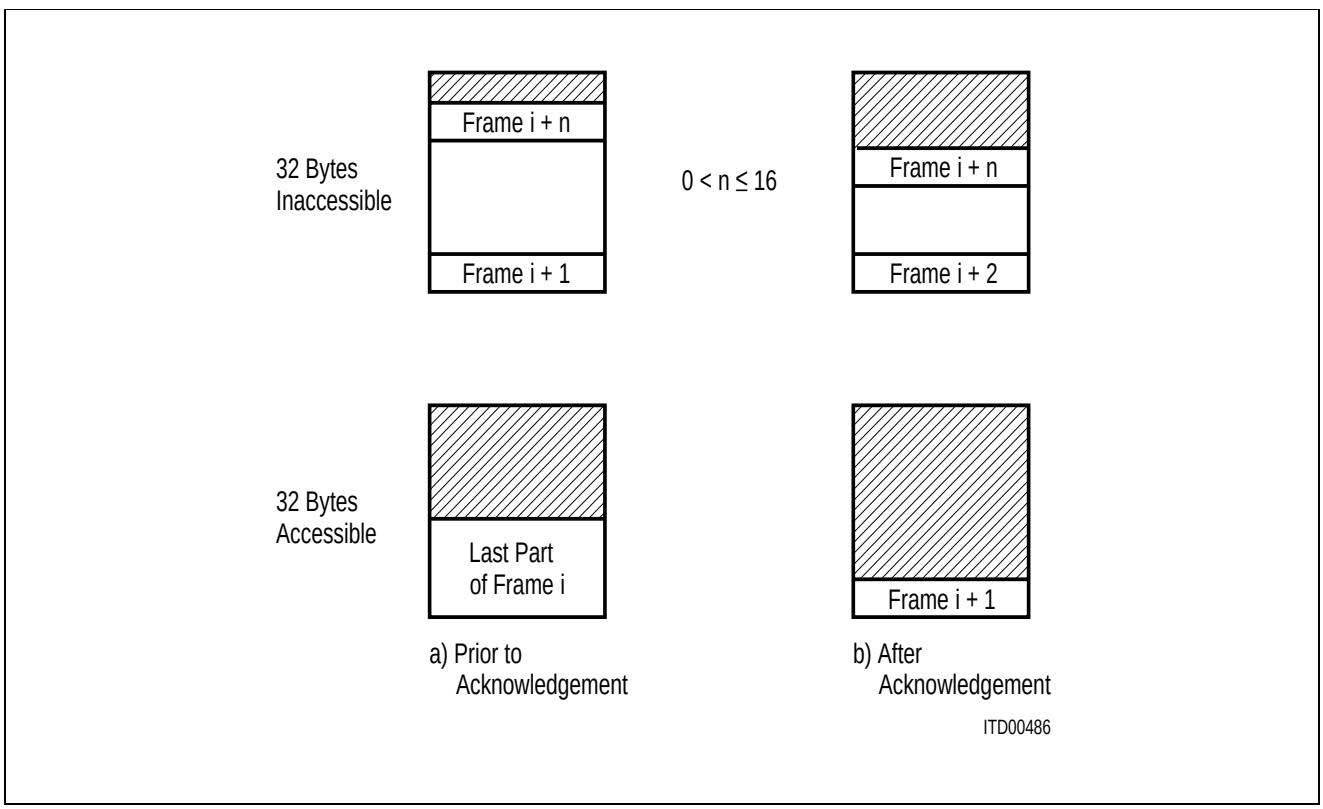


Figure 22
Configuration of RFIFO (Short Frames)

Note: The number of 17 frames applies e.g. for the HSCX operating in the auto or non-auto mode (address recognition), and short frames only containing the HDLC Address and Control field are received. Since the address is not stored, the control field is always stored first in the RFIFO, and an additional status byte is always appended at the end of each frame in the RFIFO, these frames will occupy two bytes.

5 Serial Interface (Layer-1 Functions)

The two serial interfaces of the HSCX provide two fully independent communications channels, supporting layer-1 functions to a high degree by various means of clock generation and clock recovery.

5.1 Clock Modes

The HSCX includes an internal Oscillator (OSC) as well as independent Baudrate Generator (BRG) and Digital Phase Locked Loop (DPLL) circuitry for each serial channel.

The transmit and receive clock can be either generated
- – externally, and supplied via the R×CLK and/or T×CLK pins, or
- – internally, by means of the
  - * OSC and/or BRG, and
  - * DPLL, recovering the receive (and optionally transmit) clock from the received data stream if an external crystal is connected to the R×CLKA-A×CLKA pins.

Totally, there are 8 different clocking modes programmable via the CCR1 register, providing a wide variety of clock generation and clock pin functions, as shown in **table 5.**

Table 5
Overview of Clock Modes

Clock			
Type	**Source**	**Generation**	**Mode**
Receive Clock	R×CLK Pins	Externally	0, 1, 5
	DPLL		2, 3, 6, 7
	OSC	Internally	4
Transmit Clock	T×CLK Pins		0, 2, 6
	R×CLK Pins	Externally	1, 5
	DPLL		3, 7
	BRG/16	Internally	2, 6
	OSC		4

The transmit clock pins (T×CLK) may also output clock or control signal in certain clock modes if programmed as outputs via the CCR2 register (TIO bit set).

The clocking source for the DPLL's is always the internal BRG; the scaling factor (divider) of the BRG can be programmed through CCR2 and BGR registers between 1,2,4,6. . .2048.

The HSCX system clock is always derived from the transmit clock thus eliminating the need for additional clock sources.

Clock Mode 0 (External Clocks)

Separate, externally generated receive and transmit clocks are forwarded to the HSCX via their respective pins.

Clock Mode 1 (Receive/Transmit Strobes)

Externally generated, but identical receive and transmit clocks are forwarded via R × CLK pins. In addition, a receive strobe can be connected via A×CLK and a transmit strobe via T × CLK pins. The operating mode can be applied in time division multiplex applications or for adjusting disparate transmit and receive data rates.

Clock Mode 2 (Receive Clock from DPLL)

The BRG is driven with an external clock (R × CLK) and it delivers a reference clock for the DPLL which in turn generate the receive clock. Depending on the programming of the CCR2 register (TSS bit), the transmit clock will be either an external clock signal (T × CLK) or the clock delivered by the BRG divided by 16. In this case, the transmit clock can be output via T × CLK (CCR2 : TIO = 1).

Clock Mode 3 (Receive and Transmit Clock from DPLL)

The BRG is fed with an externally generated clock via R × CLK and supplies the reference clock for DPLL, which generates **both** the receive and transmit clock. This clock can also be output via T × CLK pin.

Clock Mode 4 (OSC-Direct)

The receive and transmit clocks are **directly** supplied by the OSC. In addition this clock can be output via T × CLK.

Clock Mode 5 (Time-Slots)

This operating mode has been designed for application in time-slot oriented PCM systems.

The receive and transmit clock is identical for each channel and must be supplied externally via R × CLK pins. The HSCX receives and transmits only during certain time-slots of programmable width (1. . .256 bit, via RCCR and XCCR registers) and location with respect to a frame synchronization signal, which must be delivered to the HSCX via the
A × CLK pin. One of up to 64 time-slots can be programmed independently for receive and transmit direction via TSAR and TSAX registers, and an additional clock shift of 0…7 bits via TSAR, TSAX, and CCR2 registers. Together with bits XCS0 and RCS0 (LSB of clock shift), located in the CCR2 register, there are 9 bits to determine the location of a time-slot.

According to the value programmed via those bits, the receive/transmit window (time-slot) starts with a delay of 1 (minimum delay) up to 512 clock periods following the frame synchronization signal and is active during the number of clock periods programmed via RCCR, XCCR (number of bits to be received/transmitted within a time-slot) as shown in **figure 23.**

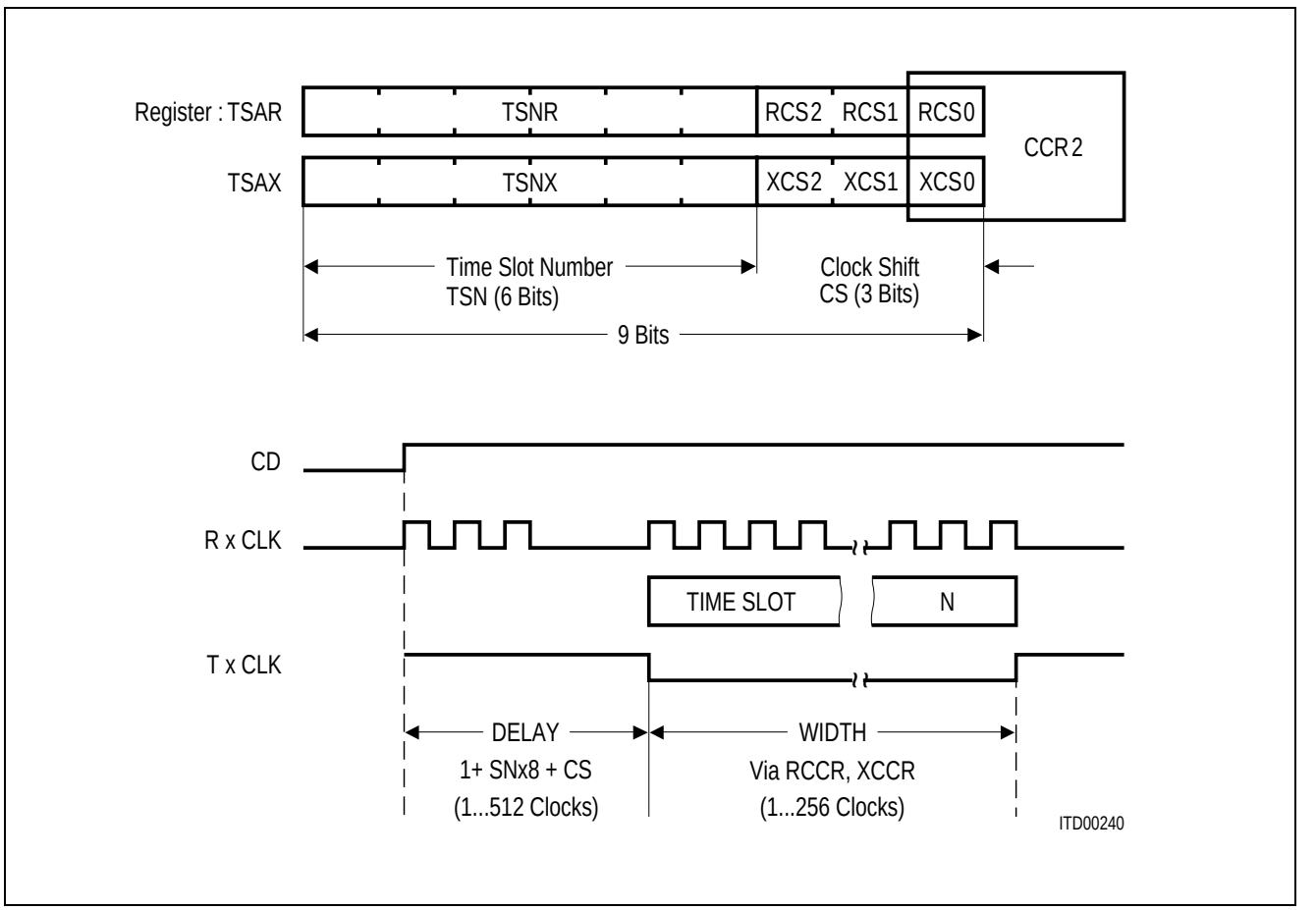


Figure 23
Location of Time-Slots

The transmit time-slot is additionally indicated by a control signal via T × CLK, which output is set to log 0 during the transmit window.

Note: In extended transparent mode the width of the time-slots has to be n × 8 bit.

$\overline{\text{RTS}}$ Signal in Clock Mode 5

When using the $\overline{\text{RTS}}$ signal in clock mode 5, it has to be considered, that the $\overline{\text{RTS}}$ signal is deactivated after the transmission of the second last bit (instead of the last) of a closing flag, if that second last bit is the last bit of a time-slot "window". In other words, $\overline{\text{RTS}}$ is inactive during the transmission of the last bit, transmitted in the next time-slot window. **See figure 24**.

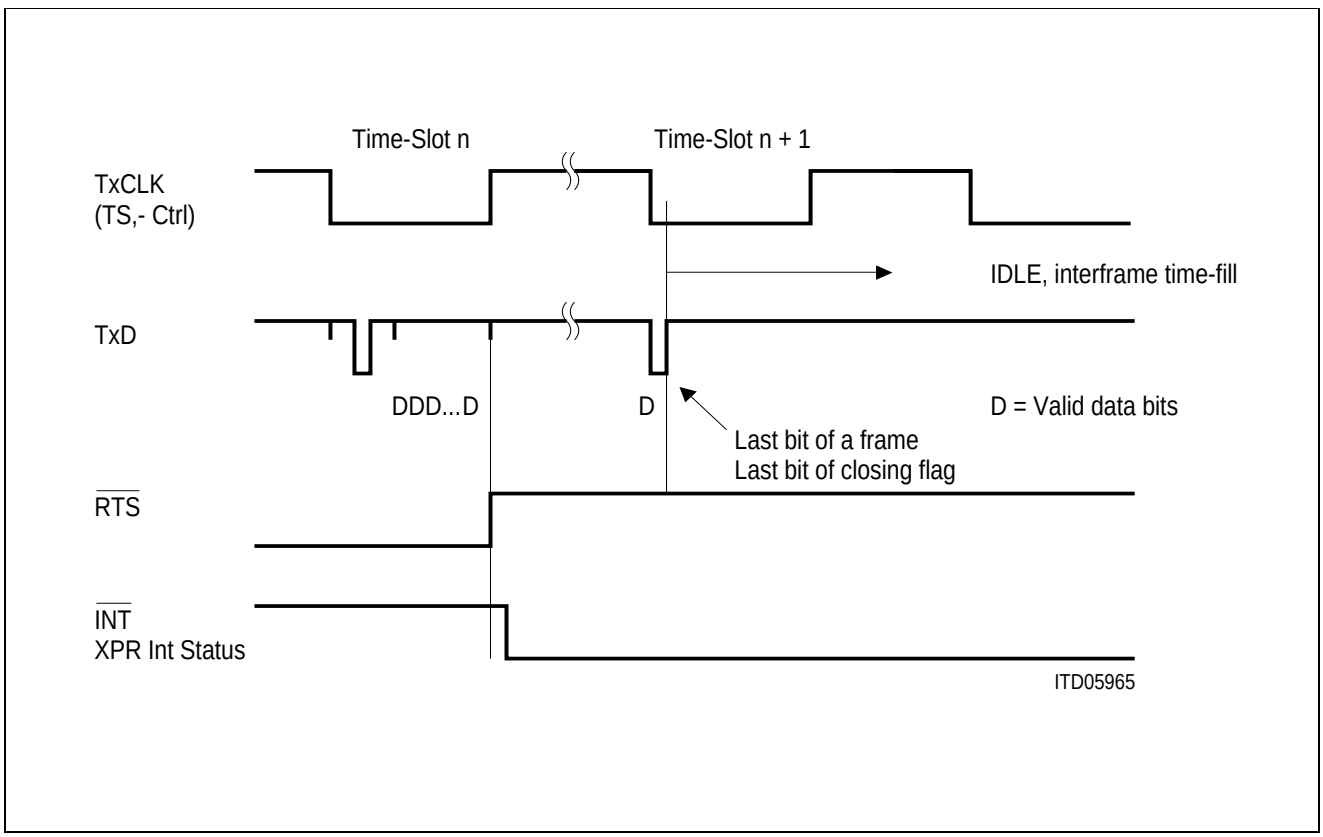


Figure 24

This must be considered for applications, where several transmitters are sharing the same time-slot on a **non** open-drain bus, e.g. a balanced bus, not using collision detection as the resolution mechanism. One such application is slave stations in a point-to-multipoint configuration sharing the same time-slot and using NRM auto-mode. Thus, $\overline{\text{RTS}}$ and the time-slot marker TxCLK cannot simply be gated to generate a driver control signal. Instead the following recommendations apply:

a) Do not use the $\overline{\text{RTS}}$ signal directly in clock mode 5 e.g. to enable drivers for TxD in a balanced bus configuration. Instead, use an arrangement of the type shown in the **figure 25** or

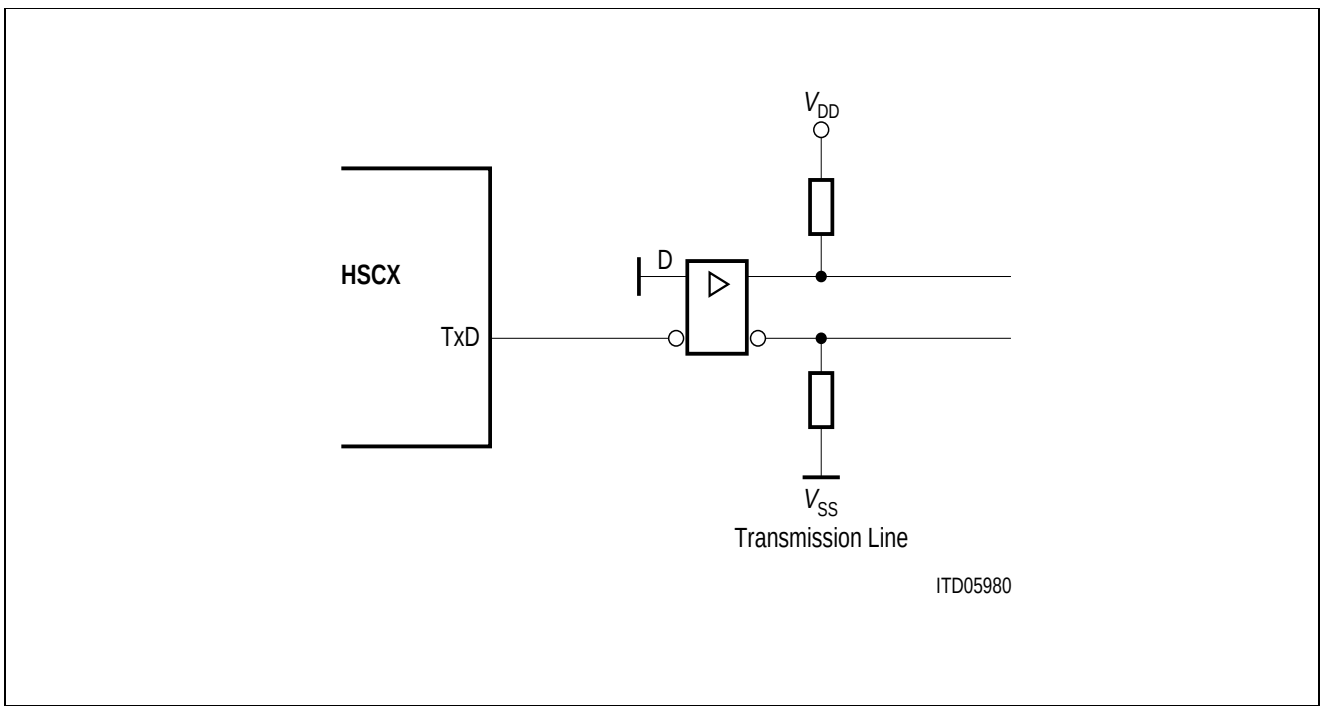


Figure 25

b) delay the rising edge of $\overline{RTS}$ (e.g. for NRM mode with balanced bus).

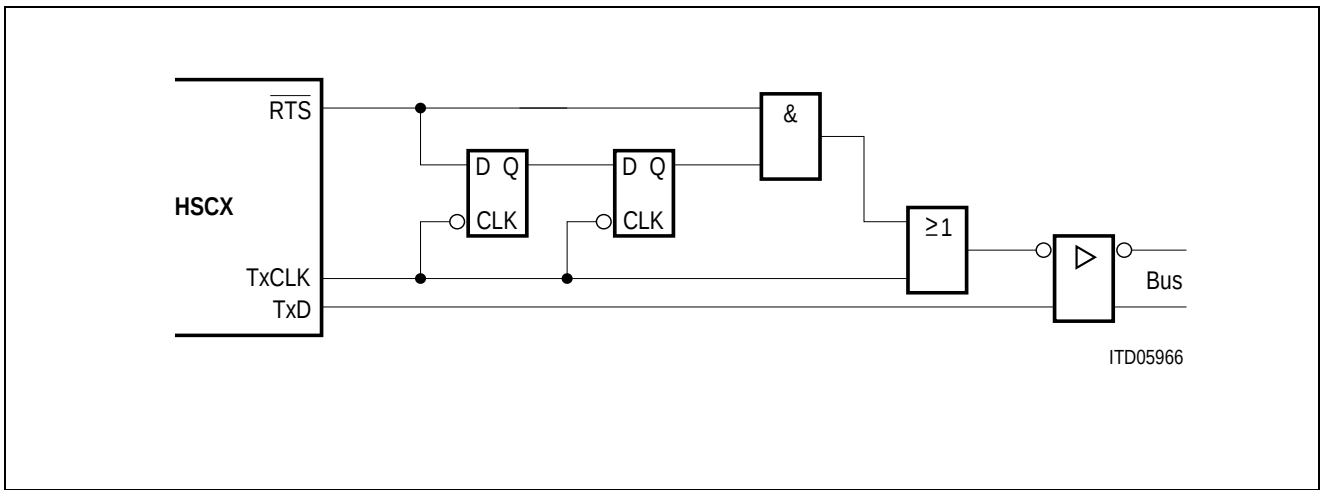


Figure 26

Timing diagram for recommendation b):

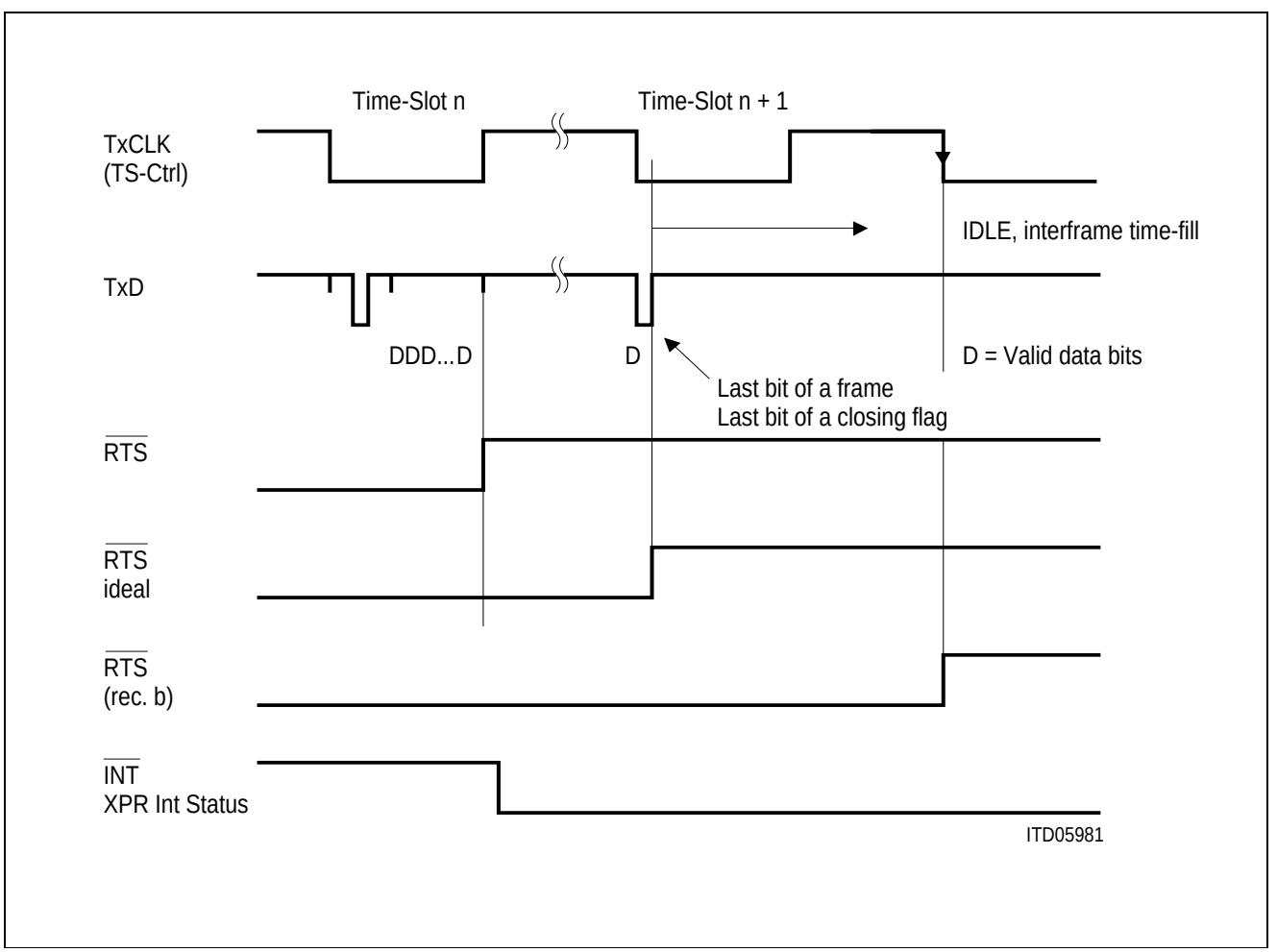


Figure 27

$\overline{\text{CTS}}$ Signal in Clock Mode 5

In clock mode 5 the $\overline{\text{CTS}}$ signal is evaluated not only in the time-slot “window“, but also between the time-slot “windows“. If data transmission must not be stopped, $\overline{\text{CTS}}$ has to be active, even between the time-slot “windows“, until the transmission of the frame has been completed. In other words, a deactivation of $\overline{\text{CTS}}$ stops the transmitter immediately.

Note: When several HDLC channels are sharing the **same** time-slot on a bus without using the bus collision detection, the strobe signals (AxCLKA/B) can be used to select/ deselect particular time-slot “windows“ for an individual HDLC channel.

Clock Mode 6 (OSC – Receive Clock from DPLL)

This clock mode equals the features of Clock Mode 2, with the only exception that the clock for the BRG is delivered by the OSC and must not be provided externally.

Clock Mode 7 (OSC – Receive and Transmit Clock from DPLL)

Similar to Clock Mode 3, but BRG clock is provided by OSC.

Summary
The features of the different clock modes are summarized in **table 6.**

Table 6
Clock Modes of HSCX

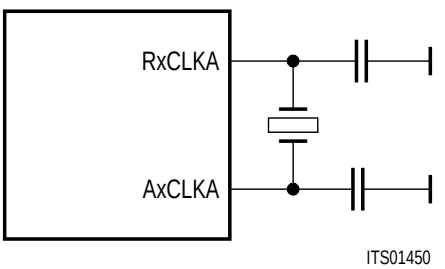
Channel Configuration			Clock Sources				Control Sources					Timer Source
Clock Mode CCR1 CM2, CM1, CM0	CCR2 TSS	TIO	BRG	DPLL	REC	TRM	CD	R-Strobe	X-Strobe	F-Sync	Output via TxCLK	TCP
0	0	0	–	–	RxCLK	TxCLK	AxCLK	–	–	–	–	TxCLK
1	0	0	–	–	RxCLK	RxCLK	–	AxCLK	TxCLK	–	–	RxCLK
2	0	0	RxCLK	BRG	DPLL	TxCLK	AxCLK	–	–	–	–	TxCLK
2	1	1	RxCLK	BRG	DPLL	BRG/16	AxCLK	–	–	–	BRG/16	DPLL
3	0	1	RxCLK	BRG	DPLL	DPLL	AxCLK	–	–	–	DPLL	DPLL
4	0	0	–	–	OSC	OSC	TxCLK	–	–	–	–	OSC
4	0	1	–	–	OSC	OSC	...	–	–	–	OSC	OSC
5	0	0	–	–	RxCLK	RxCLK	TxCLK	(TSAR)	(TSAX)	AxCLK	TS-Control	RxCLK
6	0	0	OSC	BRG	DPLL	TxCLK	–	–	–	–	–	TxCLK
6	1	0	OSC	BRG	DPLL	BRG/16	TxCLK	–	–	–	–	BRG/16
6	1	1	OSC	BRG	DPLL	BRG/16	–	–	–	–	BRG/16	BRG/16
7	0	0	OSC	BRG	DPLL	DPLL	TxCLK	–	–	–	–	DPLL
7	0	1	OSC	BRG	DPLL	DPLL	–	–	–	–	DPLL	DPLL

Note: 1) The maximum data rate in an externally clocked operating mode is 4.1 Mbit/s. In an internally clocked operating mode with an external reference clock, or using the OSC, the maximum clock rate is 12 MHz or 19.2 MHz if the scaling factor of the BRG is programmed to 1. The maximum data rate will be 1200 kbit/s.

2) The ratio between the receive frequency (fr) and the transmit frequency (fx) for a channel must satisfy the condition fr/fx less than 3 in clock modes 0, 2, 6; there are no restrictions on the phase shift. Slower transmit data rates can be realized with receive and transmit strobes (clock mode 1).

3) The clock modes 4, 6, 7 use the internal OSC and need an external quartz crystal to be connected at the RxCLK A-AxCLK A pins.
It is not necessary to use two separate crystals for the two serial channels, instead it is sufficient to apply the crystal to channel A and provide the reference clock for channel B by externally connecting the AxCLKA and RxCLKB pins. The SAB 82526 also uses the RxCLK A-AxCLK A pins to connect to an external quartz crystal.

Normally 33 pF capacitors are used for frequencies below 10 MHz and 22 pF capacitors are used for frequencies above 10 MHz.



To guarantee oscillation use the capacitances which are specified by the crystal manufacturer.

5.2 Clock Recovery (DPLL)

The HSCX offers the advantage of recovering the receive clock from the receive data by means of internal DPLL circuitry, thus eliminating the need to transfer additional clock information via the serial link.

For this purpose, the DPLL is supplied with a reference clock from BRG which is 16 times the data clock rate (clock mode 2, 3, 6, 7). Additionally, the transmit clock may be obtained dividing the output of the BRG by a constant factor of 16 (clock mode 2, 6; TSS bit in CCR2 set) or also directly from the DPLL (clock mode 3, 7).

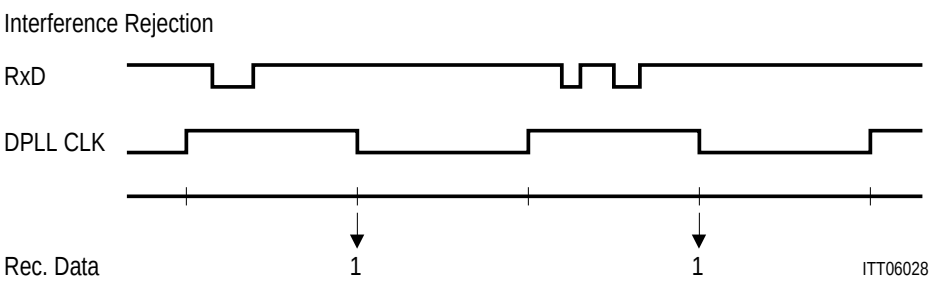


Figure 28a

The DPLL circuits implemented in the HSCX are optimized with respect to the HDLC protocol. The main task of the DPLL is to derive a receive clock and to adjust its phase to the incoming data stream in order to enable the bit sampling in the middle of a bit-cell with the falling edge of the receive clock. For this purpose, edges in the receive data, indicating the begin of a bit-cell, are necessary.

When using the NRZI encoding, the zero insert/zero delete method ensures that a sufficient number of edges occur in the data stream during the reception of an HDLC frame. Furthermore a completely new "one insertion" mechanism has been implemented with the HSCX, which also guarantees sufficient number of edges when using NRZ encoding (especially for bus configurations, **see chapter 6.5** for details).

The following functions have been implemented to facilitate a high-speed and reliable synchronization (**see figures 28**).

– Interference Rejection

In the case where two or more edges appear in the data stream within a time period of 16 reference clocks, these are detected as interference without performing additional adjustments.

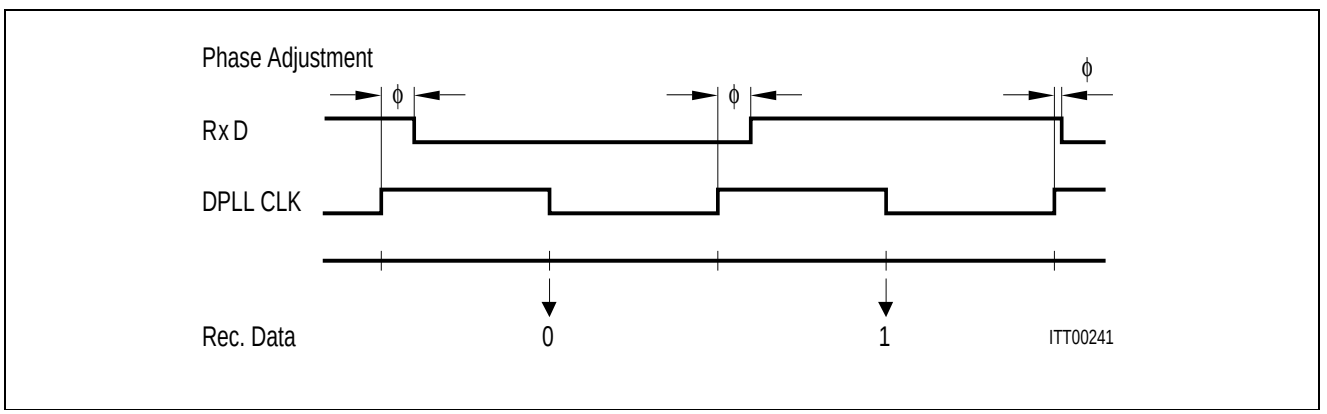


Figure 28b

– Phase Adjustment

In the case where an edge with a phase angle of 20 to 112 degrees appears in the data stream within the time window, the phase will be adjusted by 1/16 of the data clock.

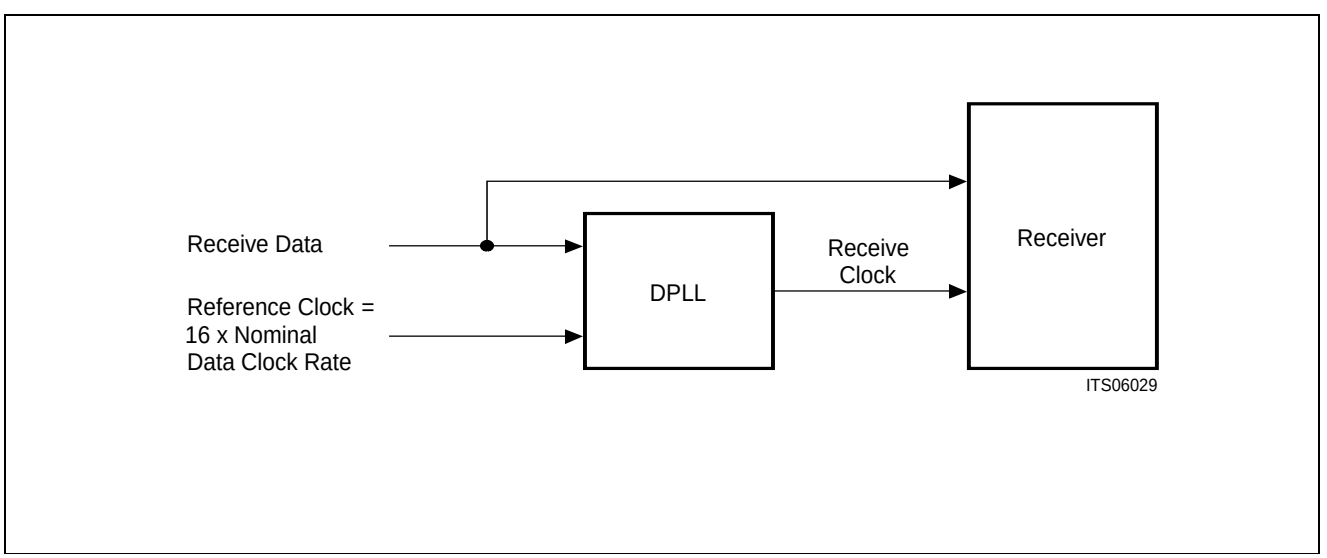


Figure 28c

– Phase Shift

In the case the DPLL detects an edge in the data stream in the range of DPLL count 5 to 10 (Phase Shift) and this is the only one in the assumed bit cell period, then the DPLL receive clock phase is shifted by a certain DPLL count value.

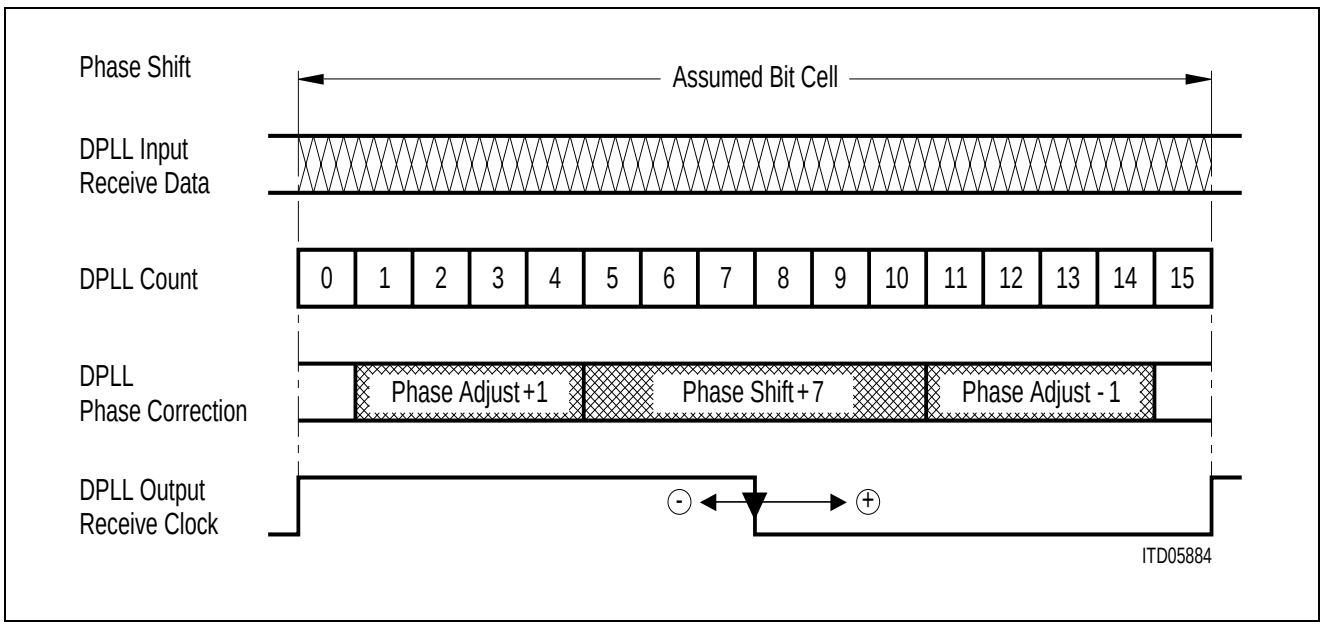


Figure 28d
Synchronization of the Data Clock in DPLL Mode: Interference Rejection and Phase Adjustment

The DPLL value and its corresponding phase shift in degree is listed below for the HSCX versions VA3 and V2.1:

HSCX Version	DPLL Count	Phase Shift
VA3	8	180°
V2.1	7	157,5°

Note: The operating characteristics of the DPLL therefore allow a phase jitter of 18.75% of the frequency.

5.3 Bus Configuration

Beside the point-to-point configuration, the HSCX effectively supports point-to-multipoint (pt-mpt, or bus) configurations by means of internal idle and collision detection/collision resolution methods.

In a pt-mpt configuration, comprising a central station (master) and several peripheral stations (slaves), or in a multimaster configuration (**see figure 6**)**,** data transmission can be initiated by each station over a common transmit line (bus). In case more than one station attempt to transmit data simultaneously (collision), the bus is assigned to one station by a collision-resolution procedure implemented by the HSCX. The bus assignment function is based on a priority principle with both fixed and rotating priorities that enables each station to access the bus in a predeterminable time. As a result, any number of transmitters can be connected to the serial bus.

Prerequisites for bus operation are:

– NRZ encoding
– OR connection of data at the bus
– feedback of bus information (C×DA/C×DB input)

The bus configuration is selected via the CCR1 register.

Note: Central clock supply for each station is not necessary if both the receive and transmit clock is recovered by the DPLL (clock mode 7). In this case, the function of the DPLL also minimizes the phase shift between the transmit clocks of the individual transmitters so that an opening flag sequence will be sufficient to allow a correct collision detection.

The bus mode can be operated independently of the clock mode, e.g. also during clock mode 1 (receive and transmission strobe) or clock mode 5 (programmable time-slots).

Bus Access Procedure

The idle state of the bus is identified by eight or more successive 1's. In case of a transmit request in the HSCX, the frame is transmitted and the bus is identified as busy with the first zero of the opening flag (start flag).

After the frame has been transmitted, the bus becomes available again by transmitting 1's.

Note: If the bus is occupied by other transmitters and/or there is no transmit request in the HSCX, log 1 will be continuously transmitted at the T×DA/T×DB output.

Collisions

During the transmitting process, the data transmitted from the HSCX is compared with the data on the bus. In case an erroneous bit is detected (log 1 sent and log 0 detected, or vice versa) the frame is immediately aborted, and idle (log 1) is transmitted. Transmission will be initiated again by the HSCX as soon as possible.

Since a transmitted zero is given priority over a 1 due to the OR connection at the bus, and since the individually combined stations in the address field of the transmitted HDLC frame differ from one another, the fact that a collision has occurred will be detected prior to or at the latest within the address field. The frame of the transmitter with the highest temporary priority (address field) is not affected and is transmitted without interruptions. All other transmitters terminate their operation immediately.

Note: If a wired OR connection has been realized by an external pull-up resistor without decoupling, the data output (T×DA/T×DB) can be used as an open drain output and connected directly to the C×DA, C×DB input.

Priority Principle

When the HDLC frame has been successfully transmitted by the HSCX, the priority is decremented. In order to transmit an additional frame, ten successive 1's must be present on the bus. This fact is used as a criterion to ensure that the higher priority transmitters do not contain any transmit requests. It is now possible to transmit a frame and the priority can be increased again (8 successive 1's). This method offers a priority allocation based on the selection of a particular address. It also ensures that each subscriber can access the bus at a pre-determinable time.

Timing Modes

If a bus configuration has been selected, the HSCX provides two timing modes, differing in the period between sending data and evaluation of the transmitted data for collision detection.

- timing mode 1 (CCR1: SC1, SC0 = 01)
  Data is output with the rising edge of the transmit clock via the T×D pins, and evaluated 1/2 clock period later with the falling clock edge at the C×D pins.
- timing mode 2 (CCR1: SC1, SC0 = 11)
  Data is output with the falling clock edge and evaluated with the next falling clock edge. Thus one complete clock period is available during data output and their evaluation.

Functions of RTS Output

In clock modes 0, 1, 4 and 5, the RTS output can be programmed via CCR2 (SOC bits) to be active when a frame is being transmitted. The signal is delayed by one clock period with respect to the data output T×DA/T×DB, and marks all data bits that could be transmitted without collision. In this way a configuration may be implemented in which the bus access is resolved on a local basis (collision bus) and where the data are sent one clock period later on a separate transmission line.

If the RTS output is used to control an external driver it has to be ANDed with the TxD pin in order to drive the first bit correctly.

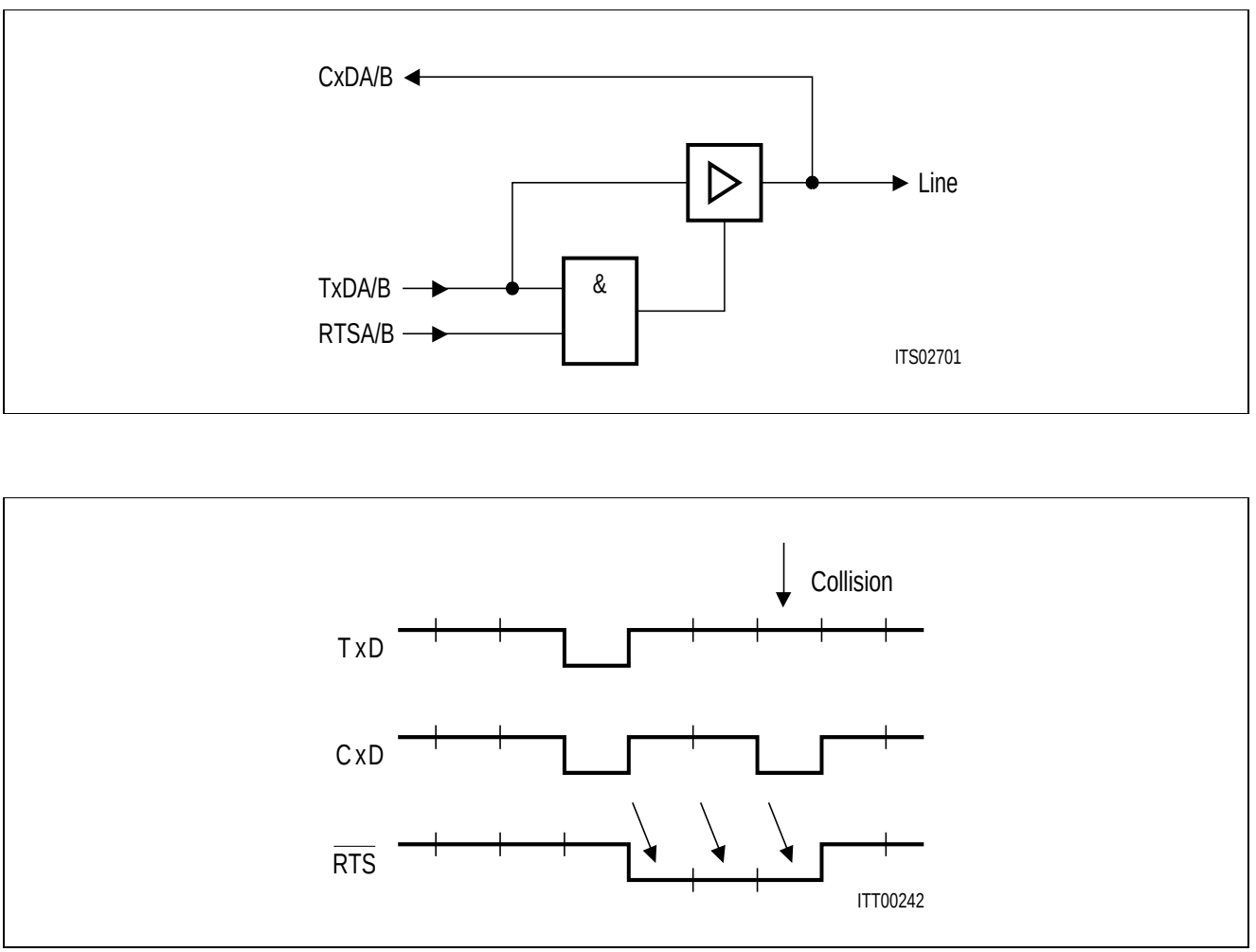


Figure 29
Request-to-Send in Bus Operation

Note: For regular and special RTS functions refer to **chapter 5.5 and 6.6.**

5.4 Data Encoding

In the point-to-point configuration, the HSCX supports both NRZ and NRZI data encoding (selectable via CCR1 register).

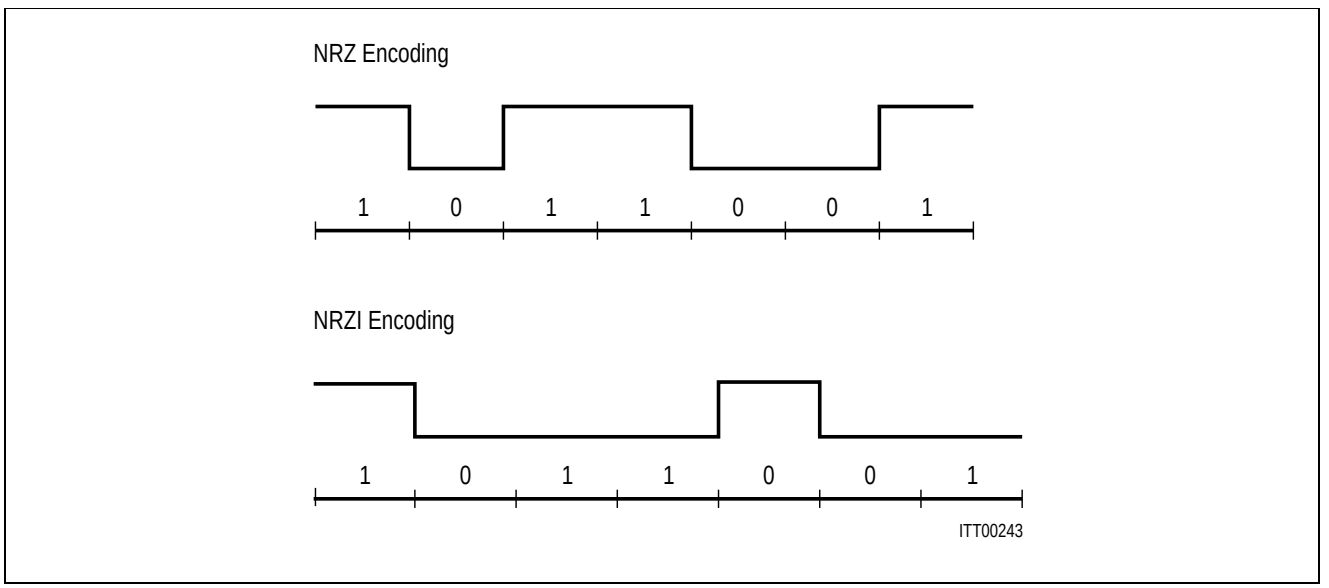


Figure 30
NRZ Encoding/NRZI Encoding

During NRZI encoding, level changes are interpreted as log 0, and no changes in level as log 1. Since no more than 5 successive log 1's can appear in a HDLC frame, this type of encoding is especially suitable in clock modes, where the clock is recovered from the received data by means of the DPLL circuits, because at least one transition appears within 5 clock cycles.

Thus, NRZI coding is especially recommended in clock modes 2, 3, 6, 7.
Data output is performed with the rising, data input with the falling clock edge.

5.5 Modem Control Functions (RTS/CTS, CD)

RTS/CTS Handshaking

The HSCX provides two pins (RTS, CTS) per serial channel supporting the standard RTS-CTS modem handshaking procedure to control the HDLC transmitters.

Data output is performed with the rising clock edge, data input with the falling clock edge. A transmit request will be indicated by outputting log 0 at the request-to-send output (RTSA/ RTSB). It is also possible to program the RTS outputs by software. After having received the permission to transmit (CTSA/CTSB) the HSCX transmits a frame.
In the case where permission to transmit is withdrawn during the transmission process, the frame is aborted (idle). After a new permission to transmit has been received and if all of the data are still available in the HSCX, the terminated frame will be re-transmitted (self-recovery), without interrupting the CPU. However, if the permission to transmit is withdrawn after the 32nd byte in the information field, the transmitter and the XFIFO are reset, the RTS output is deactivated and an interrupt is generated for the µC.

$\overline{\text{CTS}}$ Signal Clock Mode 5

In clock mode 5 the $\overline{\text{CTS}}$ signal is evaluated not only in the time-slot "window", but also between the time-slot "windows". $\overline{\text{CTS}}$ must not be disabled during the transmission of a frame. Even between the time-slot "windows" $\overline{\text{CTS}}$ has to be active until the transmission of the frame has been completed. Thus, $\overline{\text{CTS}}$ cannot be used to select/deselect particular time-slot "windows" for HSCX.

Note: In the case where permission to transmit is not required, the CTSA/CTSB inputs can be connected directly to V_{SS}.

Additionally, any state transition on the CTS input pin will generate an interrupt indicated via the EXIR register, if this function is enabled by setting the CIE bit in the CCR2 register.

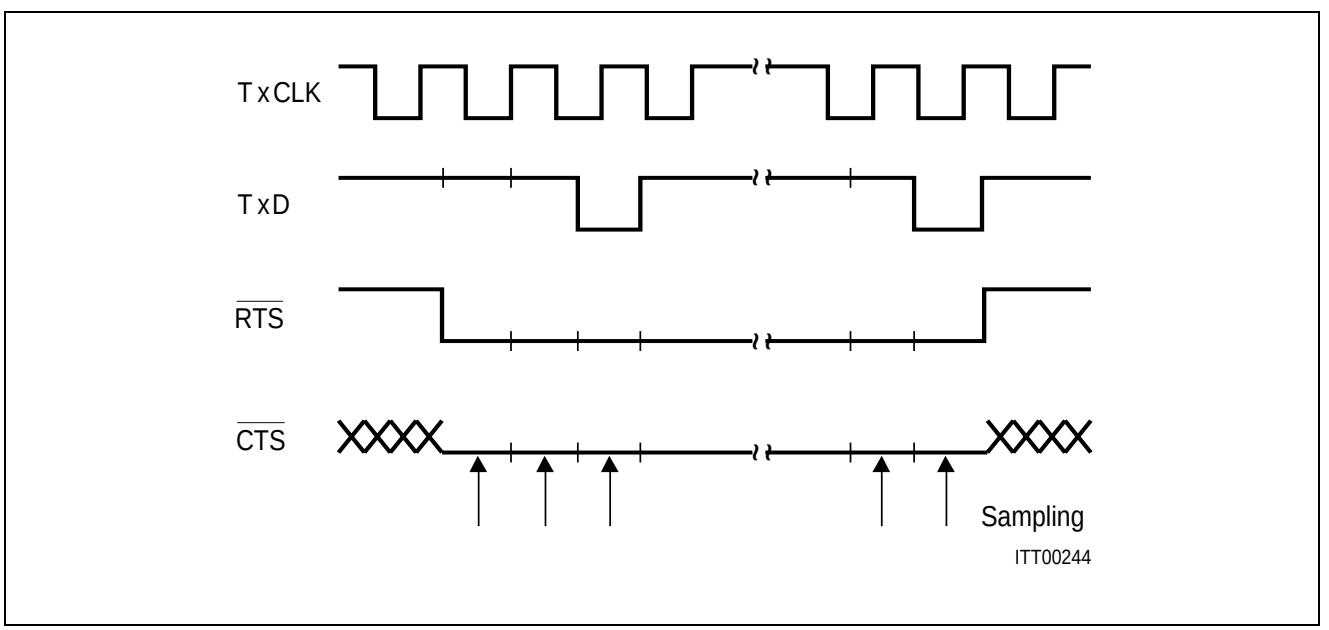


Figure 31
RTS-CTS Handshaking

Carrier Detect (CD) Receiver Control

Similar to the RTS/CTS control for the transmitter, the HSCX supports the carrier detect modem control function for the serial receivers, if the Carrier Detect Auto Start (CAS) function is programmed setting the CAS bit in the XBCH register. This function is always available in clock modes 0, 2, 3 via the A×CLK pin, and in clock modes 4, 6, 7 via the T× CLK pin only if it has been programmed as input clearing the TIO bit in the CCR2 register. In clock mode 1 the CD function is not supported (**see table 6** for an overview).

If the CAS function is selected, the respective HDLC receiver is enabled and data reception is started when an high level is sampled at the CD input.

6 Special Functions

6.1 Fully Transparent Transmission and Reception

When programmed to the extended transparent mode via the MODE register (MDS1, MDS0 = 11), each channel of the HSCX supports fully transparent data transmission and reception without HDLC framing overhead, i.e. without

- FLAG insertion and deletion
- CRC generation and checking
- Bit-stuffing mechanism.

In order to enable fully transparent data transfer, RAC bit in MODE has to be reset and FF_H has to be written to XAD1, XAD2 and RAH2.

Data transmission is always performed out of the transmit FIFO by directly shifting the contents of the XFIFO via the serial transmit data pin (T×D). Transmission is initiated by setting CMDR : XTF (08_H); end of transmission is indicated by EXIR : EXE (40_H).

In receive direction, the character currently assembled via the receive data line (R×D) is available in the RAL1 register. Additionally, in extended transparent mode 1 (MODE: MDS1, MDS0, ADM = 111), the received data is shifted into the RFIFO.

This feature can be profitably used e.g. for:

- user specific protocol variations
- the application of character oriented protocols (e.g. BISYNC)
- test purposes, line intentionally violation of HDLC protocol rules (e.g. wrong CRC)

Character synchronization can be achieved either in

- clock mode 1, with an external receive strobe input to A×CLK pin, or
- clock mode 5, with a programmed time-slot and a frame synchronization signal input to A × CLK.

Using clock mode 1 or 5 multiples of 8 bits received per time-slot.

6.2 Cyclic Transmission (Fully Transparent)

If the extended transparent mode is selected, the HSCX supports the continuous transmission of the transmit FIFO's contents.

After having written 1 to 32 bytes to the XFIFO, the command

XREP.XTF.XME

via the CMDR register (bit 7. . .0 = "00101010" = 2AH) forces the HSCX to repeatedly transmit the data stored in the XFIFO via T×D pin.

The cyclic transmission continues until a reset command (CMDR : XRES) is issued, after which continuous '1'-s are transmitted.

Note: In DMA-mode the command XREP, XTF has to be written to CMDR.

6.3 Continuous Transmission (DMA Mode only)

If data transfer from system memory to the HSCX is done by DMA (DMA bit in XBCH set), the number of bytes to be transmitted is usually defined via the Transmit Byte Count registers (XBCH, XBCL : bits XBC11. . .XBC0).

Setting the "Transmit Continuously" (XC) bit in XBCH, however, the byte count value is ignored and the DMA interface of the HSCX will continuously request for transmit data any time 32 bytes can be stored in the XFIFO.

This feature can be used e.g. to

- continuously transmit voice or data onto a PCM highway (clock mode 5/extended transparent mode), or to
- transmit frames exceeding the byte count programmable via XBCH, XBCL (frames with more than 4095 bytes).

Note: If the XC bit is reset during continuous transmission, the transmit byte count becomes valid again, and the HSCX will request the amount of DMA transfers programmed via XBC11. . .XBC0. Otherwise the continuous transmission is stopped when a data underrun condition occurs in the XFIFO, i.e. the DMA controller does not transfer further data to the HSCX. In this case continuous '1'-s (IDLE), without appending a CRC, are transmitted.

6.4 Receive Length Check Feature

The HSCX offers the possibility to supervise the maximum length of received frames and to terminate data reception in case this length is exceeded.

This feature is controlled via the special Receive Length Check Register (RLCR).

The function is enabled by setting the RC (Receive Check) bit in RLCR and programming the maximum frame length via bits RL6. . .RL0[1].

According to the value written to RL6. . .RL0, the maximum receive length can be adjusted in multiples of 32-byte blocks as follows:

$$\text{MAX. LENGTH} = (\text{RL} + 1) \times 32.$$

All frames exceeding this length are treated as if they have been aborted from the opposite station, i.e. the CPU is informed via a

– RME interrupt, and the
– RAB bit in RSTA register is set!

To distinguish between frames really aborted from the opposite station, the receive byte count (readable from RBCH, RBCL registers) exceeds the maximum receive length (via RL6. . .RL0) by one or two bytes in this case.

The check includes all data that is copied into the RFIFO. It does not include the address byte (s) if address recognition is selected. It includes the RSTA value in all operating modes.

[1] The frame length includes all bytes which are stored in the RFIFO.

6.5 One Bit Insertion

Similar to the zero bit insertion (bit-stuffing) mechanism, as defined by the HDLC protocol, the HSCX offers a completely new feature of inserting/deleting a one after seven consecutive zeros in the transmit/receive data stream, if the serial channel is operating in a bus configuration.

This method is profitable if clock recovery should be performed by DPLL.

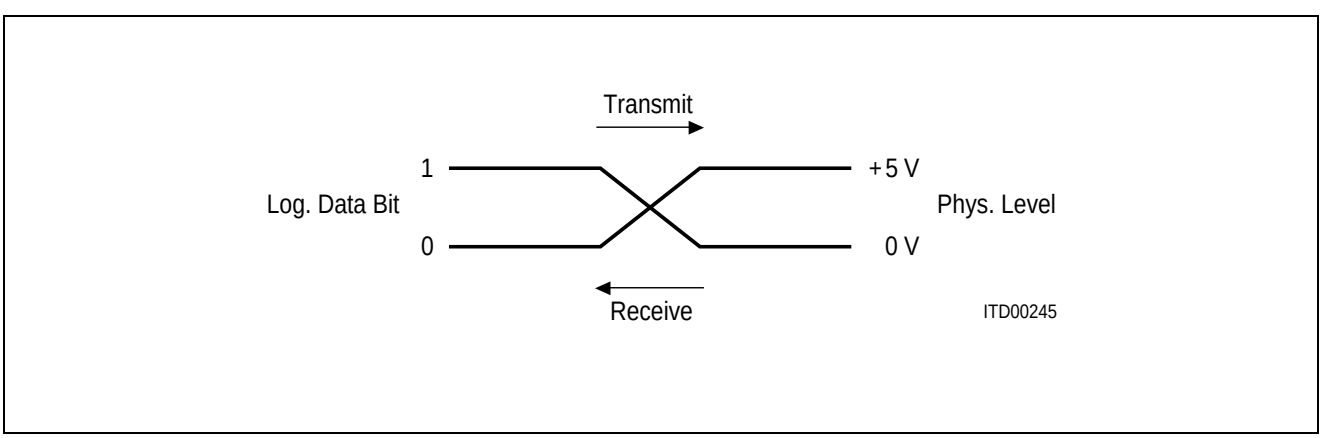
Since only NRZ data encoding is supported in a bus configuration (**see chapter 5.4**), there are possibly long sequences without edges in the receive data stream in case of successive "0"-s received, and the DPLL may loose synchronization.

Using the one bit insertion feature by setting the OIN bit in the CCR1 register, however, it is guaranteed that at least after
– 5 consecutive "1"-s a "0" will appear (bit-stuffing), and
– 7 consecutive "0"-s a "1" will appear (one insertion)
and thus a correct function of the DPLL is ensured.

Note: As with the bit-stuffing, this method is fully transparent to the user, but it is not in accordance with the HDLC protocol, i.e. it can only be applied in private systems using HSCX circuits exclusively.

6.6 Data Inversion

When NRZ data encoding has been selected, the HSCX may transmit and receive data inverted, i.e. a



"one" bit is transmitted as phys. zero (0 V) and a "zero" bit as phys. one (+ 5 V) via the T×D line.

This feature is selected by setting the DIV bit in the CCR2 register.

Please note that data cannot be inverted in bus mode unless you invert the T×D / R×D signal before it is sent into C×D.

6.7 Special RTS Function

Beyond the regular RTS function, signifying the transmission of a frame (Request To Send), the RTS output may be programmed for a special function via SOC1, SOC0 bits in the CCR2 register, provided the serial channel is operating in a bus configuration in clock mode 0, 1, or 5.

– If SOC1, SOC0 bits are set to ’11’; the RTS output is active (= low) during the reception of a frame.

– If SOC1, SOC0 bits are set to ’10’; the RTS output function is disabled and the RTS pin remains always high.

6.8 Test Mode

To provide for fast and efficient testing, the HSCX can be operated in the test mode by setting the TLP bit in the MODE register.

The on-chip serial input and output (T×DA – R×DA, T×DB – R×DB) are connected generating a local loopback.

R×DA and R×DB input is ignored. T×DA and T×DB remain active.

As a result, the user can perform a self-test of the HDLC channels of the HSCX.

7 Operational Description

7.1 RESET

The HSCX is forced into the reset state if a high signal is input to the RES pin for a minimum period of 1.8 µs. During RESET, the HSCX is temporarily in the power-up mode, and a subset of the registers is initialized with defined values.

After RESET, the HSCX is in power down mode, and the following registers contain defined values:

Table 7
RESET Values

Register	RESET Value	Meaning
CCR1	00_H	– power down mode serial port configuration; pt-pt, NRZ coding, transmit data pins are open drain outputs – clock mode 0
CCR2	00_H	RTS pin normal function – CTS and RFS interrupts disabled no data inversion
MODE	00_H	auto-mode 1 byte address field external timer mode – receivers inactive RTS output controlled by HSCX, timer resolution: k = 32.768, no testloop
STAR	48_H	XFIFO write enable receive line inactive no commands executing
ISTA EXIR	00_H	– no interrupts masked
CMDR	00_H	no commands
XBCH RBCH	00_H	– interrupt controlled data transfer (DMA disabled) – full-duplex LAPB/LAPD operation of LAP controller – carrier detect auto start of receiver disabled
XCCR RCCR	00_H	1-bit time-slot

7.2 Initialization

After reset the CPU has to write a minimum set of registers and an optionally set dependent on the required features and operating modes.

First, the configuration of the serial port and the clock mode has to be defined via the CCR1 register. The clock mode must be set before power-up, or in the same step with power-up.

The CPU may switch the HSCX between power-up and power-down mode, which has no influence upon the contents of the registers, i.e. the internal state remains stored.

In power-down mode however, all internal clocks and the oscillator circuitry are disabled, no interrupts are forwarded to the CPU.

This state can be used as standby mode, when the HSCX is temporarily not used, thus lessening the power consumption to a high degree.

The individual operating mode must be defined writing the MODE register.

The need for programming further registers depends on the selected features (clock mode, operating mode, address mode, user demands) according to the following tables:

Clock Mode	Register
0, 1	–
2, 3, 4, 6, 7	BGR, CCR2
5	CCR2, TSAR, TSAX, XCCR, RCCR

Table 8
Register Setup

Operating Mode \ Address Mode	2 Byte Address Field (MODE: ADM = 1)	1 Byte Address Field (MODE: ADM = 0)
Auto	TIMR XAD1 XAD2 RAH1 RAH2 RAL1 RAL2	RAH1 set to 00_H RAH2 RAL1 RAL2
Non Auto	RAH1 RAH2 RAL1 RAL2	RAH1 set to 00_H RAH2 set to 00_H RAL1
Transparent	RAH1 RAH2	–

Table 9
User Demand Registers

User Demand	Register
CTS/RFS Interrupt Provided	CCR2
Selective Interrupts Should be Masked	MASK
Timer will be used by CPU (external timer mode)	TIMR
DMA Controlled Data Transfer	XBCH
Receive Length Check Feature	RLCR
Extended (module 128) Counting	RAH2

7.3 Operational Phase

After having performed the initialization, the CPU switches each individual channel of the HSCX into operational phase by setting the PU bit in the CCR1 register (power-up, if not already done during initialization).
Initially, the CPU should bring the transmitter and receiver to a defined state by issuing a XRES (transmitter reset) and RHR (receiver reset) command via the CMDR register. If data reception should be performed, the receiver must be activated by setting the RAC bit in MODE to 1.
If no "Clear to send" function is provided via a modem, the CTS pin of the HSCX must be connected directly to ground, in order to enable data transmission.
Now the HSCX is ready to transmit and receive data. The control of the data transfer phase is mainly done by commands from CPU to HSCX via the CMDR register, and by interrupt indications from HSCX to CPU.
Additional status information, which does not trigger an interrupt, is available in the STAR register.

7.4 Data Transmission

Interrupt Mode

In transmit direction 2×32 byte FIFO buffers (transmit pools) are provided for each channel. After checking the XFIFO status by polling the Transmit FIFO Write Enable bit (XFW in STAR register) or after a Transmit Pool Ready (XPR) interrupt, up to 32 bytes may be entered by the CPU to the XFIFO.
The transmission of a frame can then be started issuing a XTF or XIF command via the CMDR register. If the transmit command does not include an end of message indication (CMDR : XME), the HSCX will repeatedly request for the next data block by means of a XPR interrupt as soon as no more than 32 bytes are stored in the XFIFO, i.e. a 32-byte pool is accessible to the CPU.
This process will be repeated until the CPU indicates the end of message per command, after which frame transmission is finished correctly by appending the CRC and closing flag sequence.
In case no more data is available in the XFIFO prior to the arrival of XME, the transmission of the frame is terminated with an abort sequence and the CPU is notified per interrupt (EXIR : XDU). The frame may also be aborted per software (CMDR : XRES).
The data transmission sequence, from the CPU's point of view, is outlined in **figure 32.**

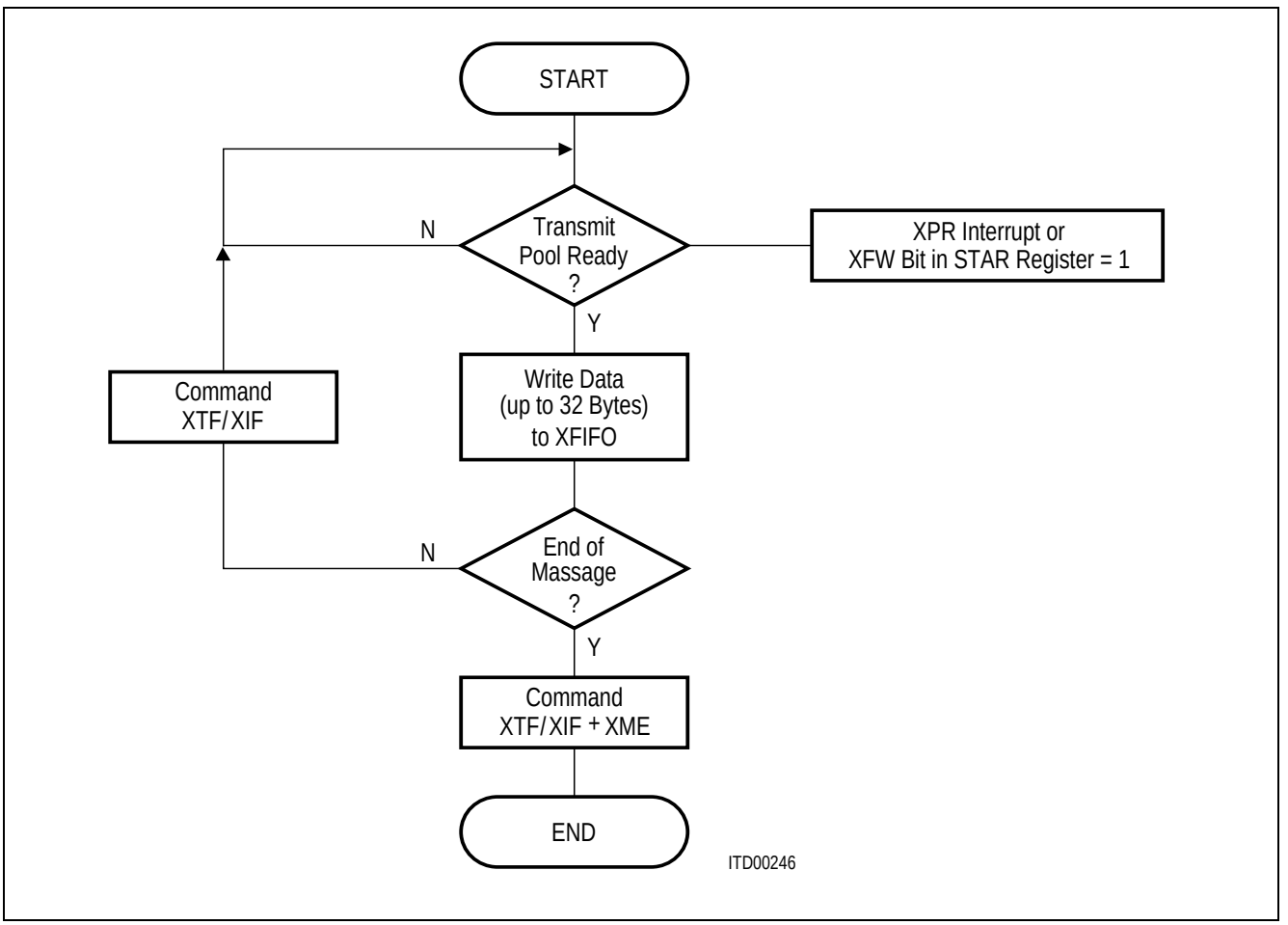


Figure 32
Interrupt Driven Data Transmission (Flow Diagram)

The activities at both serial and CPU interface during frame transmission (supposed frame length = 70 bytes) is shown in **figure 33.**

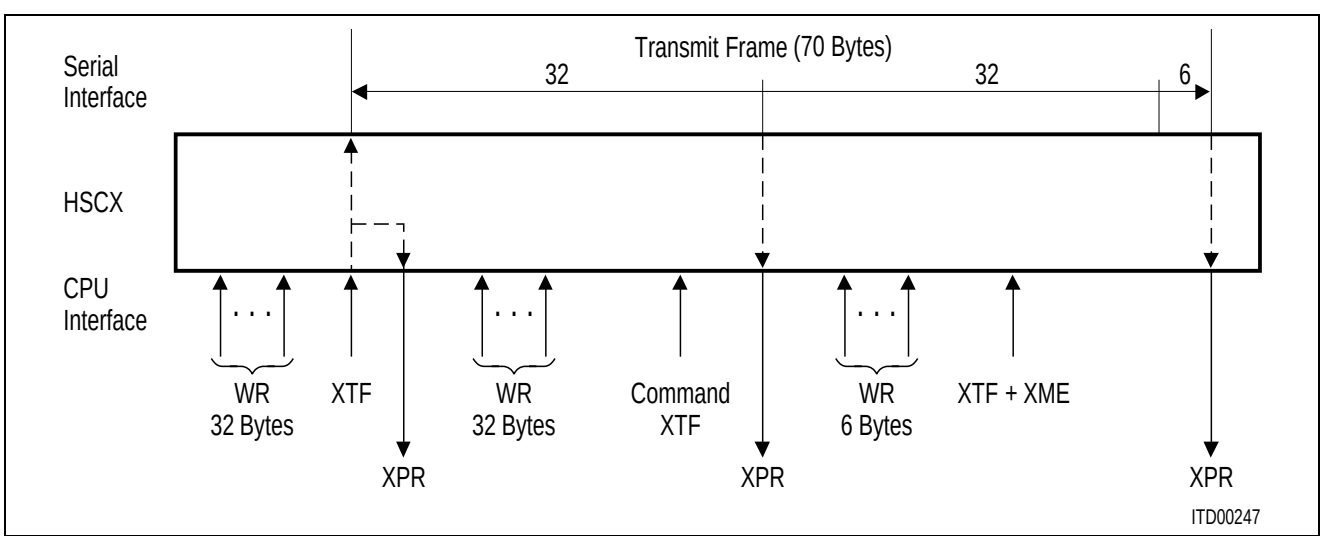


Figure 33
Interrupt Driven Transmission Sequence Example

Back to Back Frames

If two or more frames should be transmitted in a high speed sequence without interframe time fill, the transmission sequence according **figure 34** has to be used.

This means that the closing flag will be immediately followed by an opening flag. The HSCX receiver, however, is capable of receiving frames separated by only one (shared) flag.

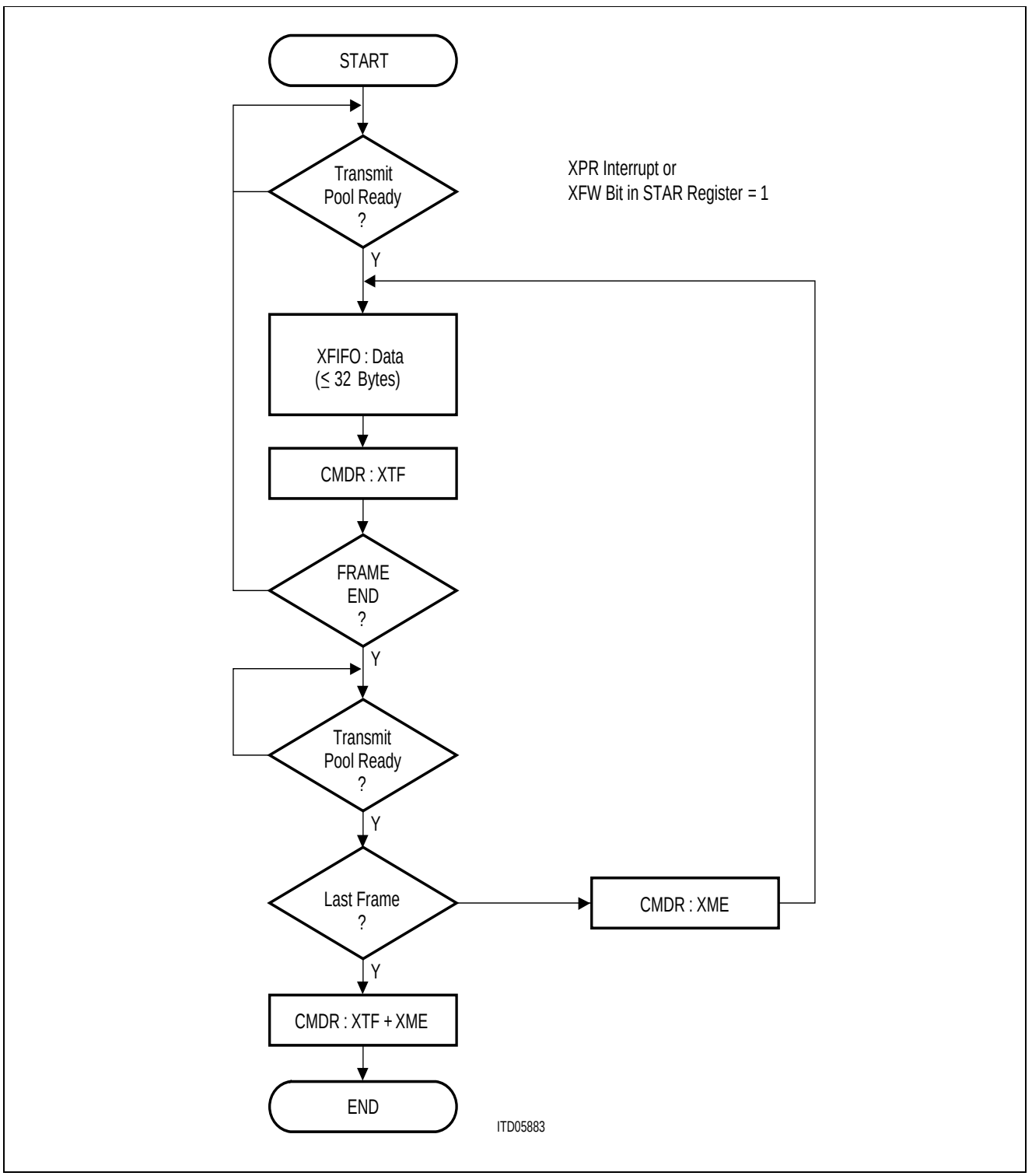


Figure 34
Continuous Frames Transmission (Flow Diagram)

The activities during frame transmission (supposed two frames, 18 bytes and 52 bytes) is shown in **figure 35.**

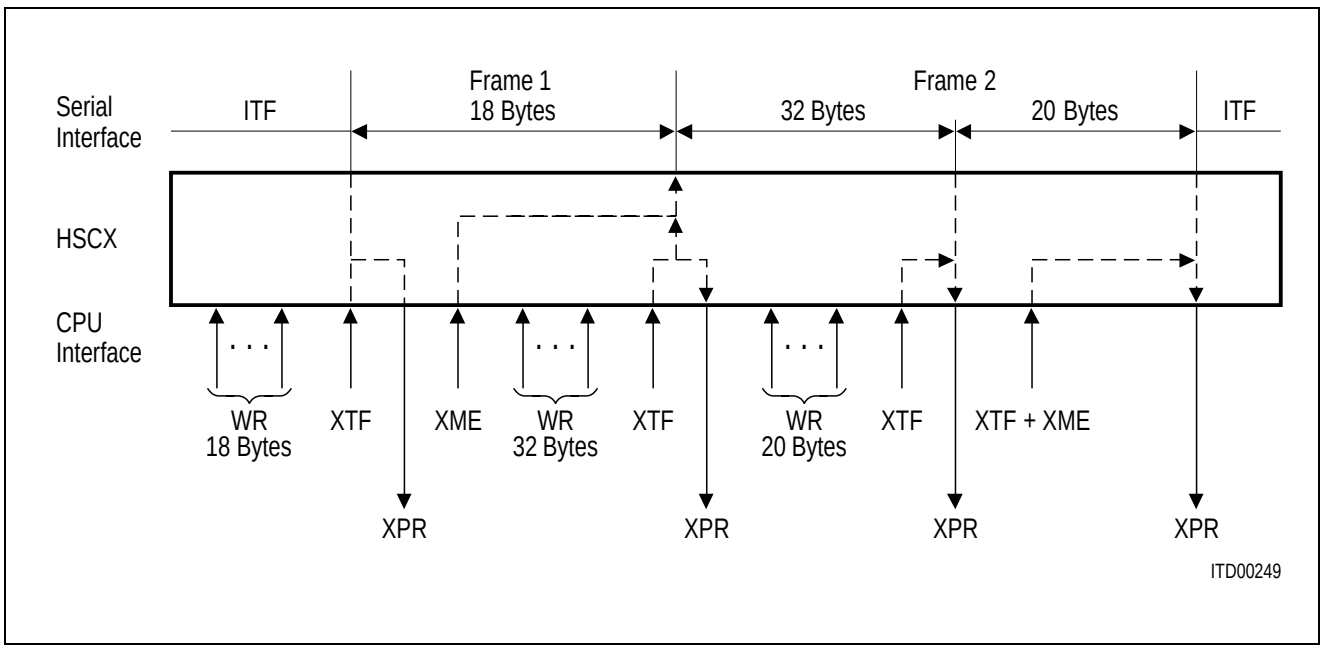


Figure 35
Continuous Frames Transmission Sequence Example

DMA Mode

Prior to the data transmission, the length of the next frame to be transmitted must be programmed via the Transmit Byte Count Registers (XBCH, XBCL). The resulting byte count equals the programmed value plus one byte, i.e. since 12 bits are provided via XBCH, XBCL (XBC11. . .XBC0) a frame length of 1 up to 4096 bytes (4 Kbytes) can be selected.

After this, data transmission can be initiated by command (XTF or XIF). The HSCX will then autonomously request the correct amount of write bus cycles by activating the DRQT line. Depending on the programmed frame length, block data transfers of

$n \times 32$-bytes + remainder (n = 0, 1,…128)

are requested everytime a 32-byte FIFO half (transmit pool) is empty and accessible to the DMA controller.

The following figure gives an example of a DMA driven transmission sequence with a supposed frame length of 70 bytes, i.e. programmed transmit byte count (XCNT) equal 69 bytes.

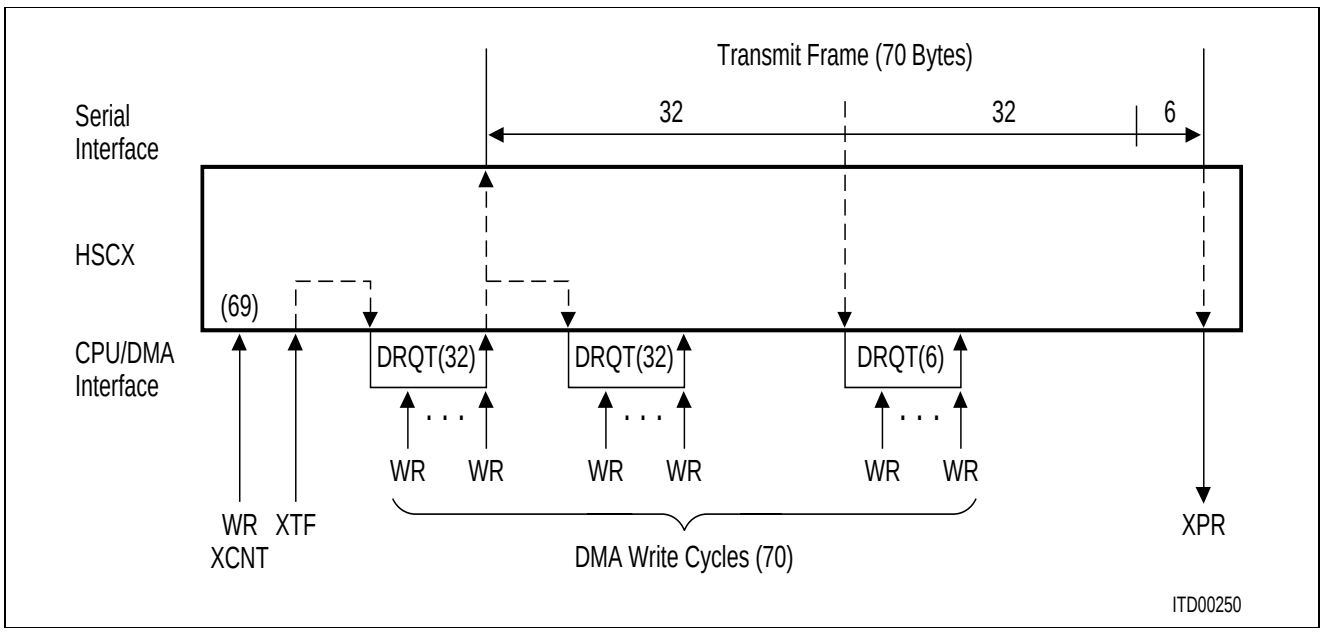


Figure 36
DMA Driven Transmission Sequence Example

7.5 Data Reception

Interrupt Mode

Also 2×32 byte FIFO buffers (receive pools) are provided for each channel in receive direction.

There are two different interrupt indications concerned with the reception of data:

– RPF (Receive Pool Full) interrupt, indicating that a 32 byte block of data can be read from the RFIFO and the received message is not yet complete.

– RME (Receive Message End) interrupt, indicating that the reception of one message is completed, i.e. either

- one message with less than 32 bytes, or the
- last part of a message with more than 32 bytes

is stored in the RFIFO.

After an interrupt has been processed, i.e. the received data has been read from the RFIFO, this must be explicitly acknowledged by the CPU issuing a RMC (Receive Message Complete) command.

The CPU has to handle the RPF interrupt before additional 32 bytes are received via the serial interface which would cause a "Receive Data Overflow" condition.

In addition to the message end (RME) interrupt, the following information about the received frame is stored by the HSCX in special registers and/or RFIFO:

Table 10
Status Information after RME Interrupt

Length of message (bytes) →	RBCH, RBCL	register
Address combination and/or →	RSTA	RFIFO: last byte
Address field →	RAL1	RFIFO
Control field →	RHCR	RFIFO
Type of frame (COMMAND/RESPONSE) →	RSTA	RFIFO: last byte
CRC result (good/bad) →	RSTA	RFIFO: last byte
Valid frame (yes/no) →	RSTA	RFIFO: last byte
ABORT sequence recognized (yes/no) →	RSTA	RFIFO: last byte
Data overflow →	RSTA	RFIFO: last byte

The following figure gives an example of an interrupt controlled reception sequence, supposed that a long frame (66 bytes) followed by two short frames (6 bytes each) are received.

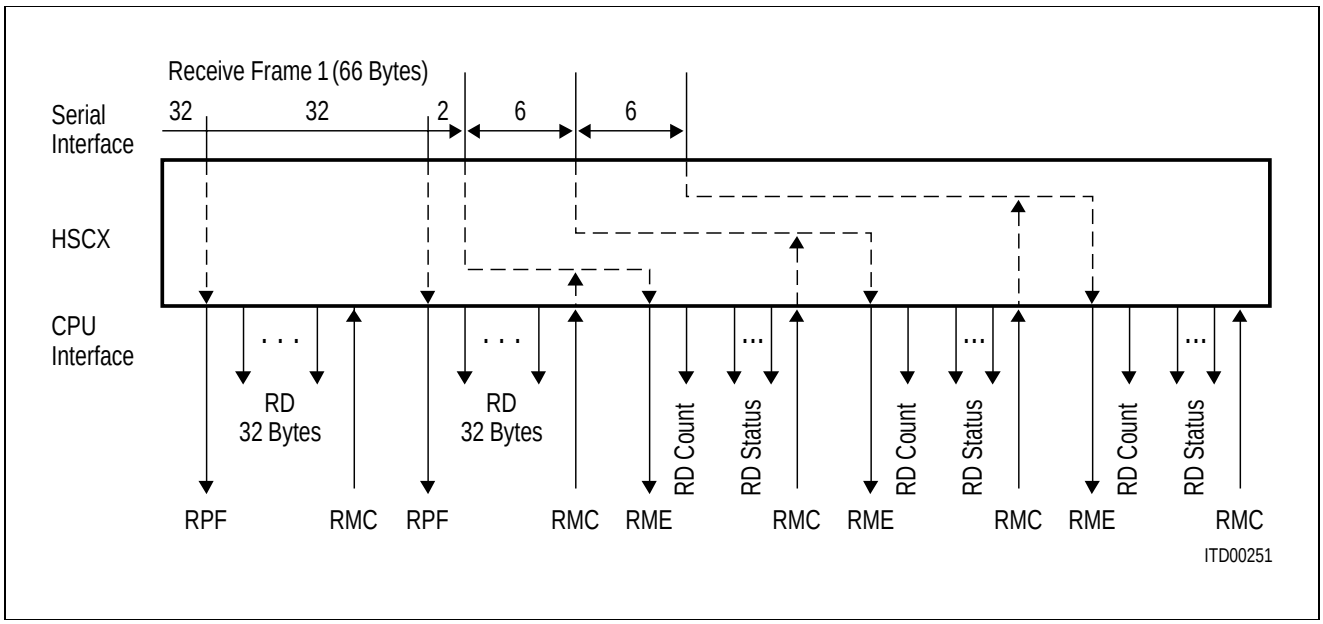


Figure 37
Interrupt Driven Reception Sequence Example

DMA Mode

If the RFIFO contains 32 bytes, the HSCX autonomously requests a block data transfer by DMA activating the DRQR line as long as the start of the 32nd read cycle. This forces the DMA controller to continuously perform bus cycles till 32 bytes are transferred from the HSCX to the system memory.

If the RFIFO contains less than 32 bytes (one short frame or the last part of a long frame) the HSCX requests a block data transfer depending on the contents of the RFIFO according to the following table:

RFIFO Contents (Bytes)	DMA Request (Bytes)
1, 2, 3	4
4 - 7	8
8 - 15	16
16 - 32	32

Note: All available status informations after RME are summarized in **table 10.**

After the DMA controller has been set up for the reception of the next frame, the CPU must be issue a RMC command to acknowledge the completion of the receive frame processing.

The HSCX will not initiate further DMA cycles by activating the DRQR line prior to the reception of RMC.

Note: It's also possible to set up the DMA controller immediately after the start of a frame has been detected using the HSCX's RFS (Receive Frame Start) interrupt option (**see chapter 4.3**).

The following figure gives an example of a DMA controlled reception sequence, supposed that a long frame (66 bytes) followed by two short frames (6 bytes each) are received.

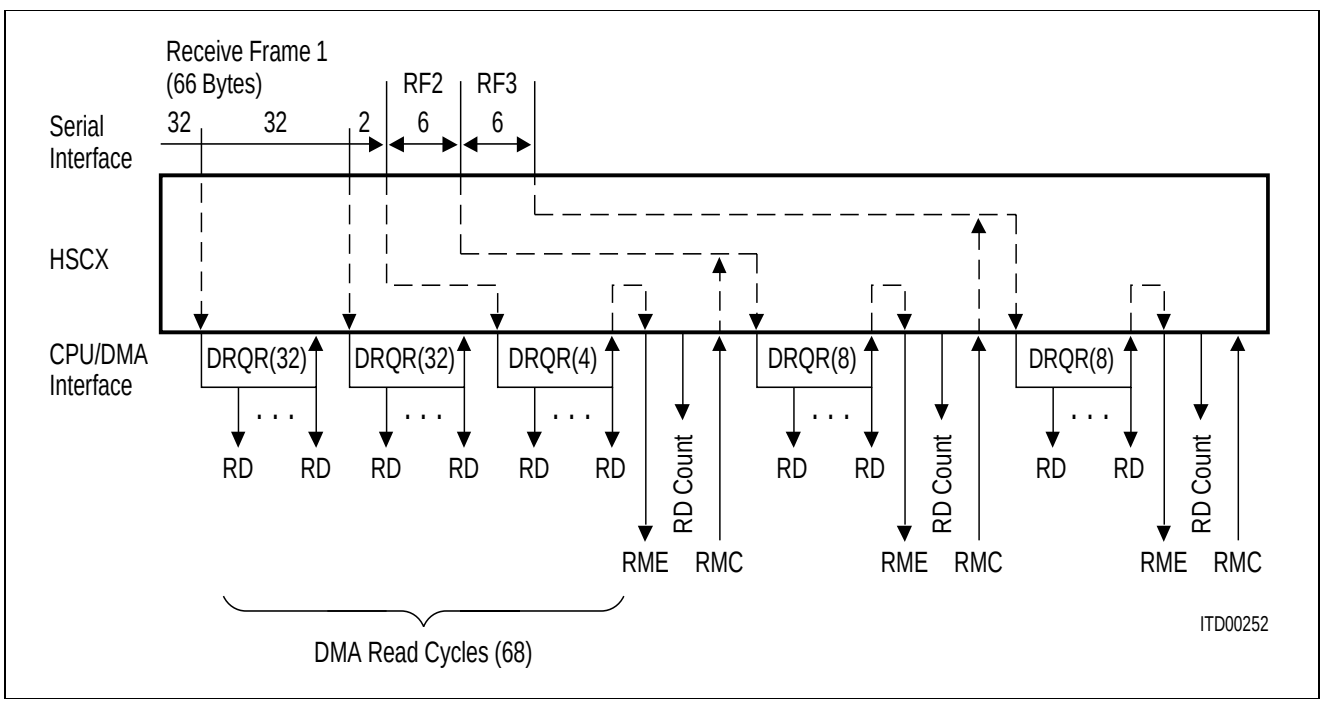


Figure 38
DMA Driven Reception Sequence Example

8 Detailed Register Description

8.1 Register Address Arrangement

Table 11
Layout of Register Addresses

ADDRESS Channel A	ADDRESS Channel B	REGISTER Read	REGISTER Write		Refer to page:	
00 ⋮ 1F	40 ⋮ 5F	RFIFO	XFIFO	Receive/Transmit FIFO	73	74
20	60	ISTA	MASK	Interrupt STAtus/Mask	75	76
21	61	STAR	CMDR	STAtus/CoManD	79	80
22	62	MODE		MODE	82	
23	63	TIMR		TIMer	84	
24	64	EXIR	XAD1	EXtended Interrupt/Transmit ADdress 1	85	85
25	65	RBCL	XAD2	Receive Byte Count Low/Transmit ADdress 2	86	86
26	66	–	RAH1	Receive Address High 1	–	87
27	67	RSTA	RAH2	Receive STAtus/Rec. Addr. High 2	87	87
28	68	RAL1	RAL1	Receive Address Low 1	90	
29	69	RHCR	RAL2	Receive HDLC Control/Receive Addr. Low 2	91	90
2A	6A	–	XBCL	Transmit Byte Count Low	–	92
2B	6B	–	BGR	Baudrate Generator Register	–	92
2C	6C	CCR2		Channel Configuration Register 2	93	
2D	6D	RBCH	XBCH	Receive/Transmit Byte Count High	96	95
2E	6E	VSTR	RLCR	Version STatus/Receive Frame Length Check	96	97
2F	6F	CCR1		Channel Configuration Register 1	97	
30	70	–	TSAX	Time-Slot Assignment Transmit	–	99
31	71	–	TSAR	Time-Slot Assignment Receive	–	99
32	72	–	XCCR	Transmit Channel Capacity	–	99
33	73	–	RCCR	Receive Channel Capacity	–	99

Note: Channel A is not implemented in SAB 82526

8.2 Register Definitions

Receive FIFO (Read) RFIFO (00. . .1F/40. . .5F)

- Interrupt Controlled Data Transfer (Interrupt Mode)
  selected if DMA bit in XBCH is reset.

Up to 32 bytes of receive data can be read from the RFIFO following an RPF or an RME interrupt.

RPF Interrupt: Exactly 32 bytes to be read.
RME Interrupt: Number of bytes to be determined by reading the RBCL, RBCH registers.

- DMA Controlled Data Transfer (DMA Mode)
  selected if DMA bit in XBCH

If the RFIFO contains 32 bytes, the HSCX autonomously requests a block data transfer by DMA activating the DRQR line as long as the start of the 32nd read cycle. This forces the DMA controller to continuously perform bus cycles till 32 bytes are transferred from the HSCX to the system memory, (level triggered, demand transfer mode of DMA controller).

If the RFIFO contains less than 32 bytes (one short frame or the last of a long frame) the HSCX requests a block data transfer depending on the contents of the RFIFO according to the following table:

RFIFO Contents (Bytes)	DMA Request (Bytes)
1, 2, 3	4
4 - 7	8
8 - 15	16
16 - 32	32

Additionally an RME interrupt is issued after the last byte has been transferred.

As a result, the DMA controller may transfer more bytes as actually valid in the current received frame. The valid byte count must therefore be determined by reading the RBCH, RBCL registers following the RME interrupt.

Transmit FIFO (WRITE) XFIFO (00. . .1F/40. . .5F)

- Interrupt Mode
  selected if DMA bit in XBCH is reset.

Up to 32 bytes of transmit data can be written to the XFIFO following an XPR interrupt.

- DMA Mode
  selected if DMA bit in XBCH is set.

Prior to any data transfer, the actual byte count of the frame to be transmitted must be written to the XBCH, XBCL registers by the user.

If data transfer is then initiated via the CMDR register (command XTF or XIF), the HSCX autonomously requests the correct amount of block data transfers ($n \times 32 + REST$, $n = 0, 1, \ldots$).

Note: Addresses within the address space of the FIFO's are interpreted equally, i.e. the actual data byte can be accessed with any address within the valid scope.

Interrupt Status Register (READ)

	7							0	
ISTA	RME	RPF	RSC	XPR	TIN	ICA	EXA	EXB	(20/60)

Value after RESET: 00_H

RME. . .Receive Message End

One message up to 32 bytes or the last part of a message greater then 32 bytes has been received and is now available in the RFIFO. The message is complete!
The actual message length can be determined reading the RBCH, RBCL registers.
Additional information is available in the RSTA register.

RPF. . .Receive Pool Full

A block of 32 bytes of a message is stored in the RFIFO. The message is not yet completed!
Note: This interrupt is only generated in Interrupt Mode!

RSC. . .Receive Status Change (significant in auto-mode only!)

A status change (receiver ready/receiver not ready) of the opposite station has been detected in auto-mode. (i.e. the HSCX has received a RR/RNR supervisory frame according to the HDLC protocol.) The current status can be read from the STAR register (RRNR bit).

XPR. . .Transmit Pool Ready

A data block of up to 32 bytes can be written to the transmit FIFO.

TIN. . .Timer Interrupt

The internal timer and repeat counter has been expired. (**See also description of TIMR register!**)

ICA … Interrupt of Channel A (Channel B only)

Indicates, that an interrupt is caused by channel A and the interrupt source(s) is (are) indicated in the ISTA register of channel A (i.e. at least one bit of the ISTA register of channel A is set).

EXA … Extended Interrupt of Channel A (Channel B only)

An interrupt is caused by channel B and source(s) is (are) indicated in the EXIR register of channel B.

Note: The ICA, EXA, and EXB bit are present in channel B only and point to the ISTA (CHA), EXIR (CHA), and EXIR (CHB) registers.

After the HSCX has requested an interrupt by turning its $\overline{INT}$ pin to low, the CPU must first read the ISTA register of channel B and check the state of these bits in order to determine which interrupt source(s) of which channel(s) has caused the interrupt. More than one interrupt source may be indicated by a single interrupt request.

After the respective register has been read, EXA, and EXB are reset. All other bits will be reset after reading ISTA. To prevent malfunctions, each bit is individually monitored and reset.

To generate edges at the $\overline{INT}$ pin it is necessary to mask all interrupts at the end of the interrupt service routine and write back the old mask to the mask register.

Mask Register (WRITE)

	7							0	
MASK	RME	RPF	RSC	XPR	TIN	ICA	EXA	EXB	(20/60)

Value after RESET: 00_H (all interrupts enabled)

Each interrupt source can be selectively masked by setting the respective bit in MASK (bit positions corresponding to ISTA register). Masked interrupts are not indicated when reading ISTA. Instead, they remain internally stored and will be indicated after the respective MASK bit is reset.

Note: In the event of an extended interrupt, no interrupt request will be generated with a masked EXA, EXB bit, although this bit is set in ISTA.

Extended Interrupt Register (READ)

Value after RESET: 00_H

	7							0	
EXIR	XMR	XDU EXE	PCE	RFO	CSC	RFS	0	0	(24/64)

XMR … Transmit Message Repeat

The transmission of the last message has to be repeated because
- the HSCX has received a negative acknowledgement in auto-mode,
- or a collision has occurred after sending the 32nd data byte of a message in a bus configuration.
- or CTS (transmission enable) has been withdrawn after sending the 32nd data byte of a message in point-to-point configuration.

XDU/EXE … Transmit Data Underrun/Extended Transmission End

The actual frame has been aborted with IDLE, because the XFIFO holds no further data, but the frame is not yet complete!

In extended transparent mode, this bit indicates the transmission-end condition.

Note: It is not possible to send transparent-, or I-frames when a XMR or XDU interrupt is indicated.

PCE … Protocol Error (significant in auto-mode only!)

The HSCX has detected a protocol error, i.e. it has received
– an S-, or I-frame with incorrect N (R)
– an S-frame containing an I-field.

RFO … Receive Frame Overflow

One frame could not be stored due to occupied RFIFO (i.e. whole frame has been lost). This interrupt can be used for statistical purposes and indicates, that the CPU does not respond quickly enough to an incoming RPF, or RME interrupt.

CSC … Clear to send Status Change

Indicates, that a state transition has occurred at the CTS pin. The actual state can be read from STAR register (CTS bit).

This interrupt must be enabled setting the CIE bit in CCR2.

RFS. . .Receive Frame Start

This is an early receiver interrupt activated after the start of a valid frame has been detected, i.e. after a valid address check in operation modes providing address recognition, otherwise after the opening flag (transparent mode 0), delayed by two bytes.

After an RFS interrupt, the contents of

- RHCR
- RAL1
- RSTA – bit 3-0

  are valid and can be read by the CPU.

This interrupt must be enabled setting the RIE bit in CCR2.

Status Register (READ)

Value after RESET: 48_H

	7							0	
STAR	XDOV	XFW	XRNR	RRNR	RLI	CEC	CTS	WFA	(21/61)

XDOV … Transmit Data Overflow

More than 32 bytes have been written to the XFIFO.

XFW … Transmit FIFO Write Enable

Data can be written to the XFIFO.

Note: XFW is valid if CEC = 0 only!

XRNR … Transmit RNR (significant in auto-mode only!)

Indicates the status of the HSCX.
0 … receiver ready
1 … receiver not ready

RRNR … Receive RNR (significant in auto-mode only!)

Indicates the status of the remote station.
0 … receiver ready
1 … receiver not ready

RLI … Receive Line Inactive

Neither FLAGs as interframe time fill nor frames are received via the receive line.

Note: Significant in point-to-point configurations!

CEC … Command Executing

0 … no command is currently executed, the CMDR register can be written to.
1 … a command (written previously to CMDR) is currently executed, no further command can be temporarily written via CMDR register.

Note: CEC will be active at most 2.5 transmit clock periods. If the HSCX is in power down mode CEC will stay active.

CTS … Clear To Send State

If the CIE bit in CCR2 is set, this bit indicates the state of the CTS pin.
0 … CTS is inactive (high signal at CTS)
1 … CTS is active (low signal at CTS)

WFA … Waiting for Acknowledgement (significant in auto-mode only)

Indicates the ’Waiting for Acknowledgement’ status of HSCX.

Command Register (WRITE)

Value after RESET: 00_H

	7							0	
CMDR	RMC	RHR	RNR XREP	STI	XTF	XIF	XME	XRES	(21/61)

Note: The maximum time between writing to the CMDR register and the execution of the command is 2.5 clock cycles. Therefore, if the CPU operates with a very high clock in comparison with the HSCX's clock, it's recommended that the CEC bit of the STAR register is checked before writing to the CMDR register to avoid any loss of commands.

RMC … Receive Message Complete

Confirmation from CPU to HSCX, that the actual frame or data block has been fetched following an RPF or RME interrupt, thus the occupied space in the RFIFO can be released.

Note: In DMA mode, this command is only issued once after a RME interrupt. The HSCX does not generate further DMA requests prior to the reception of this command.

RHR … Reset HDLC Receiver

All data in the RFIFO and the HDLC receiver deleted.

In auto-mode, additionally the transmit and receive sequence number counters are reset.

RNR/XREP … Receiver Not Ready/Transmission Repeat

The function of this command depends on the selected operation mode (MDS1, MDS0, ADM bit in MODE):

- Auto-mode: RNR

The status of the HSCX receiver is set. Determines, whether a received frame is acknowledged via an RR, or RNR supervisory frame in auto-mode.

0 … Receiver Ready (RR)
1 … Receiver Not Ready (RNR)

- Extended transparent mode 0, 1 : XREP

Together with XTF and XME set (write 2 A_H to CMDR), the HSCX repeatedly transmits the contents of the XFIFO (1 … 32 bytes) without HDLC framing fully transparent, i.e. without FLAG, CRC insertion, bit stuffing.

The cyclic transmission is stopped with an XRES command!

STI … Start Timer

The internal timer is started.

Note: The timer is stopped by rewriting the TIMR register after start.

XTF … Transmit Transparent Frame

- Interrupt mode

After having written up to 32 bytes the XFIFO, this command initiates the transmission of a transparent frame. An opening flag sequence is automatically added to the data by the HSCX.

- DMA mode

After having written the length of the frame to be transmitted to the XBCH, XBCL registers, this command initiates the data transfer from system memory to HSCX by DMA. Serial data transmission starts as soon as 32 bytes are stored in the XFIFO.

XIF … Transmit I-Frame (used in auto-mode only!)

Initiates the transmission of an I-frame in auto-mode. Additional to the opening flag sequence, the address and control field of the frame is automatically added by HSCX.

XME … Transmit Message End (used in interrupt mode only!)

Indicates, that the data block written last to the transmit FIFO completes the actual frame. The HSCX can terminate the transmission operation properly by appending the CRC and the closing flag sequence to the data.

In DMA mode, the end of the frame is determined by the transmit byte count in XBCH, XBCL! This bit must not be set in DMA mode.

XRES … Transmit Reset

The contents of the XFIFO is deleted and IDLE is transmitted. This command can be used by the CPU to abort a frame currently in transmission. After setting XRES an XPR interrupt is generated in every case.

Mode Register (READ/WRITE)

Value after RESET: 00_H

	7							0	
MODE	MDS1	MDS0	ADM	TMD	RAC	RTS	TRS	TLP	(22/62)

MDS1, MDS0 … Mode Select

The operating mode of the HDLC controller is selected.

00 … auto-mode
01 … non-auto mode
10 … transparent mode
11 … extended transparent mode

ADM … Address Mode

The meaning of this bit varies depending on the selected operating mode:

- Auto-mode, non-auto mode

Defines the length of the HDLC address field.
0 … 8-bit address field
1 … 16-bit address field

In transparent modes, this bit differentiates between two sub-modes:

- Transparent mode

0 … transparent mode 0; no address recognition.
1 … transparent mode 1; high byte address recognition.

- Extended transparent mode; without HDLC framing.

0 … extended transparent mode 0; received data in RAL1.
1 … extended transparent mode 1; received data in RFIFO and RAL1.

Note: In extended transparent modes, the RAC bit must set to "0" to enable fully transparent reception!

TMD … Timer Mode

The operation mode of the internal timer is set.

0 … external mode

The timer is controlled by the CPU and can be started at any time setting the STI bit in CMDR.

1 … internal mode

The timer is used internally by the HSCX for time-out and retry conditions in auto-mode. (refer to the description of the TIMR register)

RAC … Receiver Active

Switches the receiver to inoperational state.

0 … HDLC receiver inactive

1 … HDLC receiver active

In extended transparent modes this bit must be reset to enable fully transparent reception!

RTS … Request To Send

Defines the state and control of RTS pin.

0 … The RTS pin is controlled by the HSCX autonomously.

RTS is activated when a frame transmission starts and deactivated after the transmission operation is completed.

1 … The RTS pin is controlled by the CPU.

If this bit is set, the RTS pin is activated immediately and remains active till this bit is reset (not valid in bus configuration).

TRS … Timer Resolution

The resolution of the internal timer (factor k, see description of TIMR register) is selected

0 … k = 32.768

1 … k = 512

TLP … Test Loop

RxD is disconnected from the mechanical pin and internally connected to TxD of the same channel. TxD pin remains active.

Timer Register (READ/WRITE)

	75	40	
TIMR	CNT	VALUE	(23/63)

VALUE … Sets the time period t_1 as follows:

$t_1 = k \times (\text{VALUE} + 1) \times \text{TCP}$

where

- k is the timer resolution factor which is either 32.768 or 512-clock cycles dependent on the programming of TRS bit in MODE.
- TCP is the clock period of transmit data.

CNT … Interpreted differently dependent on the selected timer mode (bit TMD in MODE).

- Internal timer mode (MODE.TMD = 1)

  retry counter (in HDLC known as N2)

  CNT indicates the number of S-commands (max. 6) which are transmitted autonomously by the HSCX after expiration of time period t_1, in case an I-frame is not acknowledged by the opposite station.

  If CNT is set to 7, the number of S-commands is unlimited.

- External timer mode (MODE,TMD = 0)

  CNT plus VALUE indicates the time period t_2 after which a timer interrupt will be generated. The time period t_2 is

  $t_2 = 32 \times k \times \text{CNT} \times \text{TCP} + t_1$

  If CNT is set to 7, a timer interrupt periodically generated after the expiration of t_1.

Transmit Address Byte 1 (WRITE)

	7			0	
XAD1 2-byte address	XAD1 (high byte)		0	(0)	(24/64)
1-byte address	XAD1 (COMMAND)				

XAD1 (and XAD2) can be programmed with one individual address byte which is appended automatically to the frame by HSCX in auto-mode. The function depends on the selected address mode (bit ADM in MODE).

– 2-byte address field (MODE.ADM = 1)

XAD1 forms the high byte of the 2-byte address field. Bit 1 must be set to 0! According to the ISDN LAPD protocol, bit 1 is interpreted as the C/R (COMMAND/RESPONSE) bit. This is manipulated automatically by the HSCX dependent on the setting of the CRI bit in RAH1:

	Bit 1 (C/R)	
Commands transmit	1	0
Responses transmit	0	1
	CRI = 1	CRI = 0

(In the ISDN, the high address byte is known as SAPI).

In accordance with the HDLC protocol, bit 0 should be set to 0, indicating the extension of the address field to two bytes.

– 1-byte address field (MODE.ADM = 0)

According with the X.25 LAPB protocol, XAD1 indicates a COMMAND.

Transmit Address Byte 2 (WRITE)

	7	0	
XAD2 2-byte address	XAD2 (low byte)		(25/65)
1-byte address	XAD2 (RESPONSE)		

Second individually programmable address byte.

– 2-byte address (MODE.ADM = 1)

  XAD2 builds up the low byte of the 2-byte address field
  (In the ISDN, the low address byte is known as TEI)

– 1-byte address (MODE.ADM = 0)

  According to the X.25 LAPB protocol, XAD2 indicates a RESPONSE,

Note: XAD1, XAD2 registers are used only if the HSCX is operated in auto-mode.

Receive Byte Count Low (READ)

	7	0	
RBCL	RBC7	RBC0	(25/65)

Together with RBCH (bits RBC11 – RBC8), the length of the actual received frame (1…4095 bytes) can be determined. These registers must be read by the CPU following an RME interrupt.

Receive Address Byte High Register 1 (WRITE)

	7			0	
RAH1	RAH1		CRI	0	(26/66)

In operating modes that provide high byte address recognition, the high byte of the received address is compared with the individual programmable values in RAH1, or RAH2.

RAH1 … Value of the first individual high address byte

CRI … Command/Response Interpretation (auto-mode and non-auto mode only)

The setting of the CRI bit affects the meaning of the C/R bit in RSTA as follows:

C/R meaning	C/R value	
Commands received	0	1
Responses received	1	0
	CRI = 1	CRI = 0

Important: If the 1 byte address field is selected in auto-mode, RAH1 must be set to 00_H.

Receive Address Byte High Register 2 (WRITE)

	7	0		1	0	
RAH2	RAH2			MCS	0	(27/67)

RAH2 … Value of second individual programmable high address byte.

MCS … Module Count Select; valid in auto-mode only.

The MCS bit adjusts the control field format according to the HDLC (ISDN/LAPD).

0 … basic operation (modulo 8)
1 … extended operation (modulo 128)

Note: When modulo 128 is selected, in auto-mode the "RHCR" register contains compressed information of the extended control field (see RHCR, register description). RAH1, RAH2 registers are used in auto and non-auto operating modes when a 2-byte address field has been selected (MODE.ADM = 1) and in the transparent mode 0.
RAH2 has to be initialized.

Receive Status Register (READ)

	7							0	
RSTA	VFR	RDO	CRC	RAB	HA1	HA0	C/R	LA	(27/67)

VFR … Valid Frame

Determines whether a valid frame has been received.

1 … Valid
0 … Invalid

An invalid frame is either

- a frame which is not an integer number of 8 bits (n × 8 bits) in length (e.g. 25 bit), or
- a frame which is too short depending on the selected operation mode via MODE (MDS1, MDS0, ADM) as follows:

- Auto-/non-auto mode (16-bit address): 4 bytes
- Auto-/non-auto mode (8-bit address): 3 bytes
- Transparent mode 1:3 bytes.
- Transparent mode 0:2 bytes.

Note: Shorter frames are not reported.

RDO … Receive Data Overflow

A data overflow has occurred within the actual frame.
Caution: Data loss because the CPU did not serve RME or RPF interrupt in time.

CRC … CRC compare/check

0 … CRC check failed; received frame contains errors.
1 … CRC check o.k.; received frame is error-free.

RAB … Receive Message Aborted

The received frame was aborted from the transmitting station.
According to the HDLC protocol, this frame must be discarded by the CPU.

HA1, HA0 … High Byte Address Compare; significant only if 2-byte address mode has been selected.

In operating modes which provide high byte address recognition, the HSCX compares the high byte of a 2-bytes address with the contents of two individual programmable registers (RAH1, RAH2) and the fixed values FE_H and FC_H (group address).

Dependent on the result of this comparison, the following bit combinations are possible:

10 … RAH1 has been recognized
00 … RAH2 has been recognized
01 … group address has been recognized

Note: If RAH1, RAH2 contain the identical values, the combination 00 will be omitted.

C/R … Command/Response; significant only, if 2-byte address mode has been selected.

Value of the C/R bit (bit of high address byte) in the received frame. The interpretation depends on the setting of the CRI bit in the RAH1 register. Refer also to the description of RAH1 register.

LA … Low Byte Address Compare; not significant in transparent and extended transparent operating modes.

The low byte address of a 2-byte address field, or the single address byte of a 1-byte address field is compared with two programmable registers (RAL1, RAL2)
0 … RAL2 has been recognized
1 … RAL1 has been recognized
According to the X.25 LAPB protocol, RAL1 is interpreted as COMMAND and RAL2 interpreted as RESPONSE.

Note: RSTA corresponds to the last received HDLC frame; it is duplicated into RFIFO for every frame (last byte of frame).

Receive Address Byte Low Register 1 (READ/WRITE)

	7		0	
RAL1	RAL1			(28/68)

The general function (READ/WRITE) and the meaning or contents of this register depends on the selected operating mode:

- Auto-/non-auto mode (16-bit address) – **WRITE only**:
  RAL1 can be programmed with the value of the first individual low address byte.
- Auto-/non-auto mode (8-bit address) – **WRITE only**:
  According to X.25 LAPB protocol, the address in RAL1 is recognized as COMMAND address.
- Transparent mode 1 (high byte address recognition) – **READ only**:
  RAL1 contains the byte following the high byte of the address in the receive frame (i.e. the second byte after the opening flag).
- Transparent mode 0 (no address recognition) – **READ only**:
  RAL1 contains the first byte after the opening flag (first byte of received frame).
- Extended transparent modes 0, 1 – **READ only**:
  RAL1 contains the actual data byte currently assembled at the R × D pin, by passing the HDLC receiver (fully transparent reception without HDLC framing).

Receive Address Byte Low Register 2 (WRITE)

	7		0	
RAL2	RAL2			(29/69)

Value of the second individual programmable low address byte. If a one byte address field is selected, RAL2 is recognized as RESPONSE according to X.25 LAPB protocol.

Receive HDLC Control Register (READ)

	7						0	
RHCR	RHCR							(29/69)

Value of the HDLC control field corresponds to the last received frame.

Note: RHCR is duplicated into RFIFO for every frame.

	Contents of RHCR	
Mode	**Modulo 8 (MCS = 0)**	**Modulo 128 (MCS = 1)**
Auto-mode,1-byte address (U-frames) (Note 1)	Control field	Control field (Note 2)
Auto-mode, 2-byte address (U-frames) (Note 1)	Control field	Control field (Note 2)
Auto-mode, 1-byte address (I-frames) (Note 1)	Control field	Control field in compressed form (Note 3)
Auto-mode, 2-byte address (I-frames) (Note 1)	Control field	Control field in compressed form (Note 3)
Non-auto mode, 1-byte address	2nd byte after flag	
Non-auto mode, 2-byte address	3rd byte after flag	
Transparent mode 1	3rd byte after flag	
Transparent mode 0	2nd byte after flag	

Note 1: S-frames are handled automatically and are not transferred to the microprocessor.

Note 2: For U-frames (bit 0 of RHCR = 1) the control field is as in the modulo 8 case.

Note 3: For I-frames (bit 0 of RHCR = 0) the compressed control field has the same format as in the modulo 8 case, but only the three LSB's of the receive and transmit counters are visible:

bit	7	6	5	4	3	2	1	0
	N(R)			P	N(S)			0

Transmit Byte Count Low (WRITE)

	7						0	
XBCL	XBC7						XBC0	(2A/6A)

Together with XBCH (bits XBC11…XBC8) this register is used in DMA mode only, to program the length (1…4095 bytes) of the next frame to be transmitted.

This allows the HSCX to request the correct amount of DMA cycles after an XTF or XIF command via CMDR.

Note: The number of transmitted bytes is XBC + 1, e.g. if the content of XBC is 00 exactly one byte will be transmitted.

Baudrate Generator Register (WRITE)

	7						0	
BGR	BR7						BR0	(2B/6B)

BR7 – BR0…Baudrate, bit 7 - 0

Together with bits BR9, BR8 of CCR2, the division factor of the baudrate generator is adjusted.

Dependent on the programmed value N in BR9 – BR8 (N = 0…1023) the division factor k results as follows:

$k = (N + 1) \times 2$

Channel Configuration Register 2 (READ/WRITE)

Value after RESET: 00_H

The meaning of the individual bits in CCR2 depends on the selected clock mode via CCR 1 as follows:

CCR2

clock mode 0,1	SOC1	SOC0	0	0	0	CIE	RIE	DIV	(2C/6C)
clock mode 2,6	BR9	BR8	BDF	TSS	TIO	CIE	RIE	DIV	
clock mode 3,7	BR9	BR8	BDF	0	TIO	CIE	RIE	DIV	
clock mode 5	SOC1	SOC0	XCS0	RCS0	TIO	CIE	RIE	DIV	
clock mode 4	SOC1	SOC0	0	0	TIO	CIE	RIE	DIV	

SOC1, SOC0 … Special Output Control

In a bus configuration (selected via CCR1) the function of pin RTS can be defined
00 … RTS output is activated during the transmission of a frame.
10 … RTS output is always high (RTS disabled).
11 … RTS indicates the reception of a data frame (active low).
In point-to-point configuration (selected via CCR1) the T × D and R × D pins may be flipped
0X … data is transmitted on T × D, received on R × D pin (normal case)
1X … data is transmitted on R × D, received on T × D pin

BR9, BR8 … Baudrate, Bit 9-8 (higher significant bits, refer to description of BGR register).

BDF … Baudrate Division Factor

0 … The division factor of the baudrate generator is set to 1 (constant).
1 … The division factor is adjusted with BR9 – BR0 bits of CCR2 and BRG register.

TSS … Transmit Clock Source Select

0 … The transmit clock is input to the T × CLKA/T × CLKB pins.
1 … The transmit clock is derived from the baudrate generators output divided by 16.

TIO … Transmit Clock Input Output Switch

0 … T × CLKA, T × CLKB pins are inputs
1 … T × CLKA, T × CLKB pins are outputs

CIE … Clear To Send Interrupt Enable

Any state transition at the CTS input pin may cause an interrupt which is indicated in the EXIR register (CSC bit). The actual state at the CTS pin can be determined reading the CTS bit of the STAR register.
0 … disable
1 … enable

RIE … Receive Frame Start Interrupt Enable

When, the RFS interrupt (via EXIR) is enabled!

DIV … Data Inversion

Only valid if NRZ data encoding is selected. Data is transmitted and received inverted.

XCS0, RCS0 … Transmit/Receive Clock Shift, Bit 0

Together with bits XCS2, XCS1 (RCS2, RCS1) in TSAX (TSAR) the clock shift relative to the frame synchronization signal of the transmit (receive) time-slot can be adjusted.
A clock shift of 0 … 7 bits is programmable (clock mode 5 only!).

Transmit Byte Count High (WRITE)

Value after RESET: 000xxxxx

	7				3	0	
XBCH	DMA	NRM	CAS	XC	XBC11	XBC8	(2D/6D)

DMA … DMA Mode

Selects the data transfer mode of HSCX to system memory.
0 … Interrupt controlled data transfer (interrupt mode)
1 … DMA controlled data transfer (DMA Mode)

NRM … Normal Response Mode

Valid in auto-mode only! Use in auto-mode only; reset this bit in non auto-mode, transparent mode, and extended transparent mode.
Determines the function of the LAP controller:
0 … full-duplex LAPB/LAPD operation
1 … half-duplex NRM operation

CAS … Carrier Detect Auto Start

When set, a high at the CD (A × CLK) pin enables the respective receiver and data reception is started.

Note: CAS has to be "0" for clock mode 1 and 5

XC … Transmit Continuously

Only valid if DMA mode is selected!
If the XC bit is set, the HSCX continuously requests for transmit data ignoring the transmit byte count programmed via XBCH, XBCL.

XBC11 … XBC8 … Transmit Byte Count (most significant bits)

Valid only if DMA mode is selected!
Together with XBC7 … XBC0 the length of the frame to be programmed.

Received Byte Count High (READ)

Value after RESET: 000xxxxx

	7				3		0	
RBCH	DMA	NRM	CAS	OV	RBC11		RBC8	(2D/6D)
	see XBCH							

DMA, NRM, CAS … These bits represent the read-back value programmed in XBCH (see XBCH!)

OV … Counter Overflow

More than 4095 bytes received!
The received frame exceeded the byte count in RBC11 … RBC0.

RBC11 … RBC8 … Receive Byte Count (most significant bits)

Together with RBCL (bits RBC7 … RBC0) the length of the received frame can be determined.

Version Status Register (READ)

	7				3		0	
VSTR	CD	0	0	0	VN3		VN0	(2E/6E)

CD … Carrier Detect

This bit represents the inverted state at the CD (A×CLK) pin even when CAS is not enabled.

1 … CD active (low)
0 … CD inactive (high)

VN3 … VN0 … Version Number of Chip

0:000 … Version A1
2:010 … Version A2
4:100 … Version A3
5:101 … Version 2.1

Receive Length Check Register (WRITE)

	7							0	
RLCR	RC	RL6						RL0	(2E/6E)

RC … Receive Check (on/off)

0 … receive length check feature disabled
1 … receive length check feature enabled

Note: All bytes stored in the RFIFO are relevant for the receive length check feature including the receiver status byte.

RL … Receive Length

The maximum receive length after which data reception is suspended can be programmed here. Depending on the value RL programmed via RL6 … RL0, the receive length is (RL + 1) × 32 bytes! A frame exceeding this length is treated as if it was aborted by the opposite station (RME Interrupt, RAB bit set).

In this case, the Receive Byte Count (RBCH, RBCL) is greater than the programmed receive length.

Channel Configuration Register 1 (READ/WRITE)

Value after RESET: 00_H

	7							0	
CCR1	PU	SC1	SC0	ODS	ITF OIN	CM2	CM1	CM0	(2F/6F)

PU … Switches between Power Up and Power Down mode

0 … power down (standby)
1 … power up (active)

SC1, SC0. . .Serial Port Configuration

00 … NRZ data encoding
10 … NRZI data encoding
01 … bus configuration, timing mode 1
11 … bus configuration, timing mode 2

Note: If bus configuration is selected, only NRZ coding is supported.

ODS … Output Driver Select

Defines the function of the transmit data pins (T × DA, T × DB)
0. . .T × D pins are open drain outputs
1. . .T × D pins are push-pull outputs

Note: Since in time-slot oriented systems the T × D pin is not tristated automatically out of the programmed time-slot, the T × D pin should be configured as open drain in time-slot oriented bus systems.

ITF/OIN … Interframe Time Fill/One Insertion

The function of this bit depends on the selected serial port configuration (bit SC0)

- Point-to-point configurations: ITF
  Determines the idle (= no data to send) state of the transmit data pins (T × DA, T × DB)
  0 … Continuous IDLE sequences are output (T × D pins remain in the "1" state)
  1 … Continuous FLAG sequences are output ("01111110" bit patterns)
- Bus configurations: OIN
  In bus configurations, the ITF is implicitly set to 0, i.e. continuous "1"s are transmitted, and data encoding is NRZ!
  When this bit is set, a "ONE" insertion (deletion) mechanism is activated, inserting a "1" after seven consecutive "0"s in the transmit data stream or deleting a "1" in the receive data stream.
  Similar to the HDLC's bit-stuffing mechanism (inserting a "0" after five consecutive "1"s), this method proves to be advantageous when the receive clock is recovered from the receive data stream by means of DPLL, because it is guaranteed that at least after seven bits a transition occurs in the receive data in case of long "0" sequences!

CM2, CM1, CMO … Clock Mode

Selects one of the 8 different clock modes

000	clock mode 0
.	.
.	.
.	.
111	clock mode 7

Time-Slot Assignment Register Transmit (WRITE)

This registers is only used in clock mode 5!

	7			2	1	0	
TSAX	TSNX				XCS2	XCS1	(30/70)

TSNX … Time-Slot Number Transmit

Selects one of up 64 possible time-slots (00_H – $3F_H$) in which data is transmitted. The number of bits per time-slot can be programmed via XCCR.

XCS2, XCS1 … Transmit Clock Shift, Bit 2-1

Together with the XCS0 in CCR2, the transmit clock shift can be adjusted.

Time-Slot Assignment Register Receive (WRITE)

This register is only used in clock mode 5!

	7					0	
TSAR	TSNR				RCS2	RCS1	(31/71)

TSNR … Time-Slot Number Receive

Defines one of up to 64 possible time-slots (00_H – $3F_H$) in which data is received. The number of bits per time-slot can be programmed via RCCR.

RCS2, RCS1 … Receive Clock Shift, Bit 2-1

Together with bit RCS0 in CCR2, the receive clock shift can be adjusted.

Transmit Channel Capacity Register (WRITE)

Value after RESET: 00_H
This register is only used in clock mode 5.

	7		0	
XCCR	XBC7		XBC0	(32/72)

XBC7 … XBC0 … Transmit Bit Count, Bit 7-0

Defines the number of bits to be transmitted with a time-slot:
Number of bits = XBC + 1. (1 … 256 bits/time-slot)

Receive Channel Capacity Register (WRITE)

Value after RESET: 00_H
This register is only used in clock mode 5.

	7		0	
RCCR	RBC7		RBC0	(33/73)

RBC7 … RBC0 … Receive Bit Count, Bit 7-0

Defines the number of bits to be received within a time-slot:
Number of bits = RBC + 1. (1 … 256 bits/time-slot)

9 Electrical Characteristics

Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Ambient temperature under bias: SAB SAF	T_A T_A	0 to 70 – 40 to 85	°C °C
Storage temperature	T_{stg}	– 65 to 125	°C
Voltage on any pin with respect to ground	V_S	– 0.4 to V_{DD} + 0.4	V
Maximum voltage on any pin	V_{max}	6	V

Note: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

Characteristics

SAB: T_A = 0 to 70 °C; V_{DD} = 5 V ± 5 %; V_{SS} = 0 V
SAF: T_A = – 40 to 85 °C; V_{DD} = 5 V ± 5 %; V_{SS} = 0 V

Parameter		Symbol	Limit Values		Unit	Condition
			min.	max.		
L-input voltage		V_{IL}	– 0.4	0.8	V	
H-input voltage		V_{IH}	2.0	V_{CC} + 0.4	V	
L-output voltage		V_{OL}		0.45	V V	I_{OL} = 7 mA (pins T × D, R × D) I_{OL} = 2 mA (all other)
H-output voltage H-output voltage		V_{OH} V_{OH}	2.4 V_{DD} – 0.5		V V	I_{OH} = – 400 µA I_{OH} = – 100 µA
Power supply current	operational	I_{CC}		8	mA	V_{DD} = 5 V, C_p = 4 MHz Inputs at 0 V/V_{DD}, no output loads
	power down	I_{CC}		1.5	mA	
Input leakage current Output leakage current		I_{LI} I_{LO}		10	µA	0 V < V_{IN} < V_{DD} to 0 V 0 V < V_{OUT} < V_{DD} to 0 V

Capacitances

T_A = 25 °C; V_{DD} = 5 V ± 5 %; V_{SS} = 0 V, f_C = 1 MHz, unmeasured pins returned to GND.

Parameter	Symbol	Limit Values		Unit
		typ.	max.	
Input capacitance f_C = 1 MHz	C_{IN}	5	10	pF
Output capacitance	C_{OUT}	8	15	pF
I/O	$C_{I/O}$	10	20	pF

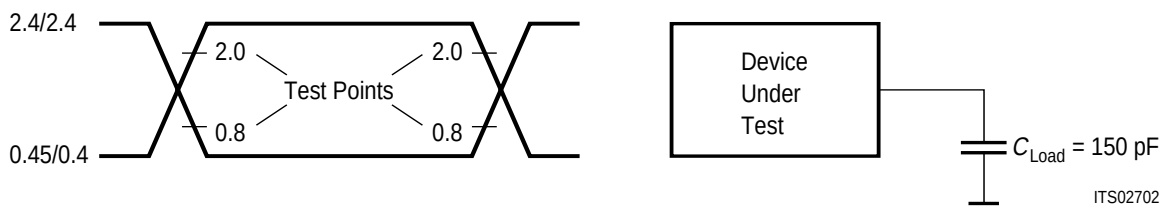
Characteristics

SAB: T_A = 0 to 70 °C; V_{DD} = 5 V ± 5 %
SAF: T_A = – 40 to 85 °C; V_{DD} = 5 V ± 5 %

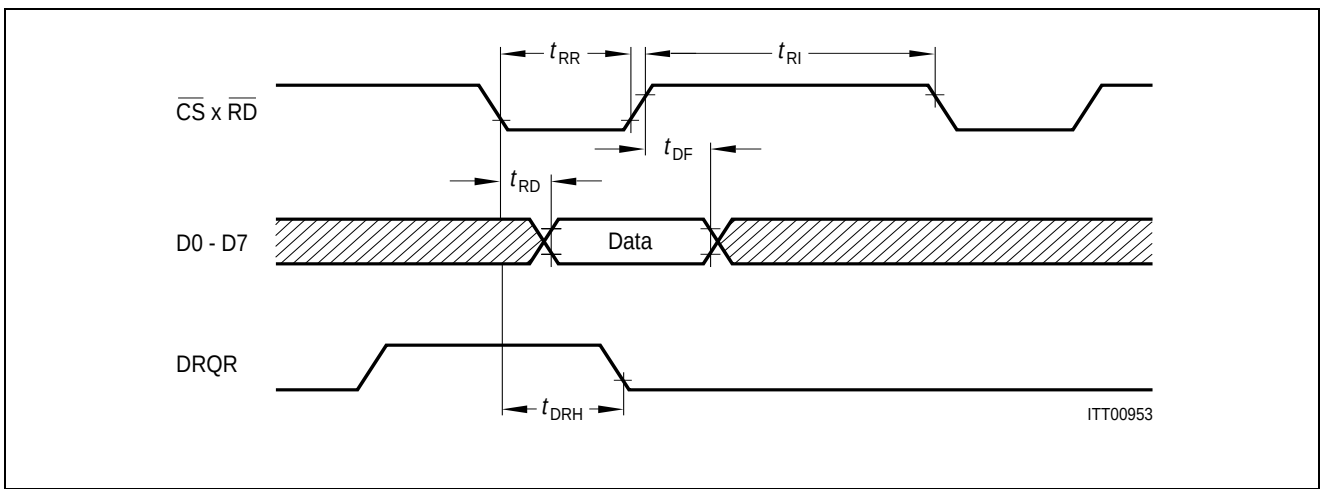
Inputs are driven to 2.4 V for a logical "1" and to 0.4 V for a logical "0". Timing measurements are made at 2.0 V for a logical "1" and at 0.8 V for a logical "0".

The AC testing input/output waveforms are shown below.

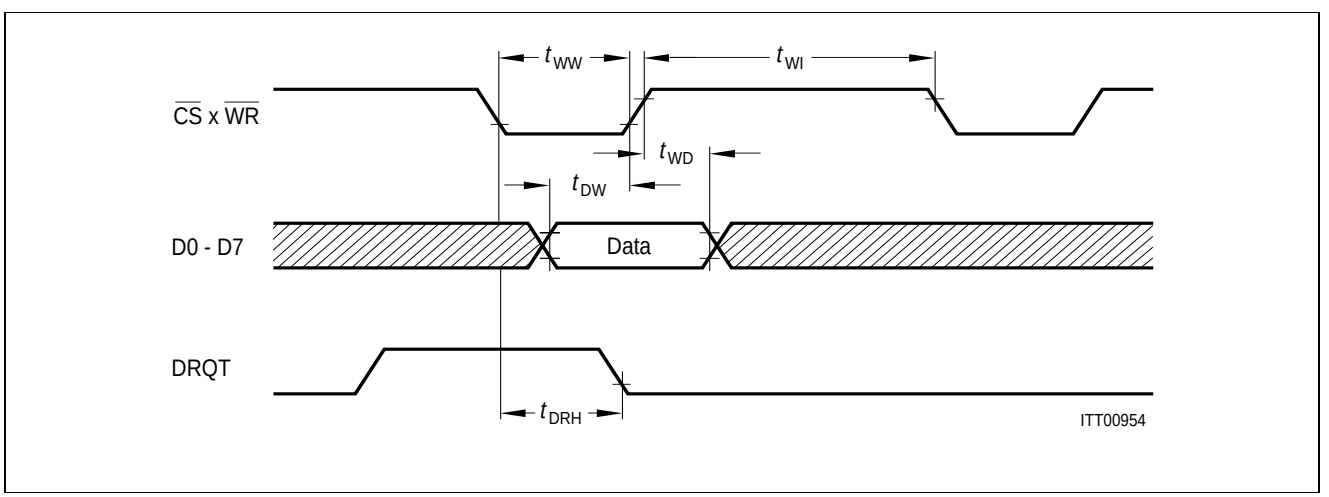
Input/Output Waveform for AC Tests



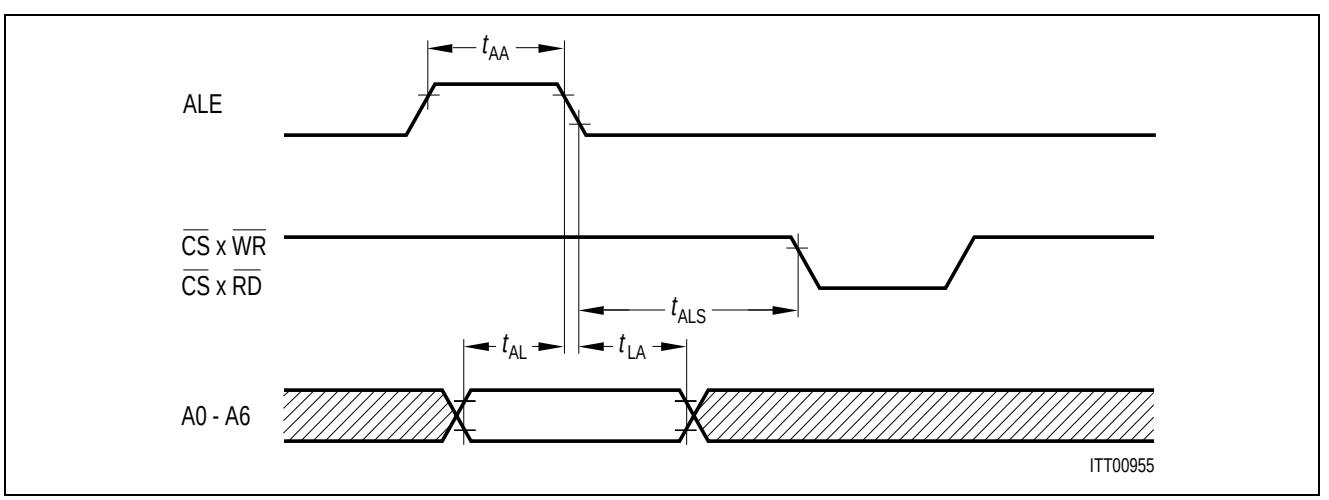
Microcontroller Interface Timing Intel Bus Mode



µP Read Cycle

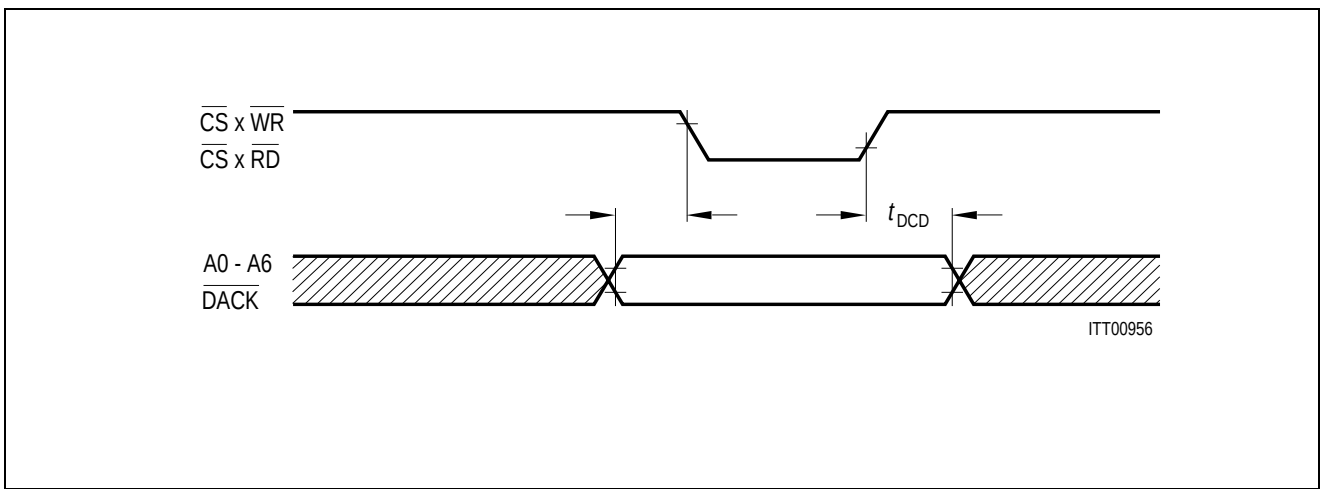


µP Write Cycle



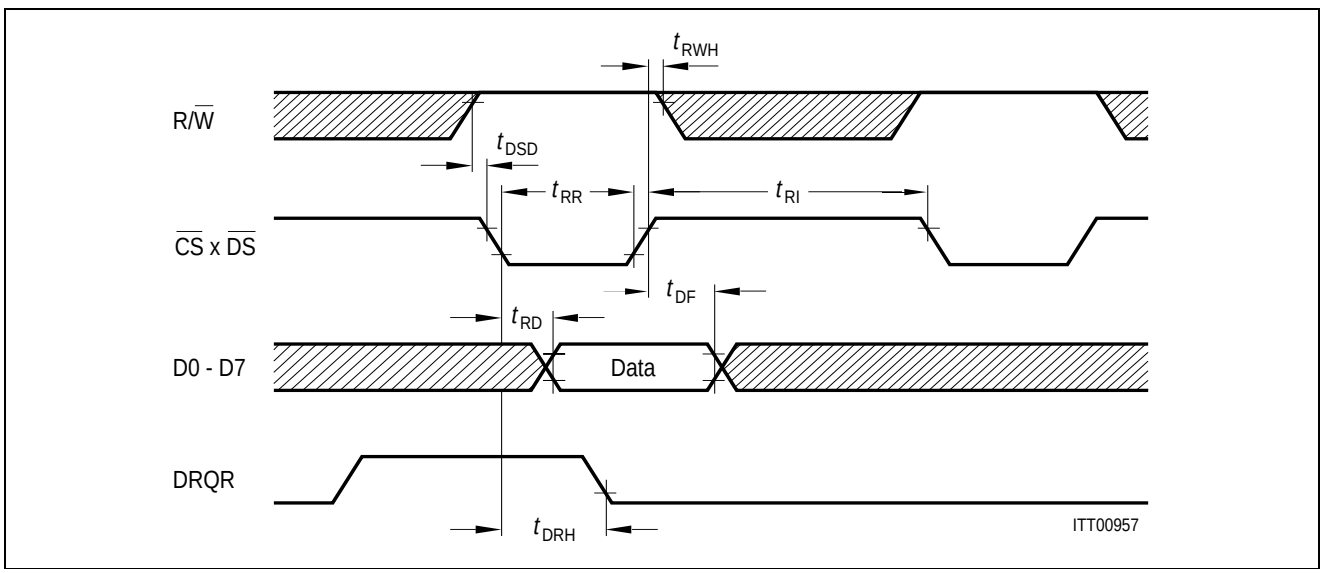
Multiplexed Address Timing

Microcontroller Interface Timing Intel Bus Mode

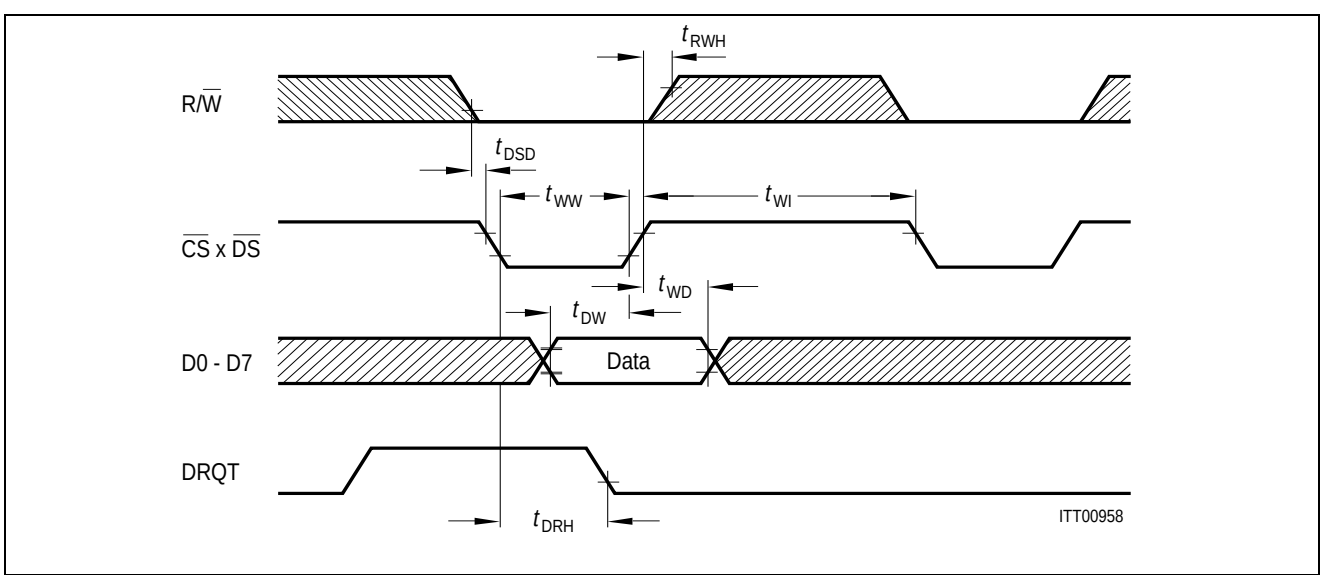


Address Timing

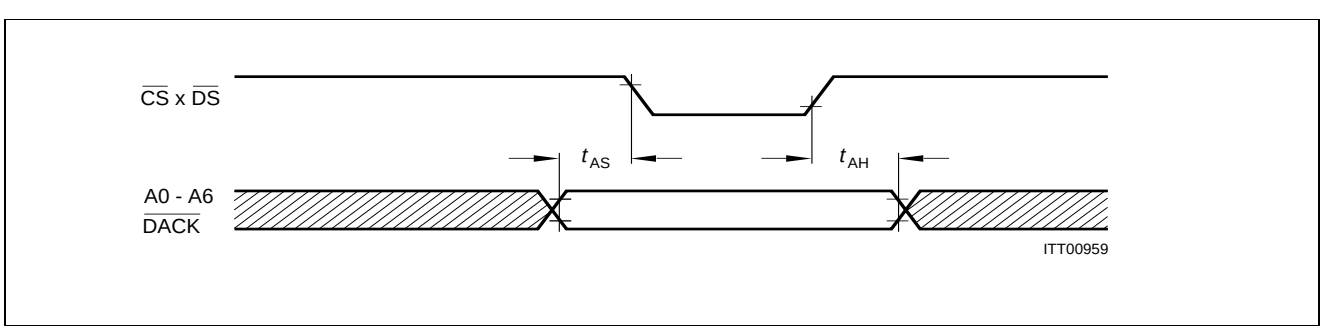
Motorola Bus Mode



µP Read Cycle



µP Write Cycle



Address Timing

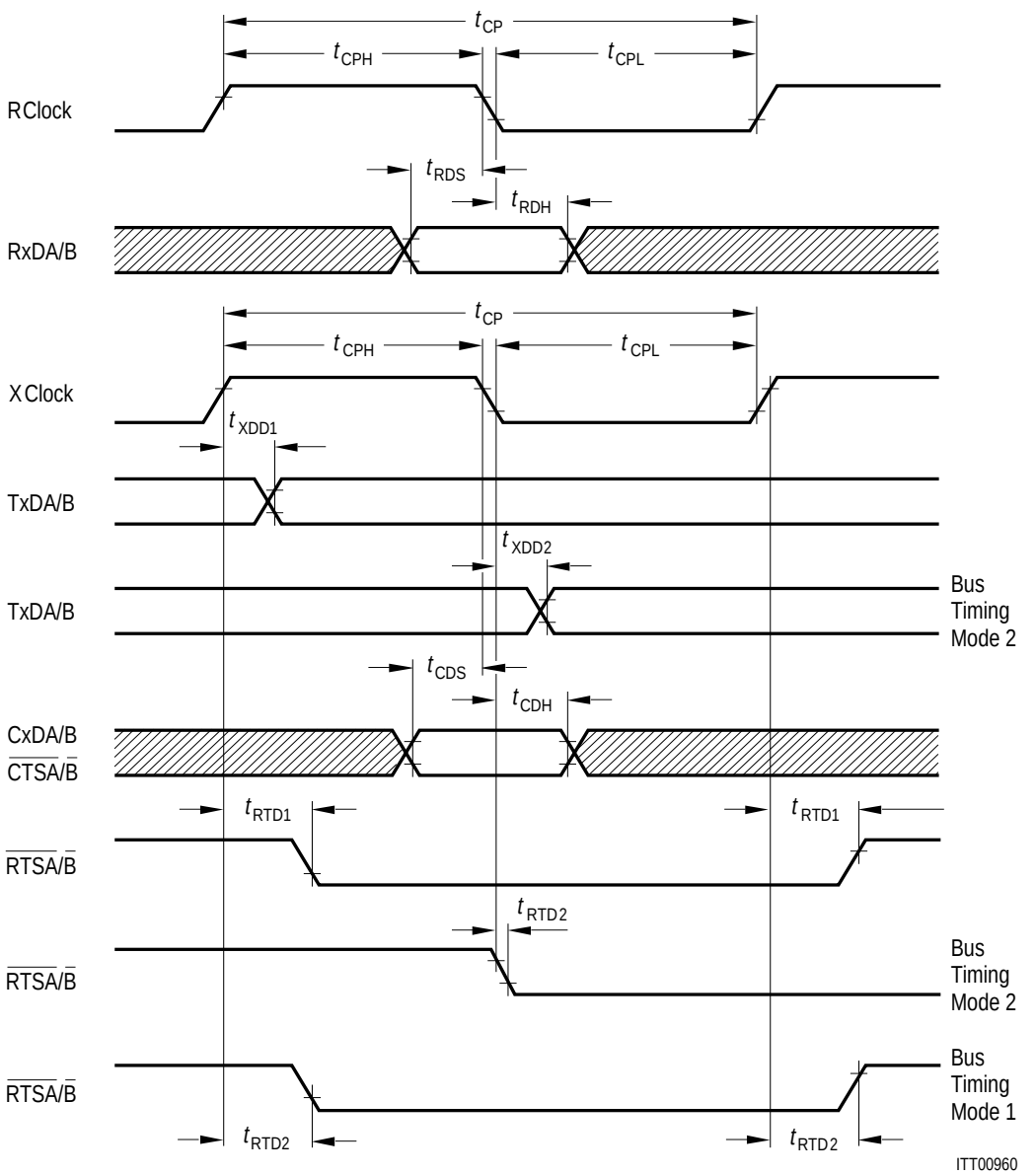
Interface Timing

Parameter	Symbol	Limit Values			Unit
		min.	max.		
			SAB	SAF	
ALE pulse width	t_{AA}	25			ns
Address setup time to ALE	t_{AL}	10			ns
Address hold time from ALE	t_{LA}	10			ns
Address latch setup time to $\overline{WR}$, $\overline{RD}$	t_{ALS}	0			ns
Address setup time to $\overline{WR}$, $\overline{RD}$	t_{AS}	10			ns
Address hold time from $\overline{WR}$, $\overline{RD}$	t_{AH}	10			ns
DMA request delay: SAB SAF	t_{DRH}		80 90	80 90	ns ns
$\overline{RD}$ pulse width	t_{RR}	70			ns
Data output delay from $\overline{RD}$	t_{RD}		60	70	ns
Data float delay from $\overline{RD}$	t_{DF}		25	25	ns
$\overline{RD}$ control interval	t_{RI}	35			ns
$\overline{WR}$ pulse width	t_{WW}	60			ns
Data setup time to $\overline{WR}$ x $\overline{CS}$/$\overline{DS}$ x $\overline{CS}$	t_{DW}	10			ns
Data hold time from $\overline{WR}$ x $\overline{CS}$/$\overline{DS}$ x $\overline{CS}$	t_{WD}	10			ns
$\overline{WR}$ control interval	t_{WI}	60			ns
$\overline{RD}$ delay after $\overline{WR}$ set up	t_{DSD}	0			ns

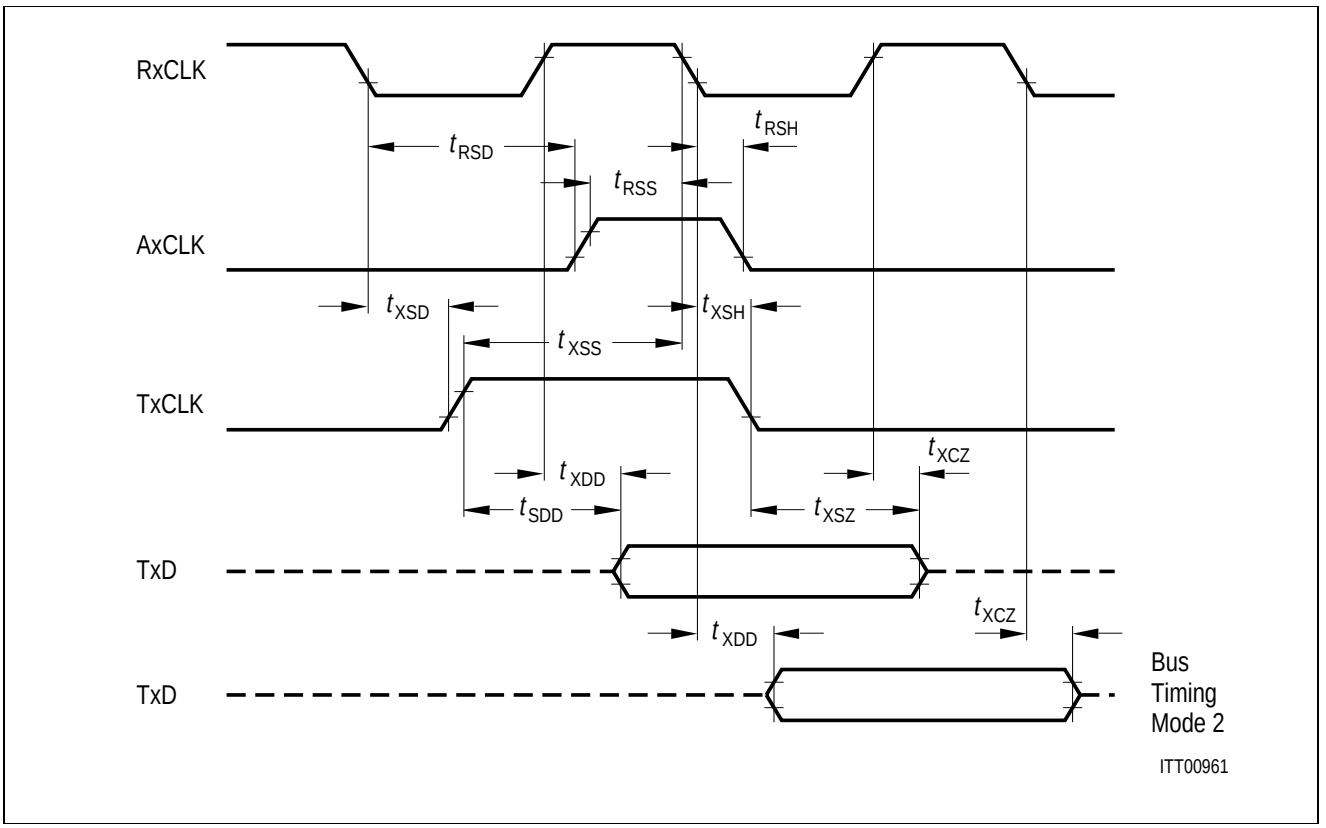
Serial Interface Timing

Receive data setup	t_{RDS}	20			ns
Receive data hold	t_{RDH}	5			ns
Collision data setup	t_{CDS}	5			ns
Collision data hold	t_{CDH}	30			ns
Transmit data delay, falling clock edge	t_{XDD2}	20	68	75	ns
Transmit data delay, rising clock edge	t_{XDD1}	10	68	75	ns
Request to send delay 1	t_{RTD1}	10	120	120	ns
Request to send delay 2	t_{RTD2}	10	85	85	ns
Clock period	t_{CP}	240			ns
Clock period LOW	t_{CPL}	90			ns
Clock period HIGH	t_{CPH}	90			ns

Serial Interface Timing

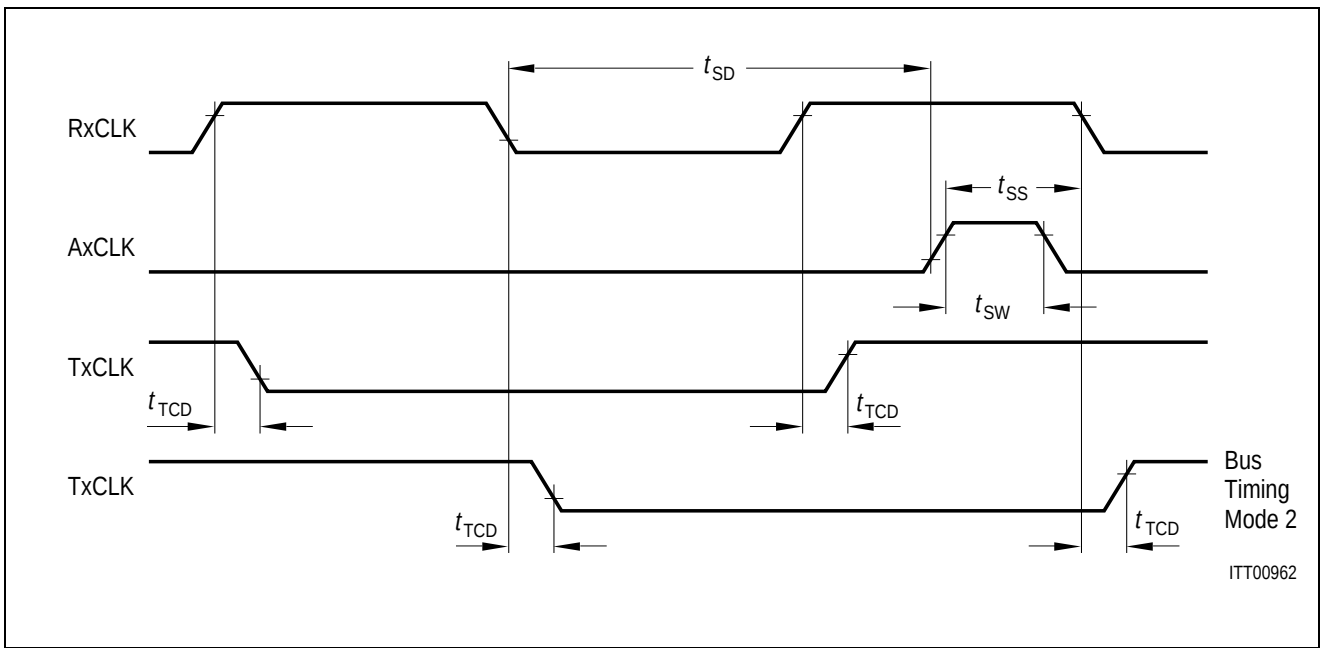


Strobe Timing (Clock Mode1)



Parameter	Symbol	Limit Values		Unit
		min.	max.	
Receive strobe delay	t_{RSD}	30		ns
Receive strobe setup	t_{RSS}	60		ns
Receive strobe hold	t_{RSH}	30		ns
Transmit strobe delay	t_{XSD}	30		ns
Transmit strobe setup	t_{XSS}	60		ns
Transmit strobe hold	t_{XSH}	30		ns
Transmit data delay	t_{XDD}		68	ns
Strobe data delay	t_{SDD}		90	ns
High impedance from clock	t_{XCZ}		50	ns
High impedance from strobe	t_{XSZ}		50	ns

Clock Mode 5



Synchronization Timing

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Sync pulse delay	t_{SD}	30		ns
Sync pulse setup	t_{SS}	30		ns
Sync pulse width	t_{SW}	40		ns
Time-slot control delay	t_{TCD}	10	75	ns

Clock Mode 2, 3, 6, 7

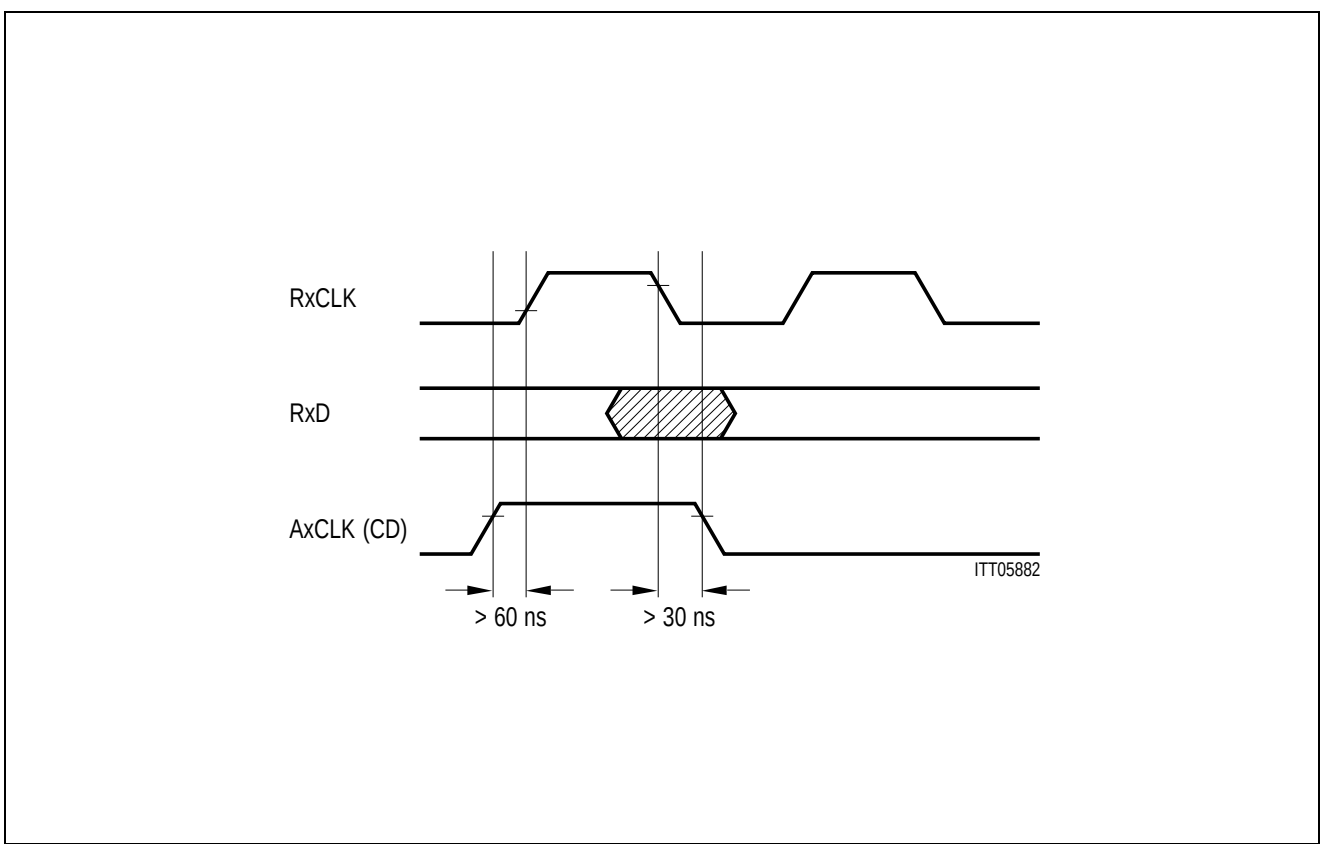
Internal Clocking

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Clock frequency Baudrate generator used	f_{CLK}		12.3	MHz
Clock frequency Baudrate generator not used	f_{CLK}		19.3	MHz

RESET Timing

RES Characteristics

Parameter	Symbol	Limit Values		Unit
		min.	max.	
RES HIGH	t_{RWH}	1800		ns



CD Timing

10 Quartz Specifications

Characterization of Quartz Crystals for the HSCX

– Mode of oscillation	parallel resonance
– Frequency calibration tolerance	50 ppm
– Frequency shift during lifetime	10 ppm
– Temperature coefficient/frequency drift	50 ppm within the temperature range
– Motional capacitance	15 fF ± 20%
– Effective serial resistance	≤ 50 Ω for 19.2 MHz
– Shunt capacitance	≤ 7 pF
– Drive level	1 mW
– Recommended type	HC - 49/U (ANSI - standard)

Appendix A

Upgrades of HSCX Version A3

The HSCX Version A3 is fully upward compatible to Version A2. The differences with respect to HSCX Technical Manual Rev. 2.89 are shown in **table 12**.

Table 12
Differences HSCX A2 – HSCX A3

Differences	Ver. A2	Ver. A3	User Manual Chapter
t_{RI}, t_{WI}	70 ns	60 ns	9
t_{AA}	50 ns	25 ns	9
t_{LA}	20 ns	10 ns	9
t_{DRH}	85 ns	80 ns	9
t_{RD}	120 ns	100 ns; SAF110 ns	9
t_{RDS}	5 ns	20 ns	9
t_{RDH}	30 ns	5 ns	9
t_{XDD}	70 ns	68 ns	9
t_{CDS}	0 ns	5 ns	9
t_{AH}	20 ns	10 ns	9
t_{DW}	30 ns	10 ns	9
IOL value, pin T×D	2 mA	7 mA	9
VSTR value	02H	04H	8

The following additional features are implemented in HSCX A3.

- Transmission in back to back frames.
  Two or more frames may be transmitted continously without interframe time fill
- T×D, R×D flip
  In clock modes 0, 1, 4 and 5 pins R×D and T×D may be flipped
  (refer to CCR2 Register SOC0 and SOC1 bit)
- Status Register
  In auto-mode, START: bit 0 indicates the 'Waiting for Acknowledgement' status

Upgrades of HSCX Version V2.1

3 Version ID

The bits VN3 … VN0 of the Version Status Register (VSTR) contain the value 5 for version V2.1. All HSCX version numbers are listed below:

VN3 … 0	Version
0: 000	VA1
2: 010	VA2
4: 100	VA3
5: 101	**V2.1**

4 RNR Flow Control in Auto-Mode

No more timing restrictions exist for **HSCX V2.1** when the CPU accesses the RNR-bit of the Command Register (CMDR).

5 I-Frames with P = 0 in NRM Auto-Mode

In multipoint configurations using the HDLC normal response mode (NRM) the P-bit of the control field carries out the polling function. The primary station normally polls the other secondary stations by transmitting either RR frames with P = 1 or I-frames with P = 1. I-frames with P = 0 may be used by the primary station to transmit data to an individual secondary station without requesting data from this station at the same time. In this case the secondary station will receive and acknowledge this I-frame, but will not react by transmitting any data to the primary station.

In the following it is assumed that the secondary station is waiting for transmission.

A secondary station using an HSCX VA3 in NRM auto-mode will transmit data to the primary station after it has received an I-frame with of P = 0 or = 1.

The new **HSCX V2.1** handles the P-Bit of I-frames according to ISO 4335. It will transmit data to the primary station after it has received an I-frame with P = 1, but not after an I-frame has been received with P = 0.

6 Transmission of Back-to-Back Frames

The new **HSCX V2.1** supports back-to-back frame transmission in all clock modes without any problem, including the strobe modes (clock mode 1 and 5).

7 $\overline{\text{INT}}$ Output Signal

The $\overline{\text{INT}}$ output signal of the **HSCX V2.1** does not change its value during a write access to the HSCX ($\overline{\text{CS}}$ x $\overline{\text{WR}}$ for Intel and $\overline{\text{DS}}$ x $\overline{\text{WR}}$ for Motorola).

8 Clock Recovery (DPLL)

In case the DPLL detects an edge in the data stream in the range of DPLL count 5 to 10 (Phase Shift) and this is the only one in the assumed bit cell period, then the DPLL receive clock phase is shifted by a certain DPLL count value. The DPLL value and its corresponding phase shift in degree is listed below for the HSCX versions VA3 and V2.1:

HSCX Version	DPLL Count	Phase Shift
VA3	8	180 °
V2.1	**7**	**157.5** °

Differences	Ver. A3	Ver. 2.1
t_{RD}	100/110 ns	60/70 ns
t_{RR}	120 ns	70 ns
t_{RI}	60 ns	35 ns
$t_{XDD1\ min}$	20 ns	10 ns
$t_{RTD1\ min}$	30 ns	10 ns
$t_{RTD2\ min}$	20 ns	10 ns
$t_{TCD\ min}$	20 ns	10 ns

Appendix B

HSCX Auto-Mode: Specific Points

HSCX auto-mode of SAB 82525/SAB 82520 (HSCX/HSCC) is optimized for a window size of one. Therefore the following simplifications are made:

- No REJ-frame is generated, an RR-frame will be transmitted instead. If a REJ-frame is received it will be handled like an RR-frame.
- The transmit/receive variables N(R)/N(S) are checked within the window size (i.e. one), only the LSB is evaluated.
- An I-frame with an incorrect N(R)-value is not accepted, an error interrupt (EXIR:PCE) is generated.
- The timer recovery state is cancelled if a positive acknowledgement (updated N(R)) is received.
- Selective reject is treated like RR.
- After sending an I-frame the HSCX cannot transmit any frame before an acknowledgement or an XRES-command.

Two Byte Addresses:

- An I-frame with C = 0 is accepted without error indication.

Appendix C

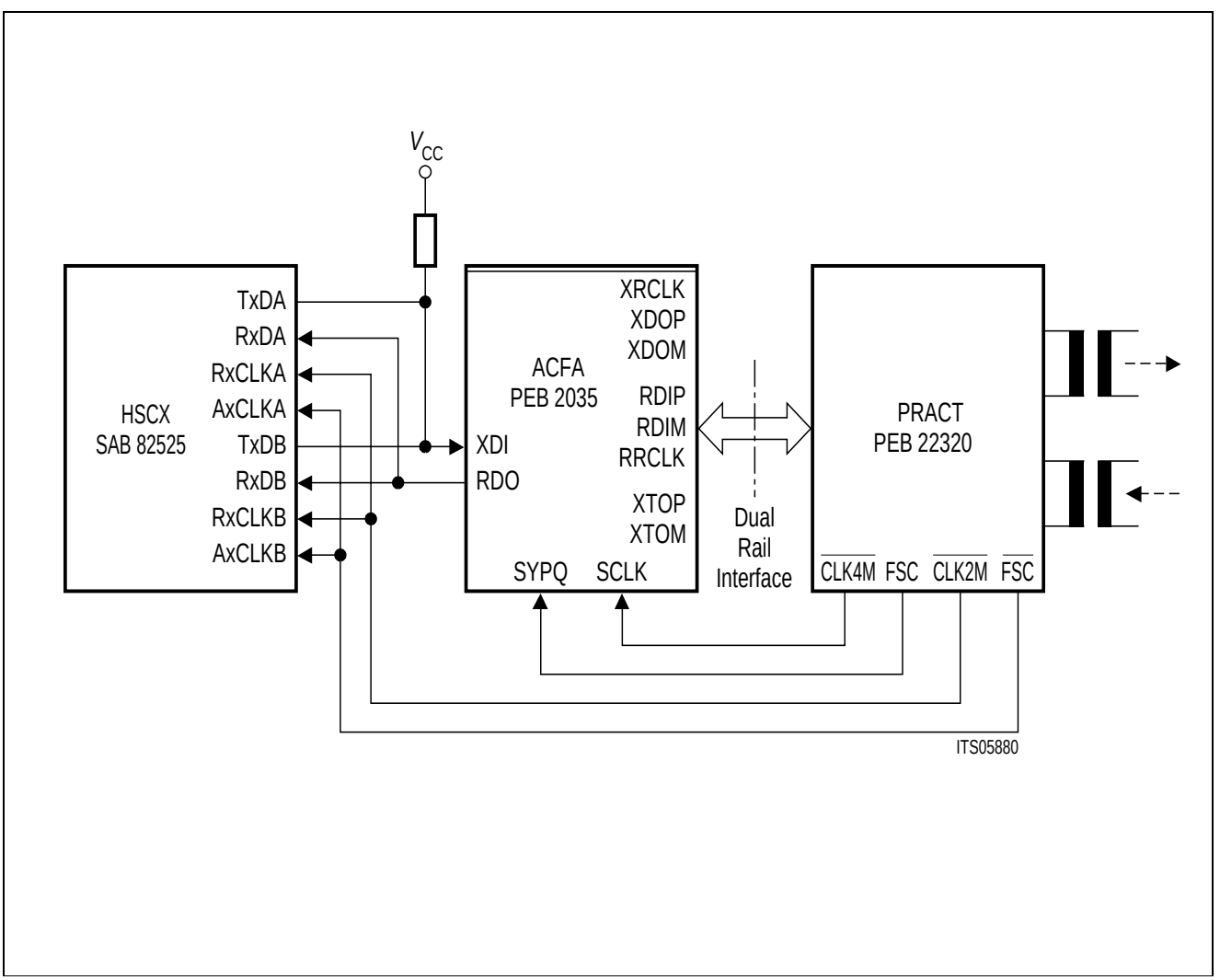
Application Example HSCX with 80(C)188 using DMA

DMA information, see **chapter 4.**

Appendix D

HSCX for Siemens Primary Access Interface

The **Siemens** devices for the Primary Access Interface are the Advanced CMOS Frame Aligner (ACFA) and the Primary Access Transceiver (PRACT). These devices can directly be connected to the HSCX without any additional glue logic. In combination with the HSCX this application is the most effective way to build a powerful and flexible Primary Access Interface, especially supporting different combined B channel paths over long distances (LAN-WAN Internetworking). The following block diagram illustrates how easy it is to integrate the HSCX into a Primary Access application based on Siemens devices.



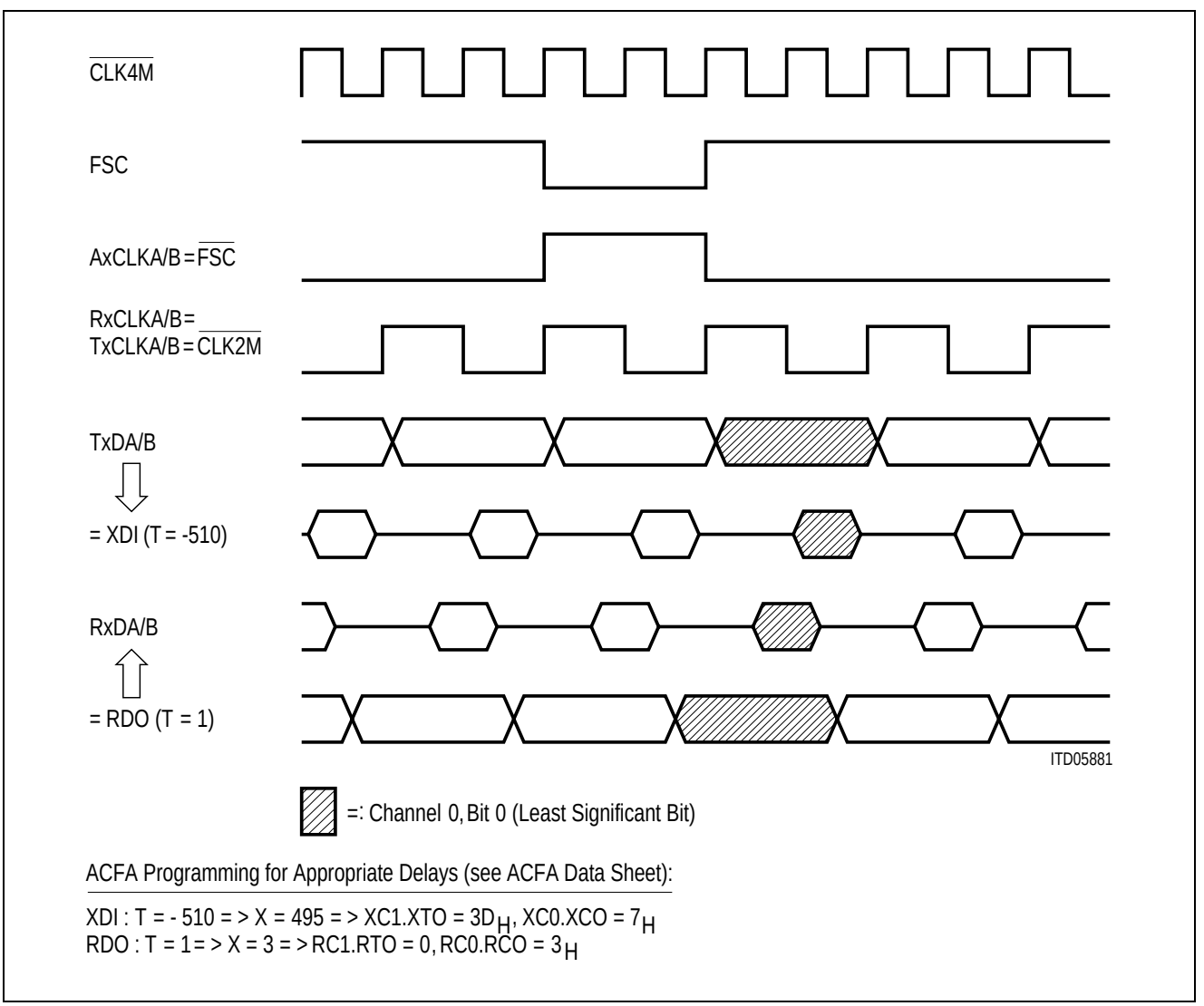
HSCX System Integration for Primary Rate Interface T1/E1 Siemens System Interface (ACFA/PRACT)

The adaption of the AxCLKA/B pulses is solved by means of shifting the receive data and transmit data in the ACFA device appropriately. In this case the AxCLKA and AxCLKB synchronization pulses are also identical. The ACFA device contains special registers to control the bit shift of the serial bit streams at the system interface (see ACFA Data Sheet). With the following register programming the bit shift selected is T = – 510 for the HSCX transmit data and T = 1 for the receive data respectively. The programming is as follows:

XDI: XC1.XTO = $3D_H$ => X = 494 => T = – 510
XC0.XCO = 07_H

RDO: RC1.RTO = 00_H => X = 3 => T = 1
RC0. RCO = 03_H

The timing in principle is depicted in the following diagram. Without all details of a typical electrical timing it illustrates how the different signals from HSCX, ACFA and PRACT are mapped in such a Primary Access system.



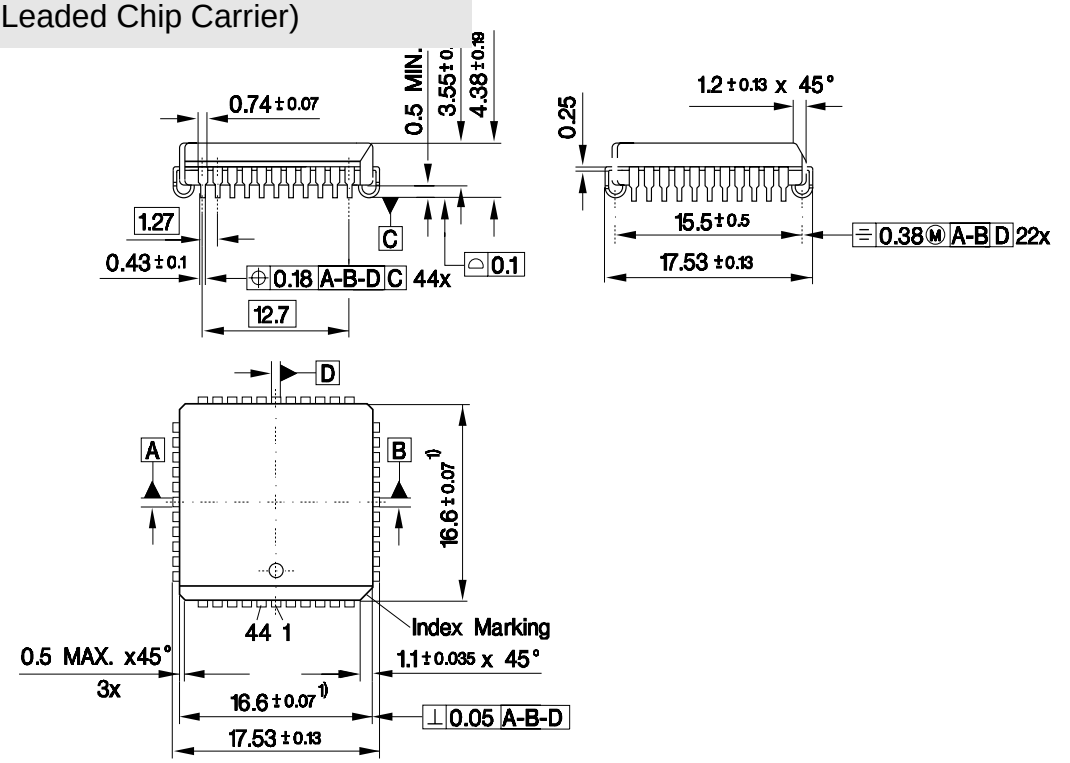
ACFA Programming for Appropriate Delays (see ACFA Data Sheet):

XDI : T = - 510 = > X = 495 = > XC1.XTO = $3D_H$, XC0.XCO = 7_H
RDO : T = 1 = > X = 3 = > RC1.RTO = 0, RC0.RCO = 3_H

HSCX Signal Mapping for Primary Rate Interface T1/E1 Siemens System Interface (ACFA/PRACT)

11 Package Outlines

Plastic Package, P-LCC-44-1 (SMD)
(Plastic-Leaded Chip Carrier)



1) Does not include plastic or metal protrusion of 0.15 max. per side

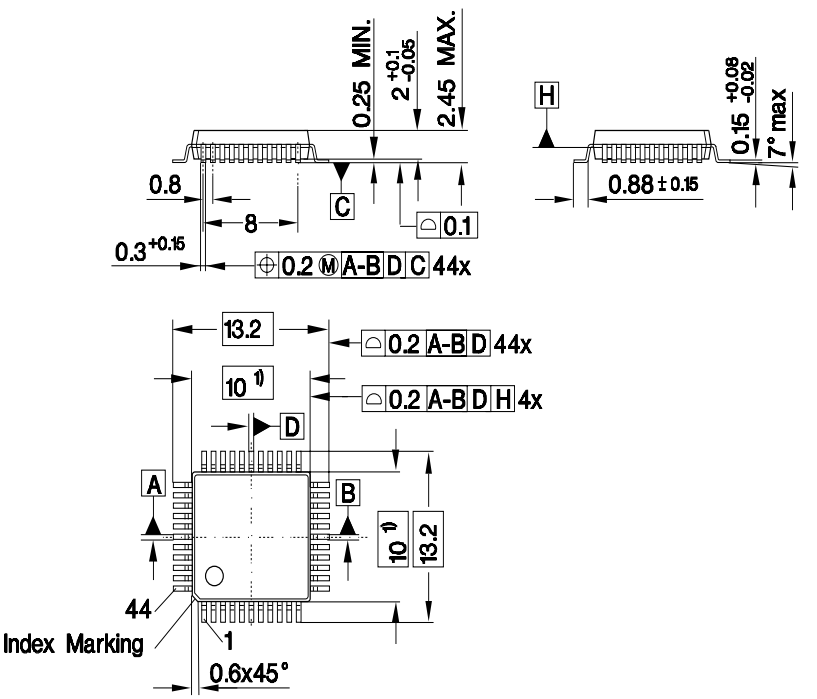
GPL05102

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”

SMD = Surface Mounted Device

Dimensions in mm

Plastic Package, P-MQFP-44-2 (SMD)
(Plastic-Leaded Chip Carrier)



1) Does not include plastic or metal protrusion of 0.25 max. per side

GPM 05622

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”

SMD = Surface Mounted Device

Dimensions in mm