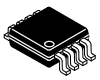
P2008A

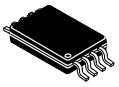
General Purpose EMI Reduction IC

ON Semiconductor®

http://onsemi.com

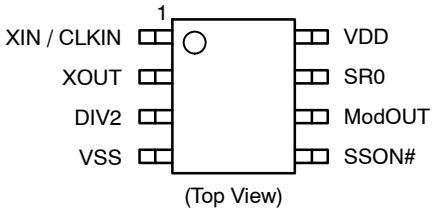


SOIC−8
S SUFFIX
CASE 751BD



TSSOP−8
T SUFFIX
CASE 948AL

PIN CONFIGURATION



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

Description

The P2008A is a versatile spread spectrum frequency modulator designed specifically for digital camera and other digital video and imaging applications. The P2008A reduces electromagnetic interference (EMI) at the clock source, allowing system wide reduction of EMI of down stream clock and data dependent signals. The P2008A allows significant system cost savings by reducing the number of circuit board layers ferrite beads, shielding and other passive components that are traditionally required to pass EMI regulations.

The P2008A uses the most efficient and optimized modulation profile approved by the FCC and is implemented in a proprietary all digital method.

The P2008A modulates the output of a single PLL in order to “spread” the bandwidth of a synthesized clock, and more importantly, decreases the peak amplitudes of its harmonics. This results in significantly lower system EMI compared to the typical narrow band signal produced by oscillators and most frequency generators. Lowering EMI by increasing a signal’s bandwidth is called ‘spread spectrum clock generation.’

Applications

The P2008A is targeted towards cable, xDSL, fax modem, set−top box, USB controller, DSC, and other embedded systems.

Features

- FCC Approved Method of EMI Attenuation
- Provides up to 15 dB of EMI Suppression
- Generates a 1X or $^1/_2$X Low EMI Spread Spectrum Clock of the Input Frequency
- Input Frequency Range: 4 MHz to 32 MHz
- Internal Loop Filter Minimizes External Components and Board Space
- Spreading Ranges from ±0.8% to ±3.2%
- SSON# Control Pin for Spread Spectrum Enable and Disable Options
- Low Cycle−to−Cycle Jitter
- 3.3 V Operating Voltage
- Ultra−low Power CMOS Design
- Available in 8−pin SOIC and TSSOP Packages
- These are Pb−Free Devices

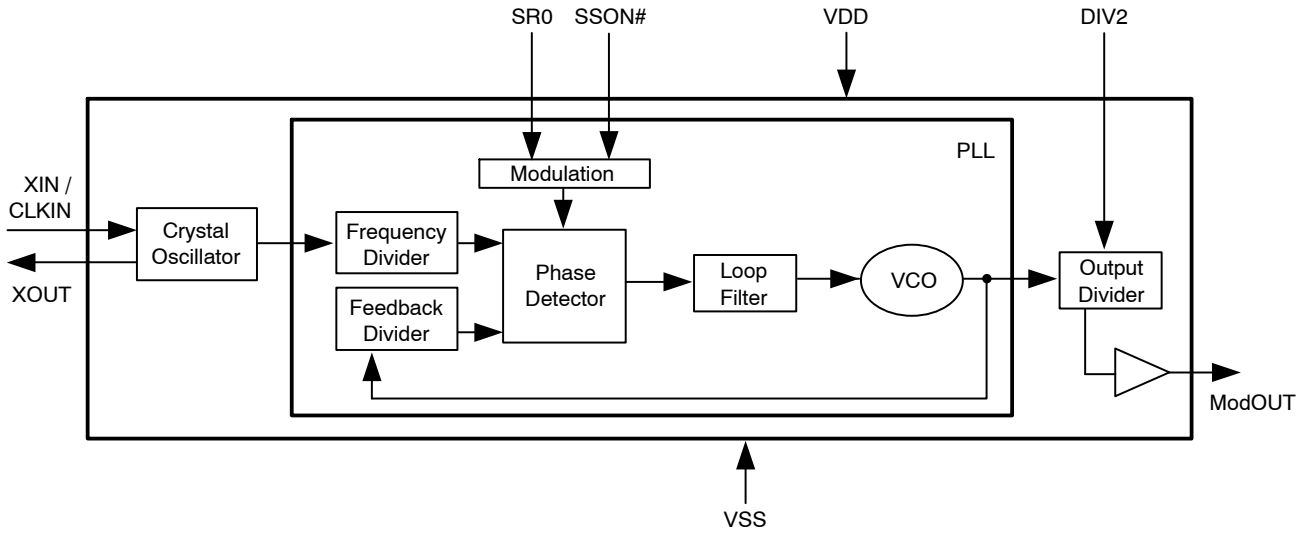


Figure 1. Block Diagram

Table 1. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating	Unit
VDD, V_{IN}	Voltage on any pin with respect to Ground	−0.5 to +4.6	V
T_{STG}	Storage temperature	−65 to +125	°C
T_A	Operating temperature	0 to +70	°C
T_s	Max. Soldering Temperature (10 sec)	260	°C
T_J	Junction Temperature	150	°C
T_{DV}	Static Discharge Voltage (As per JEDEC STD22− A114−B)	2	KV

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 2. DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Unit
V_{IL}	Input low voltage	VSS−0.3	−	0.8	V
V_{IH}	Input high voltage	2.0	−	VDD+0.3	V
I_{IL}	Input low current (pull−up resistors on inputs SR0 and DIV2)	−	−	−35	μA
I_{IH}	Input high current (pull−down resistor on input SSON#)	−	−	35	μA
I_{XOL}	XOUT Output Low Current (@ 0.4 V, VDD = 3.3 V)	−	3	−	mA
I_{XOH}	XOUT Output High Current (@ 2.5 V, VDD = 3.3 V)	−	3	−	mA
V_{OL}	Output low voltage (VDD = 3.3 V, I_{OL} = 10 mA)	−	−	0.4	V
V_{OH}	Output high voltage (VDD = 3.3 V, I_{OH} = 10 mA)	2.5	−	−	V
I_{CC}	Dynamic supply current normal mode (3.3 V, and 15 pF loading)	6.0	7.0	8.3	mA
I_{DD}	Static supply current standby mode	−	0.6	−	mA
VDD	Operating voltage	3.0	3.3	3.6	V
t_{ON}	Power up time (first locked clock cycle after power up)	−	0.18	−	mS
Z_{OUT}	Clock output impedance	−	50	−	Ω

Table 3. AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter		Min	Typ	Max	Unit
f_{IN}	Input frequency		4	20	32	MHz
f_{OUT}	Output frequency	DIV2 = 0	2	10	16	MHz
		DIV2 = 1	4	20	32	
t_{LH} (Note 1)	Output rise time (measured at 0.8 V to 2.0 V)		0.7	0.9	1.1	nS
t_{HL} (Note 1)	Output fall time (measured at 2.0 V to 0.8 V)		0.6	0.8	1.0	nS
t_{JC}	Jitter (cycle−to−cycle)		–	–	360	pS
t_D	Output duty cycle		45	50	55	%

1. t_{LH} and t_{HL} are measured into a capacitive load of 15 pF.

Table 4. PIN DESCRIPTION

Pin#	Pin Name	Type	Description
1	XIN / CLKIN	I	Crystal connection or external reference frequency input. This pin has dual functions. It can be connected either to an external crystal or an external reference clock.
2	XOUT	O	Crystal connection. If using an external reference, this pin must be left unconnected.
3	DIV2	I	Digital logic input used to select normal output mode or divide−by−two output mode. When this pin is HIGH, the frequency of the output clock is the same as the input clock frequency. When it is tied low, the output frequency is half the input clock frequency. This pin has an internal pull−up resistor.
4	VSS	P	Ground to entire chip. Connect to system ground.
5	SSON#	I	Digital logic input used to enable Spread Spectrum function (Active LOW). Spread Spectrum function enabled when LOW, disabled when HIGH. This pin has an internal pull−low resistor.
6	ModOUT	O	Spread spectrum clock output.
7	SR0	I	Digital logic input used to select Spreading Range (Refer to *Modulation Output and Spreading Selection* Table.) This pin has an internal pull−up resistor.
8	VDD	P	Power supply for the entire chip

Table 5. MODULATION OUTPUT AND SPREADING SELECTION (ModOUT = XIN / CLKIN)

	Output Frequency Range DIV2 = 1							
SR0	8 MHz	12 MHz	16 MHz	20 MHz	24 MHz	28 MHz	32 MHz	Modulation Rate
0	±2.2%	±1.8%	±1.2%	±1.1%	±1.0%	±0.9%	±0.8%	(XIN / CLKIN/20) * 62.5 KHz
1	±3.2%	±2.5%	±2.0%	±1.6%	±1.4%	±1.25%	±0.15%	

Table 6. MODULATION OUTPUT AND SPREADING SELECTION (ModOUT = $^1/_2$ XIN / CLKIN)

	Output Frequency Range DIV2 = 0							
SR0	4 MHz	6 MHz	8 MHz	10 MHz	12 MHz	14 MHz	16 MHz	Modulation Rate
0	±2.0%	±1.8%	±1.2%	±1.1%	±1.0%	±0.9%	±0.8%	(XIN / CLKIN/20) * 62.5 KHz
1	±3.2%	±2.6%	±2.0%	±1.6%	±1.4%	±1.25%	±0.15%	

Spread Spectrum

The *Modulation Output and Spreading Selection* Tables illustrate the two possible spread spectrum options. The optimal setting should minimize system EMI to the fullest without affecting system performance. The spreading is described as a percentage deviation of the center frequency (Note: The center frequency is the frequency of the external reference input on XIN / CLKIN, Pin1).

Example:

The P2008A is designed for communications, digital video and imaging applications. It is not only optimized for operation in the 4 MHz – 32 MHz range, but its output frequency can be extended down to one half of the input clock frequency using the divide−by−two feature. This feature extends low frequency as low as to 2 MHz. Setting Pin 3 low (DIV2 = 0; Divide−by−two mode) sets the output frequency (ModOUT) to half the frequency of the input clock (XIN / CLKIN). This is a simple way to generate a spread spectrum modulated low frequency clock when only a higher frequency signal is available. If you want the output frequency to be the same as the input, you can either set DIV2=1 or leave it unconnected.

Selecting the P2008A's spread options is a matter of either setting SR0=1 or SR0=0. Setting SR0=0 set as a lower modulation spread, while setting it to 1 introduces a wider spectral spread in the output clock. Refer to *Modulation output and Spreading Selections* Tables. The example given in the figure below shows the device set to the divide−by−two mode (DIV2=0) with a lower spectrum range (SR0=0). The versatility provided by allowing both clock division and spread spectrum on one chip is already proving to be a popular solution among leading system manufacturers.

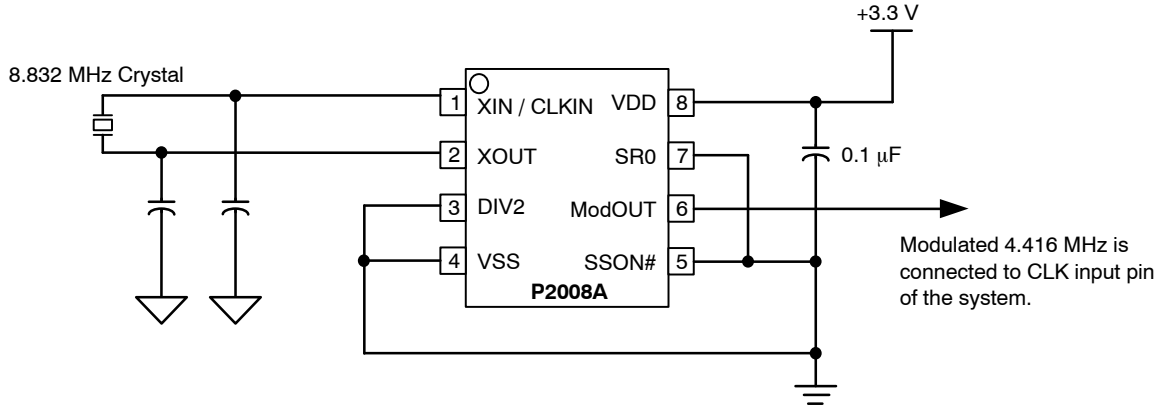
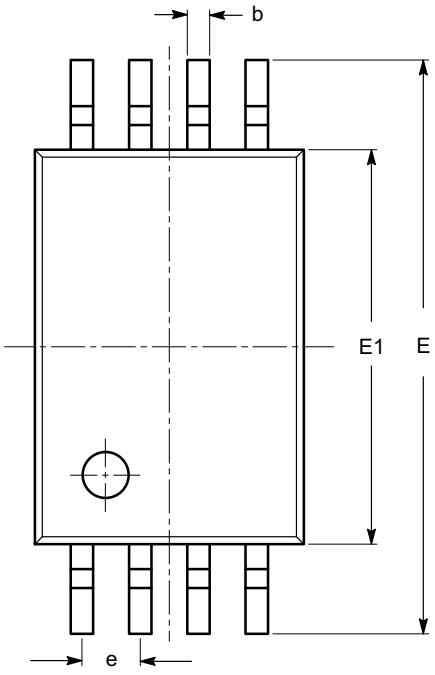


Figure 2. P2008A Application Schematic

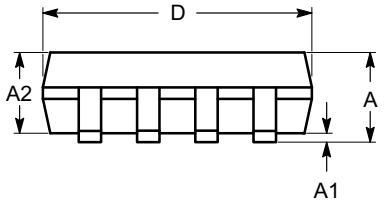
PACKAGE DIMENSIONS

TSSOP8, 4.4x3
CASE 948AL−01
ISSUE O

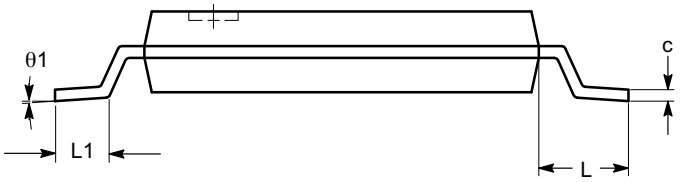


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			1.20
A1	0.05		0.15
A2	0.80	0.90	1.05
b	0.19		0.30
c	0.09		0.20
D	2.90	3.00	3.10
E	6.30	6.40	6.50
E1	4.30	4.40	4.50
e	0.65 BSC		
L	1.00 REF		
L1	0.50	0.60	0.75
θ	0º		8º



SIDE VIEW



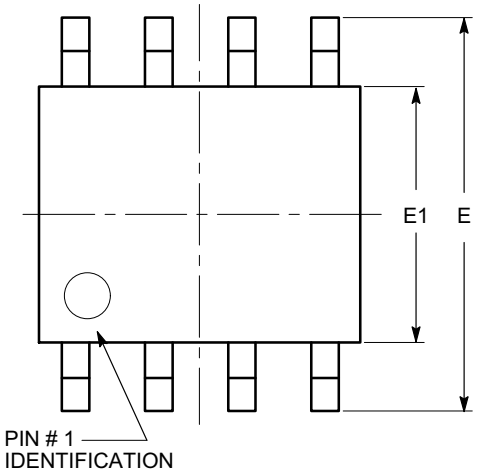
END VIEW

Notes:

(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-153.

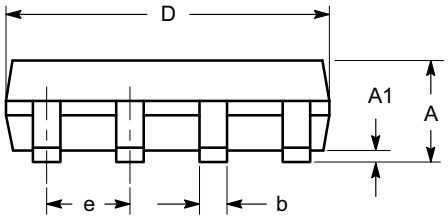
PACKAGE DIMENSIONS

SOIC 8, 150 mils
CASE 751BD−01
ISSUE O

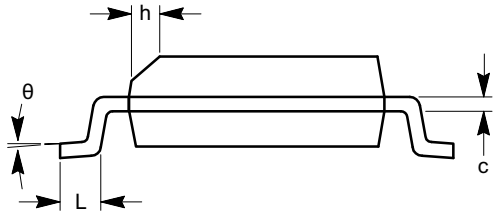


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	1.35		1.75
A1	0.10		0.25
b	0.33		0.51
c	0.19		0.25
D	4.80		5.00
E	5.80		6.20
E1	3.80		4.00
e	1.27 BSC		
h	0.25		0.50
L	0.40		1.27
θ	0º		8º



SIDE VIEW



END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MS-012.

Table 7. ORDERING INFORMATION

Part Number	Marking	Package Type	Temperature
P2008AF−08ST	P2008AF	8−PIN SOIC, TUBE, Pb Free	Commercial
P2008AF−08SR	P2008AF	8−PIN SOIC, TAPE AND REEL, Pb Free	Commercial
P2008AF−08TT	P2008AF	8−PIN TSSOP, TUBE, Pb Free	Commercial
P2008AF−08TR	P2008AF	8−PIN TSSOP, TAPE AND REEL, Pb Free	Commercial
P2008AG−08ST	P2008AG	8 PIN SOIC, TUBE, Green	Commercial
P2008AG−08SR	P2008AG	8−PIN SOIC, TAPE AND REEL, Green	Commercial
P2008AG−08TT	P2008AG	8−PIN TSSOP, TUBE, Green	Commercial
P2008AG−08TR	P2008AG	8−PIN TSSOP, TAPE AND REEL, Green	Commercial

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
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P2008A/D